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CL-SH451
Product Bulletin

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High-Performance Fast Sync/Async SCSI Disk Controller

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FEATURES

Microcontroller Interface

■ Supports high-speed microcontroller interfaces

■ Supports multiplexed or non-multiplexed address/data microcontrollers

■ Supports direct microcontroller access to the SCSI Bus

■ Supports direct microcontroller access to buffer memory and seven external switches

■ Supports auto-wait or scheduled access to WCS and buffer memory

■ Separate host- and disk-interrupt structures for flexible interrupt or polled-firmware design

SCSI Interface

■ Supports SCSI-2 Initiator and Target Modes

■ Supports synchronous DMA/PIO transfers up to 10 Mbytes/second (asynchronous up to 5 Mbytes/second)

■ Supports up to 15-byte synchronous transfer offsets and 28 programmable transfer periods

■ Controls synchronous transfer overrun/underrun

■ Supports programmable automated SCSI phase execution

■ Detects selected and reselected conditions automatically

■ Integrates 48-mA and active pull-up SCSI Bus drivers

■ Programmable push-pull SCSI Bus drivers
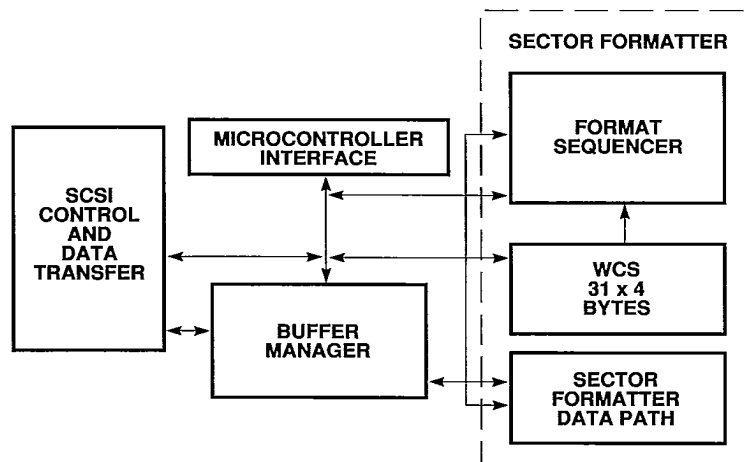
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OVERVIEW

The CL-SH451 is a high-performance, high-speed single-chip controller for disk drive systems. The CL-SH451 design combines a local microcontroller port, extensive hardware support for the SCSI interface, a five-channel Buffer Manager, and an advanced Sector Formatter. With the addition of only a few discrete components for the device-level interface, the CL-SH451, along with a local microcontroller, system ROM and RAM, and an optional data separator, completes a disk controller subsystem with high performance at a low overall cost.

A local microcontroller provides the CL-SH451 with initial operating parameters that include disk sector format, the type and size of buffer memory, and SCSI Host control. During data transfer operations, the CL-SH451 requires only minimal intervention from the local microcontroller.

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Functional Block Diagram

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CL-SH451
High-Performance SCSI Disk Controller

FEATURES (cont.)

Sector Formatter

- Full-track multi-sector transfer capability
- Transfers SCSI information to/from the micro-controller through a 16-byte FIFO under Automatic Programmed I/O (PIO)
- Programmable Format Sequencer Writable Control Store (WCS — 31 x 4 bytes)
- Supports up to 64-MHz NRZ data rates
- 1-bit serial or 2-bit parallel NRZ interface
- Allows split data field processing for embedded servo and zoned designs
- Provides 16-bit CRC and 88-bit Reed-Solomon ECC with on-the-fly correction
- Programmable on-the-fly error burst length

Buffer Manager

- Five-channel, circular buffer control with priority resolution

- Direct buffer addressing up to 256K bytes of SRAM and 4 Mbytes of DRAM
- Supports scatter/gather operation for LRU cache support
- Supports Streaming Mode, and automatic host and disk operation in the same circular buffer simultaneously (with a mechanism to prevent overrun and underrun)
- Permits concurrent buffer memory throughput of up to 17.5 Mbytes/second
- Flexible buffer segmentation logic
- Automatic SCSI disconnect/reconnect with local interrupt for programmable buffer threshold and buffer empty/full conditions

Technology

- 100-pin Quad Flat Pack (QFP or VQFP) package
- Advanced, low-power, double-metal CMOS technology
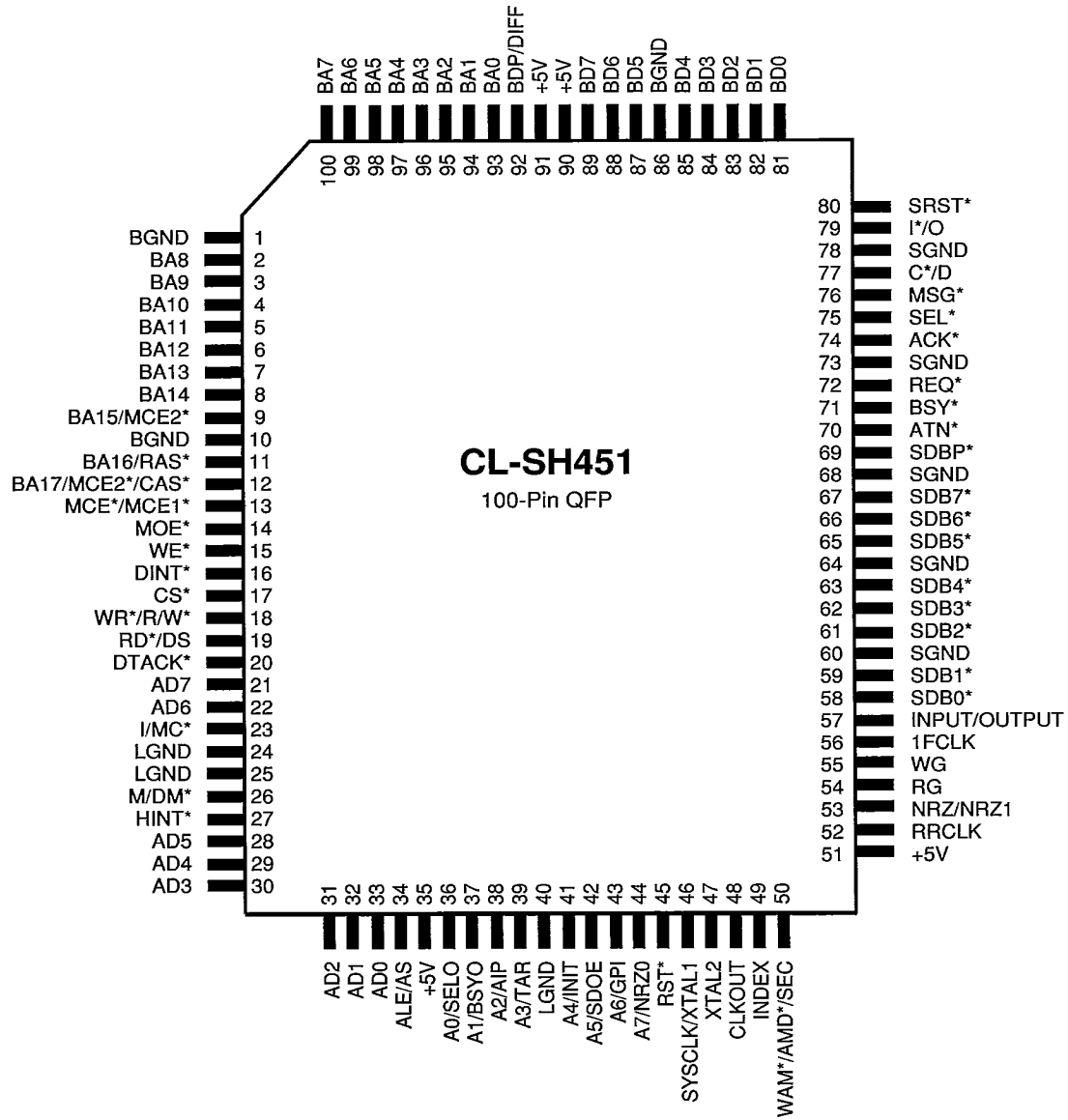
OVERVIEW (cont.)

The microcontroller-to-CL-SH451 communication path is a multiplexed/non-multiplexed address and data bus similar to that provided by the Intel® 8051 and the Motorola® 68HC11 class of controllers. (There is a configuration signal available to allow for either family of data control signal methods). The CL-SH451 has centralized status registers with interrupt capability. These features allow firmware designers flexibility in writing polled loops or interrupt handlers that provide real-time process control critical in embedded controller drive applications.

The SCSI Host interface is designed for compliance with the SCSI-2 specification. This ensures long-term compatibility for both the hardware and the firmware developed around the CL-SH451. The CL-SH451 has significant SCSI automation features that minimize command overhead and firmware intervention. Routine bus control operations such as arbitration, selection and reselection are automatically sequenced in hardware. Additionally, the CL-SH451 automatically handles SCSI selection with messages (identify, tag) and/or command. The receive command, disconnect sequence and command-complete sequence are also automated.

The Sector Formatter provides the disk data and control functions. The Sector Formatter is capable of handling NRZ data rates up to 64 MHz and can

perform automatic multi-sector transfers up to a complete track, while handling multiple data-segments per sector. The Sector Formatter is sub-divided into a Format Sequencer and the Sector Formatter Data path. The Format Sequencer uses a 31-word-by-4-byte Writable Control Store (WCS) to hold a user-written program. This program contains the control information for the disk track and sector format. The Sector Formatter data path consists of the NRZ-data-handling circuitry that includes the serializer/deserializer (SERDES), the 88-bit Reed-Solomon ECC and 16-bit CRC error control logic, the SERDES parity logic, and the data signals to the Buffer Manager interface.

The Buffer Manager controls the flow of data between the host and disk interfaces. These interfaces store and retrieve data from the buffer memory using interleaved access cycles. The component is programmable to provide all of the necessary address and control signals for RAM devices of varying access times. The CL-SH451 also allows fully automatic host-to-media and media-to-host multisector transfers, while monitoring the state of the buffer to identify buffer full/empty conditions, and programmable data thresholds. These conditions are monitored to automatically disconnect or reconnect from the SCSI Bus.

CL-SH451 Pin Diagram

The CL-SH451 is a 100-Pin QFP.

Left side pins (1–30):

Pin	Signal
1	BGND
2	BA8
3	BA9
4	BA10
5	BA11
6	BA12
7	BA13
8	BA14
9	BA15/MCE2*
10	BGND
11	BA16/RAS*
12	BA17/MCE2*/CAS*
13	MCE*/MCE1*
14	MOE*
15	WE*
16	DINT*
17	CS*
18	WR*/R/W*
19	RD*/DS
20	DTACK*
21	AD7
22	AD6
23	I/MC*
24	LGND
25	LGND
26	M/DM*
27	HINT*
28	AD5
29	AD4
30	AD3

Top pins (100–81):

Pin	Signal
100	BA7
99	BA6
98	BA5
97	BA4
96	BA3
95	BA2
94	BA1
93	BA0
92	BDP/DIFF
91	+5V
90	+5V
89	BD7
88	BD6
87	BD5
86	BGND
85	BD4
84	BD3
83	BD2
82	BD1
81	BD0

Right side pins (80–51):

Pin	Signal
80	SRST*
79	I*/O
78	SGND
77	C*/D
76	MSG*
75	SEL*
74	ACK*
73	SGND
72	REQ*
71	BSY*
70	ATN*
69	SDBP*
68	SGND
67	SDB7*
66	SDB6*
65	SDB5*
64	SGND
63	SDB4*
62	SDB3*
61	SDB2*
60	SGND
59	SDB1*
58	SDB0*
57	INPUT/OUTPUT
56	1FCLK
55	WG
54	RG
53	NRZ/NRZ1
52	RRCLK
51	+5V

Bottom pins (31–50):

Pin	Signal
31	AD2
32	AD1
33	AD0
34	ALE/AS
35	+5V
36	A0/SELO
37	A1/BSYO
38	A2/AIP
39	A3/TAR
40	LGND
41	A4/INIT
42	A5/SDOE
43	A6/GPI
44	A7/NRZ0
45	RST*
46	SYSCLK/XTAL1
47	XTAL2
48	CLKOUT
49	INDEX
50	WAM*/AMD*/SEC

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PIN DESCRIPTION

Symbol	Pin Number	Type	Description
Microcontroller Interface Pins			
DINT*	16	O, OD, Z	Disk Interrupt
CS*	17	I	Chip Select
WR*/R/W*	18	I	Write Strobe/Read/Write
RD*/DS	19	I	Read Strobe/Data Strobe
DTACK*	20	OD	Data Transfer Acknowledge
I/MC*	23	I	Intel/Motorola
HINT*	27	O, OD, Z	Host Interrupt
AD0:7	33-28, 22-21	I/O	Local Microcontroller Address/Data Bus
A0/SELO	36	I/O	Local Microcontroller Address 0/Select Out
A1/BSYO	37	I/O	Microcontroller Address 1/Busy Out
A2/AIP	38	I/O	Microcontroller Address 2/Arbitration in Progress
A3/TAR	39	I/O	Microcontroller Address 3/Target
A4/INIT	41	I/O	Microcontroller Address 4/Initiator
A5/SDOE	42	I/O	Microcontroller Address 5/SCSI Data Bus Output Enable
A6/GPI	43	I/O	Microcontroller Address 6/GPI
A7/NRZ0	44	I/O	Microcontroller Address 7/NRZ0
M/DM*	26	I	Multiplexed/Non-multiplexed Address Configuration
ALE/AS	34	I	Address Latch Enable/Address Strobe
RST*	45	I	Reset
SCSI Bus Interface Pins			
SDB0*:7*	58-59, 61-63, 65-67	I/O, OD	SCSI Data Bus
SDBP*	69	I/O, OD	SCSI Data Bus Parity
ATN*	70	I/O, OD	SCSI Attention
BSY*	71	I/O, OD	SCSI Busy
ACK*	74	I/O, OD	SCSI Acknowledge
SRST*	80	I/O, OD	SCSI Reset
MSG*	76	I/O, OD	SCSI Message
SEL*	75	I/O, OD	SCSI Select
C*/D	77	I/O, OD	SCSI Command/Data
REQ*	72	I/O, OD	SCSI Request
I*/O	79	I/O, OD	SCSI Input/Output
Buffer Manager Interface Pins			
BD0:7	81-85, 87-89	I/O	Buffer Memory Data Bus
BDP/DIFF	92	I/O	Buffer Memory Data Parity/Differential Enable
BA0:14	93-100, 2-8	O	Buffer Memory Address Lines
BA15/MCE2*	9	O	Buffer Memory Address 15/MCE2*
BA16/RAS*	11	O	Buffer Memory Address 16/RAS*
A17/MCE2*/CAS*	12	O	Buffer Memory Address 17/MCE2*/CAS*
MCE*/MCE1*	13	O	Memory Chip Enable/Memroy Chip Enable 1
MOE*	14	O	Memory Output Enable
WE*	15	O	Write Enable
SYSCLK/XTAL1	46	I	System Clock/XTAL1 (Crystal Input 1)
XTAL2	47	I	XTAL2 (Crystal Input 2)
CLKOUT	48	O	Clock Output
Sector Formatter Interface Pins			
INPUT/OUTPUT	57	I/O	Format Sequencer Input/Output
INDEX	49	I	Index
WAM*/AMD*/SECTOR	50	I/O	Write Address Mark/Address Mark Detect/Sector
RG	54	O	Read Gate
WG	55	O	Write Gate
RRCLK	52	I	Read Reference Clock
NRZ/NRZ1	53	I/O	Non-return to Zero
1FCLK	56	I	1FCLK (clocks ECC correction circuitry)
Power and Ground Pins			
BGND	1, 10, 86	N/A	Buffer Ground Pins
LGND	24, 25, 40	N/A	Logic Ground Pins
+5V	35, 51, 90, 91	N/A	Power Supply (+5 volt) Pins
SGND	60, 64, 68, 73, 78	N/A	High Current SCSI Ground Pins

NOTES: * denotes negative-true signal. I indicates input pin; O indicates output pin; I/O indicates input/output pin; OD indicates open-drain output pin; Z indicates tri-state output or input/output pins. All unused input pins must be tied to GND or VDD appropriately. SGND, BGND, and LGND are connected to three separate ground rings internally.

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High-Performance SCSI Disk Controller

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ADVANTAGES

Unique Features	Benefits
• *Programmable wait states for microcontroller*	Allows the fastest microcontrollers to operate without degrading bus performance.
• *Pin-configurable microcontroller data control interface*	Allows for direct connect to Intel- or Motorola-style microcontrollers.
• *Separate disk and host microcontroller interrupts*	Supports faster, more direct interrupt processing by microcontroller.
• *15-byte offset in Synchronous Mode*	Greater flexibility for synchronous data transfer negotiations.
• *16-byte FIFO for automatic PIO transfers*	Decreases command and information transfer overhead.
• *Five Buffer Manager DMA channels*	Enables read-look-ahead for high performance.
• *Direct 256-Kbyte–SRAM or 4-Mbyte–DRAM addressing*	Increases buffer size alternatives to support caching.
• *Odd parity buffer verification*	Improves data integrity between host and disk data transfers.
• *Variable buffer segmentation logic*	Allows protected data segments in buffer.
• *Advanced-programmable branch conditions in the Writable Control Store (WCS) program*	Supports flexible, automated defect management and retry algorithms.
• *Conditional Format Sequencer execution of up to four paths*	Supports end-of-track, retry and defect management code.
• *Programmable read synchronization timeout*	Simplifies ID and Data Field searches.
• *'On-the-fly' error correction circuitry*	Enables automatic high-speed ECC correction.
• *Multiple data field processing within the ECC*	Provides support for embedded servo drives, zoned-recorded drives, and large defect skipping.
• *Automatic disconnect/reconnect on programmable buffer empty/full threshold*	Optimizes SCSI Bus utilization.
• *Automatic multisector transfer between host and disk*	Reduces local microcontroller real-time response.
• *Minimal latency support*	Reduces the rotational latency by an average of one-half revolution.
• *Programmable power management*	Reduces power consumption for small form-factor drives.
• *2-bit parallel NRZ interface*	Faster data transfers to/from the controller.

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