APPLICATION NOTE
AVAILABLE
AN56

High Speed NOVRAM

X20CZ16

FEATURES

- **Fast access time: 35ns**
- **High reliability**
  - **—Endurance: 10^5 nonvolatile store operations**
  - **—Retention: 10 years minimum**
- **Power-on recall**
  - **—EEPROM data automatically recalled into RAM upon power-up**
- **Low power CMOS**
  - **—Standby: 1mA**
- **Infinite EEPROM array recall, and RAM read and write cycles**
- **Hardware store initiation (store cycle time < 10ms)**
- **Available in the 32-lead plastic leadless chip carrier package**

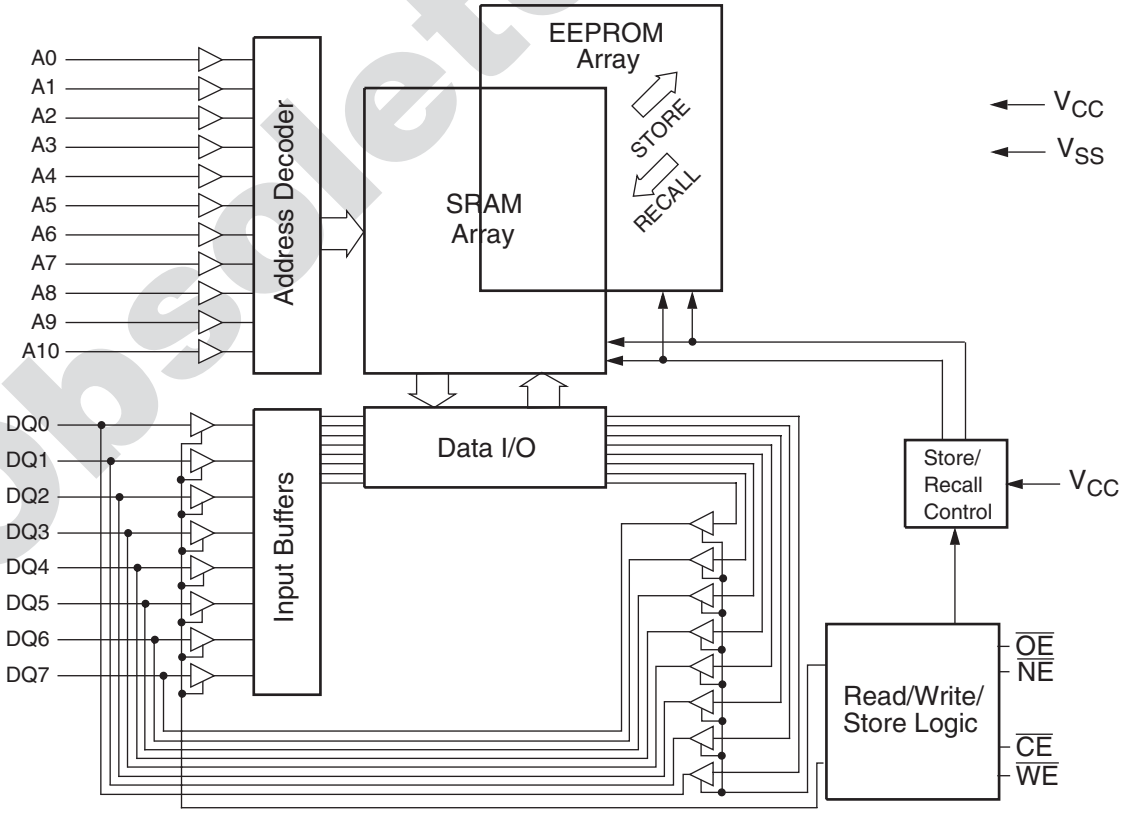
DESCRIPTION

The Xicor X20CZ16 is a 2K x 8 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (EEPROM). The X20CZ16 is fabricated with advanced CMOS floating gate technology to achieve high speed with low power and wide power-supply margin.

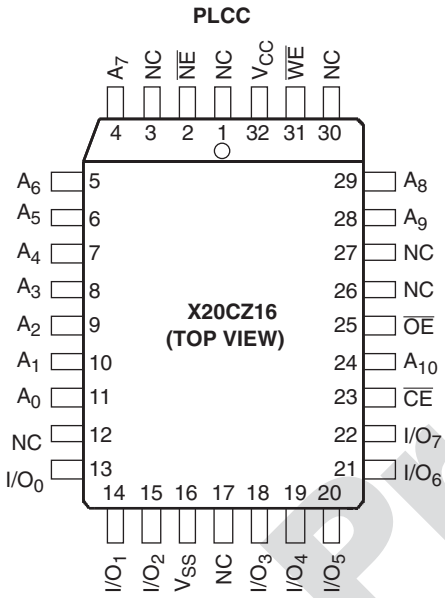
The NOVRAM design allows data to be easily transferred from RAM to EEPROM (store) and EEPROM to RAM (recall). The store operation is completed in 10ms or less and the recall operation is completed in 20µs or less. An automatic array recall operation reloads the contents of the EEPROM into RAM upon power-up.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from EEPROM, and a minimum 100,000 store operations to the EEPROM. Data retention is specified to be greater than 10 years.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

Part Number	Access Time	Temperature Range	Package
X20CE16JI-35	-35 = 35 ns	-40°C to 85°C	J = 32-Lead PLCC

PIN DESCRIPTIONS

PLCC	Symbol	Description
11, 10, 9, 8, 7, 6, 5, 4, 29, 28, 24	A_0–A_{10}	Address inputs
13, 14, 15, 18, 19, 20, 21, 22	I/O_0–I/O_7	Data input/output
31	$\overline{WE}$	Write enable
23	$\overline{CE}$	Chip enable
25	$\overline{OE}$	Output enable
2	$\overline{NE}$	Nonvolatile enable
32	V_{CC}	+5V
16	V_{SS}	Ground
1, 3, 12, 17, 26, 27, 30	NC	No connect

ABSOLUTE MAXIMUM RATINGS*

Temperature under bias ..... –65°C to +135°C
Storage temperature ..... –65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... –0.3V to V_{CC} + 0.5V
D.C. output current 10mA
Lead temperature (soldering, 10 seconds)..... 300°C
Power Supply Voltage (V_{CC} to V_{SS}) .....-0.5V to +7.0V

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Industrial	–40°C	+85°C

Supply Voltage	Limits
X20CZ16	5V ±10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{CC1}	V_{CC} current (active)		100	mA	$\overline{NE}$ = $\overline{WE}$ = V_{IH}, $\overline{CE}$ = $\overline{OE}$ = V_{IL} Address inputs = 0.4V/2.4V levels @ f = 20MHz All I/Os = open
I_{CC2}	V_{CC} current during store		7	mA	All inputs = V_{IH} All I/Os = open
I_{SB1}	V_{CC} standby current (TTL input)		27	mA	$\overline{CE}$ = V_{IH}, All other inputs = V_{IH} All I/Os = open
I_{SB2}	V_{CC} standby current (CMOS input)		1	mA	All inputs = V_{CC} – 0.3V All I/Os = open
I_{LI}	Input leakage current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(1)	Input LOW voltage	–0.3	0.8	V	
V_{IH}(1)	Input HIGH voltage	2.2	V_{CC} + 0.3	V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 4mA
V_{OH}	Output HIGH voltage	2.4		V	I_{OH} = –4mA

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$(2)	Input/output capacitance	7	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input capacitance	8	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

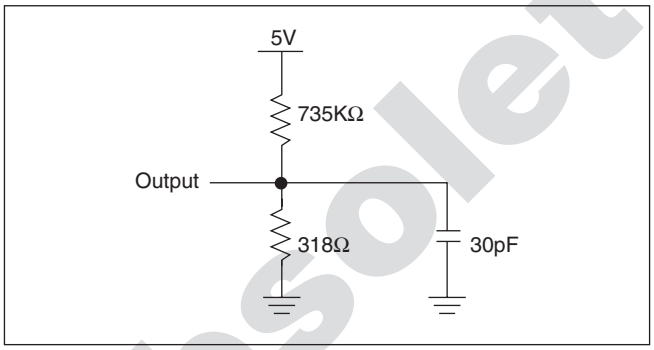
ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Store cycles	100,000	Store cycles
Data retention	10	Years

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not selected	Output high Z	Standby
L	H	H	L	Read RAM	Output data	Active
L	L	H	H	Write “1” RAM	Input data high	Active
L	L	H	H	Write “0” RAM	Input data low	Active
L	H	L	L	Array recall	Output high Z	Active
L	L	L	H	Nonvolatile store	Output high Z	Active
L	H	H	H	Output disabled	Output high Z	Active
L	L	L	L	Not allowed	Output high Z	Active
L	H	L	H	No operation	Output high Z	Active

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don’t Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

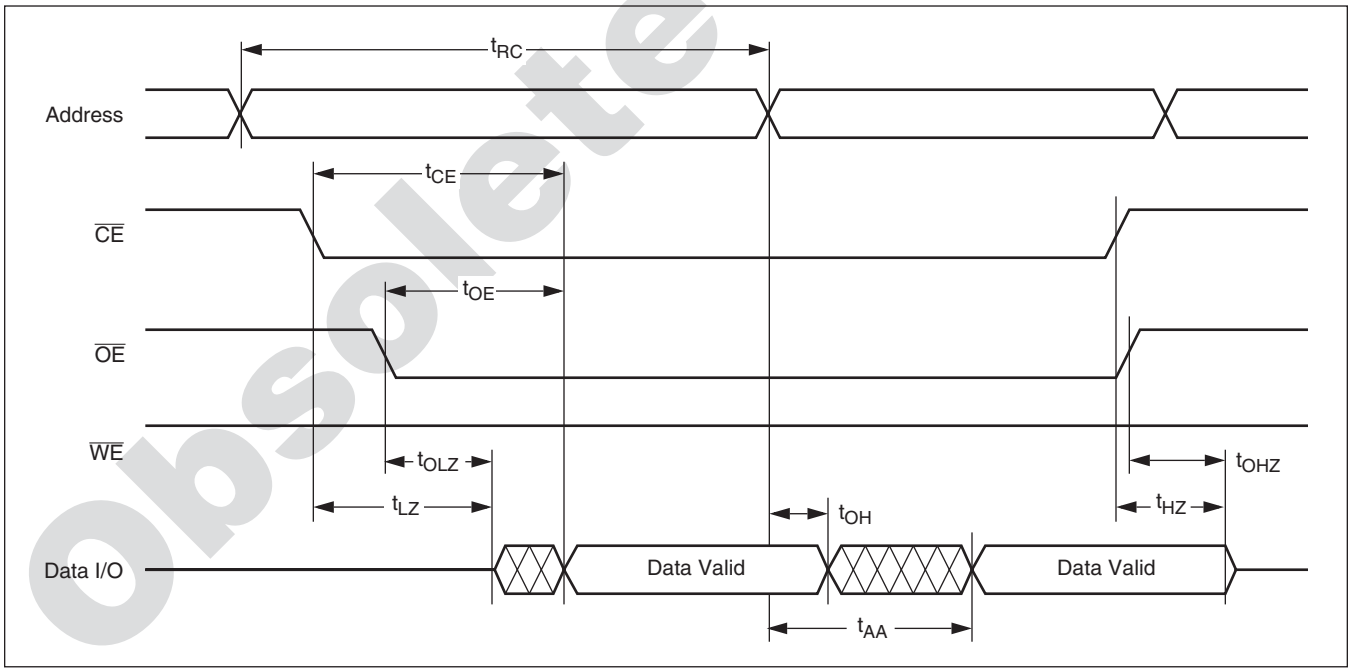
A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Read Cycle Limits

Symbol	Parameter	X20CZ16-35 –40 to +85°C		Unit
		Min.	Max.	
t_{RC}(3)	Read cycle time	35		ns
t_{CE}	Chip enable access time		35	ns
t_{AA}	Address access time		35	ns
t_{OE}	Output enable access time		20	ns
t_{LZ}(3)	Chip enable to output in low Z	5		ns
t_{OLZ}(3)	Output enable to output in low Z	0		ns
t_{HZ}(3)	Chip disable to output in high Z	0	15	ns
t_{OHZ}(3)	Output disable to output in high Z	0	15	ns
t_{OH}(3)	Output hold from address change	3		ns

Note: (3) These parameters are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured, with C_L = 5pF, from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Read Cycle

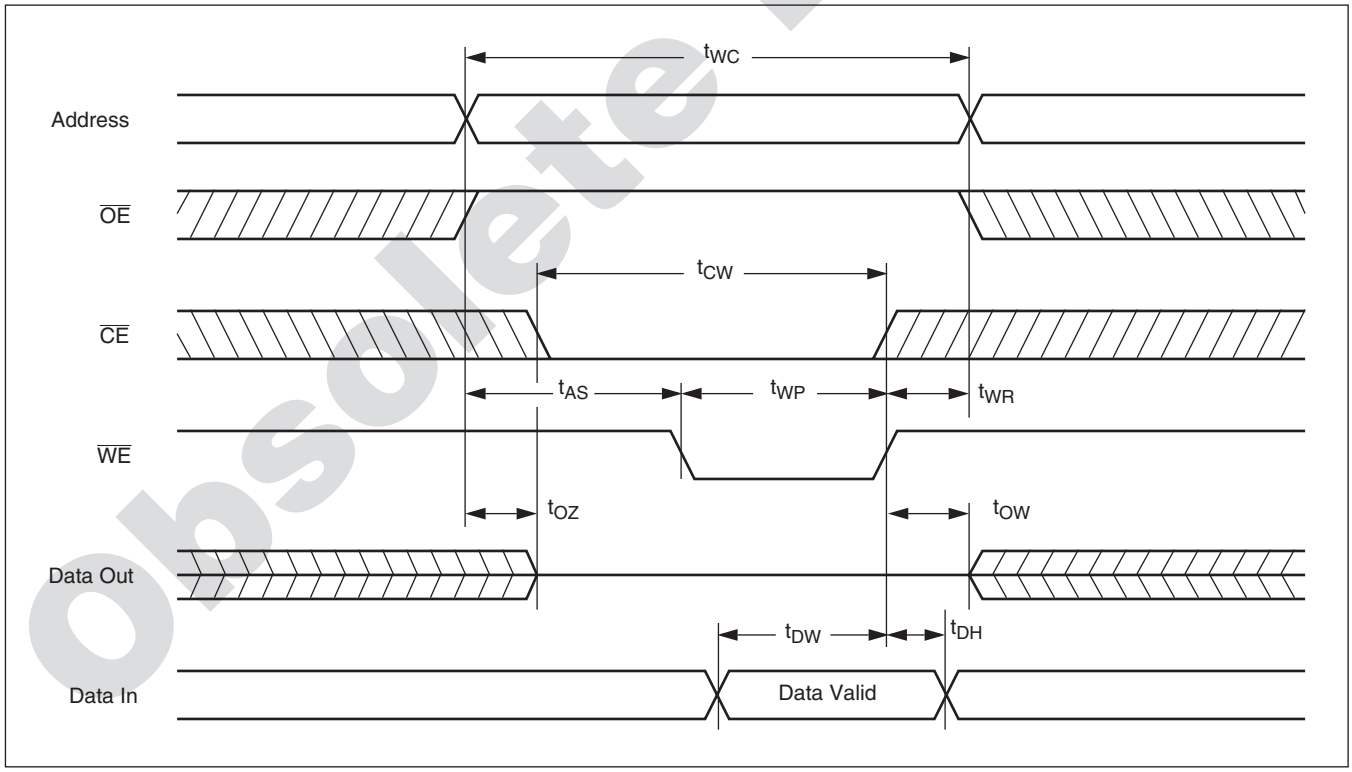


Write Cycle Limits

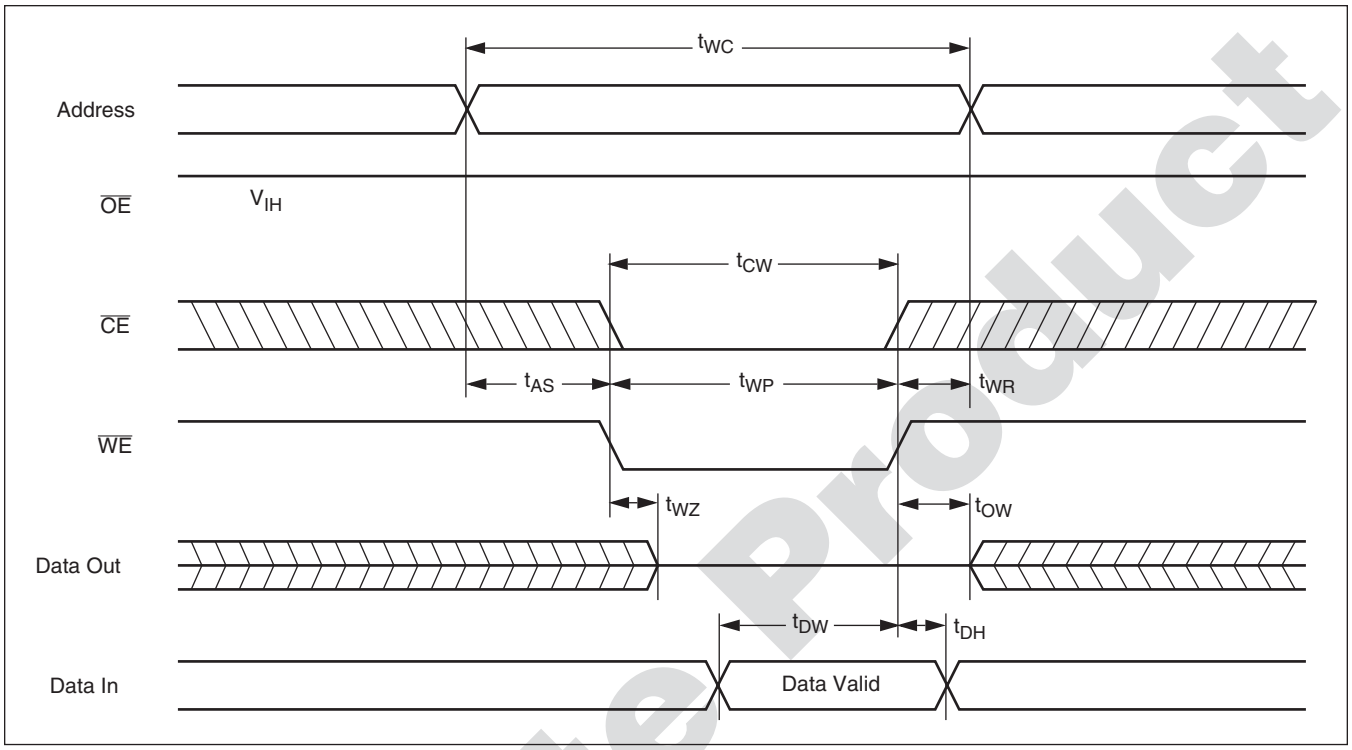
Symbol	Parameter	X20CZ16-35		Unit
		Min.	Max.	
t_{WC}(4)	Write cycle time	35		ns
t_{CW}	Chip enable to end of write input	30		ns
t_{AS}	Address setup time	0		ns
t_{WP}	Write pulse width	30		ns
t_{WR}	Write recovery time	0		ns
t_{DW}	Data setup to end of write	30		ns
t_{DH}	Data hold time	0		ns
t_{WZ}(4)	Write enable to output in high Z		15	ns
t_{OW}(4)	Output active from end of write	5		ns
t_{OZ}(4)	Output enable to output in high Z		20	ns

Note: (4) These parameters are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



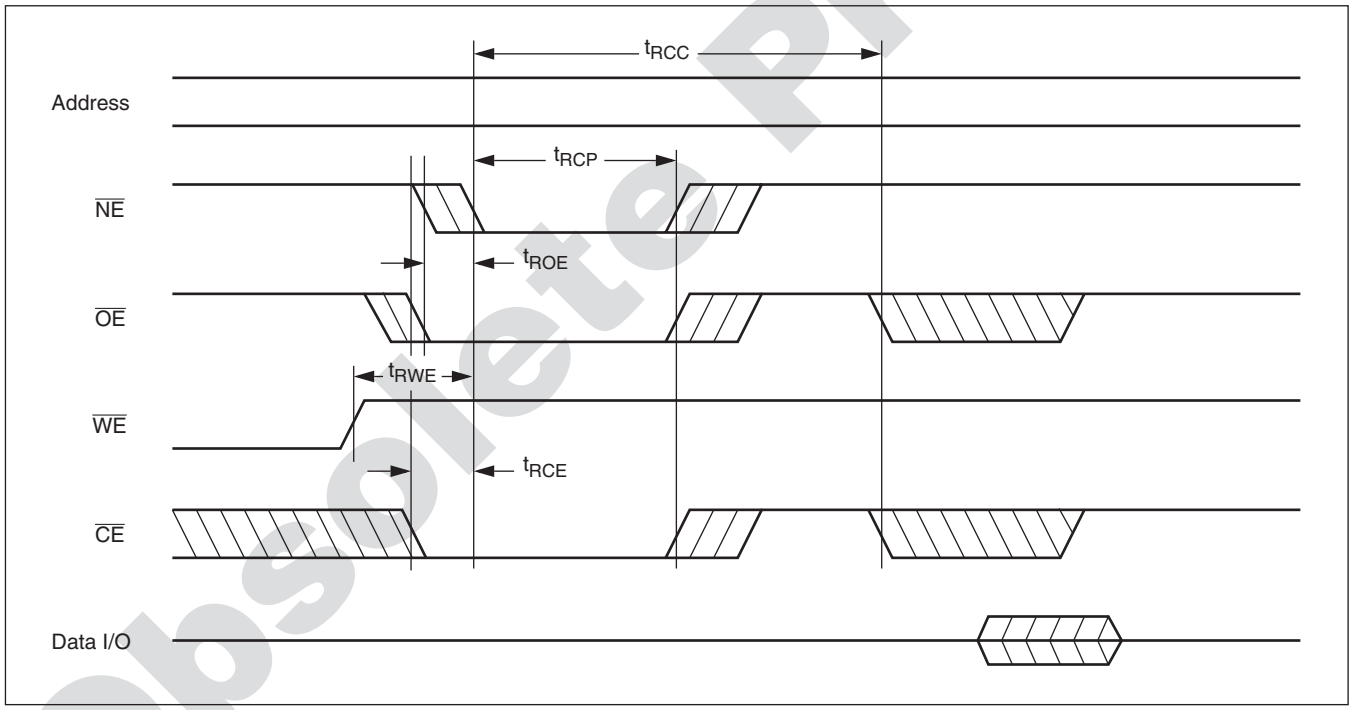
ARRAY RECALL CYCLE LIMITS(6)

Symbol	Parameter	X20CZ16-35		Unit
		Min.	Max.	
t_{RCC}	Array recall cycle time		20	µs
t_{RCP}(5)	Recall pulse width to initiate recall	30		ns
t_{RWE}	$\overline{WE}$ setup time to $\overline{NE}$	5		ns
t_{ROE}	$\overline{OE}$ setup time to $\overline{NE}$	5		ns
t_{RCE}	$\overline{CE}$ setup time to $\overline{NE}$	5		ns

Notes: (5) The Recall Pulse Width (t_{RCP}) is a minimum time that $\overline{NE}$, $\overline{OE}$ and $\overline{CE}$ must be LOW simultaneously to insure data integrity, $\overline{NE}$ and $\overline{CE}$.

(6) The limits shown are for $\overline{NE}$ initiated recall. The setup times and pulse width requirements for the active signals in $\overline{CE}$ initiated and $\overline{OE}$ initiated recalls are identical.

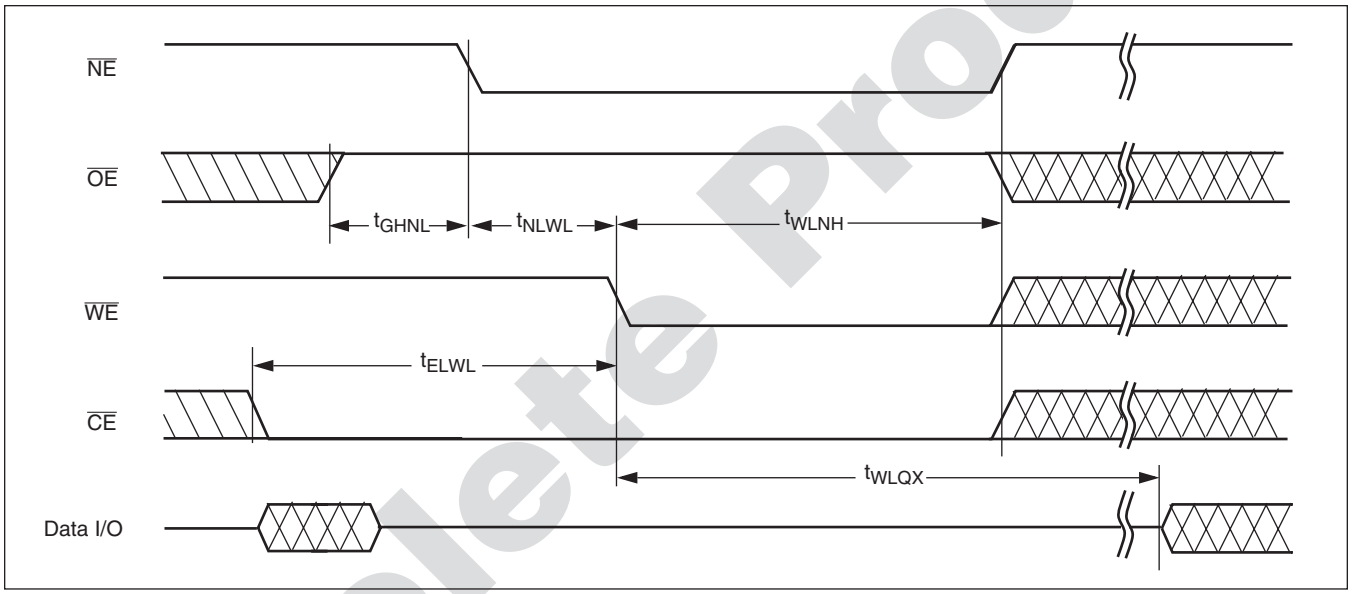
Array Recall Cycle



STORE CYCLES

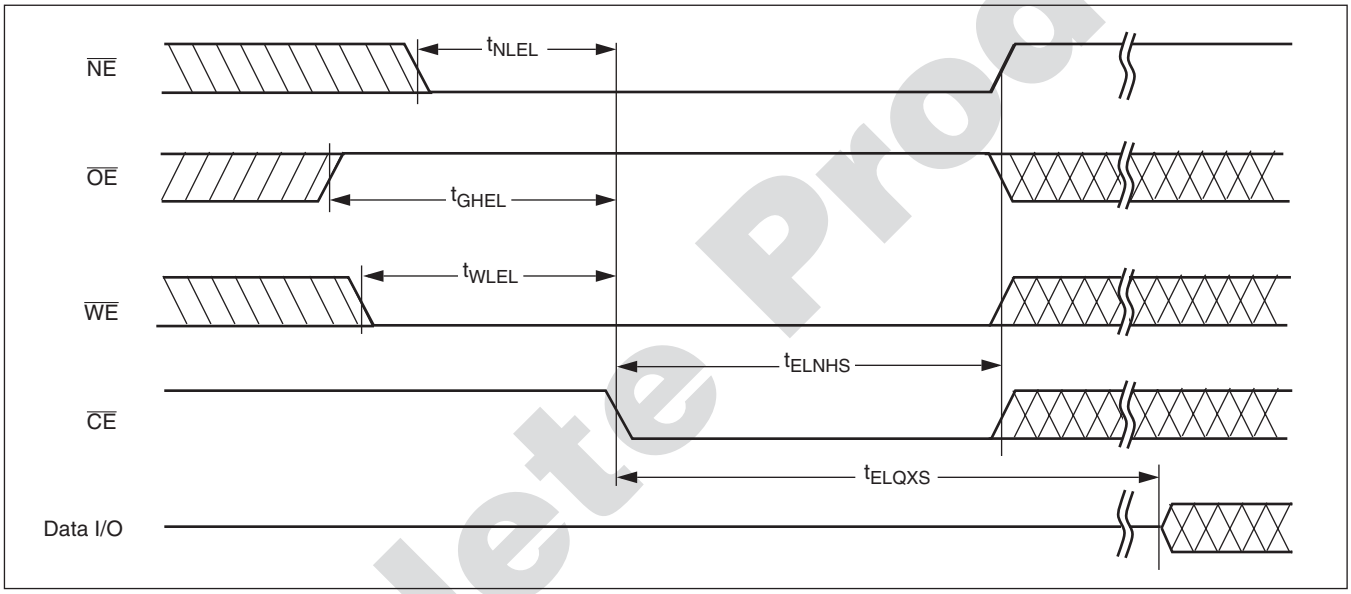
Symbol	Store Cycle $\overline{WE}$-controlled	X20CZ16-35		Unit
		Min.	Max.	
t_{WLQX}	STORE cycle time		10	ms
t_{WLNH}	STORE initiation cycle time	30		ns
t_{GHNL}	Output disable setup to $\overline{NE}$ fall	5		ns
t_{NLWL}	$\overline{NE}$ setup	5		ns
t_{ELWL}	Chip enable setup	5		ns

Store Cycle: $\overline{WE}$ Controlled



Symbol	Store Cycle $\overline{CE}$-controlled	X20CZ16-35		Unit
		Min.	Max.	
t_{ELQXS}	STORE cycle time		10	ms
t_{ELNHS}	STORE initiation cycle time	30		ns
t_{GHEL}	Output disable setup to $\overline{CE}$ fall	5		ns
t_{NLEL}	$\overline{NE}$ setup	5		ns
t_{WLEL}	Write enable setup	5		ns

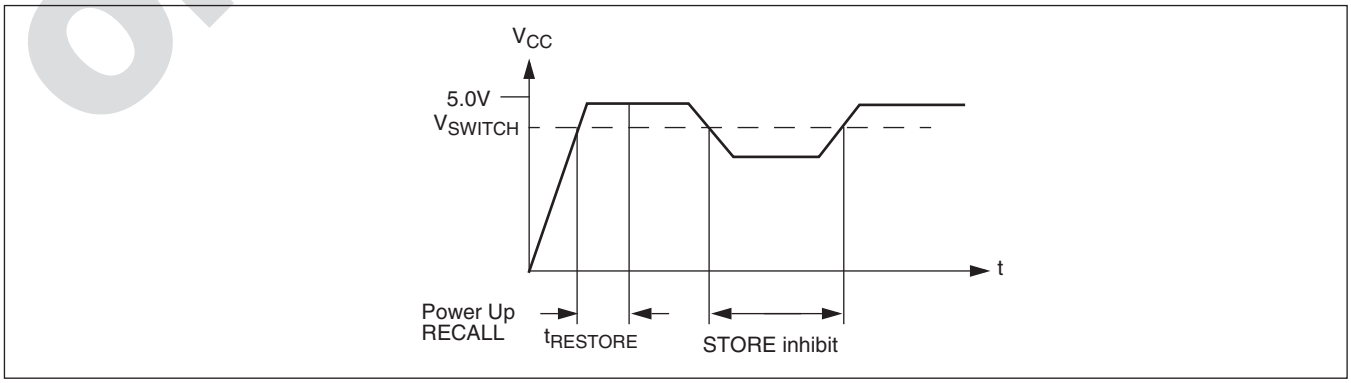
Store Cycle: $\overline{CE}$ Controlled



STORE CYCLE INHIBIT AND AUTOMATIC POWER UP RECALL

Symbol	Store Cycle Inhibit and Automatic Power Up RECALL	Min.	Max.	Unit
$t_{RESTORE}$	Power up RECALL duration(7)(2)		650	µs
V_{SWITCH}	Low voltage trigger level	4.0	4.5	V

Note: (7) $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.



DETAILED PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$, or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X20CZ16 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the static RAM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls the store and recall function to the EEPROM array.

DEVICE OPERATION

The X20CZ16 has two separate modes of operation: SRAM mode and nonvolatile mode, determined by the state of the $\overline{NE}$ pin. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the STORE operation) or from EEPROM to SRAM (the RECALL operation). In this mode SRAM functions are disabled.

SRAM Read

The X20CZ16 performs a READ cycle whenever $\overline{CE}$ and $\overline{OE}$ are LOW while $\overline{WE}$ and $\overline{NE}$ are HIGH. The address specified on pads A0–A10 determines which of the 2048 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{RC}. If the READ is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs will be valid at t_{CE} or at t_{OE}, whichever is later. The data outputs will repeatedly respond to address changes within the t_{RC} access time without the need for transition on any control input pins, and will remain valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH or $\overline{WE}$ or $\overline{NE}$ is brought LOW.

SRAM Write

A WRITE cycle is performed whenever $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on pins DQ0–7 will be written into the memory if it is valid t_{DW} before the end of a $\overline{WE}$ controlled WRITE or t_{DW} before the end of a $\overline{CE}$ controlled WRITE.

It is recommended that $\overline{OE}$ is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{OE}$ is left LOW, internal circuitry will turn off the output buffers t_{WZ} after $\overline{WE}$ goes LOW.

Noise Consideration

The X20CZ16 is a high speed memory and therefore must have a high frequency bypass capacitor of approximately 0.1 µF connected between V_{CC} and V_{SS} using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

Hardware Nonvolatile STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{CE}$ and $\overline{WE}$ are LOW while $\overline{OE}$ is HIGH. While any sequence to achieve this state will initiate a STORE, only $\overline{WE}$ initiation and $\overline{CE}$ initiation are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During a STORE cycle, previous nonvolatile data is erased the SRAM contents are then programmed into nonvolatile elements. Once a STORE cycle is initiated, further input and output is disabled and the DQ0–7 pins are tristated until the cycle is completed.

If $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active, indicating the end of the STORE.

Hardware Nonvolatile RECALL

A RECALL cycle is performed when $\overline{CE}$, $\overline{OE}$ and $\overline{NE}$ are LOW while $\overline{WE}$ is HIGH. Like the STORE cycle, RECALL is initiated when the last of the three clock-signals goes to the RECALL state. Once initiated, the RECALL cycle will complete, during which all inputs are ignored. When the RECALL completes, any READ or WRITE state on the input pins will take effect.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. The RECALL in no way alters the data in the nonvolatile cells. The nonvolatile data can be recalled an unlimited number of times.

Like the STORE cycle, a transition must occur on some control pins to cause a RECALL, preventing inadvertent multi-triggering.

Automatic Power Up RECALL

On power up, once V_{CC} exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated. The voltage on the V_{CC} pin must not drop below V_{SWITCH} once it has risen above it in order for the RECALL to operate properly. Due to this automatic RECALL, SRAM operation cannot commence until $t_{RESTORE}$ after V_{CC} exceeds V_{SWITCH}. If the X20CZ16 is in a WRITE state at the end of power up RECALL, the SRAM data will be corrupted.

To help avoid this situation, a 10 KΩ resistor should be connected between $\overline{WE}$ and system V_{CC}.

Hardware Protection

The X20CZ16 offers two levels of protection to suppress inadvertent STORE cycles. If the control signals ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$) remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will not be started. The STORE (or RECALL) will be initiated only after a transition on any one of these signals to the required state. In addition to multi-trigger protection, the X20CZ16 offers hardware protection through V_{CC} Sense. When $V_{CC} < V_{SWITCH}$ the externally initiated STORE operation will be inhibited.

Low Average Active Power

The X20CZ16 has been designed to draw significantly less power when $\overline{WE}$ is LOW (chip enabled) but the access cycle time is longer than 55 ns.

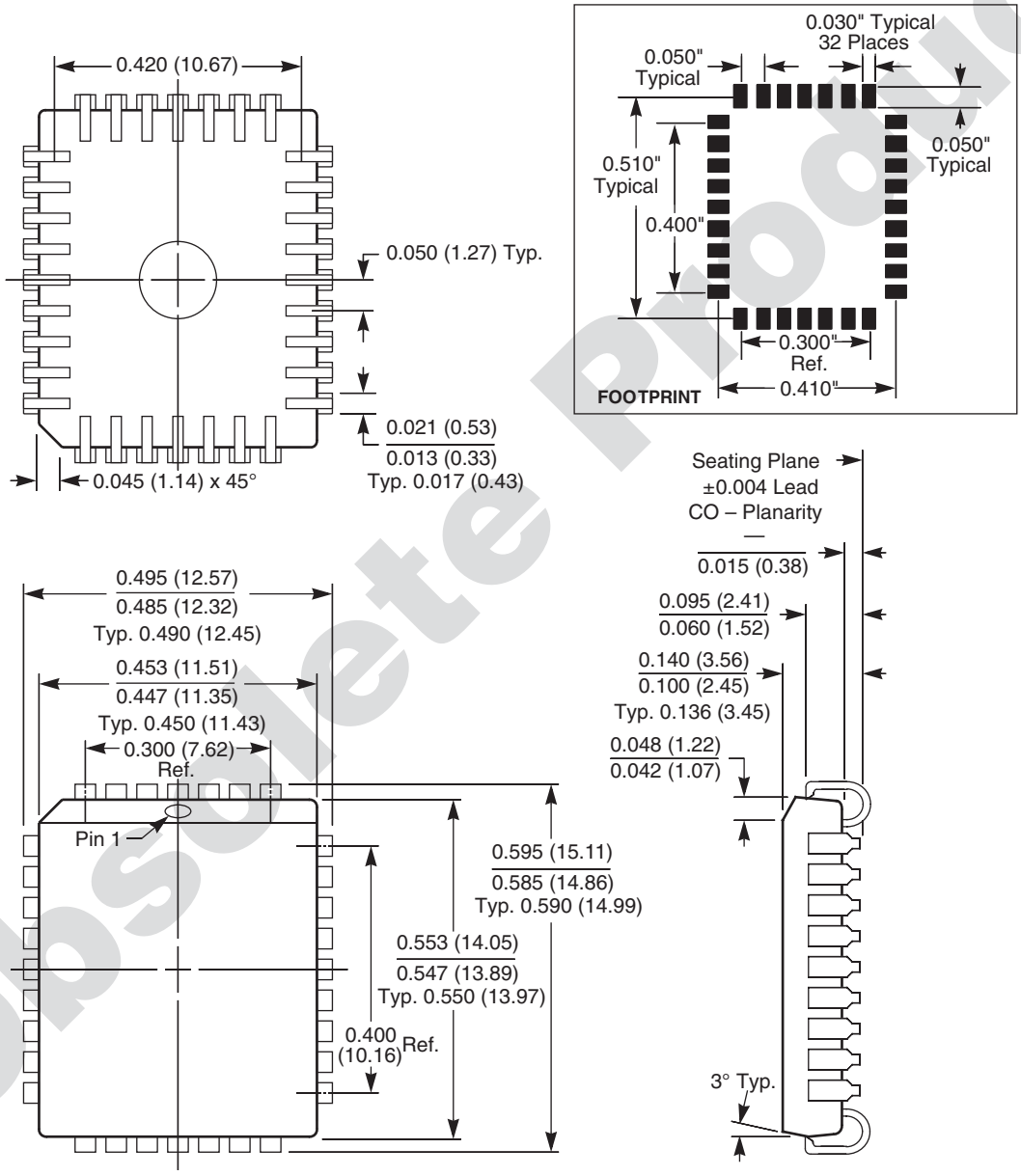
When $\overline{WE}$ is HIGH the chip consumes only standby current.

The overall average current drawn by the part depends on the following items:

1. CMOS or TTL input levels
2. The time during which the chip is disabled ($\overline{CE}$ HIGH)
3. The cycle time for accesses ($\overline{CE}$ LOW)
4. The ratio of READs to WRITEs
5. The operating temperature
6. The V_{CC} level

PACKAGING INFORMATION

32-Lead Plastic, PLCC, Package Code J32



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.