ECL DIGITAL DELAY LINES
SERIES E10 - ECL 10K INTERFACED
SERIES E100 - ECL 100K INTERFACED

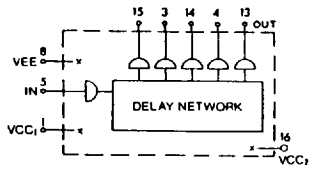
NEW PRODUCT

- Industry's widest selection!
- Economical cost, prompt delivery
- Fast 2nSec rise time typical
- Standard 16 pin DIP on ECL 10K, 24 pin DIP on ECL 100K
- Surface Mount design available
- High-Speed CMOS design available

TEST CONDITIONS @25°C
Pulse width: 2× Total Delay
Pulse Spacing: 5× Total Delay
Pulse Amplitude: -1.0V provided by open emitter ECL 10K gate
Supply Voltage (VEE): 5.2VDC ECL 10K, -4.5 VDC ECL 100K
Ground (Vcc): 0V
ECL 10K outputs connected to external pull down 100Ω resistor to -2V
ECL 100K outputs connected to external pull down 50Ω resistor to -2V
Total Delay and Tap tolerance: ±5% or ±1nS whichever is greater

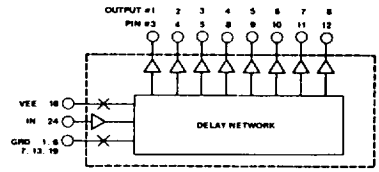
TYPE E105 - ECL10K 5 TAP

Total Delay (nS)	Tap Delay (nS)	SCHEMATIC
10	2	
15	3	
20	4	
25	5	
30	6	
40	8	
50	10	
60	12	
80	16	
100	20	



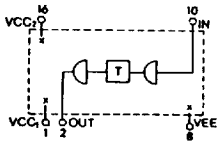
TYPE E1008 - ECL100K 8 TAP

Total Delay (nS)	Tap Delay (nS)	SCHEMATIC
8	1	
16	2	
24	3	
32	4	
40	5	
48	6	
56	7	
64	8	
72	9	
80	10	
160	20	
200	25	



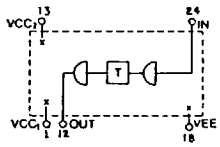
TYPE E101 - ECL10K SINGLE OUTPUT

Delay (nS)	SCHEMATIC
5	
10	
15	
20	
25	
50	
75	
100	



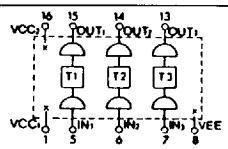
TYPE E1001 - ECL100K SINGLE OUTPUT

Delay (nS)	SCHEMATIC
5	
10	
15	
20	
25	
50	
75	
100	
150	
200	



TYPE E103 - ECL10K 3 INDEPENDENT DELAYS *

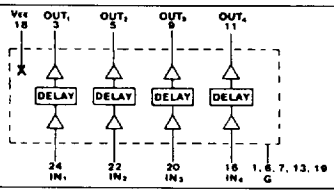
Delay (nS)	SCHEMATIC
5	
10	
15	
20	
25	
50	



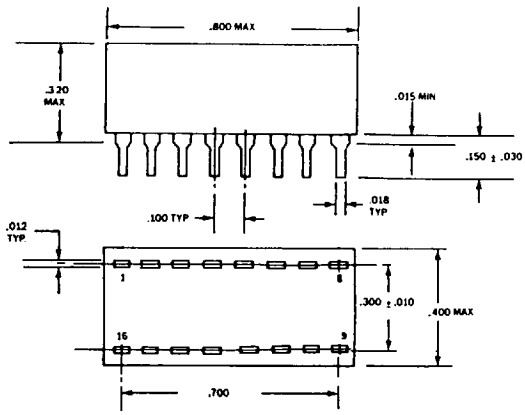
* Also available in a double delay output

TYPE E1004 - ECL100K 4 INDEPENDENT DELAYS

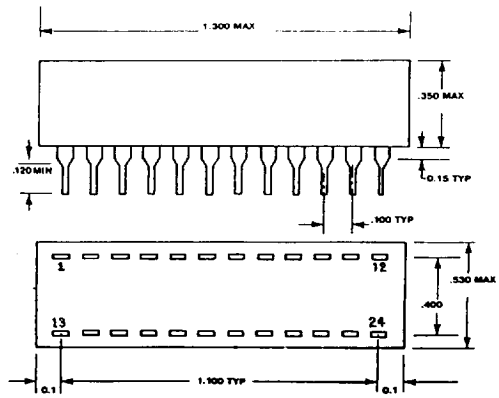
Delay (nS)	SCHEMATIC
5	
10	
15	
20	
25	
50	
75	
100	



10K ECL DIMENSIONS
(unused pins are removed)



100K ECL DIMENSIONS
(unused pins are removed)



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