

SERIES 630 5-TAPS 8 PIN SIP H-CMOS DIGITAL DELAY MODULES

- 8 Pin Single-In-Line Package • H-Cmos Logic
- 5 Equally Spaced Taps

Specifications:

- Supply Voltage : 4.75 to 5.25VDC
- Logic 1 Input Voltage : 3.2v
- Logic 0 Input Voltage : 0.9v
- Logic 1 Output Voltage : 4.5v
- Logic 0 Output Voltage : 0.1v
- Input Current : 1 μ A Max
- Supply Current : ICCH = 5mA, ICCL = 20 μ A
- Fan-Out : 10 LSTTL Loads Min
- Rise-Time : 8NS TYP. (measured from 0.8v to 2.0v)
- Operating Temp Range : 0°C to 70°C
- Temp Coefficient : 300 PPM/°C

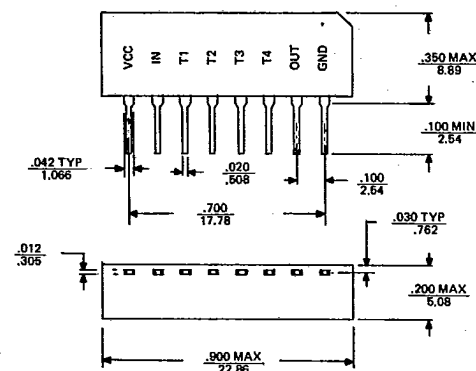
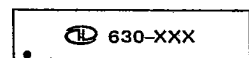
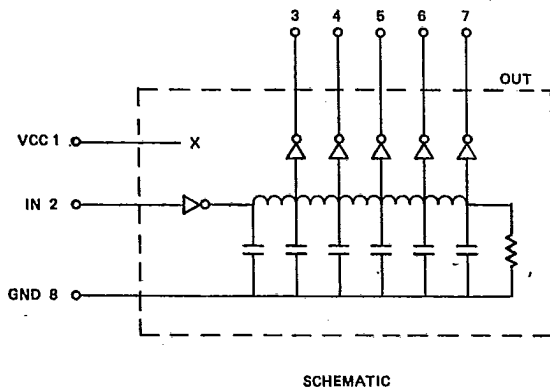


Electrical Specifications at 25°C (Measured with no Loads on Taps)

Part Number	Total Delay Nanosecond (1)	Tap To Tap Delay NSEC (1)
630-4*	4 $\pm$ 1	1 $\pm$ 0.5
630-5*	5 $\pm$ 1	1.2 $\pm$ 0.5
630-6*	6 $\pm$ 1	1.5 $\pm$ 0.5
630-8*	8 $\pm$ 2	2 $\pm$ 0.5
630-10*	10 $\pm$ 2	2.5 $\pm$ 0.5
630-12*	12 $\pm$ 2	3 $\pm$ 0.5
630-16*	16 $\pm$ 2	4 $\pm$ 0.6
630-25	25 $\pm$ 2	5 $\pm$ 0.8
630-30	30 $\pm$ 2	6 $\pm$ 1
630-35	35 $\pm$ 2	7 $\pm$ 1
630-40	40 $\pm$ 2	8 $\pm$ 1
630-45	45 $\pm$ 2.2	9 $\pm$ 1
630-50	50 $\pm$ 2.5	10 $\pm$ 2
630-60	60 $\pm$ 3	12 $\pm$ 2
630-75	75 $\pm$ 3.5	15 $\pm$ 2
630-100	100 $\pm$ 5.0	20 $\pm$ 2
630-125	125 $\pm$ 5.5	25 $\pm$ 2
630-150	150 $\pm$ 6.0	30 $\pm$ 3
630-175	175 $\pm$ 8.7	35 $\pm$ 3.5
630-200	200 $\pm$ 10	40 $\pm$ 4
630-250	250 $\pm$ 12.5	50 $\pm$ 5

Note: (1) Measured at 1.5v level leading edge.

*Time Delay measured with respect to 1st Tap.



INCHES .XXX $\pm$.010
MILLIMETERS .XX $\pm$.26