



128Kx32 SRAM MODULE PRELIMINARY*

FEATURES

- Access Times of 15, 17, 20, 25, 35ns
- Packaging:
 - 68 Lead, Plastic PLCC, 24.71 mm (0.973 inch) square
- Organized as 128Kx32
- Commercial and Industrial Temperature Ranges
- TTL Compatible Inputs and CMOS Outputs
- PJ Pinout for Commercial Applications
- G2 Pinout for Upgrade Path to Military Grade Device
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

* This data sheet describes a product under development, not fully characterized and is subject to change without notice.

FIG. 1 PIN CONFIGURATION FOR WPS128K32P-XPJX, PJ pinout for Commercial Applications

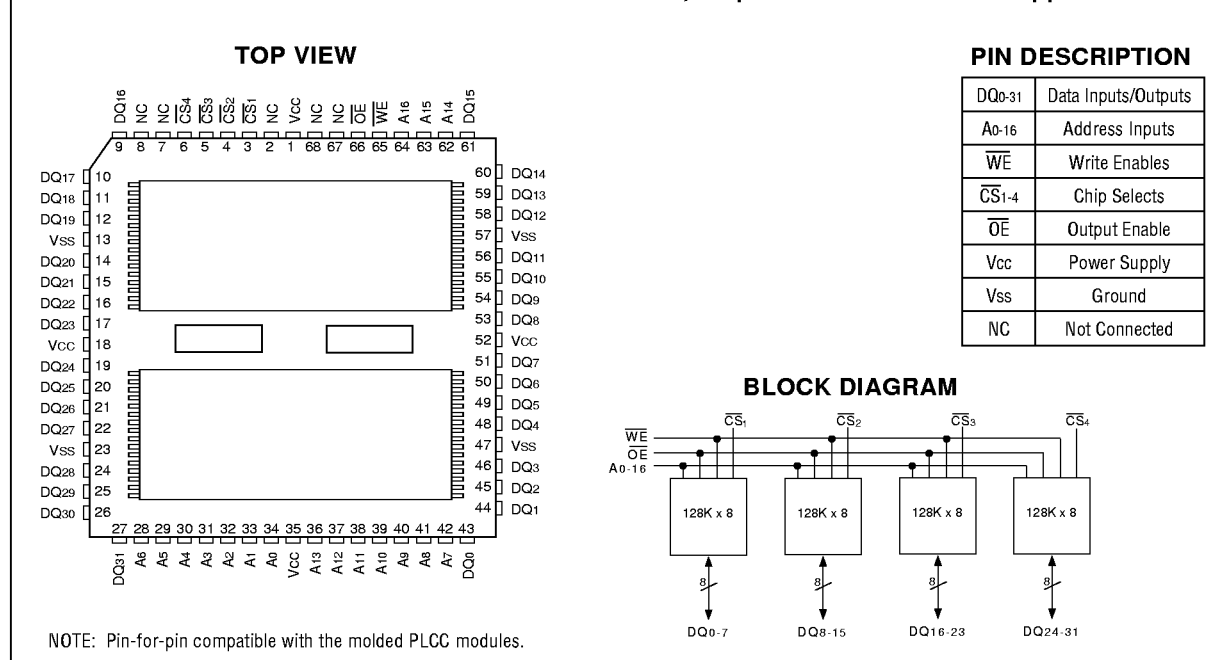
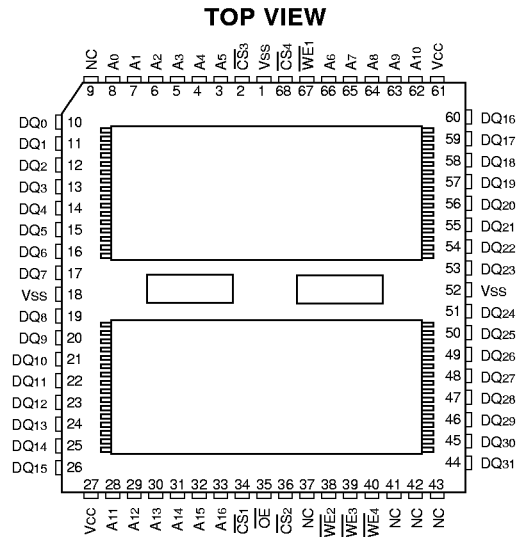




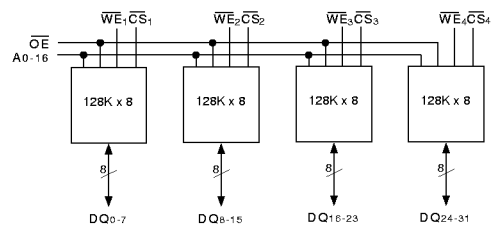
FIG. 2 PIN CONFIGURATION FOR WPS128K32G-XPJX, for upgrade to Military Grade Devices



PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Com.)	T _A	0	+70	°C
Operating Temperature (Ind.)	T _A	-40	+85	°C
Storage Temperature	T _{stg}	-55	+125	°C
Signal Voltage Relative to V _{ss}	V _g	-0.5	V _{cc} + 0.5	V
Supply Voltage	V _{cc}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(@ T_A = +25°C)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{cc}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{cc} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp (Com.)	T _A	0	+70	°C
Operating Temp (Ind.)	T _A	-40	+85	°C

Parameter	Symbol	Condition	Max	Unit
OE Capacitance	C _{OE}	V _{IN} = 0V, f = 1.0MHz	50	pF
WE Capacitance	C _{WE}	V _{IN} = 0V, f = 1.0MHz	20	pF
			20	
		G pinout		
		P pinout		
$\overline{CS}$ 1-4 Capacitance	C _{CS}	V _{IN} = 0V, f = 1.0MHz	20	pF
DQ0-31 Capacitance	C _{I/O}	V _{IN} = 0V, f = 1.0MHz	20	pF
A0-16 Capacitance	C _{AD}	V _{IN} = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(V_{cc} = 5V, V_{ss} = 0V, T_A = -40 to +85°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{cc} = 5.5, V _{IN} = V _{ss} to V _{cc}		10	μA
Output Leakage Current	I _{LO}	$\overline{CS}$ = V _{IH} , $\overline{OE}$ = V _{IH} , V _{OUT} = V _{ss} to V _{cc}		10	μA
Operating Supply Current x 32 Mode	I _{cc} x 32	$\overline{CS}$ = V _{IL} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{cc} = 5.5		450	mA
Standby Current	I _{SB}	$\overline{CS}$ = V _{cc} , $\overline{OE}$ = V _{IH} , f = 5MHz, V _{cc} = 5.5		50	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA, V _{cc} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA, V _{cc} = 4.5	2.4		V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{cc} - 0.3V

**AC CHARACTERISTICS**(V_{CC} = 5.0V, T_A = -40 to +85°C)

Parameter Read Cycle	Symbol	<u>-15</u>		<u>-17</u>		<u>-20</u>		<u>-25</u>		<u>-35</u>		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	15		17		20		25		35		ns
Address Access Time	t _{AA}		15		17		20		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		ns
Chip Select Access Time	t _{ACS}		15		17		20		25		35	ns
Output Enable to Output Valid	t _{OE}		8		9		10		12		20	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	3		3		3		3		3		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		0		0		0		0		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		7		8		8		10		20	ns
Output Disable to Output in High Z	t _{OHZ} ¹		7		8		8		10		20	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS(V_{CC} = 5.0V, T_A = -40 to +85°C)

Parameter Write Cycle	Symbol	<u>-15</u>		<u>-17</u>		<u>-20</u>		<u>-25</u>		<u>-35</u>		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	15		17		20		25		35		ns
Chip Select to End of Write	t _{CW}	11		12		13		15		25		ns
Address Valid to End of Write	t _{AW}	11		12		13		15		25		ns
Data Valid to End of Write	t _{DW}	9		10		10		10		20		ns
Write Pulse Width	t _{WP}	11		12		13		15		25		ns
Address Setup Time	t _{AS}	0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		0		0		0		0		ns
Output Active from End of Write	t _{OW} ¹	3		3		3		3		4		ns
Write Enable to Output in High Z	t _{WHZ} ¹		8		10		10		11		15	ns
Data Hold Time	t _{DH}	3		3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.



FIG. 3
TIMING WAVEFORM - READ CYCLE

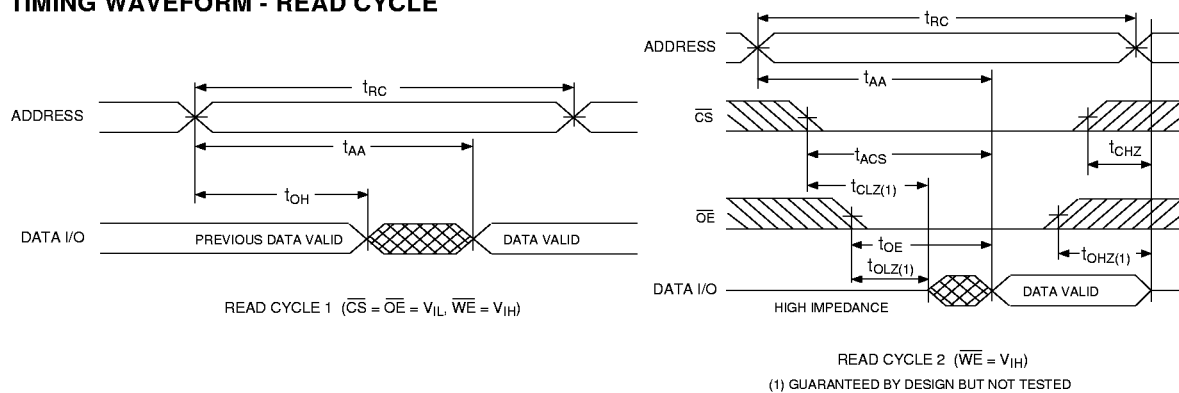


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED
($\overline{OE}$ IS INACTIVE - HIGH)

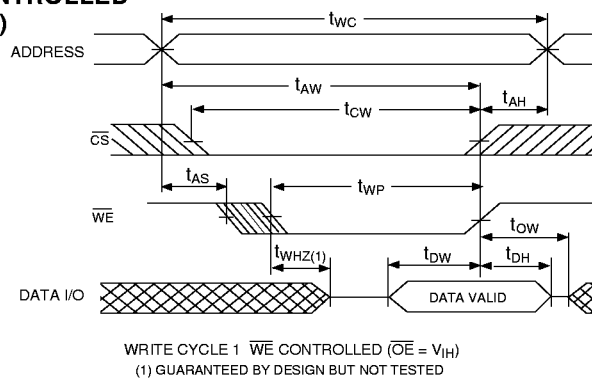
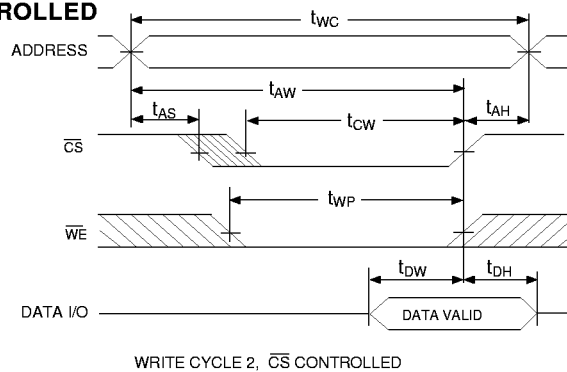
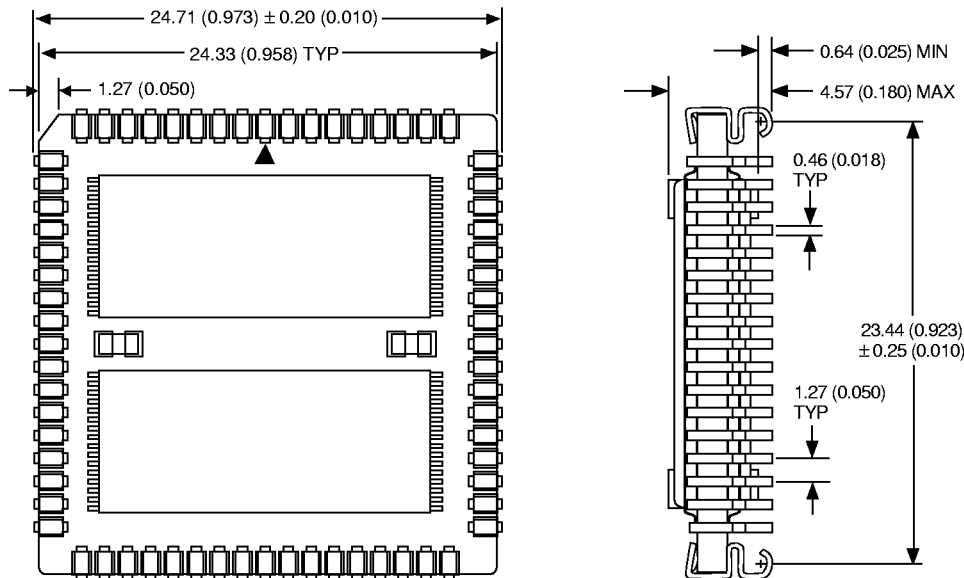


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

**PACKAGE 708: 68 LEAD PLCC**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P S 128K 32 X - XX P J X

DEVICE GRADE:

C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C

PACKAGE TYPE:

PJ = 68 Lead Plastic PLCC

ACCESS TIME (ns)**IMPROVEMENT MARK**

G = G2 pinout for upgrade path to military grade device
P = PJ pinout for commercial applications

ORGANIZATION, 128K x 32**SRAM****Plastic Multichip Module****WHITE MICROELECTRONICS**