

**LINE BUFFER**  
**5K-WORD BY 16-BIT/10K-WORD BY 8-BIT****Description**

The  $\mu$ PD485506 is a high speed FIFO (First In First Out) line buffer. Word organization can be changed either 5,048 words by 16 bits or 10,096 words by 8 bits. Its CMOS static circuitry provides high speed access and low power consumption.

The  $\mu$ PD485506 can be used for one line delay and time axis conversion in high speed facsimile machines and digital copiers.

Moreover, the  $\mu$ PD485506 can execute read and write operations independently on an asynchronous basis. Thus the  $\mu$ PD485506 is suitable as a buffer for data transfer between units with different transfer rates and as a buffer for the synchronization of multiple input signals.

There are four versions, E, K, P, X and L. This data sheet can be applied to the version X and L. These versions operate with different specifications. Each version is identified with its lot number (refer to **7. Example of Stamping**).

**Features**

- 5,048 words by 16 bits (Word mode) /10,096 words by 8 bits (Byte mode)
- Asynchronous read/write operations available
- Variable length delay bits; 21 to 5,048 bits or 10,096 bits (Cycle time: 25 ns)  
15 to 5,048 bits or 10,096 bits (Cycle time: 35 ns)
- Power supply voltage  $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$
- Suitable for sampling two lines of A3 size paper (16 dots/mm)
- All input/output TTL compatible
- 3-state output
- Full static operation; data hold time = infinity

**Ordering Information**

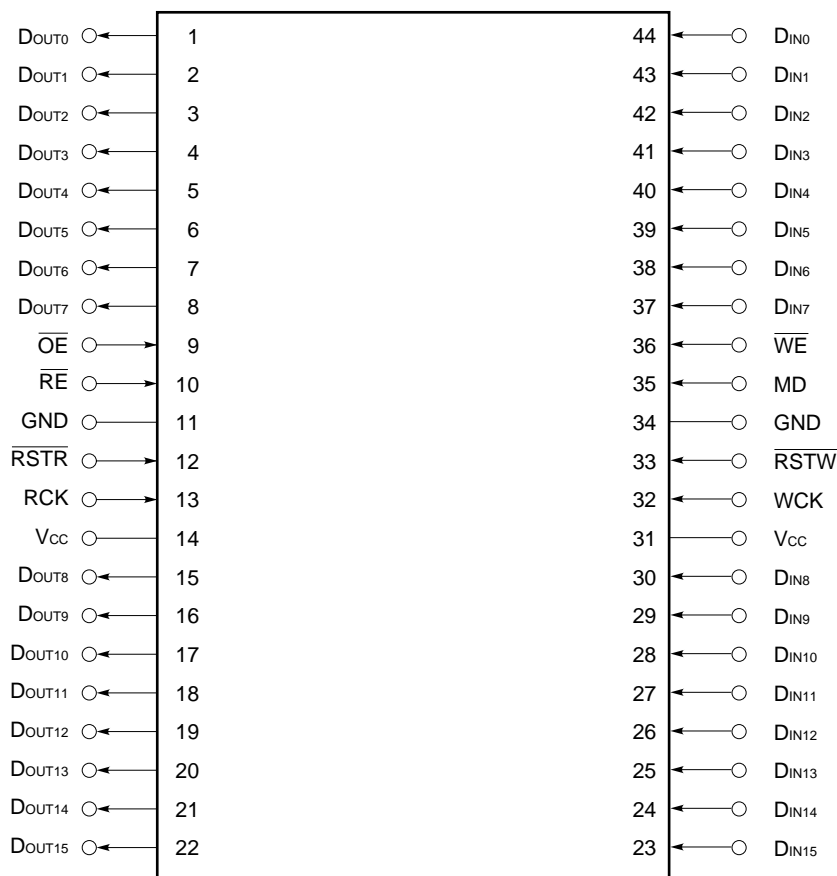
Part Number	R/W Cycle Time	Package
$\mu$ PD485506G5-25-7JF	25 ns	44-pin plastic TSOP (II) (10.16 mm (400))
$\mu$ PD485506G5-35-7JF	35 ns	

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

★ Pin Configuration (Marking side)

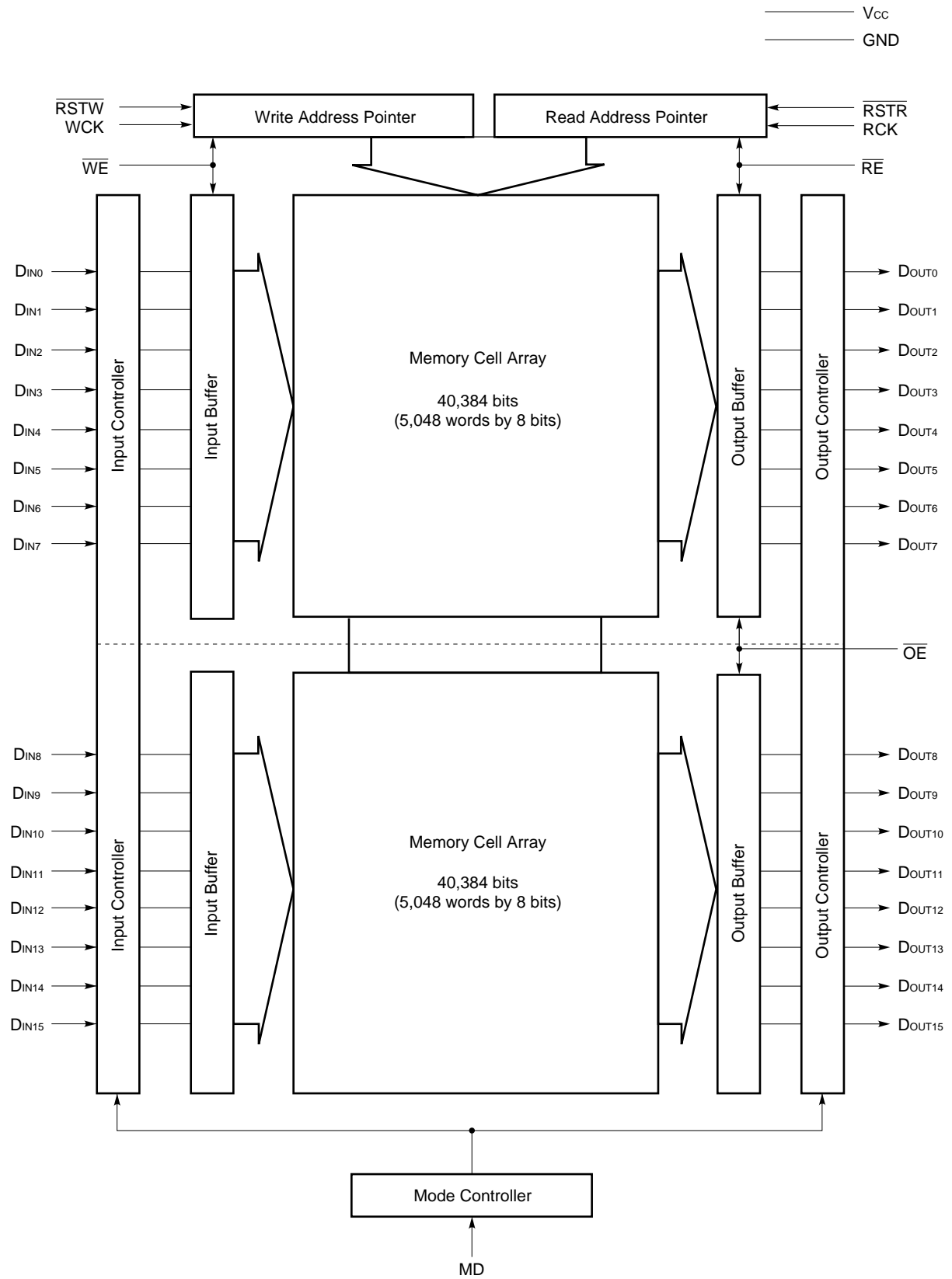
44-pin plastic TSOP (II) (10.16 mm (400))  
[μPD485506G5-7JF]



- DIN0 to DIN15 : Data Inputs
- DOUT0 to DOUT15 : Data Outputs
- WCK : Write Clock Input
- RCK : Read Clock Input
- WE : Write Enable Input
- RE : Read Enable Input
- OE : Output Enable Input
- RSTW : Reset Write Input
- RSTR : Reset Read Input
- MD : Mode Set Input
- Vcc : +5.0 V Power Supply
- GND : Ground

**Remark** Refer to **Package Drawing** for the 1-pin index mark.

Block Diagram



## 1. Input/Output Pin Function

Pin			I/O	Function
Pin Number	Symbol	Pin Name		
44 – 37, 30 – 23	D <sub>IN0</sub>   D <sub>IN15</sub>	Data Input	In	Write data input pins. The data inputs are strobed by the rising edge of WCK at the end of a cycle and the setup and hold times (t <sub>DS</sub> , t <sub>DH</sub> ) are defined at this point.
1 – 8, 15 – 22	D <sub>OUT0</sub>   D <sub>OUT15</sub>	Data Output	Out	Read data output pins. The access time is regulated from the rising edge of RCK at the beginning of a cycle and defined by t <sub>AC</sub> .
33	$\overline{\text{RSTW}}$	Reset Write Input	In	Reset input pin for the initialization of the write address pointer. The state of $\overline{\text{RSTW}}$ is strobed by the rising edge of WCK at the beginning of a cycle and the setup and hold times (t <sub>RS</sub> , t <sub>RH</sub> ) are defined.
12	$\overline{\text{RSTR}}$	Reset Read Input	In	Reset input pin for the initialization of the read address pointer. The state of $\overline{\text{RSTR}}$ is strobed by the rising edge of RCK at the beginning of a cycle and the setup and hold times (t <sub>RS</sub> , t <sub>RH</sub> ) are defined.
36	$\overline{\text{WE}}$	Write Enable Input	In	Write operation control signal input pin. When $\overline{\text{WE}}$ is in the disable mode (“H” level), the internal write operation is inhibited and the write address pointer stops at the current position.
10	$\overline{\text{RE}}$	Read Enable Input	In	Read operation control signal input pin. When $\overline{\text{RE}}$ is in the disable mode (“H” level), the internal read operation is inhibited and the read address pointer stops at the current position. The data outputs remain valid for that address.
9	$\overline{\text{OE}}$	Output Enable Input	In	Output operation control signal input pin. When $\overline{\text{OE}}$ is in the disable mode (“H” level), the data out is inhibited and the output changes to high impedance. The internal read operation is executed at that time and the read address pointer incremented in synchronization with the read clock.
32	WCK	Write Clock Input	In	Write clock input pin. When $\overline{\text{WE}}$ is enabled (“L” level), the write operation is executed in synchronization with the write clock. The write address pointer is incremented simultaneously.
13	RCK	Read Clock Input	In	Read clock input pin. When $\overline{\text{RE}}$ is enabled (“L” level), the read operation is executed in synchronization with the read clock. The read address pointer is incremented simultaneously.
35	MD	Mode Set Input	In	Mode set input pin. The level of MD gives the operation mode. When MD is in “L” level, 5,048 words by 16 bits configuration with D <sub>IN0</sub> - D <sub>IN15</sub> , D <sub>OUT0</sub> - D <sub>OUT15</sub> is enabled. When MD is in “H” level, 10,096 words by 8 bits configuration with D <sub>IN0</sub> - D <sub>IN7</sub> , D <sub>OUT0</sub> - D <sub>OUT7</sub> is enabled.

**2. Operation Mode**

μPD485506 is a synchronous memory. All signals are strobed at the rising edge of the clock (RCK, WCK). For this reason, setup time and hold time are specified for the rising edge of the clock (RCK, WCK).

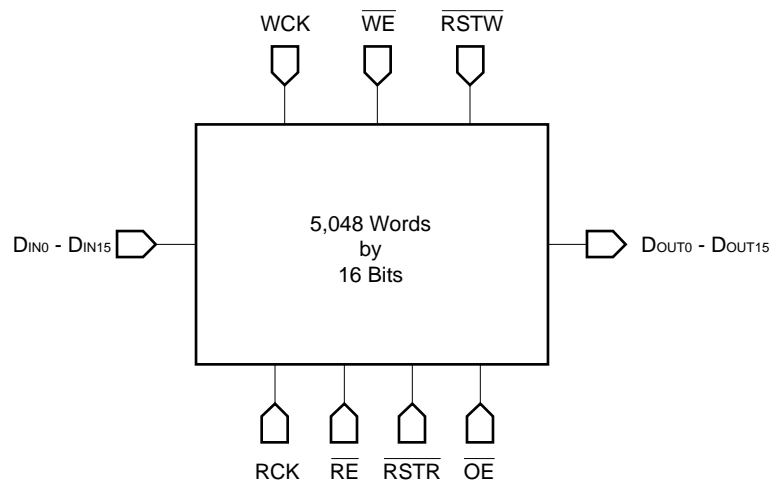
**2.1 Mode Set Cycle (5,048 words by 16 bits or 10,096 words by 8 bits organization)**

μPD485506 has a capability of selecting from two operation modes by judging the MD level when  $\overline{\text{RSTW}}$  or  $\overline{\text{RSTR}}$  is enabled in the reset cycle.

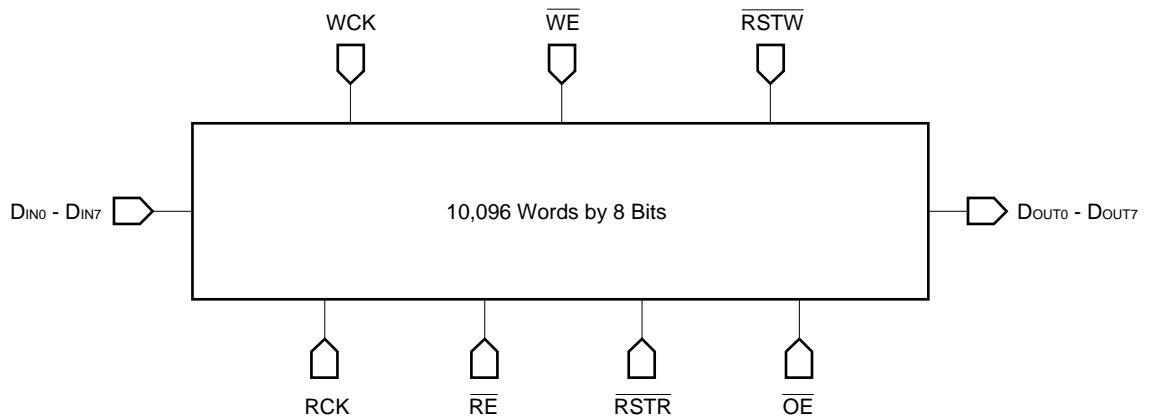
MD Level	Bit Configuration	Data Inputs/Outputs	Control Signal
“L”	5,048 words by 16 bits	D <sub>IN0</sub> - D <sub>IN15</sub>	WCK, $\overline{\text{WE}}$ , $\overline{\text{RSTW}}$
		D <sub>OUT0</sub> - D <sub>OUT15</sub>	RCK, $\overline{\text{RE}}$ , $\overline{\text{RSTR}}$
“H”	10,096 words by 8 bits	D <sub>IN0</sub> - D <sub>IN7</sub>	WCK, $\overline{\text{WE}}$ , $\overline{\text{RSTW}}$
		D <sub>OUT0</sub> - D <sub>OUT7</sub>	RCK, $\overline{\text{RE}}$ , $\overline{\text{RSTR}}$

**Caution** Don't change the MD level during a reset cycle. (See Figure 4.6, 7, 8, 9 Mode Set Cycle Timing Chart)

**5,048 Words by 16 Bits FIFO**



**10,096 Words by 8 Bits FIFO**



**Remark** Fix D<sub>IN8</sub> - D<sub>IN15</sub> to “L” or “H” level in the 10,096 words by 8 bits mode.

## 2.2 Write Cycle

When the  $\overline{WE}$  input is enabled ("L" level), a write cycle is executed in synchronization with the WCK clock input.

The data inputs are strobed by the rising edge of the clock at the end of a cycle so that read data after a one-line (5,048 bits or 10,096 bits) delay and write data can be processed with the same clock. Refer to Write Cycle Timing Chart.

When  $\overline{WE}$  is disabled ("H" level) in a write cycle, the write operation is not performed during the cycle which the WCK rising edge is in the  $\overline{WE} = \text{"H"}$  level ( $t_{WEW}$ ). The WCK does not increment the write address pointer at this time.

Unless inhibited by  $\overline{WE}$ , the internal write address will automatically wrap around from 5,047 to 0 and begin incrementing again.

## 2.3 Read Cycle

When the  $\overline{RE}$  input is enabled ("L" level), a read cycle is executed in synchronization with the RCK clock input. When the  $\overline{OE}$  input is also enabled ("L" level) at that time, data is output after  $t_{AC}$ . Refer to Read Cycle Timing Chart.

When  $\overline{RE}$  is disabled ("H" level) in a read cycle, the read operation is not performed during the cycle which the RCK rising edge is in the  $\overline{RE} = \text{"H"}$  level ( $t_{REW}$ ). The RCK does not increment the read address pointer at this time.

## 2.4 Write Reset Cycle/Read Reset Cycle

After power up, the  $\mu$ PD485506 requires the initialization of internal circuits because the read and write address pointers are not defined at that time.

It is necessary to satisfy setup requirements and hold times as measured from the rising edge of WCK and RCK, and then input the  $\overline{RSTW}$  and  $\overline{RSTR}$  signals to initialize the circuit.

Write and read reset cycles can be executed at any time and the address pointer returns zero. Refer to Write Reset Cycle Timing Chart, Read Reset Cycle Timing Chart.

**Remark** Write and read reset cycles can be executed at any time and do not depend on the state of  $\overline{RE}$ ,  $\overline{WE}$  or  $\overline{OE}$ .

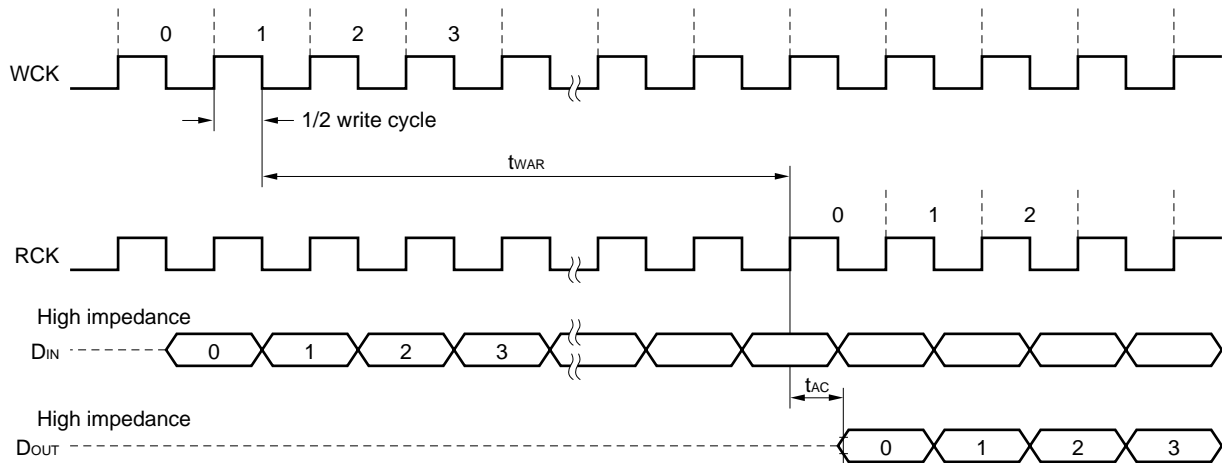
**Operation-related Restriction**

Following restriction exists to read data written in a write cycle.

Read the written data after an elapse of  $1/2$  write cycle +  $t_{WAR}$  since the write cycle ends (see **Figure 2.1**).

If  $t_{WAR}$  is not satisfied, the output data may undefined.

**Figure 2.1 Delay Bits Restriction Timing Chart**



**Remark** This timing chart describes only the delay bits restriction, and does not defines the  $\overline{WE}$ ,  $\overline{RE}$ ,  $\overline{RSTW}$ ,  $\overline{RSTR}$  signals.

### 3. Electrical Specifications

All voltages are referenced to GND.

#### Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	$V_T$		-0.5 <sup>Note</sup> to $V_{CC} + 0.5$	V
Supply voltage	$V_{CC}$		-0.5 to +7.0	V
Output current	$I_o$		20	mA
Operating ambient temperature	$T_A$		0 to 70	°C
Storage temperature	$T_{stg}$		-55 to +125	°C

**Note** -3.0 V MIN. (Pulse width = 10 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

#### Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{CC}$		4.5	5.0	5.5	V
High level input voltage	$V_{IH}$		2.4		$V_{CC} + 0.5$	V
Low level input voltage	$V_{IL}$		-0.3 <sup>Note</sup>		+0.8	V
Operating ambient temperature	$T_A$		0		70	°C

**Note** -3.0 V MIN. (Pulse width = 10 ns)

#### DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Operating current	$I_{CC}$				140	mA
Input leakage current	$I_i$	$V_i = 0$ to $V_{CC}$ , Other Input 0 V	-10		+10	μA
Output leakage current	$I_o$	$V_o = 0$ to $V_{CC}$ , $D_{OUT}$ : High impedance	-10		+10	μA
High level output voltage	$V_{OH}$	$I_{OH} = -1$ mA	2.4			V
Low level output voltage	$V_{OL}$	$I_{OL} = 2$ mA			0.4	V

#### Capacitance ( $T_A = 25$ °C, $f = 1$ MHz)

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	$C_i$				10	pF
Output capacitance	$C_o$				10	pF

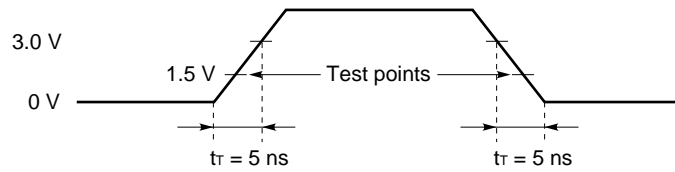


AC Characteristics (Recommended Operating Conditions unless otherwise noted) Notes 1, 2, 3

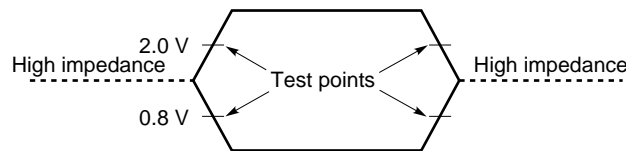
Parameter	Symbol	μPD485506-25		μPD485506-35		Unit	Notes
		MIN.	MAX.	MIN.	MAX.		
Write clock cycle time	t <sub>WCK</sub>	25		35		ns	
Write clock pulse width	t <sub>WCW</sub>	11		12		ns	
Write clock precharge time	t <sub>WCP</sub>	11		12		ns	
Read clock cycle time	t <sub>RCK</sub>	25		35		ns	
Read clock pulse width	t <sub>RCW</sub>	11		12		ns	
Read clock precharge time	t <sub>RCP</sub>	11		12		ns	
Access time	t <sub>AC</sub>		18		25	ns	
Write data-read delay time	t <sub>WAR</sub>	470		470		ns	
Output hold time	t <sub>OH</sub>	5		5		ns	
Output low-impedance time	t <sub>LZ</sub>	5	18	5	25	ns	4
Output high-impedance time	t <sub>HZ</sub>	5	18	5	25	ns	4
Input data setup time	t <sub>DS</sub>	7		10		ns	
Input data hold time	t <sub>DH</sub>	3		3		ns	
MD Set setup time	t <sub>MS</sub>	20		20		ns	
MD Set hold time	t <sub>MH</sub>	10		10		ns	
MD Set time	t <sub>MD</sub>	0		0		ns	5
Output low-impedance time (Mode change)	t <sub>LZM</sub>	5	18	5	25	ns	4
Output high-impedance time (Mode change)	t <sub>HZM</sub>	5	18	5	25	ns	4
RSTW/RSTR Setup time	t <sub>RS</sub>	7		10		ns	6
RSTW/RSTR Hold time	t <sub>RH</sub>	3		3		ns	6
RSTW/RSTR Deselected time (1)	t <sub>RN1</sub>	3		3		ns	7
RSTW/RSTR Deselected time (2)	t <sub>RN2</sub>	7		10		ns	7
WE Setup time	t <sub>WES</sub>	7		10		ns	8
WE Hold time	t <sub>WEH</sub>	3		3		ns	8
WE Deselected time (1)	t <sub>WEN1</sub>	3		3		ns	9
WE Deselected time (2)	t <sub>WEN2</sub>	7		10		ns	9
RE Setup time	t <sub>RES</sub>	7		10		ns	10
RE Hold time	t <sub>REH</sub>	3		3		ns	10
RE Deselected time (1)	t <sub>REN1</sub>	3		3		ns	11
RE Deselected time (2)	t <sub>REN2</sub>	7		10		ns	11
OE Setup time	t <sub>OES</sub>	7		10		ns	10
OE Hold time	t <sub>OEH</sub>	3		3		ns	10
OE Deselected time (1)	t <sub>OEN1</sub>	3		3		ns	11
OE Deselected time (2)	t <sub>OEN2</sub>	7		10		ns	11
WE Disable time	t <sub>WEW</sub>	0		0		ms	
RE Disable time	t <sub>REW</sub>	0		0		ms	
OE Disable time	t <sub>OEW</sub>	0		0		ms	
Write reset time	t <sub>RSTW</sub>	0		0		ms	
Read reset time	t <sub>RSTR</sub>	0		0		ms	
Transition time	t <sub>T</sub>	3	35	3	35	ns	

- Notes**
1. AC measurements assume  $t_r = 5 \text{ ns}$ .
  2. AC Characteristics test condition

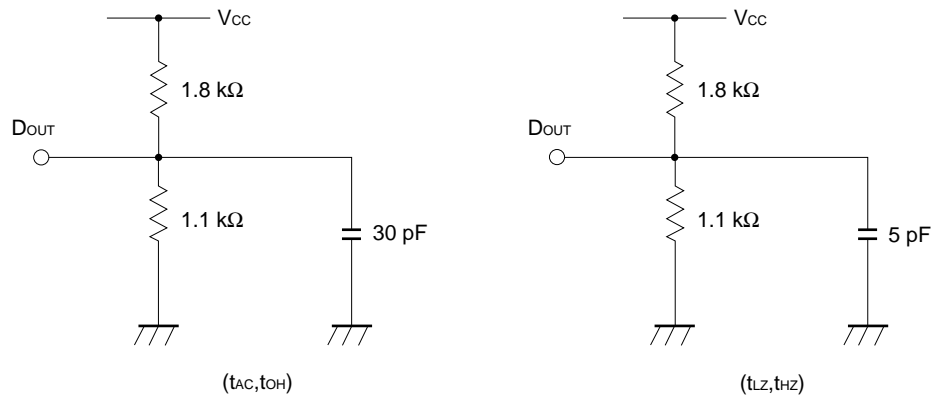
Input Timing Specification



Output Timing Specification

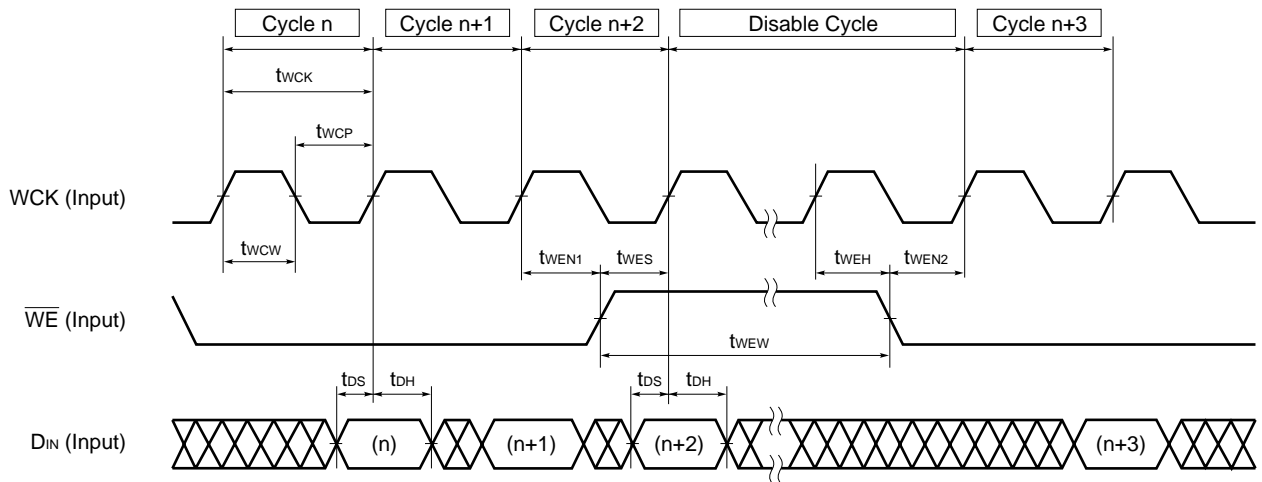


Output Loads for Timing



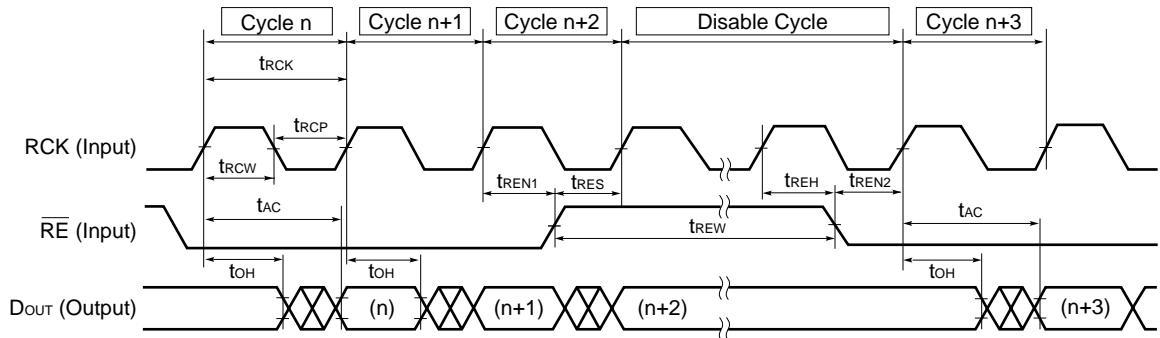
3. Input timing reference levels = 1.5 V. Output timing reference levels;  $V_{OH} = 2.0 \text{ V}$ ,  $V_{OL} = 0.8 \text{ V}$ .
4.  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{LZM}$  and  $t_{HZM}$  are measured at  $\pm 200 \text{ mV}$  from the steady state voltage. Under any conditions,  $t_{LZ} \geq t_{HZ}$  and  $t_{LZM} \geq t_{HZM}$ .
5. Mode set signal (MD) must be input synchronously with write reset signal ( $t_{RSTW}$  period) or read reset signal ( $t_{RSTR}$  period). Under this condition,  $t_{RSTW} = t_{MD}$  ( $t_{RSTR} = t_{MD}$ ).
6. If either  $t_{RS}$  or  $t_{RH}$  is less than the specified value, reset operations are not guaranteed.
7. If either  $t_{RN1}$  or  $t_{RN2}$  is less than the specified value, reset operations may extend to cycles preceding or following the period of reset operations.
8. If either  $t_{WES}$  or  $t_{WEH}$  is less than the specified value, write disable operations are not guaranteed.
9. If either  $t_{WEN1}$  or  $t_{WEN2}$  is less than the specified value, internal write disable operations may extend to cycles preceding or following the period of write disable operations.
10. If either  $t_{RES}$  or  $t_{REH}$ ,  $t_{OES}$  or  $t_{OEH}$  is less than the specified value, read disable operations are not guaranteed.
11. If either  $t_{REN1}$  or  $t_{REN2}$ ,  $t_{OEN1}$  or  $t_{OEN2}$  is less than the specified value, internal read disable operations may extend to cycles preceding or following the period of read disable operations.

**Write Cycle Timing Chart**



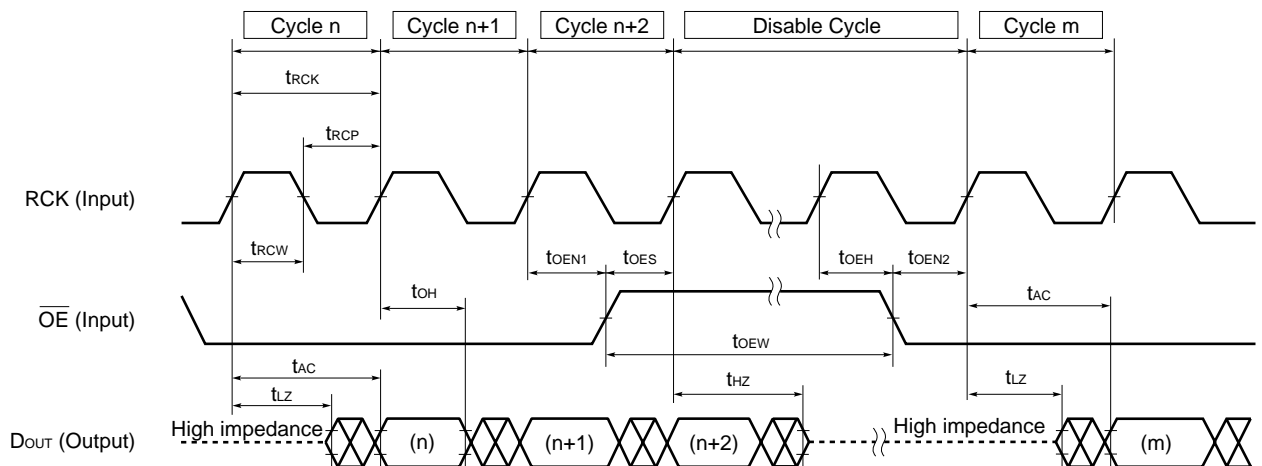
**Remark**  $\overline{RSTW}$  = "H" level

**Read Cycle Timing Chart ( $\overline{RE}$  Control)**



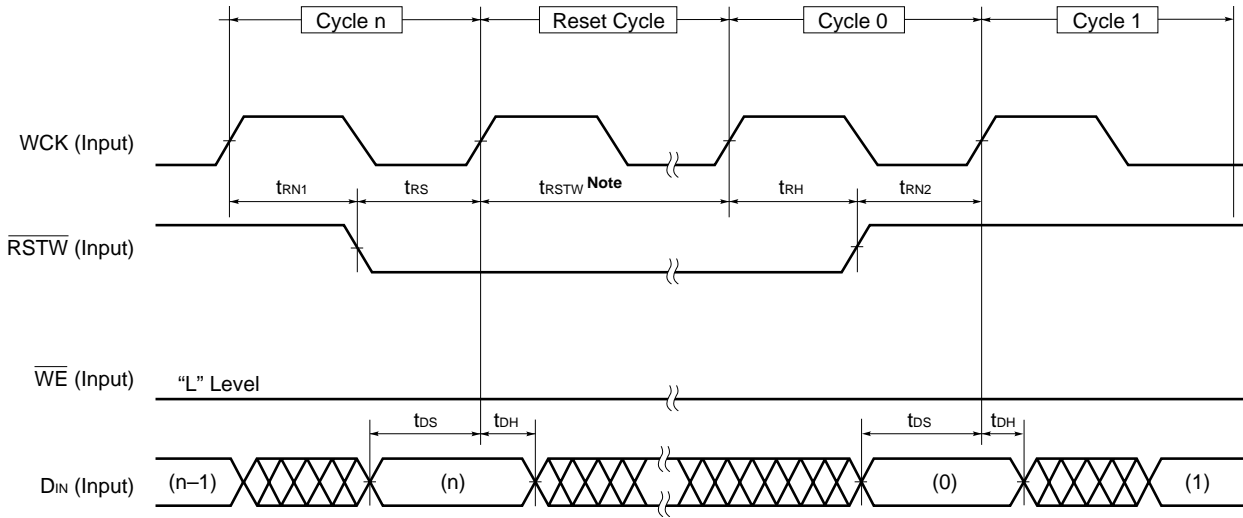
**Remark**  $\overline{OE}$  = "L" level,  $\overline{RSTR}$  = "H" level

**Read Cycle Timing Chart ( $\overline{OE}$  Control)**



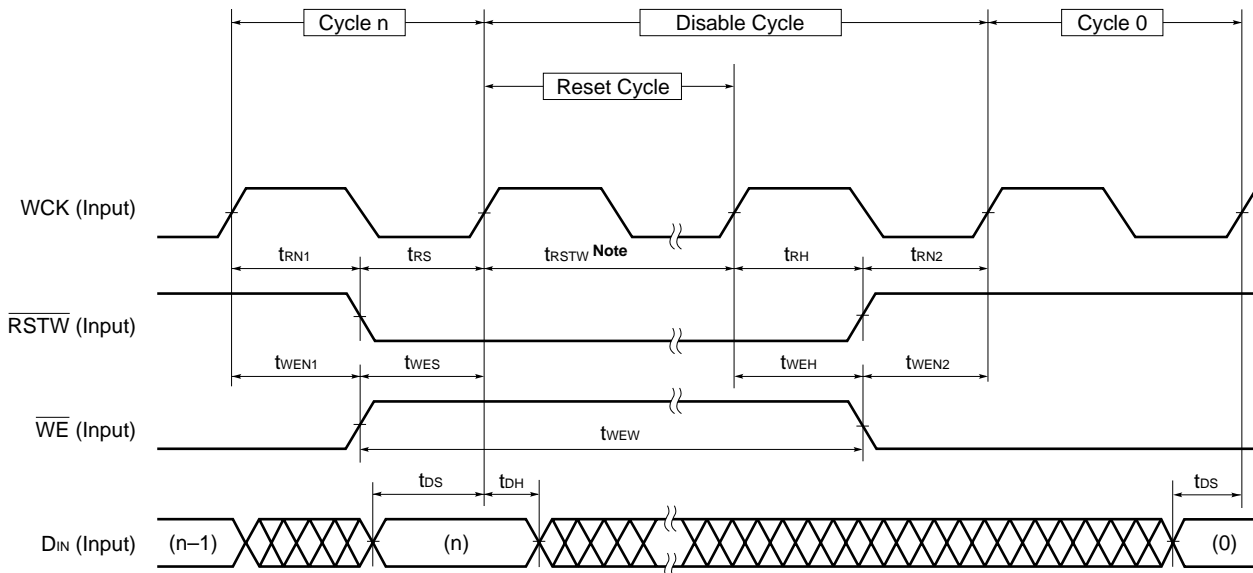
**Remark**  $\overline{RE}$  = "L" level,  $\overline{RSTR}$  = "H" level

**Write Reset Cycle Timing Chart ( $\overline{WE} = \text{Active}$ )**



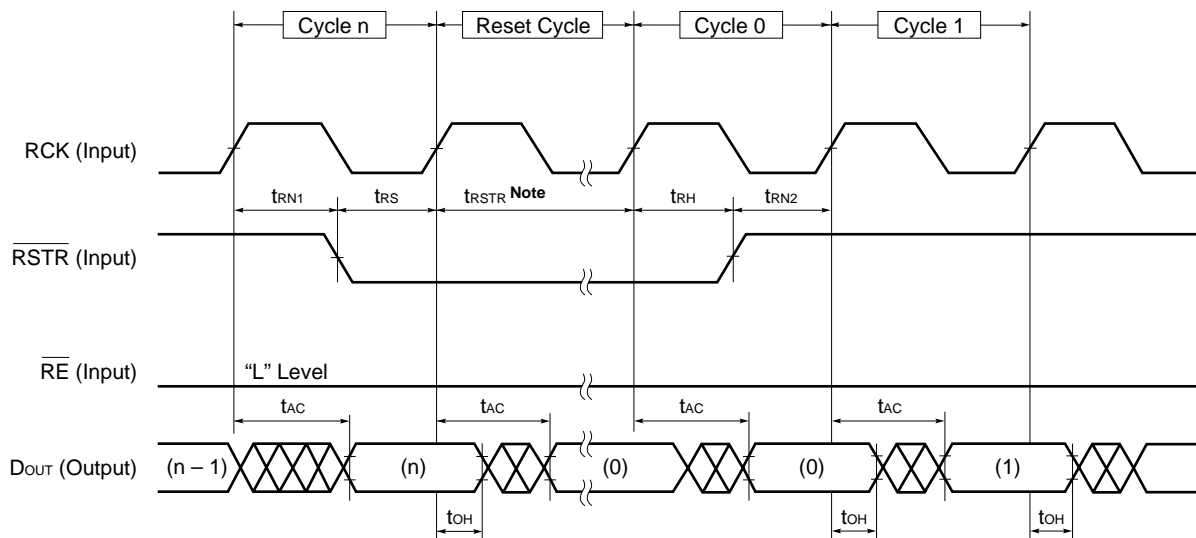
**Note** In write reset cycle, reset operation is executed even without a reset cycle ( $t_{RSTW}$ ).  
WCK can be input any number of times in a reset cycle.

**Write Reset Cycle Timing Chart ( $\overline{WE} = \text{Inactive}$ )**



**Note** In write reset cycle, reset operation is executed even without a reset cycle ( $t_{RSTW}$ ).  
WCK can be input any number of times in a reset cycle.

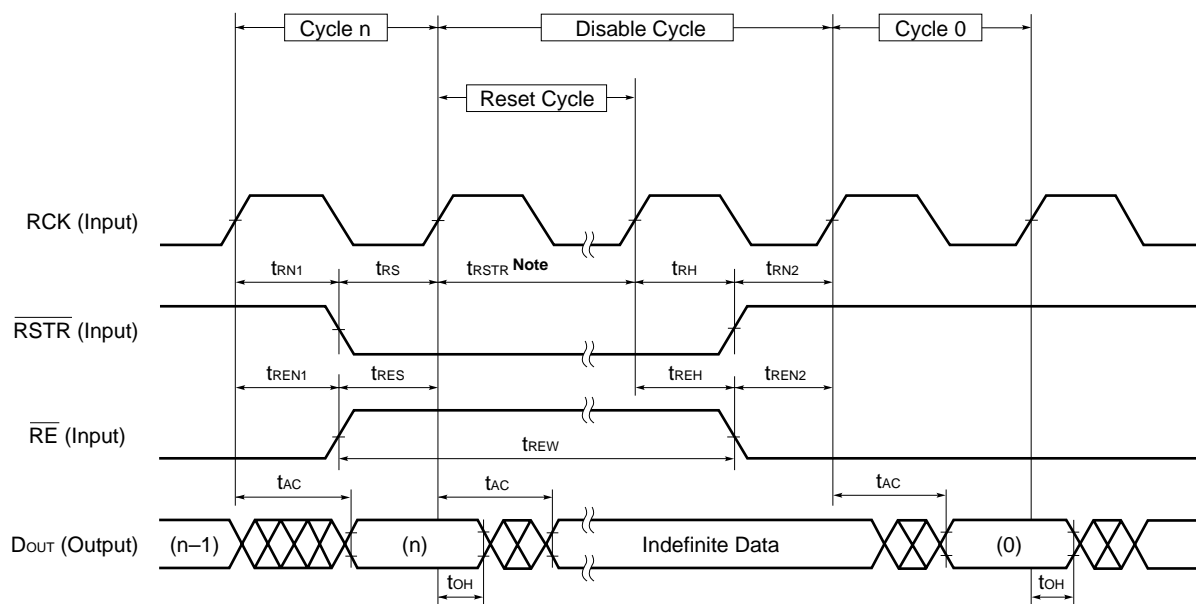
Read Reset Cycle Timing Chart ( $\overline{RE} = \text{Active}$ )



**Note** In read reset cycle, reset operation is executed even without a reset cycle ( $t_{RSTR}$ ).  
RCK can be input any number of times in a reset cycle.

**Remark**  $\overline{OE} = \text{"L" level}$

Read Reset Cycle Timing Chart ( $\overline{RE} = \text{Inactive}$ )



**Note** In read reset cycle, reset operation is executed even without a reset cycle ( $t_{RSTR}$ ).  
RCK can be input any number of times in a reset cycle.

**Remark**  $\overline{OE} = \text{"L" level}$



### 4.2 n Bit Delay

It is possible to make delay read from the write data with the μPD485506.

- (1) Perform a reset operation in the cycle proportionate to the delay length (see **Figure 4.3**).
- (2) Shift the input timing of write reset ( $\overline{RSTW}$ ) and read reset ( $\overline{RSTR}$ ) depending on the delay length (see **Figure 4.4**).
- (3) Shift the address by disabling  $\overline{RE}$  for the period proportionate to the delay length (see **Figure 4.5**).

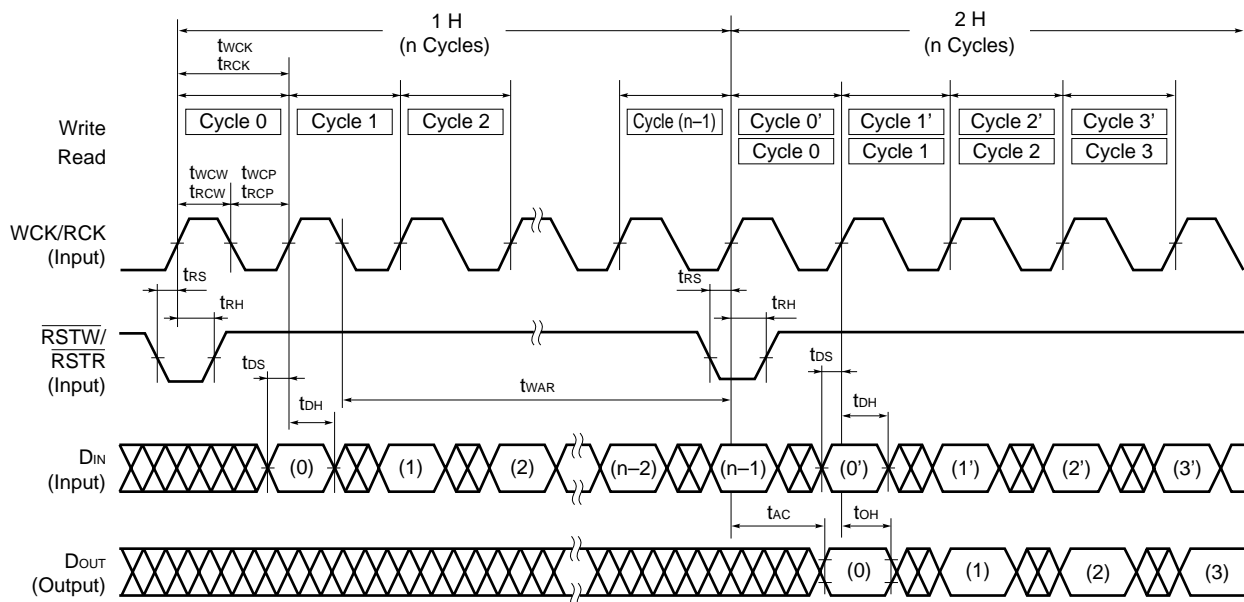
n bit: Delay bits from write cycle to read cycle correspond to a same address cell.

### Restrictions

Delay bits n can be set from minimum bits to maximum bits depending on the operating cycle time.  
Refer to **2. Operation Mode Operation-related Restriction**.

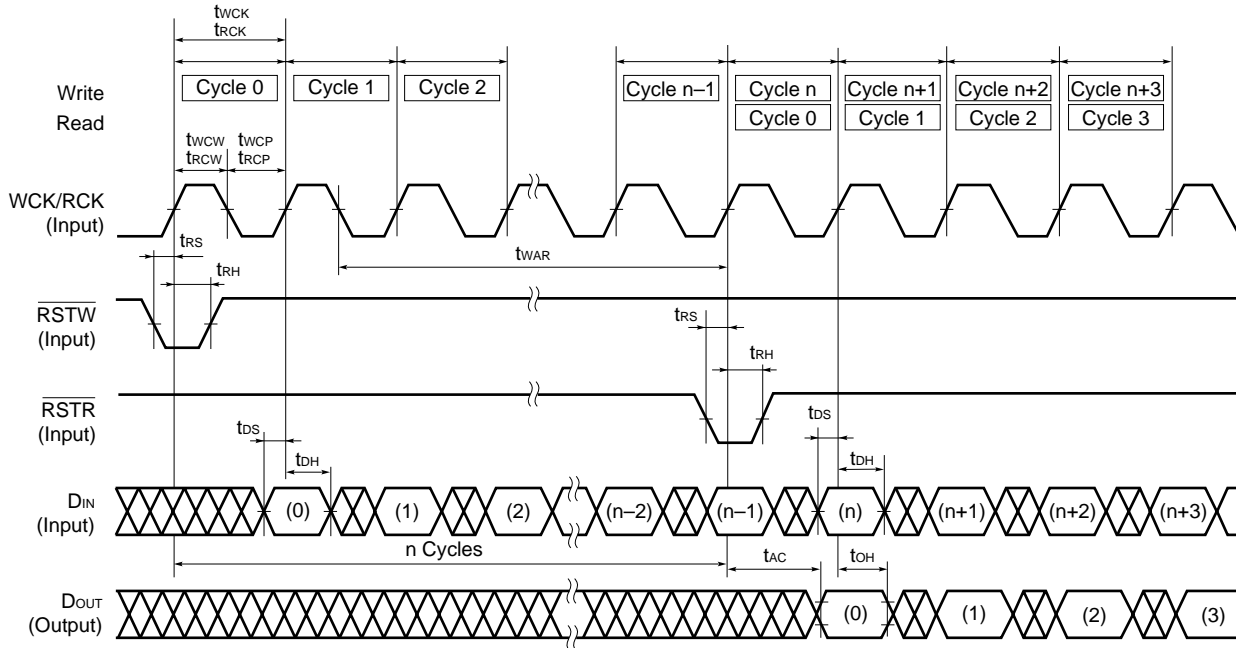
Cycle Time	MIN.	MAX.	
		MD = "L" Level	MD = "H" Level
25 ns	21 bits	5,048 bits	10,096 bits
35 ns	15 bits	5,048 bits	10,096 bits

**Figure 4.3 n-Bit Delay Line Timing Chart (1)**



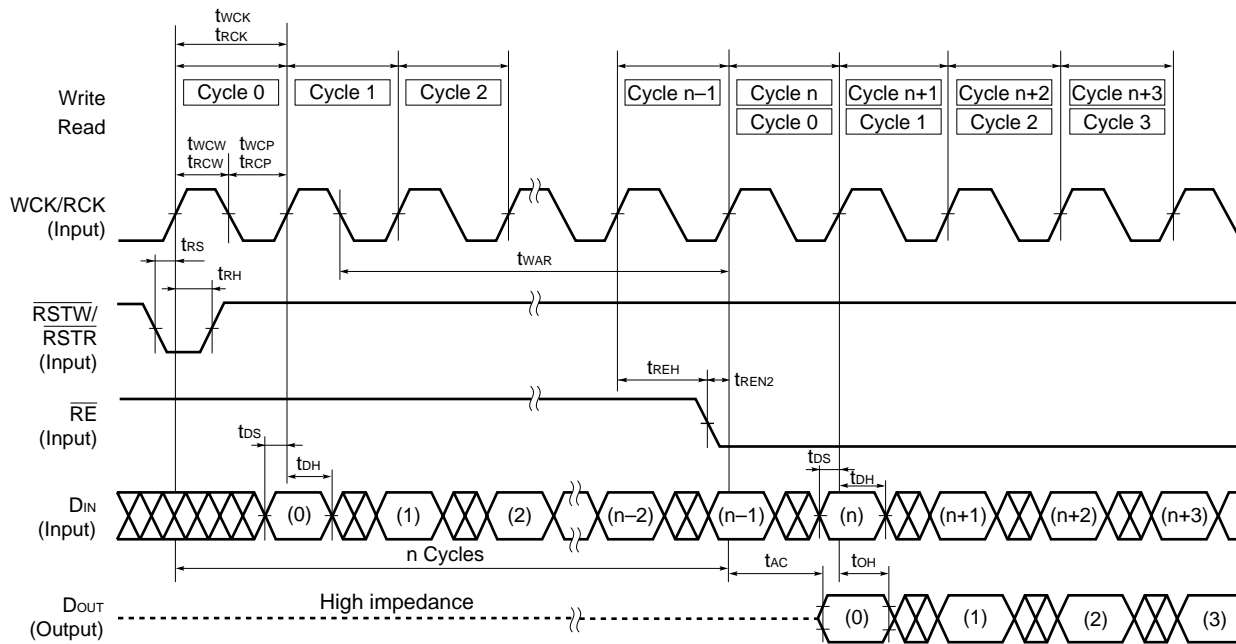
**Remark**  $\overline{RE}$ ,  $\overline{WE}$ ,  $\overline{OE}$  = "L" level

Figure 4.4 n-Bit Delay Line Timing Chart (2)



Remark  $\overline{RE}$ ,  $\overline{WE}$ ,  $\overline{OE}$  = "L" level

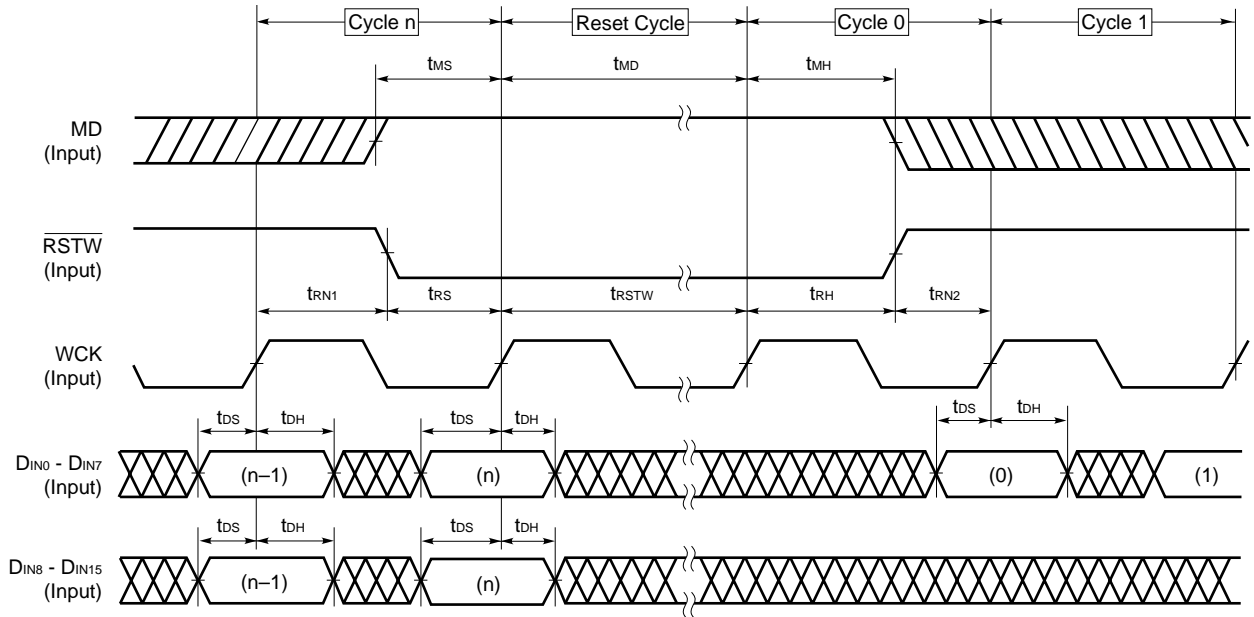
Figure 4.5 n-Bit Delay Line Timing Chart (3)



Remark  $\overline{WE}$ ,  $\overline{OE}$  = "L" level

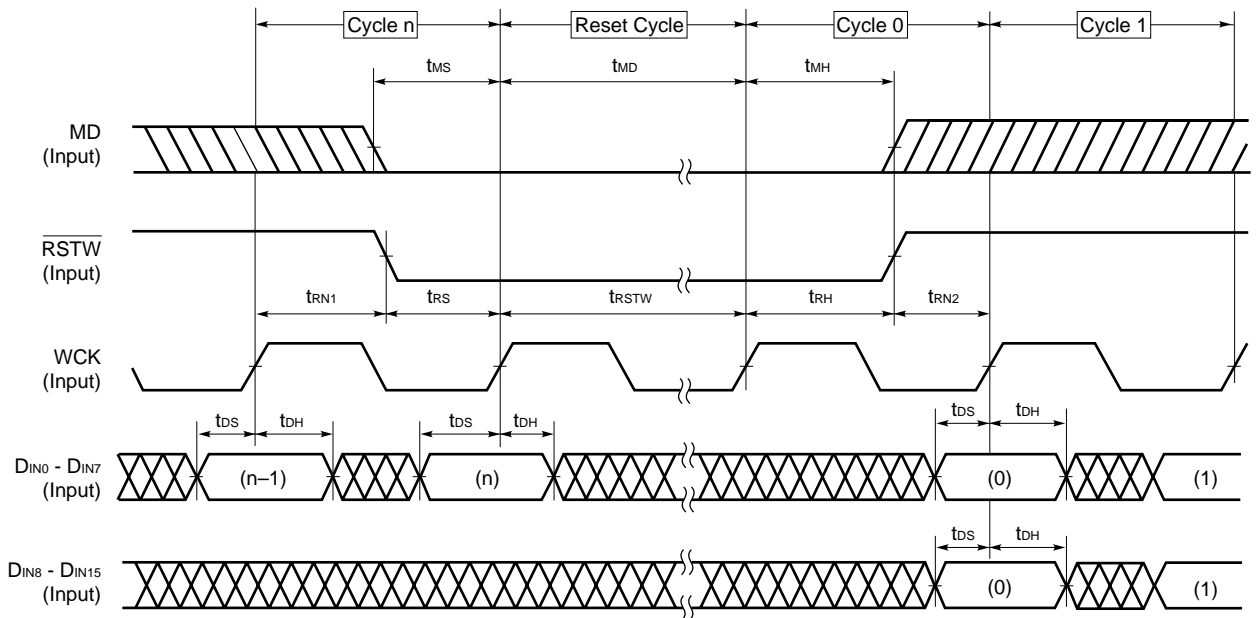


Figure 4.6 Mode Set Cycle Timing Chart (Write) (1)



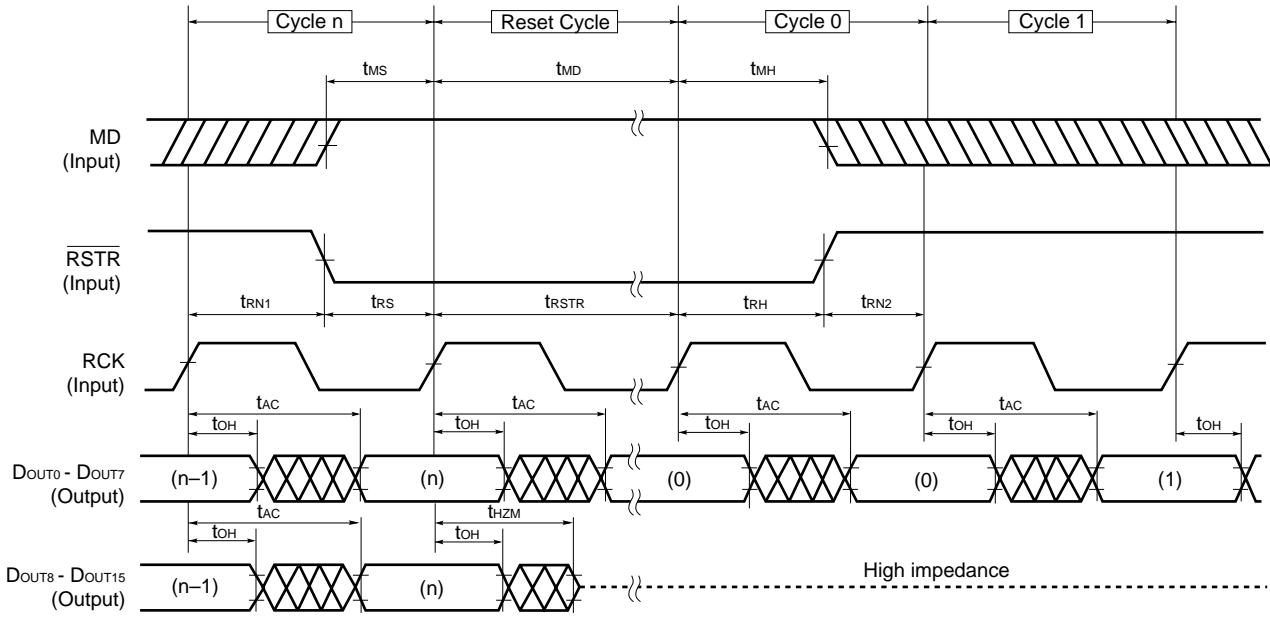
Remark  $\overline{WE}$  = "L" level

Figure 4.7 Mode Set Cycle Timing Chart (Write) (2)



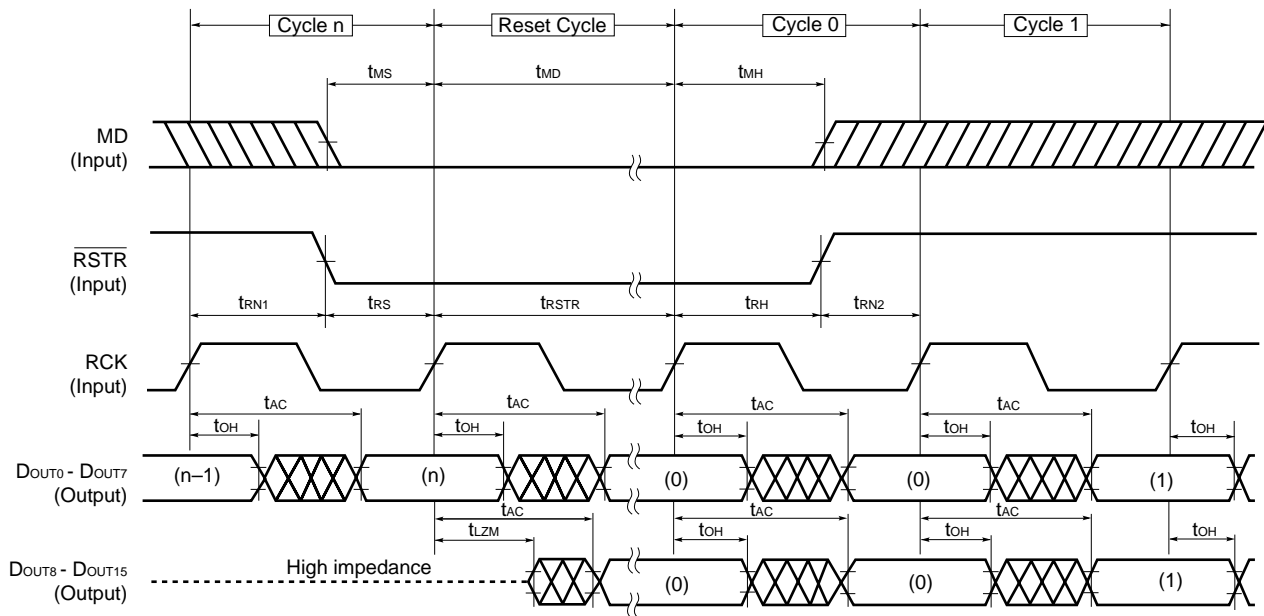
Remark  $\overline{WE}$  = "L" level

Figure 4.8 Mode Set Cycle Timing Chart (Read) (1)



Remark  $\overline{RE}, \overline{OE}$  = "L" level

Figure 4.9 Mode Set Cycle Timing Chart (Read) (2)



Remark  $\overline{RE}, \overline{OE}$  = "L" level

**4.3 Double-speed Conversion**

**Figure 4.10** shows an example timing chart of double-speed and twice reading operation ( $f_R = 2f_W$ , 5,048 by 2 cycles or 10,096 by 2 cycles<sup>Note</sup>) for a write operation ( $f_W = 5,048$  cycles or 10,096 cycles).

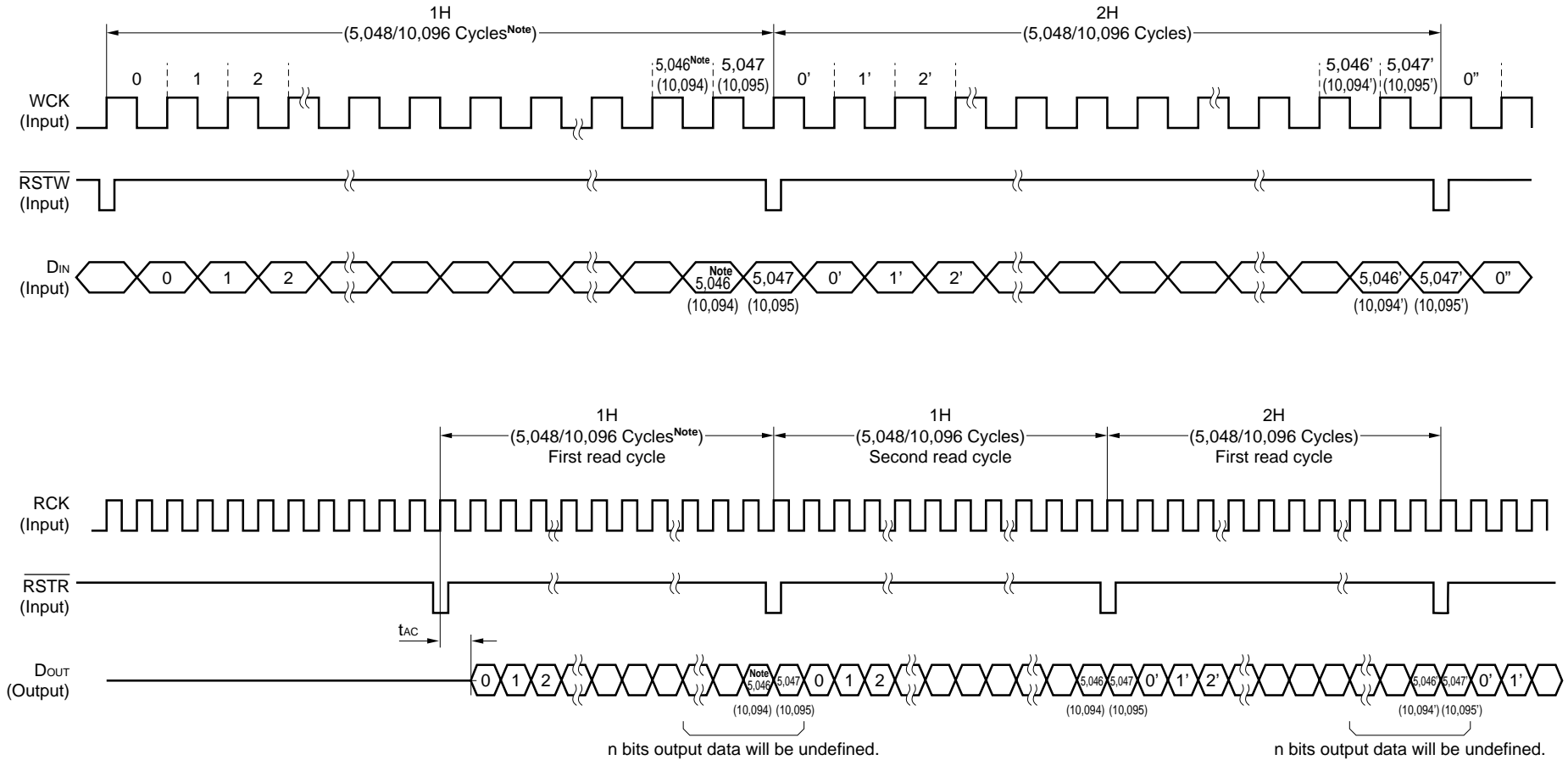
**Caution** The read operation collide with the write operation on the same line, last n bits output data (5,048 –n to 5,048/10,096 –n to 10,096) in the first read operation will be undefined (see Figure 4.10 Double-speed Conversion Timing Chart).

Undefined bits mentioned above depend on the cycle time.

Read Cycle Time	Undefined Bits
25 ns	21 bits
35 ns	15 bits

**Note** 5,048 cycles by 16 bits/10,096 cycles by 8 bits

Figure 4.10 Double-speed Conversion Timing Chart

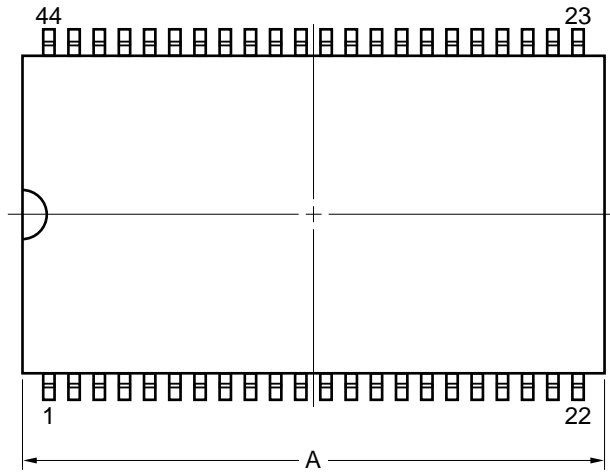


**Note** 5,048 cycles by 16 bits/10,096 cycles by 8 bits

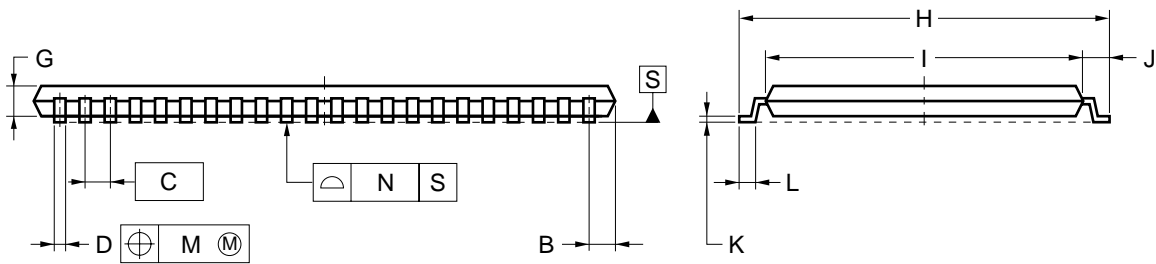
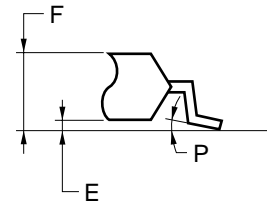
**Remark**  $\overline{RE}$ ,  $\overline{WE}$  = "L" level

★ 5. Package Drawing

44-PIN PLASTIC TSOP(II) (10.16 mm (400))



detail of lead end



**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	18.63 MAX.
B	0.93 MAX.
C	0.8 (T.P.)
D	0.32 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.05
F	1.2 MAX.
G	0.97
H	11.76±0.2
I	10.16±0.1
J	0.8±0.2
K	0.145 <sup>+0.025</sup> <sub>-0.015</sub>
L	0.5±0.1
M	0.13
N	0.10
P	3 <sup>+7°</sup> <sub>-3°</sub>

S44G5-80-7JF5-1

**6. Recommended Soldering Conditions**

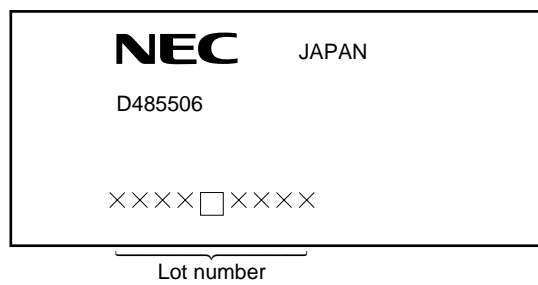
Please consult with our sales offices for soldering conditions of the μPD485506.

**Type of Surface Mount Device**

**μPD485506G5-7JF: 44-pin plastic TSOP (II) (10.16 mm (400))**

**7. Example of Stamping**

Letter E in the fifth character position in a lot number signifies version E, letter K, version K, letter P, version P, letter X, version X, and letter L, version L.



**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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