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SSI 32H4633
Hybrid Servo & Spindle Controller
Preliminary Data

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DESCRIPTION

The SSI 32H4633 is a CMOS monolithic integrated circuit housed in a 100-pin QFP and operates on a single +5V supply. In addition to supporting Winchester disk drives with embedded servo sectors and dedicated servo surface, it contains all timing and control functions necessary to start, drive, and brake a 3-phase, 4/8/12 pole brushless DC spindle motor without sensors. It also provides an 8-bit A/D converter at a conversion rate up to 250 kHz and a Motorola/Intel compatible bus interface (Motel) to popular microcontrollers such as the 8051 and 68HC11. The features for each functionally different section are summarized in the following:

FEATURES

Servo Head Positioning Control

- Servo control for Winchester disk drives with hybrid servo head positioning systems
- For use in microprocessor-based digital servo applications
- Accepts quadrature position signals N, Q from a dedicated servo demodulator
- 12-bit double-buffered cylinder crossing counter for dedicated seek algorithms
- Timing controller for embedded servo position burst sampling
- Peak detect and sample/hold circuits for up to four embedded servo bursts
- H-bridge MOSFET predriver for linear and rotary voice coil motor
- Class B linear mode and constant voltage retract mode
- Active head retract on power failure

Spindle Motor Speed Control

- 3-phase 4/8/12 pole bipolar/unipolar operation without need for sensors
- Precision speed regulation at 5400 RPM, with ±0.018% speed resolution
- "At speed" indication
- Motor peak current limiting function
- Pulse amplitude modulation (PAM) for bridge MOSFET drivers
- Dynamic braking function on power failure

Data Acquisition and Microprocessor Bus Interface

- Motel bus interface compatible with 8051 and 68HC11
- Ten internal registers and address decoding
- Internal 250 kHz 8-bit A/D and D/A converters

General Functions

- Voltage fault detection for up to two supply voltages
- Write gate guarding
- Low power CMOS design
- 100 pin QFP package

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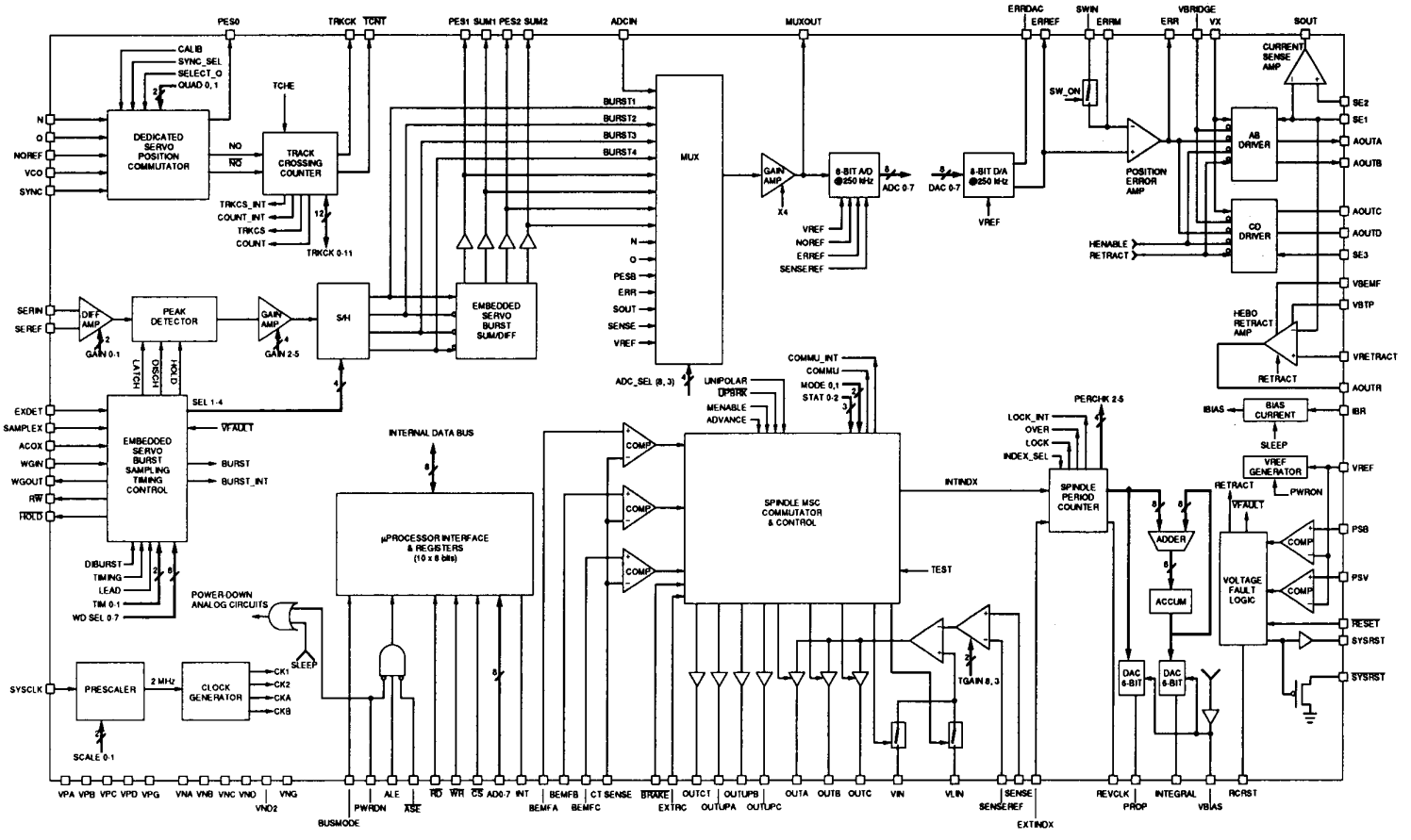

FIGURE 1: SSI 32H4633 Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H4633 can be divided into three major sections: servo head positioning control, spindle motor speed control, data acquisition and microprocessor bus interface.

SERVO HEAD POSITIONING CONTROL

The SSI 32H4633 is intended for a servo head positioner for Winchester disk drives with both embedded servo sectors and a dedicated servo surface. The servo head positioning control section contains the following functions:

1. Dedicated servo position processor
2. Embedded servo burst amplitude processor
3. Embedded servo burst timing controller
4. Servo position error amplifier
5. H-bridge MOSFET predriver
6. Actuator current sense
7. Voltage fault detection and servo head retract

Figure 2 shows dedicated servo position processor. Figure 3 shows embedded servo burst amplitude processor with embedded servo burst timing controller. Figure 4 shows servo position error amplifier, H-bridge MOSFET predriver, actuator current sense. Figure 5 shows voltage fault and servo head retract logic.

DEDICATED SERVO POSITION PROCESSOR

The dedicated servo position processor receives quadrature position information from a servo demodulator, such as SSI 32H6210, through analog inputs N, Q and NQREF. The NQREF is applied to establish a DC reference level for N and Q samples. N and Q are sampled at the falling edge of SYNC. The SYNC frequency, which is the servo frame rate on the dedicated servo surface, is generated from the servo demodulator and is no more than 500 kHz. The VCO provides the necessary clock signal to sample N and Q signals. The timing relationship among VCO, SYNC and N, Q is indicated in Figure 2. If it is not necessary to synchronize to N, Q samples, the SYNC input must be grounded and the SYNC SEL bit in the SERVO CONTROL register set HIGH. In this case, the SYSCLK input will be divided down internally to generate the frame rate to sample N and Q signals. The position processor compares N with both Q and -Q to generate digital signals NQ (N>Q) and $N\overline{Q}$ (N>-Q). Since N and Q signals span four tracks per period, NQ and $N\overline{Q}$ provide additional information on which track the head is positioned. In order to produce the position error signal PES0, the position processor selects N, Q, -N or -Q, based upon either the values of bits QUAD0 and QUAD1 when SELECT Q is enable; or the values of the digital signals NQ and $N\overline{Q}$ when SELECT Q is disabled. Note that the analog inputs N and Q to the position processor will switch to the DC reference level, NQREF, when the CALIB bit in the HYBRID SERVO CONTROL register is enabled. This allows calibrating the internal offset of the position error signal, PES0. For digital servo applications, N, Q and PES0 are provided to the internal multiplexed 8-bit A/D converter under µP control.

The SSI 32H4633 supports both hardware and software track counting techniques. The software track counting technique interfaces with bits NQ, $N\overline{Q}$ and TRKCS in the SERVO STATUS register. On each track crossing, either NQ or $N\overline{Q}$ changes state.

An internal timing hysteresis can be provided to prevent multiple state changes on NQ, $N\overline{Q}$ and TRKCS at low head velocities by setting the bit TCHE in the EMBEDDED SERVO GAIN CONTROL register. The TRKCS bit will be reset LOW when the SERVO STATUS REGISTER is read by the µP. The hardware track technique interfaces with TRKCK, an output clock intended to drive a hardware counter such as is available in the Intel 8051 family. TRKCK is normally LOW and pulses HIGH once whenever a track boundary is crossed. A 12-bit double-buffered down counter with programmable loading capability is implemented to aid seek algorithms. The counter is decremented at the LOW-TO-HIGH transition of TRKCK and the register is updated at the HIGH-TO-LOW transition of TRKCK. The 12-bit counter register stops updating after the LSB is read. This ensures consecutive reads provide information that corresponds to a single track. Therefore, one should read the LSB and then the MSB without exception. The counter will produce a LOW level on $\overline{TCNT}$ when the terminal count is reached. $\overline{TCNT}$ remains LOW until the counter is loaded with a new initial value.

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

The embedded servo burst amplitude processor extracts the fine head position error information from the embedded servo bursts. The circuit acquires up to 4 burst amplitudes BURST1, BURST2, BURST3, and BURST4 from a read data channel, such as the SSI 32P4620, through analog inputs SERIN and SEREF. The SEREF is applied to establish a DC reference level for the full wave-rectified analog signal SERIN.
To accommodate a wide range of servo burst amplitudes, the differential signal between SERIN and SEREF is scaled by a 2-bit programmable gain amplifier under µP control. The gain of the differential amplifier ranges from -6 dB to 3 dB as defined in the EMBEDDED SERVO GAIN CONTROL register. The output of the differential amplifier is then provided to a peak detector which captures the peak voltage within a time interval derived from the internal timing controller or an external timing source through SAMPLEX. The peak voltage is further scaled by a 4-bit programmable gain amplifier under µP control. Thus the gain error introduced by the peak detector can be accurately corrected with this programmable gain amplifier. The gain adjustment ranges from 0 dB to 3 dB in 0.2 dB steps, as defined in the EMBEDDED SERVO GAIN CONTROL register. Each of the following four S/H circuits transfers and holds the scaled peak voltages onto their respective holding capacitors during a time interval defined by the internal timing controller or an external timing source through ACQX. The outputs of S/H circuits, BURST1, BURST2, BURST3, and BURST4, are provided to the 8-bit A/D converter under µP control. Note that the timing windows to acquire the scaled peak voltages can be configurated in any order, as defined in the EMBEDDED SERVO TIMING WINDOW CONTROL register. Therefore, the µP can mix and commutate servo bursts to accommodate for a variety of servo burst formats and maintain the position error signal in a proper polarity. The timing controller also issues a timing signal to discharge the captive voltage for each servo burst.

The captive signals are provided to two difference circuits to extract the differential signals between BURST1, BURST2 and BURST 3, BURST4, respectively. Typically, these differential signals define the distance between the read head and the center of a data track and one of them should be zero while the read head is at the center of a data track. These outputs, available externally on PES1 and PES2, are provided to the 8-bit A/D converter under µP control. Also, two summers add BURST1, BURST2 and BURST3, BURST4, respectively, and their outputs at SUM1 and SUM2 are provided to the 8-bit A/D converter as well.

EMBEDDED SERVO BURST TIMING CONTROLLER

The embedded servo burst timing controller generates all the timing signals to sample the position bursts, as shown in Figures 3 and 4. These timing signals control the discharge, sample, and hold of the peak detector and the four S/H circuits. The EMBEDDED SERVO TIMING WINDOW CONTROL register can be programmed by the µP to select and sample the servo burst pairs in any order. The number of servo position bursts supported are either two or four. The DIBURST bit in the SERVO CONTROL register, when set HIGH, configures the internal timing controller to sample only two servo position bursts. When reset, four servo position bursts are sampled. During position burst sampling, $\overline{HOLD}$ and $R\overline{W}$ will be asserted and WGOUT held LOW.

An external timing controller may be used to provide all the timing signals for the discharge, sample, and hold of the peak detector and the four S/H circuits by setting the TIMING bit HIGH in the SERVO CONTROL register. Usually, in this mode, an external timing controller ASIC will be required to provide the timing signals at SAMPLEX and ACQX for servo position burst sampling while the internal servo timing controller is disabled.

SERVO POSITION ERROR AMPLIFIER

The servo driver has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal $\overline{RESET}$ is LOW. Otherwise the driver operates in linear mode. During linear operation, the microcontroller acquires servo burst amplitudes and analyzes them to establish a position error signal. This signal travels through an 8-bit D/A converter and is applied to an amplifier whose three connections, ERRM, ERREF and ERR, are available externally. External RC components may be used to establish the gain and bandwidth of this amplifier. Additional analog input via SWIN may be provided to this amplifier by setting the SW ON bit in the SERVO CONTROL register.

FUNCTIONAL DESCRIPTION (continued)

H-BRIDGE MOSFET PREDRIVER

The error signal ERR generated from the position error amplifier drives two precision differential amplifiers, each with a gain of 15. The differential amplifier outputs, AOUTA, AOUTB, AOUTC and AOUTD drive an external MOSFET bridge powered by VBRIDGE. Feedback from the MOSFET drain terminals via sense inputs SE1 and SE3 allow the differential amplifier gains to be established precisely. The voice coil actuator and a current sense resistor are connected in series between SE1 and SE3. Included in the output control circuitry is a crossover protection function which ensures class B operation by permitting only one MOSFET in each leg of the bridge to be in conduction. The crossover circuit can be adjusted for different MOSFET threshold voltages with a resistor connected to VX. The crossover circuitry can be commanded by the µP to shut down the MOSFET drivers and thus remove current to the external bridge.

MOTOR CURRENT SENSE

Motor current is sensed by a small resistor placed in series with the actuator. The voltage drop across the resistor is level-shifted and amplified by a differential amplifier with a gain of 4. The resulting signal, SOUT, is proportional to actuator current. This signal is externally fed back to the position error amplifier so that the error signal ERR represents the difference between the desired and actual actuator currents.

VOLTAGE FAULT DETECTION AND SERVO HEAD RETRACT

A voltage fault detector which can monitor up to two voltage supplies is included to prevent the actuator from responding to a false error signal during a power failure. Retract mode is started when a power supply failure is sensed by the PSB or PSV comparators or when $\overline{\text{RESET}}$ is pulled LOW externally. During retract, a constant voltage is applied across the actuator in order to cause a constant velocity head retraction. This is accomplished by applying the voltage stored on VBYP to AOUTD and by driving AOUTR with an amplifier that monitors SE1. The amplifier is powered by VBEMF. During retract, VRETRACT is biased by an internal voltage reference and determines the retract voltage. At other times, power is saved by disconnecting VRETRACT from the voltage reference and letting it be pulled to VBEMF by a high value resistor. External components (a diode, for instance) can be connected between VRETRACT and ground to modify the retract voltage.

An open-drain output, $\overline{\text{SYSRST}}$, which is active LOW while the servo driver is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the head is retracted. The amount of $\overline{\text{SYSRST}}$ delay is determined by the external capacitor which is connected to the pin, RCRST.

SPINDLE MOTOR SPEED CONTROL

A functional block diagram for the spindle motor control is shown in Figure 1. In conjunction with several external components, the spindle motor speed control provides the starting, accelerating, and precise rotational speed regulation functions. The circuit will control 4, 8, or 12 pole brushless DC motors without the need for Hall sensors. It will operate in either bipolar or unipolar drive mode. Control, configuration, and status monitoring are handled by the µP. The complete speed control loop is contained in the circuit and the µP is only required during start and to monitor status.

SPINDLE MOTOR START-UP

Motor starting is accomplished with the µP utilizing various features contained in the motor speed control circuitry. The µP can write to the commutation counter and set it to a predetermined value with STATE0, STATE1, STATE2 bits. The counter can then be incremented with the ADVANCE bit which also excludes internal commutations when set HIGH. Bits COMMU, PERCHK 2, 3, 4, 5 provide feedback to the µP on motor activity. The µP can enable the drivers with MENABLE and UNIPOLAR bits as required, as well as cause a "soft" brake with $\overline{\text{UPBRK}}$.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic which thereby advances and accelerates the spindle motor. The start-up process settles the motor initially by selecting the bits STATE0, STATE1, STATE2 in the SPINDLE CONTROL register to energize a proper motor winding. Motor current is enabled by setting the MEANABLE bit in the SPINDLE CONTROL register. The commutation state is advanced by providing ADVANCE pulses in the SPINDLE CONTROL register. The period of the ADVANCE pulses will be based upon the motor and load characteristics and decreased

gradually during the acceleration of the motor. The µP may look at the COMMU bit in the SPINDLE STATUS register for feedback indicating whether the motor has achieved a sufficient speed. Once the motor has achieved a sufficient speed, the µP will cease generating ADVANCE pulses and motor starting is thus completed.

SPINDLE MOTOR SPEED REGULATION

Motor speed regulation is accomplished with mixed analog and digital techniques, converting a motor speed error derived from a reference clock and a period counter into a voltage. The voltage translates into a motor current across the current sense resistor regulating the motor speed. The speed regulation loop consists of a period counter, proportional and integral channels, two 6-bit D/A converters and a linear transconductance amplifier.

In operation, the motor speed error is determined by measuring the period of each revolution with a 500 kHz clock signal. Period resolution is therefore 2 microseconds with the desired period being 5555 counts (11.11 milliseconds or 5400.54 RPM). Motor rotor position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers indicates rotor position. The back-emf is compared to a reference at CTSENSE and initiates "commutation events" when the appropriate comparison is made. The commutation is the sequential switching of the drive current to the motor windings. Since the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is thus required to delay actual commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external RC timing components connected at EXTRC. Because commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events," the one-shot circuit also provides a "noise filter" function which holds off retriggering further and blanks the back-emf comparison events for a period of time (approximately one half the commutation delay) after commutation. The commutation states are defined in the SPINDLE CONTROL register.

The period counter is loaded with a count of 5555 initially, and period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index-to-index time interval. The residual count is fed to the proportional D/A converter (5 bit plus sign) whose output is provided at PROP. No period error will output half of VBIAS at PROP, too short a period will output a value less than half of VBIAS, and too long a period will output a value greater than half of VBIAS depending on the amount of error.

When the residual count is within ± 15 counts of zero, the motor is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs at PROP and INTERGRAL are connected to VIN with an external resistor network. The resistor values should be selected to set the required loop response based upon motor requirements. The input VIN is the non-inverting input of the linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state. An external resistor is used to sense the current flowing through the drive transistor drain (and hence the motor coil current). The voltage across the sense resistor, the difference between SENSE and SENSEREF, is amplified by a programmable gain stage and fed to the inverting input of the transconductance amplifier. The gain of the programmable amplifier is determined by TGAIN0 and TGAIN1 bits.

Motor speed control includes a speed range check circuit, which provides in the SPINDLE STATUS register a LOCK status bit, when the motor is at the target speed within ±0.27%, along with OVER status bit, when the motor is over or under the target speed. The LOCK and OVER status bits are available to the µP for diagnostics and spindle fault conditions.

Additional low-speed period measurement data is available to the µP as the PERCHK2,3,4,5 bits in the SPINDLE STATUS register.

FUNCTIONAL DESCRIPTION (continued)

MOTOR PEAK CURRENT LIMITING

When the period error exceeds 256 counts too slow, the voltage at VLIM is selected as the control voltage in lieu of VIN. VLIM is to be used to set the motor peak current during start-up and acceleration.

MOTOR BRAKING

Fault conditions on power supplies and internal voltage reference generator will trigger an internal retract condition. The internal retract condition will cause all predriver outputs to the states which will turn the driver transistors off, allowing the motor to coast. $\overline{\text{BRAKE}}$ typically has a capacitor to ground attached and is connected to pin $\overline{\text{SYSRST}}$ via a resistor. $\overline{\text{SYSRST}}$ goes LOW in the retract condition, and thus $\overline{\text{BRAKE}}$ will go LOW after the RC delay. When $\overline{\text{BRAKE}}$ goes LOW, all lower drivers are activated to achieve dynamic braking of the motor. The circuitry for these operations is powered by the back-emf of the spindle motor and will operate without either 5 or 12 volt supply.

Dynamic braking can also be activated under µP control by setting $\overline{\text{UPBRK}}$ to LOW in the SPINDLE CONTROL register. During dynamic braking, the control loop is opened.

Two other motor speed control functions related to other circuit functions in the SSI 32H4633 are SLEEP mode and internal bias current. Two modes of SLEEP are provided for the SSI 32H4633, but the effect on the motor speed control is the same for both modes, i.e., all analog circuitry is de-biased, the clock is disabled, the upper driver outputs become logic HIGH (to turn off all upper drivers including the center tap if used), and the lower driver outputs become logic HIGH. The internal bias currents for analog functions are set by an external resistor connected between IBR and ground. A 22.6 KΩ, ±1% resistor should be used for proper operations.

EXTERNAL INDEX APPLICATION

Normal operation is performed with an internal index signal derived from the commutation counter (scaled via the MODE0 and MODE1 bits based upon the number of motor poles). The period of the index signals is measured and controlled by the circuit to result in a rotational rate of 5400 RPM. Within the range from 5384.9 to 5415.1 RPM, the spindle will be "in lock." After the motor is started and accelerated to speed (LOCK bit HIGH), an external index signal may be selected. Applying external index pulses at a rate within the lock range and setting INDEX SEL bit to HIGH will start the following sequence:

The circuit will complete the period measurement of the latest internal index period and then begin to measure the time between the last internal index and the next external index pulse. This will most likely be shorter than the nominal assuming the two events are asynchronous. If the period measured is not within 4.6% of the expected value, 11.11 milliseconds, the proportional and integral D/A converters will not be updated with a new correction value but will continue to output the previous value. The LOCK bit will be set to LOW indicating "out of lock." The next period measured will be between the first and second external index pulses and will presumably be within the lock range so that LOCK will be set to HIGH. If the period is within 4.5% of the desired value, the proportional and integral D/A converters will be updated. Similarly, during operation with external index, a missing index pulse would look like a gross speed error and no update on proportional and integral D/A converters will take place. The µP must perform the corrective actions in such cases, by examining LOCK bit, the PERCHK2,3,4,5 bits, and the source of the (missing) index pulses. A single missing index should require no action other than checking that LOCK returns to HIGH (in lock) in the next interval.

DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

Figure 1 shows data acquisition circuits along with the microprocessor bus interface. To facilitate microprocessor-based servo applications, the SSI 32H4633 contains a high-speed 8-bit A/D converter at a conversion rate up to 250 kHz, an 8-bit D/A converter, and Motel bus interface compatible with commonly used 12 MHz 8051 and 8 MHz 68HC11. The A/D converter can be multiplexed to sixteen different analog inputs by programming the ADC_SEL0, ADC_SEL1, ADC_SEL2 and ADC_SEL3 bits in the ADC ADDRESS register by the µP. The analog inputs can be scaled by a gain of 4 by setting the X4 bit HIGH. The output of the gain stage is available externally at MUXOUT for diagnostics. The A/D converter runs synchronously with the internal 500 kHz clock which is used for various circuits on the SSI 32H4633. Therefore, there would be a maximum of 2

microseconds of latency between a conversion request and the actual start of the conversion. Conversion is started by reading the A/D output register. The output is coded in 2's complement. Note that different voltage references corresponding to one half of the A/D full scale are used for different analog inputs as defined in the ADC ADDRESS register.

Similarly, the D/A converter runs synchronously with the internal 500 kHz clock and conversion is started by writing to the D/A input register. The output at ERRDAC is referenced to ERREF and is held constant between conversions.

The "Motel" interface to both Motorola and Intel µP's is provided for a direct connection to the SSI 32H4633. Three bus control signals are interpreted differently based upon the type of µP being used. The pin BUSMODE should be tied to HIGH for an Intel bus interface. The table below illustrates how both µPs connect to the SSI 32H4633. The $\overline{ASE}$ pin gates the AL/ASE input and can be used to shut off the ALE/AS to minimize noise on chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for Intel and Motorola µP interface are shown in Figures 5 and 6, respectively.

Intel	Motorola	32H4633
ALE	AS	ALE
$\overline{RD}$	DS;E; or Clock Phase 2	$\overline{RD}$
$\overline{WR}$	R/$\overline{W}$	$\overline{WR}$

REGISTER DESCRIPTIONS

The SSI 32H4633 contains ten 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 4-bit register address which is latched from inputs at AD0, AD1, AD2, and AD3 on the falling edge of ALE. The registers from 0 to 5 are read/write memory, the registers from 6 to 9 are write only. The registers are summarized in Table 1.

TABLE 1: SSI 32H4633 Internal Registers

ADDRESS	TYPE	REGISTER NAME
0	R/W	Interrupt Control/Status
1	R/W	Spindle Control/Status
2	R/W	Servo Control/Status
3	R/W	ADC Address/Data
4	R/W	Track Count LSB
5	R/W	Track Count MSB & Hybrid Servo Control
6	W	Error DAC Data
7	W	Embedded Servo Gain Control
8	W	Transconductance, Prescaler and Mode Control
9	W	Embedded Servo Timing Window Control

INTERRUPT CONTROL/STATUS REGISTER

Address: 0 Access: Read/Write Reset: 00
Register contents when Written to enable or disable interrupt events:

BIT	NAME	DESCRIPTION
0	COMMU INT	When set HIGH, interrupt is enabled on a state change of the back-emf commutation clock COMMU.
1	LOCK INT	When set HIGH, interrupt is enabled on a state change of the spindle speed lock.
2	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
3	TRKCS INT	When set HIGH, interrupt is enabled on each track crossing.
4	COUNT INT	When set HIGH, interrupt is enabled on the terminal count (000_H) of the track crossing counter.
5,6	-	Undefined.
7	MST INT	When set HIGH, the microprocessor signal $\overline{INT}$ is enabled.

Register contents when Read

BIT	NAME	DESCRIPTION
0	COMMU INT	Active high indicates a state change of the back-emf commutation clock COMMU.
1	LOCK INT	Active high indicates a state change of the spindle speed lock.
2	BURST INT	Active high indicates that the embedded servo position bursts are ready.
3	TRKCS INT	TRKCS INT is asserted when NQ or $N\overline{Q}$ changes state, i.e., on each track crossing.
4	COUNT INT	COUNT INT is asserted when the terminal count (000_H) of the track crossing counter is reached.
5,6	-	Undefined.
7	MST INT	Active high indicates that one or more interrupts are pending.

Each interrupt event status is reset when the µP reads the corresponding status register. Specifically, interrupt events COMMU INT and LOCK INT are reset whenever the SPINDLE STATUS register (ADDRESS=1) is read. Interrupt events TRKCS INT, COUNT INT and BURST INT are reset whenever the SERVO STATUS register (ADDRESS=2) is read. All interrupt events may be read as interrupt status regardless of their corresponding interrupt mask settings. The interrupt control register determines which event will actually cause a latched assertion of the µP signal $\overline{INT}$. Note that the MST INT is a master enable which disables all interrupt events from asserting $\overline{INT}$ when active low. Also, when read, MST INT indicates if any mask enabled interrupt events are still pending for service and reflects the internal state of the µP signal $\overline{INT}$.

SPINDLE CONTROL/STATUS REGISTER

Address: 1 Access: Read/Write Reset: 00
Register contents when Written:

BIT	NAME	DESCRIPTION
0	$\overline{\text{UPBRK}}$	When set LOW, dynamic braking will be initiated where upper drivers are disabled and lower drivers are activated.
1	UNIPOLAR	This bit is set HIGH when unipolar motor is used. For unipolar motors, all upper drivers are disabled and OUTCT is activated.
2	INDEX SEL	When set HIGH, the input signal at EXTINDX, one pulse per revolution, is selected as the spindle speed indicator. Otherwise, the internal revolution clock developed from the back-emf sensing circuit is selected.
3	MENABLE	Driver Enable Control. When set LOW, both upper and lower drivers are turned off to deny power to the motor. This overrides all other output conditions. When set HIGH, drive outputs are activated per the state of the commutation state counter.

Register contents when Written:

BIT	NAME	DESCRIPTION
4	ADVANCE	Each LOW-TO-HIGH transition advances the edge-trigged commutation state counter by one. When set HIGH, the internal clock (derived from the back-emf events) to the commutation state counter is inhibited. When set LOW, normal operation is resumed.
5 6 7	STAT0 STAT1 STAT2	Preset Commutation State. During start-up, the commutation state counter will be preset to the state decoded by these 3 bits per table 2:

TABLE 2:

STAT2	STAT1	STAT0	OUTA	OUTB	OUTC	OUTUPA	OUTUPB	OUTUPC
0	0	0	OFF	ON	OFF	ON	OFF	OFF
0	0	1	OFF	OFF	ON	ON	OFF	OFF
0	1	0	OFF	OFF	ON	OFF	ON	OFF
0	1	1	ON	OFF	OFF	OFF	ON	OFF
1	0	0	ON	OFF	OFF	OFF	OFF	ON
1	0	1	OFF	ON	OFF	OFF	OFF	ON
1	1	0	Normal Operation					
1	1	1	Normal Operation					

SPINDLE CONTROL/STATUS REGISTER (continued)

Register contents when Read:

BIT	NAME	DESCRIPTION
0	LOCK	Active high indicates that the spindle motor is within ±15 counts of the nominal value (5555 counts with the counter clocked at 500 kHz) or ±0.27%. The corresponding interrupt event LOCK INT will be reset whenever this register is read by the µP.
1	OVER	Active high indicates that the spindle speed is faster than the nominal value; active low indicates that the spindle speed is slower than the nominal value.
2	COMMU	Back-emf commutation clock divided by 2. Each state change of COMMU indicates that the commutation state counter has advanced by one. The corresponding interrupt event COMMU INT will be reset whenever this register is read by the µP.
3 4 5 6	PERCHK5 PERCHK4 PERCHK3 PERCHK2	Spindle Speed Check Bits. These bits are used to estimate the spindle speed if it is slower than the nominal value. **P2 P3 P4 P5 SPEED,rps** 0 0 0 0 SPEED ≥65 1 0 0 0 51≤ SPEED ≥65 1 1 0 0 36≤ SPEED ≥51 1 1 1 0 22≤ SPEED ≥36 1 1 1 1 SPEED ≥22
7	Undefined	

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SERVO CONTROL/STATUS REGISTER

Address: 2 Access: Read/Write Reset: 00
Register contents when Written:

BIT	NAME	DESCRIPTION
0	HENABLE	H-bridge Driver Enable. When set HIGH, H-bridge MOSFET drivers are enabled.
1	SW ON	When set HIGH, the analog switch between the ERRM and SWIN pins is turned on.
2	-	Undefined
3	TIMING	Timing Controller Disable. When set HIGH, the timing signals required to sample/hold embedded servo position bursts are derived from an external timing source via SAMPLEX and ACQX. Otherwise, the internal timing controller is used.
4	DIBURST	When HIGH, only two servo bursts, BURST1 and BURST2 are sampled. Otherwise, four servo burst amplitudes are sampled.
5	LEAD	Write Gate Guard Lead Enable. When set HIGH, the write gate guard is enabled one burst period prior to the sampling of the first position burst field. Otherwise, the write gate guard is enabled essentially at the same time as the sampling of the first position burst field.
6 7	TIM0 TIM1	Burst Field Length Select. These two bits define the time duration of each embedded servo position burst field per table below: **TIM1 TIM0 Burst Duration, µsec** 0 0 5 0 1 6 1 0 8 1 1 10

Register contents when Read:

0	-	Undefined
1	-	Undefined
2	BURST	Active HIGH indicates that the embedded servo position bursts are ready.
3	TRKCS	Active HIGH indicates a track crossing, i.e., NQ or $N\overline{Q}$ changes state.
4	COUNT	Active HIGH indicates that the terminal count (000_H) of the track crossing counter is reached.
5	-	Undefined
6	NQ	Active HIGH when N>Q and reset otherwise.
7	$N\overline{Q}$	Active HIGH when N>-Q and reset otherwise.

The corresponding interrupt events TRKCS INT, COUNT INT and BURST INT will be reset when this register is read by the µP. Also, the TRKCS, COUNT and BURST bits in this register are reset after being read.

ADC ADDRESS/DATA REGISTER

Address: 3 Access: Read/Write Reset: Undefined

Description: When Written, the least significant 4 bits of the register define the analog input to the 8-bit A/D converter. After conversion, the 8-bit digital word of the analog input is stored into the register.

Register contents when Written:

BIT	NAME	DESCRIPTION
0 1 2 3	ADC SEL0 ADC SEL1 ADC SEL2 ADC SEC3	A/D Converter Input Select. These 4 bits define the analog input to the A/D converter per table below:
4	X4	X4 Enable. When set HIGH, the analog input to the A/D converter will be multiplied by 4 before converted into a digital value.
5,6,7	-	Undefined

BIT3	BIT2	BIT1	BIT0	ADC INPUT	ADC Vref
0	0	0	0	BURST1	VREF
0	0	0	1	BURST2	VREF
0	0	1	0	BURST3	VREF
0	0	1	1	BURST4	VREF
0	1	0	0	PES1	VREF
0	1	0	1	PES2	VREF
0	1	1	0	PES0	VREF
0	1	1	1	N	NQREF
1	0	0	0	Q	NQREF
1	0	0	1	ERR	VREF
1	0	1	0	SOUT	VREF
1	0	1	1	SENSE	SENSEREF
1	1	0	0	ADCIN	VREF
1	1	0	1	VREF	VREF
1	1	1	0	SUM1	VREF
1	1	1	1	SUM2	VREF

Register contents when Read:

BIT	NAME	DESCRIPTION
0..7	ADC0..7	Digital output of the A/D converter in 2's complement format. ADC7 corresponds to the sign bit.

TRACK COUNT AND HYBRID SERVO CONTROL REGISTER

Address: 4 and 5 Access: Read/Write Reset: 00

Description: In a hybrid servo application, the dedicated servo channel is supported by a 12-bit track crossing counter with a 4-bit hybrid control register. The counter is preset by the µP and counts down by one whenever the head crosses a track boundary. The LSB 8 bits of the counter are defined at register 4 as follows:

BIT	NAME	DESCRIPTION
0..7	TRACK0..7	LSB of the track crossing counter 0..7. When written, these bits preset the track counter. When read, they reflect the counter state.

The MSB 4 bits of the counter along with the hybrid control bits are latched when the LSB 8 bits are read. The hybrid control bits, QUAD0, QUAD1, SELECT Q and CALIB are "write only." They are defined at register 5 as follows:

BIT	NAME	DESCRIPTION
0..3	TRACK8..11	MSB of track crossing counter 8..11. When written, these bits preset the track counter. When read, they reflect the counter state.
4 5	QUAD0 QUAD1	Quadrant Select. These 2 bits select the quadrant per table below: QUAD1 QUAD0 Quadrant Selected 0 0 -Q 0 1 N 1 0 -N 1 1 Q
6	SELECT Q	Quadrant Select Enable. Select quadrant with QUAD0 and QUAD1 when set HIGH.
7	CALIB	Calibration Enable. When set HIGH, the device is in the calibration mode in which analog inputs N and Q are tied to a DC reference level, NQREF; the analog input SERIN is tied to the DC reference level, SEREF.

ERROR DAC DATA REGISTER

Address: 6 Access: Write Reset: 00

BIT	NAME	DESCRIPTION
0..7	DAC0..7	Digital input to the D/A converter in 2's complement format. DAC7 corresponds to the sign bit.

EMBEDDED SERVO GAIN CONTROL REGISTER

Address: 7 Access: Write Reset: 00

BIT	NAME	DESCRIPTION
0	GAIN0	Embedded Servo Burst Amplitude Gain Select.
1	GAIN1	These two bits define the gain setting for the embedded servo differential amplifier per table below: **GAIN1 GAIN0 Gain, dB** 0 0 -6 0 1 -3 1 0 0 1 1 3
2 3 4 5	GAIN2 GAIN3 GAIN4 GAIN5	Embedded Servo Burst Amplitude Gain Select. These four bits define the gain setting for the sample/hold amplifier per table below: **GAIN5 GAIN4 GAIN3 GAIN2 Gain, dB** 0 0 0 0 0.0 0 0 0 1 0.2 0 0 1 0 0.4 0 0 1 1 0.6 0 1 0 0 0.8 0 1 0 1 1.0 0 1 1 0 1.2 0 1 1 1 1.4 1 0 0 0 1.6 1 0 0 1 1.8 1 0 1 0 2.0 1 0 1 1 2.2 1 1 0 0 2.4 1 1 0 1 2.6 1 1 1 0 2.8 1 1 1 1 3.0
6	SYNC SEL	Sync Input Select. When set HIGH, the frame rate to sample dedicated quadrature position signals N and Q is derived internally from SYSCLK. Otherwise, it is provided externally from the servo demodulator through SYNC and VCO inputs.
7	TCHE	Track Clock Hysteresis Enable. When set HIGH, an internal timing hysteresis is added for deriving the TRKCK output.

TRANSCONDUCTANCE, PRESCALER & MODE CONTROL REGISTER

Address: 8 Access: Write Reset: Bit 4 and 5 only

Bit	Name	Description
0	TEST	Test Mode Enable. When set HIGH, the device is in the test mode where the testing time for the spindle motor speed control function is shortened.
1	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH.
2 3	TGAIN0 TGAIN1	Transconductance Select. The transconductance gain of spindle motor lower drivers is defined per table below: **TGAIN1 TGAIN0 Gain** 0 0 2 0 1 4 1 0 8 1 1 16
4 5	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks which may be used, the prescaler selects a proper divider to generate a fixed clock at 500 kHz per table below: **SCALE1 SCALE0 SYSCLK(MHz) Divider** 0 0 10 20 0 1 8 16 1 0 6 12 1 1 4 8
6 7	MODE0 MODE1	Spindle Mode Control. These two bits define the number of motor poles per table below: **MODE1 MODE0 POLES COMMU/INDEX** 0 0 4 12 0 1 8 24 1 0 12 36 1 1 N/A N/A

EMBEDDED SERVO TIMING WINDOW CONTROL REGISTER

Address: 9 Access: Write Reset: 00

Description: The embedded servo position burst timing controller generates four timing windows. The sample control register matches these timing windows with four SAMPLE/HOLD circuits. The µP writes into the register a control pattern which will provide a necessary sampling to compare the required bursts in a proper polarity and sequence. In this manner, the µP can mix and commutate the bursts so that the position error signal is always in the same direction.

BIT	NAME	DESCRIPTION
0,1	WD SH1	Define timing window for SAMPLE/HOLD 1. Bit 0 is LSB.
2,3	WD SH2	Define timing window for SAMPLE/HOLD 2. Bit 2 is LSB.
4,5	WD SH3	Define timing window for SAMPLE/HOLD 3. Bit 4 is LSB.
6,7	WD SH4	Define timing window for SAMPLE/HOLD 4. Bit 6 is LSB.

The timing window is selected per table below:

MSB	LSB	S/H Timing Window
0	0	Timing window 1
0	1	Timing window 2
1	0	Timing window 3
1	1	Timing window 4

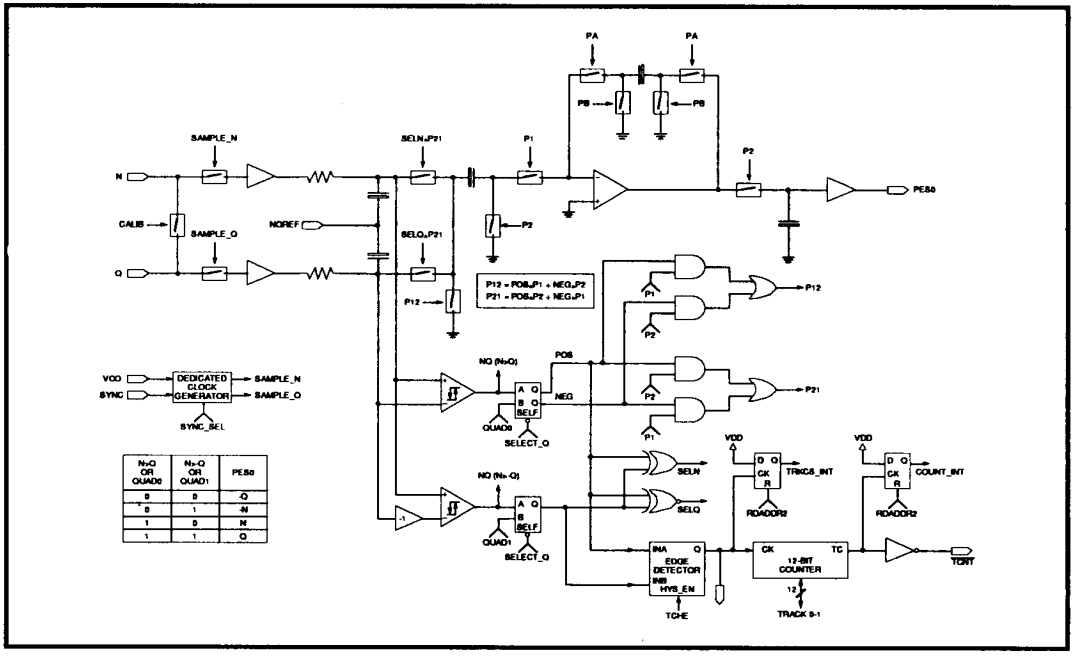

FIGURE 2: Dedicated Servo Position Processor

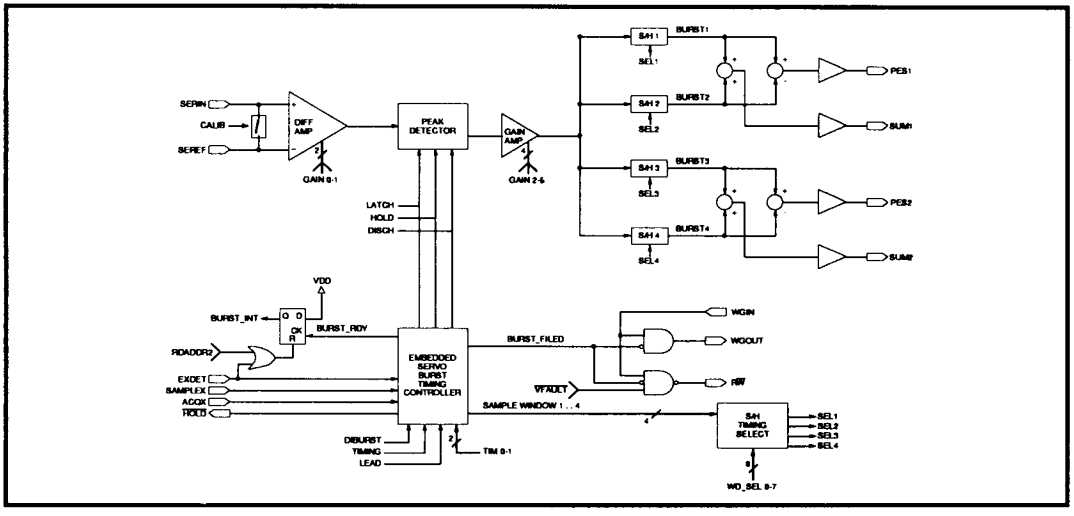

FIGURE 3: Embedded Servo Burst Amplitude Processor & Timing Controller

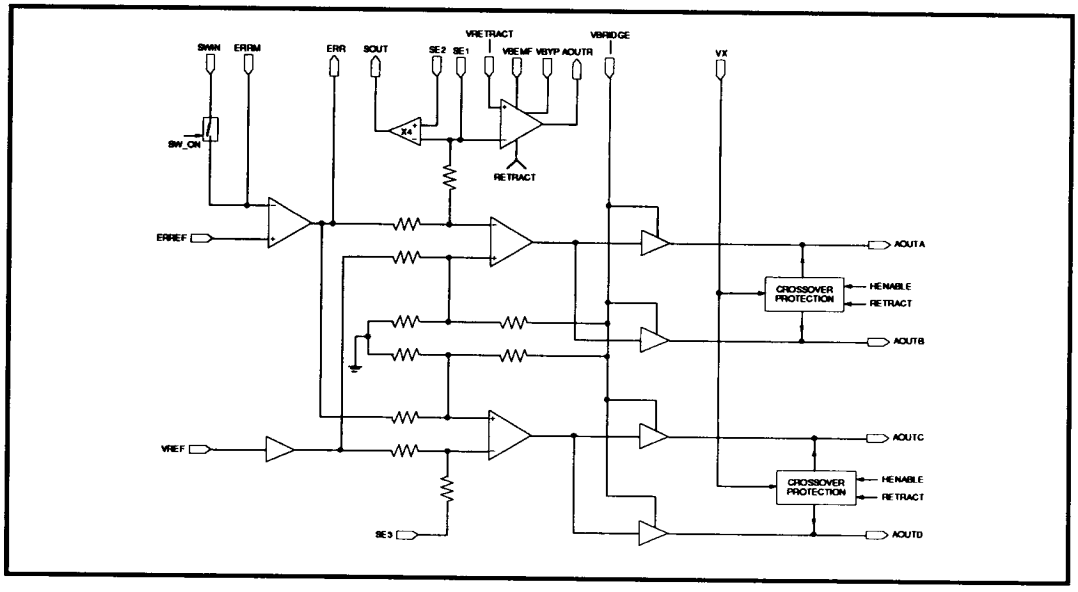

FIGURE 4: Servo Position Error Amplifier

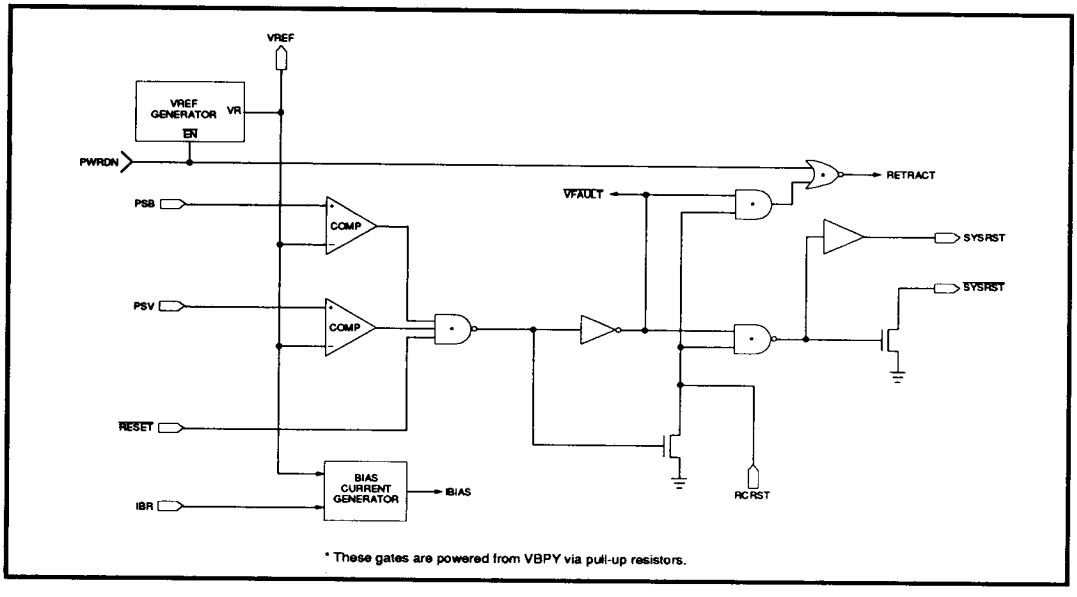

FIGURE 5: Voltage Fault & Servo Head Retract Logic

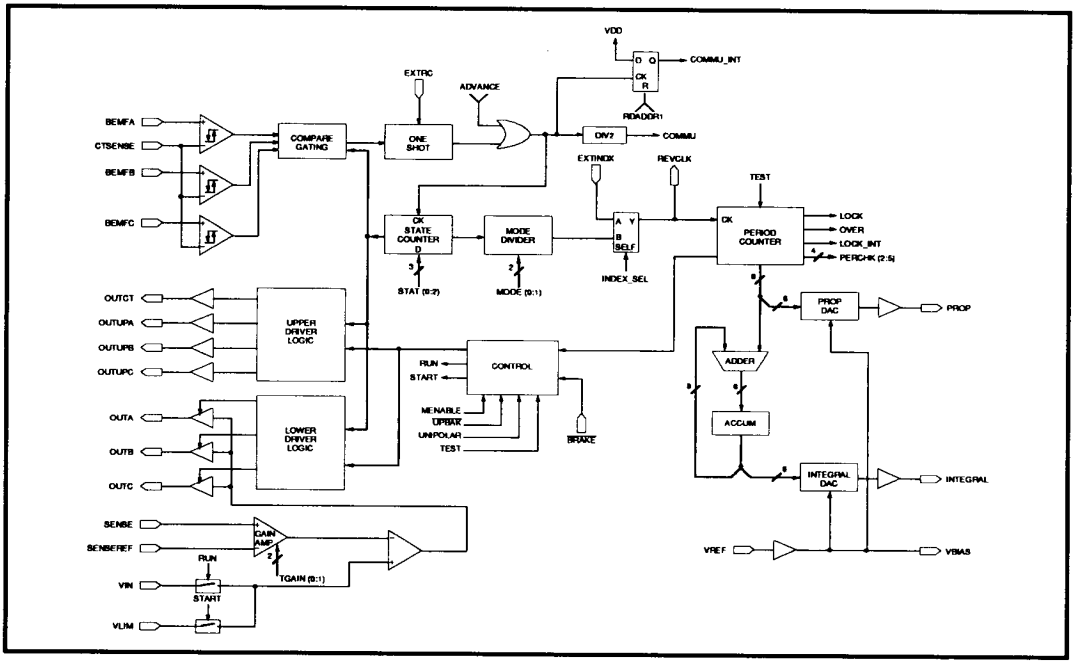

FIGURE 6: Spindle Motor Speed Control

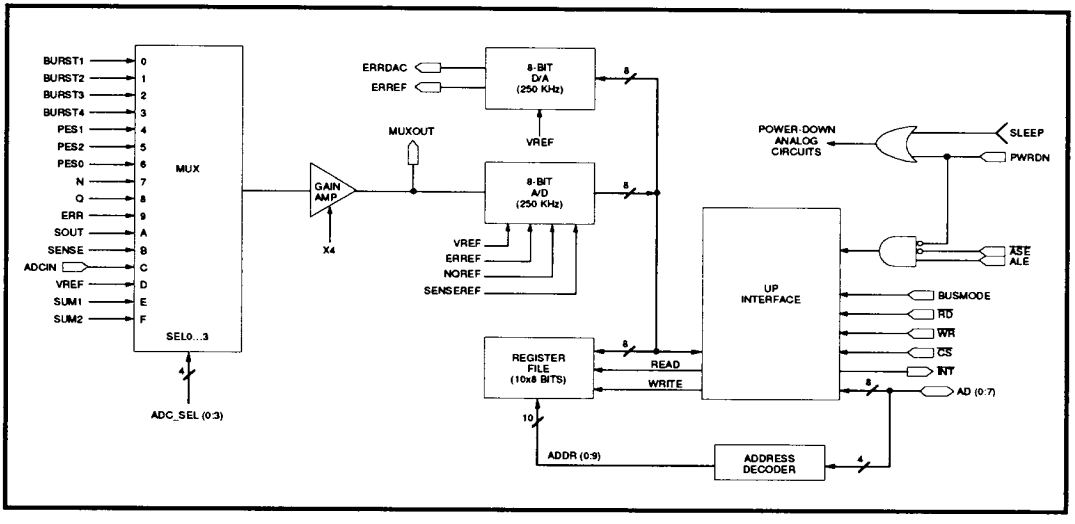

FIGURE 7: Data Acquisition & Microprocessor Bus Interface

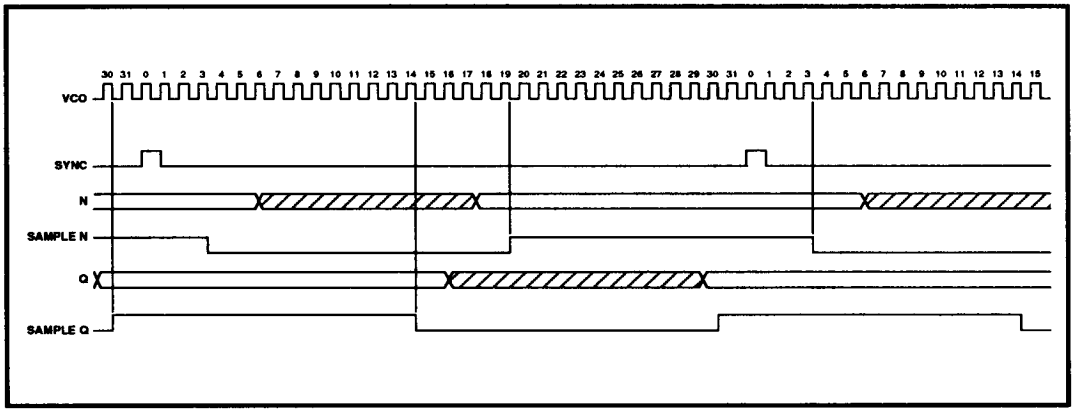

FIGURE 8: Dedicated Servo Timing Diagram

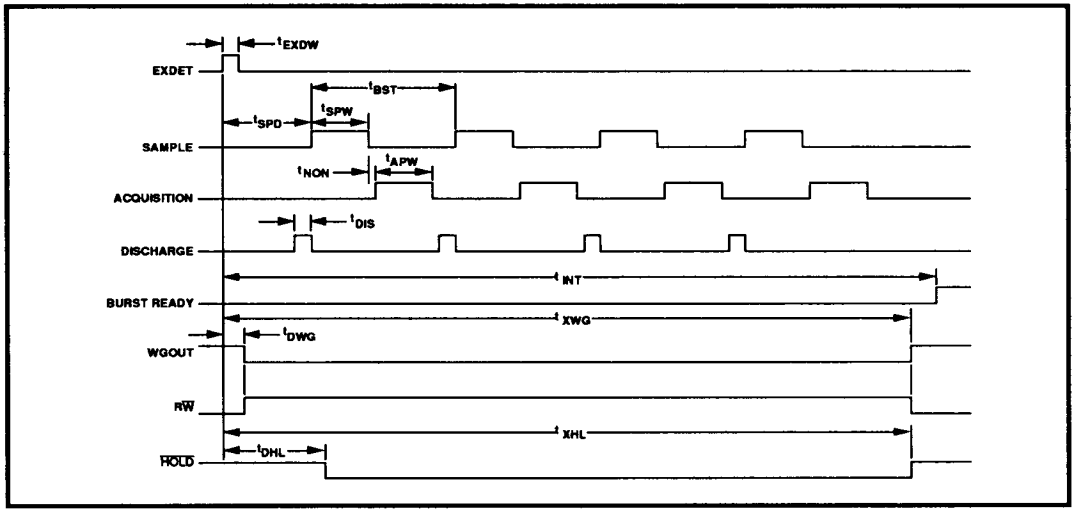

FIGURE 9: Embedded Servo Timing Diagram with Internal Timing Source

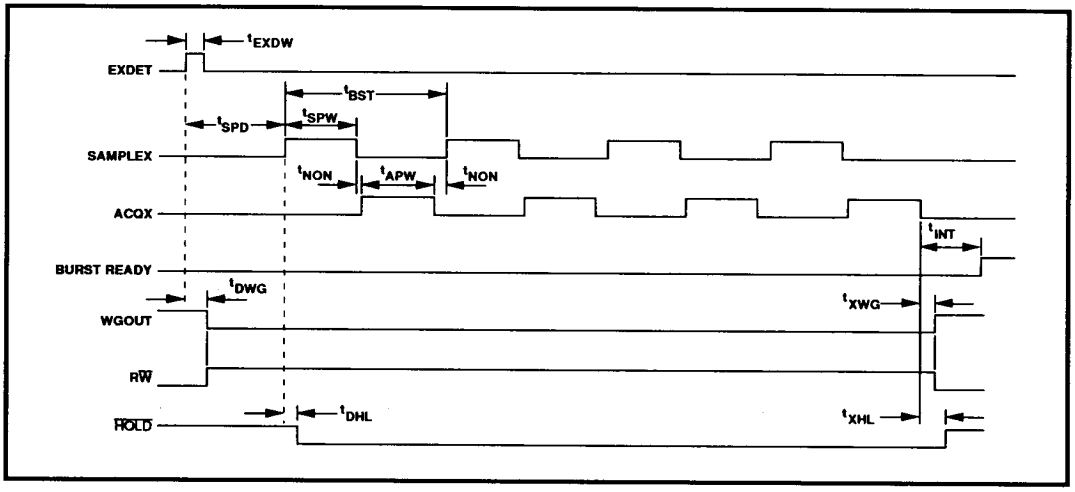

FIGURE 10: Embedded Servo Timing Diagram with External Timing Source

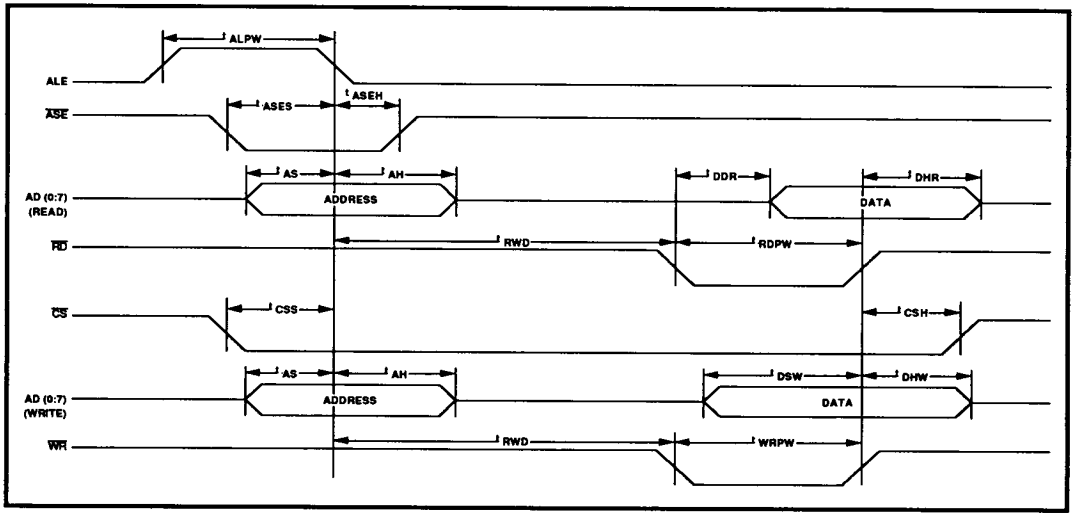

FIGURE 11: Intel Microprocessor Bus Interface Timing Diagram

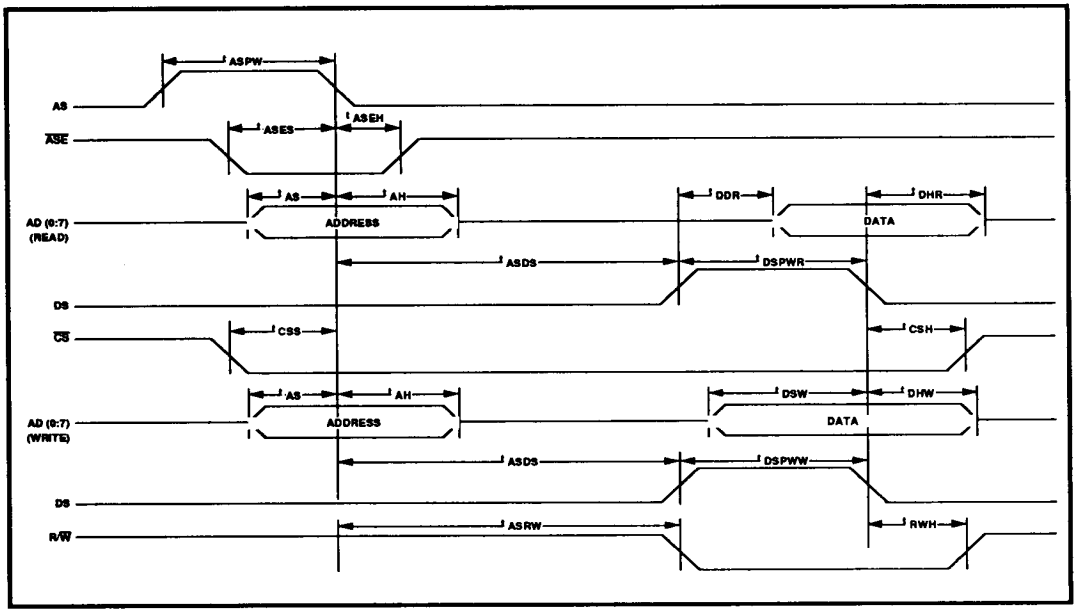

FIGURE 12: Motorola Microprocessor Bus Interface Timing Diagram

0: INTERRUPT CONTROL/STATUS			1: SPINDLE CONTROL/STATUS			2: SERVO CONTROL/STATUS			3: ADC CONTROL/STATUS			4:TRACK COUNT LSB		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	COMMU INT	COMMU INT	0	$\overline{\text{UPBAR}}$	LOCK	0	HENABLE		0	ADC SEL0	ADC0	0	TRACK0	TRACK0
1	LOCK INT	LOCK INT	1	UNIPOLAR	OV ER	1	SW ON		1	ADC SEL1	ADC1	1	TRACK1	TRACK1
2	BURST INT	BURST INT	2	INDEX SEL	COMMU	2		BURST	2	ADC SEL2	ADC2	2	TRACK2	TRACK2
3	TRKS INT	TRKS INT	3	MENABLE	PERCHK5	3	TIMING	TRKS	3	ADC SEL3	ADC3	3	TRACK3	TRACK3
4	COUNT INT	COUNT INT	4	ADVANCE	PERCHK4	4	DIBURST	COUNT	4	X4	ADC4	4	TRACK4	TRACK4
5			5	STAT0	PERCHK3	5	LEAD		5		ADC5	5	TRACK5	TRACK5
6			6	STAT1	PERCHK2	6	TIM0	NQ	6		ADC6	6	TRACK6	TRACK6
7	MST INT	MST INT	7	STAT2		7	TIM1	$\overline{\text{NQ}}$	7		ADC7	7	TRACK7	TRACK7

5: TRACK COUNT MSB & HYBRID SERVO CONTROL			6: ERROR DAC DATA			7: EMBEDDED SERVO GAIN CONTROL			8: TRANSCONDUCTANCE PRESCALER & MODE CONTROL			9: EMBEDDED SERVO TIMING WINDOW CONTROL		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	TRACK8	TRACK8	0	DAC0		0	GAIN0		0	TEST		0	WD SEL0	
1	TRACK9	TRACK9	1	DAC1		1	GAIN1		1	SLEEP		1	WD SEL1	
2	TRACK10	TRACK10	2	DAC2		2	GAIN2		2	TGAIN0		2	WD SEL2	
3	TRACK11	TRACK11	3	DAC3		3	GAIN3		3	TGAIN1		3	WD SEL3	
4	QUAD0		4	DAC4		4	GAIN4		4	SCALE0		4	WD SEL4	
5	QUAD1		5	DAC5		5	GAIN5		5	SCALE1		5	WD SEL5	
6	SELECT Q		6	DAC6		6	SYNC SEL		6	MODE0		6	WD SEL6	
7	CALIB		7	DAC7		7	TCHE		7	MODE1		7	WD SEL7	

FIGURE 13: SSI 32H4633 Register Map

PIN DESCRIPTION

This section describes the names of the pins, their symbols, their functions and their active states. The pins are grouped together into function for clarity.

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA, B, C, G	-	Analog +5V supplies. They must be shorted externally.
VPD	-	Digital +5V supply. It must be shorted to analog +5V supplies externally.
VNA, B, C, G	-	Analog grounds. They must be shorted externally.
VND, VND2	-	Digital grounds. They must be shorted to analog grounds externally.

SERVO HEAD POSITION PROCESSOR

N	I	Normal Input - Analog position signal from a dedicated servo demodulator. This input along with quadrature input is used to extract the position information from a dedicated servo surface.
Q	I	Quadrature Input - Analog position signal from a dedicated servo demodulator.
NQREF	I	Dedicated Position Error Reference - DC reference voltage for both normal and quadrature analog inputs.
SYNC	I	Sync Input - A clock signal generated from a dedicated servo demodulator. The falling edge of this clock causes the analog signals N and Q to be sampled.
VCO	I	VCO Input - A clock signal generated from a dedicated servo demodulator. The VCO should be synchronous with N and Q inputs.
TRKCK	O	Track Crossing Clock - This digital output drives external hardware track counter and is compatible with the counter function available in the Intel 8051 family of microcontrollers. It is normally LOW and pulses HIGH once per track crossing.
$\overline{\text{TCNT}}$	O	Terminal Count - The terminal count output is normally HIGH and goes LOW when the 12-bit counter reaches zero.
PES0	O	Position Error Output - Test point for the analog output of the position processor. This signal is proportional to the radial displacement of the head from the center of the current track, based upon the values of bits QUAD0, QUAD1 and SELECT Q.
SERIN	I	Embedded Servo Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Embedded Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
SAMPLEX	I	Servo Burst Sample - This TTL compatible input, when HIGH, activates the peak detector. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source.

SERVO HEAD POSITION PROCESSOR (continued)

NAME	TYPE	DESCRIPTION
ACQX	I	Servo Burst Acquisition - This TTL compatible input, when HIGH, activates the transfer of the voltage captured by the peak detector onto holding capacitors. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source.
PES1 PES2	O	Position Error Signal - Test point for differential signals which are defined as: PES1 = BURST1-BURST2 PES2 = BURST3-BURST4
SUM1 SUM2	O	Position Sum Signal - Test point for summed signals which are defined as: SUM1 = BURST1+BURST2 SUM2 = BURST3+BURST4

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION

ERRM	I	Actuator Inverting Input - Inverting input to the position error amplifier of the MOSFET predriver.
SWIN	I	This input is shorted to ERRM when the bit SW ON is set HIGH. SWIN floats otherwise.
ERR	O	Acceleration Error - Position error amplifier output. This signal is amplified by the MOSFET drivers and applied to the actuator through an external MOSFET H-bridge as follows: SE3-SE1 = 30 (ERR-VREF)
AOUTA AOUTC	O	PFET Driver - Drive signals for P channel MOSFETs connected between VBRIDGE and the voice coil actuator. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
AOUTB AOUTD	O	NFET Driver - Drive signals for N channel MOSFETs connected between the current sense resistor and the voice coil actuator.
VBRIDGE	I	Bridge Voltage Supply - Pin for connection to the voltage supply provided to external power transistors.
VRETRACT	I	Retract Voltage - In head retract mode this voltage is applied across the actuator to force the heads to move at a constant speed.
AOUTR	O	Head Retract Amplifier Output - Voltage output to drive an external head retract circuit.
SE1 SE3	I	Motor Voltage Sense Input - These inputs provide feedback to the internal MOSFET drive amplifier.
SE2	I	Motor Current Sense Input - Non-inverting input to the current sense differential amplifier. It should be connected to an external current sense resistor. The inverting input of the differential amplifier is SE1.
SOUT	O	Motor Current Sense Output - This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows: SOUT-ERREF = 4 (SE2-SE1)

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION (continued)

NAME	TYPE	DESCRIPTION
VX	O	Crossover Protection Voltage - The current source output at VX is converted to a voltage with an external resistor. The value of the resistor should be adjusted so that VX is less than the specified minimum threshold voltage of the MOSFET bridge.
VBYP	I	Bypass Voltage Supply - The VBRIDGE voltage is stored on this node for use during retract.
PSB PSV	I	Fault Voltage Comparator Inputs - Voltage inputs for the low voltage comparators. These two inputs should be connected to separate external resistor dividers. Each resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.35 volts.
VREF	O	Internal Voltage Reference - A voltage reference at 2.35 volts is generated internally for the DC reference level throughout the device. Due to limited drive capability provided with on-chip voltage reference, this pin shall be used only for connecting an external bypass capacitor of 10 µF.
IBR	O	Bias Current Reference - Pin for connection to an external resistor (from GND) to establish a reference current for bias currents used in analog circuits.
$\overline{\text{RESET}}$	I	Reset Input - When set LOW, all the internal registers are reset and a forced head retraction is activated.
$\overline{\text{SYSRST}}$	O	Reset Output - Active LOW output signal, which is generated by a supply voltage fault or $\overline{\text{RESET}}$ being pulled LOW externally.
SYSRST	O	Reset Output - Active HIGH output signal which is inverted version of $\overline{\text{SYSRST}}$.
RCRST	I	Pin for connection to an external capacitor to extend the active low duration of $\overline{\text{SYSRST}}$.

SPINDLE MOTOR SPEED CONTROL

EXTINDX	I	External Index Input - This TTL compatible input, when selected via the INDEX SEL bit, is used to provide a once-per-revolution indication of angular position and speed to the device. The falling edge of EXTINDX is the reference.
SYSCLK	I	System Clock Input - A TTL compatible input is provided to derive internal timing signals.
EXTRC	I	Pin for connection to a resistor (from VDD) and a capacitor (from GND) to provide the commutation delay. The commutation delay is 0.56 RC. After the commutation delay, the timing block provides a noise rejection interval to reject transients on the motor coils due to commutations. This noise rejection is an additional 0.29 RC. The total time (commutation delay and noise rejection internal) must be less than a commutation cycle time.

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{BRAKE}}$	I	Spindle Braking Enable - This input, when active LOW, dynamically brakes the spindle motor. A resistor (from $\overline{\text{SYSRST}}$) and a capacitor (from GND) are connected to this pin to provide a delay between the initiation of fault-induced head retraction and motor braking. RC are selected such that 1.2 RC is equal to the maximum time required for head retraction.
VBIAS	O	Buffered Bias Voltage - VBIAS is buffered VREF to be used for VLIM and motor speed setting bias. (In some applications, it is necessary to create an "offset" to the speed control loop to obtain proper speed regulation.)
PROP	O	Proportional Channel D/A Output - The proportional channel output is the least significant 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation.
INTEGRAL	O	Integral Channel D/A Output - The integral channel output is the most significant 6 bits of an 8-bit accumulator. The accumulator adds the least 8 bits of the period measurement counter to the previous value obtained from prior period measurements and accumulations.
VIN	I	Speed Control Voltage Input - The combination of external driver transistors and internal predriver circuits forms a transconductance amplifier which will define the motor current in relation to VIN. In conjunction with the SENSE input and the gain setting for the sense amplifier, the transconductance gain is given by: $g_m=I_m/VIN=1/(R_S \cdot A_V)$ where I_m is the current flowing through the spindle motor coils, R_S the current sense resistor and A_V the transconductance gain defined by TGAIN0 and TGAIN1 bits.
VLIM	I	Current Limit Setting Voltage - The spindle motor current will be limited to a value determined by R_S, VLIM and Av such that $Imax=VLIM/(R_S \cdot A_V)$. VLIM is used whenever the spindle speed is measured less than 5151 RPM.
SENSE	I	Current Sense Amplifier Noninverting Input - The external driver transistor sources are connected to a current sense resistor R_S to monitor motor current. The device will control the voltage across the sense resistor to match either VIN (during normal operation) and VLIM (during acceleration).
SENSEREF	I	Current Sense Amplifier Reference Input - Pin for a Kelvin connection to the ground side of the sense resistor.
OUTA OUTB OUTC	O	Predriver Outputs - These predriver outputs drive the gates of external power NFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF.
OUTUPA OUTUPB OUTUPC	O	Upper Pull-up Outputs - These predriver outputs drive the gates of external power PFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF.
OUTCT	O	Center Tap Predriver - This output drives an external PFET driver which connects the motor center tap to the positive power supply for unipolar drive applications. OUTCT has the same characteristics as OUTUPA,B,C and is enabled via the UNIPOLAR bit.

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
VBEMF	I	Back-emf Voltage - A power diode voltage drop from the motor power supply is defined as VBEMF. The external PFET sources are connected to VBEMF as is this pin. During power failure, this voltage is used to provide power for head retraction and motor braking.
BEMFA BEMFB BEMFC CTSENSE	I	Back-emf Inputs - Inputs to be connected to their respective motor coils and the center tap for sensing generated back-emf voltages. The device uses the back-emf voltages to determine the rotor position and effect commutation.
REVCLK	O	Revolution Clock Output - This output generates a once-per-revolution indication of motor activity derived from back-emf events.

DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

ALE	I	Address Latch Enable - Falling edge latches the register address from the AD0..AD7 address/data bus.
$\overline{ASE}$	I	Address Strobe Enable - When set LOW, this input enables ALE input to the device.
$\overline{CS}$	I	Chip Select - Active LOW signal enables the device to respond to µP read or write.
$\overline{WR}$	I	Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{RD}$	I	Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active.
AD0..AD7	I/O	Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used.
BUSMODE	I	Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected.
$\overline{INT}$	O	Interrupt Strobe - Active LOW output signals the µP to respond to the device. It is released when all the pending interrupts have been serviced by the µP.
PWRDN	I	Power-down Mode Enable - When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH.
ERRDAC	O	Error DAC Output - An 8-bit D/A output which converts a digital word from the µP into an analog signal. This signal is fed back to the position error amplifier through external RC components.
ERREF	O	Reference voltage for D/A output ERRDAC.
ADCIN	I	External A/D input.
MUXOUT	O	Test point for the X4 amplifier output which is the input to the A/D converter.

EMBEDDED SERVO TIMING CONTROLLER

NAME	TYPE	DESCRIPTION
EXDET	I	Bit Synchronization Input - The internal servo timing controller is synchronized with this TTL compatible input.
$\overline{HOLD}$	O	AGC Gain Hold - TTL compatible control signal holds the input AGC amplifier gain of a pulse detector, such as 32P4620, when pulled LOW.
WGIN	I	Write Gate Input - TTL compatible input from the storage controller.
WGOUT	O	Write Gate Output - TTL compatible control signal derived from WGIN. This output will be pulled LOW during embedded servo position burst sampling.
$R\overline{W}$	O	Read/Write Control Output - TTL compatible control signal derived from WGIN. This output will be pulled HIGH during embedded servo position burst sampling or when a low voltage fault occurs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect reliability.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Supply voltage applied at VPA, VPB, VPC, VPD, VPG	VDD		0.1		7.0	V
Signal ground applied at VNA, VNB, VNC, VND, VND2, VNG	GND		0.0		0.0	V
Bridge voltage applied at VBRIDGE	VBRIDGE		0.1		14.0	V
Bypass voltage applied at VBYP	VBYP		0.1		14.0	V
Back-emf voltage applied at VBEMF	VBEMF		0.1		20.0	V
VBEMF current if VBEMF>18V	IBEMF		-		5.0	mA
Digital input voltages	VIND		-0.3		VDD+0.3	V
Analog input voltages	VINA		-0.3		VDD+0.3	V
Storage temperature	Tstg		-65		150	°C
Lead temperature	TI		-		300	°C

OPERATING ENVIRONMENT LIMITATIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage applied at VPA,VPB,VPC,VPD,VPG	VDD		4.75	-	5.25	V
Signal ground applied at VNA,VNB,VNC,VND, VND2,VNG	GND		0.0	-	0.0	V
Bridge voltage applied at VBRIDGE	VBRIDGE		4.75	-	13.2	V
Bypass voltage applied at VBYP	VBRIDGE -VBYP		0.0	-	0.8	V
Back-emf voltage applied at VBEMF	VBRIDGE -VBEMF		-5.0	-	0.8	V
Ambient temperature	TA		0.0	-	70.0	°C
System clock (10 MHz, Max)	Fc		-	-	±0.01	%
Capacitive load on digital outputs	CL		-	-	100	pF
Analog input impedance	Rin		100	-	-	kΩ
	Cin		-	-	20	pF
Load on analog outputs	Rout		10	-	-	kΩ
	Cout		-	-	40	pF
Bias resistor (22.6 kΩ, Typ)	RBIAS		-	-	±1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

Supply current Normal mode	IDD	VDD=5.25V	-	-	50	mA
Power-down mode	-		-	-	5	mA
Output logic "1" voltage	Voh	Ioh=-0.4 mA VDD=4.75V	2.4	-	-	V
Output logic "0" voltage	Vol	Iol=1.6 mA VDD=4.75V	-	-	0.4	V
Input logic "1" voltage	Vih	VDD=4.75V	2.0	-	-	V
Input logic "0" voltage	Vil	VDD=4.75V	-	-	0.8	V

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input logic "1" current	Iih	Vih=5.25V VDD=5.25V	-	-	10	µA
Input logic "0" current	Iil	Vil=0.0 VDD=5.25V	-	-	-10	µA
Input capacitance	Cin		-	-	10	pF

FUNCTIONAL CHARACTERISTICS

Dedicated Servo Position Processor

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
N,Q comparator hysteresis		5	-	30	mV
Commutator comparator offset		-	-	±30	mV
N,Q input voltage w.r.t GND		0.5	-	3.7	V
NQREF w.r.t. GND		1.9	-	2.9	V
N,Q input voltage w.r.t NQREF		-	-	±1.1	V
Channel gain from N,Q to PES0		0.96	1.0	1.04	V/V
PES0 offset		-	-	±50	mV
PES0 output corner frequency		60	85	120	kHz

Embedded Servo Burst Amplitude Processor

SERIN w.r.t. GND		2.0	-	VDD	V
SEREF w.r.t. GND		2.0	-	3.0	V
SERIN input voltage	Channel gain=-6 dB	0.0	-	2.0	Vp
swing w.r.t. SEREF	Channel gain=0 dB	0.0	-	1.0	Vp
Servo burst frequency		0.5	-	2.0	MHz
Input impedance at		20	-	-	kΩ
SERIN, SEREF		-	-	10	pF
DC offset at PES1,PES2	BURST1=BURST2=0.5V BURST3=BURST4=0.5V	-30	-	20	mV
DC offset at SUM1,SUM2	BURST1=BURST2=0.5V BURST3=BURST4=0.5V	0	-	-250	mV

Embedded Servo Burst Amplitude Processor (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential gain error at PES1,PES2,SUM1,SUM2		-	-	±0.1	dB
Integral gain error at PES1,PES2,SUM1,SUM2		-	-	±1.0	dB
PES1,PES2 output swing w.r.t. VREF		-	-	±1.1	V
SUM1,SUM2 output swing w.r.t. VREF		-	-	1.1	V
Allowable load at PES1, PES2,		10	-	-	kΩ
SUM1,SUM2 to VREF		-	-	40	pF

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Embedded Servo Timing

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical LOW. Timing measurements are defined in Figure 3 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Burst cell time	t_{BST}				
TIM0='0' TIM1='0'		-	5.0	-	µs
TIM0='1' TIM1='0'		-	6.0	-	µs
TIM0='0' TIM1='1'		-	8.0	-	µs
TIM0='1' TIM1='1'		-	10.0	-	µs
EXDET pulse width	t_{EXDW}	0.5	-	t_{BST}	µs
Internal first sampling time from EXDET rise	t_{SPD}				
LEAD='0'		1.0	-	1.7	µs
LEAD='1'		(t_{BST}+1.0)	-	(t_{BST}+1.7)	µs
Sampling pulse width	t_{SPW}				
TIM0='0' TIM1='0'		-	2.0	-	µs
TIM0='1' TIM1='0'		-	3.0	-	µs
TIM0='0' TIM1='1'		-	5.0	-	µs
TIM0='1' TIM1='1'		-	7.0	-	µs
Acquisition pulse width	t_{APW}	-	2.0	-	µs
Discharge pulse width	t_{DIS}	-	0.75	-	µs
Nonoverlapping time between sampling & acquisition pulses	t_{NON}	-	0.25	-	µs

Embedded Servo Timing (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Burst ready interrupt from EXDET rise	t_{INT}				
DIBURST='0' LEAD='0'		$(4t_{BST}+5.2)$	-	$(4t_{BST}+5.9)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+5.2)$	-	$(2t_{BST}+5.9)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+5.2)$	-	$(5t_{BST}+5.9)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+5.2)$	-	$(3t_{BST}+5.9)$	µs
WGOUT & $\overline{RW}$ delay time from EXDET rise	t_{DWG}	0.0	-	0.1	µs
WGOUT & $\overline{RW}$ hold time from EXDET rise	t_{XWG}				
DIBURST='0' LEAD='0'		$(4t_{BST}+1.0)$	-	$(4t_{BST}+1.7)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+1.0)$	-	$(2t_{BST}+1.7)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+1.0)$	-	$(5t_{BST}+1.7)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+1.0)$	-	$(3t_{BST}+1.7)$	µs
$\overline{HOLD}$ delay time from EXDET rise	t_{DHL}				
LEAD='0'		0.2	-	0.7	µs
LEAD='1'		$(t_{BST}+0.2)$		$(t_{BST}+0.7)$	µs
$\overline{HOLD}$ hold time from EXDET rise	t_{XHL}				
DIBURST='0' LEAD='0'		$(4t_{BST}+1.0)$	-	$(4t_{BST}+1.7)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+1.0)$	-	$(2t_{BST}+1.7)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+1.0)$	-	$(5t_{BST}+1.7)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+1.0)$	-	$(3t_{BST}+1.7)$	µs

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical HIGH. Timing measurements are defined in Figure 4 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

EXDET pulse width	t_{EXDW}	0.5	-	5.0	µs
SAMPLEX delay time from EXDET rise	t_{SPD}	0.2	-	-	µs
SAMPLEX pulse width	t_{SPW}	3	-	-	µs
ACQX pulse width	t_{APW}	2	-	-	µs
Nonoverlapping time between SAMPLEX & ACQX pulses	t_{NON}	0.0	-	-	µs
Burst ready interrupt from last ACQX fall	t_{INT}	5.2	-	5.9	µs
WGOUT & $\overline{RW}$ delay time from EXDET rise	t_{DWG}	0.0	-	0.1	µs

Embedded Servo Timing (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
WGOUT & R/$\overline{W}$ hold time from last ACQX fall	t_{XWG}	1.0	-	1.7	µs
$\overline{HOLD}$ delay time from first SAMPLEX rise	t_{DHL}	0.2	-	0.7	µs
$\overline{HOLD}$ hold time from last ACQX fall	t_{XHL}	1.0	-	1.7	µs

Head Positioner MOSFET Driver

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VRETRACT voltage	VBEMF = 3V	0.3	-	0.9	V
	VBEMF = 12V	0.4	-	1.2	V
Retract offset					
VBEMF = 3V	VRETRACT = 0.5V	-70	-	50	mV
VBEMF = 6V	VBYP = 4V to 13V	-70	-	70	mV
VBEMF = 12V	I_{AOUTR}<1mA	-150	-	150	mV
Voh at AOUTR	Ioh = -1mA				
VBEMF = 4V VBYP = 4V		1.5	-	-	V
VBEMF = 3V VBYP = 4V		1.3	-	-	V
Leakage current at AOUTR	RETRACT = LOW AOUTR = 0V to 14V	-	-	1	µA
Voh at AOUTA, AOUTC	Ioh = -1 mA	VBRIDGE-1.5	-	-	V
	Ioh = -1 µA	VBRIDGE-0.1	-	-	V
Vol at AOUTA, AOUTC	Iol = 10 µA	-	-	1	V
Voh at AOUTB	Ioh = -10 µA	VBRIDGE-0.5	-	-	V
Voh at AOUTD	Ioh = -10 µA	VBYP-0.5	-	-	V
Vol at AOUTB, AOUTD	Iol = 1 mA	-	-	1	V
	Iol = 10 µA	-	-	0.2	V
Input offset at SOUT		-	-	±3	mV
SOUT/(SE1-SE2)		3.9	-	4.1	V/V
SE1/ERR, SE3/ERR		14.0	-	15.4	V/V
ERRAMP input offset		-	-	±10	mV
ERRAMP gain		1000	-	-	V/V
Output crossover time CL = 600 pF at AOUTA,C CL = 150 pF at AOUTB,D	PFET VTH = -2V NFET VTH = 2V R_X = 50 kΩ	-	-	45	µs
Input impedance at SE1, SE2,SE3		20	-	-	kΩ

Head Positioner MOSFET Driver (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output resistance at SOUT		-	-	350	Ω
Analog switch on-resistance at SWIN		-	-	600	Ω
Output resistance at ERR		-	-	100	Ω
Output voltage at VX		1.0	-	1.4	V

Voltage Reference and Voltage Fault Circuit

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPB voltage for $\overline{SYSRST}$ & RCRST in operation		2.0	-	-	V
On resistance at RCRST VPB>3.5V VBYP>4V		-	-	800	Ω
VPB>3.5V VBYP>10V		-	-	550	Ω
RCRST input threshold	VBYP=4V	0.2	-	1.2	V
IBR voltage w.r.t. VREF		-80	-	20	mV
Output voltage at VREF	|II|<10μA	2.27	2.34	2.41	V
PSB,PSV comparator offset		-	-	±15	mV

Spindle Motor Speed Control

SYSCLK duty cycle		40	-	60	%
EXTINDX pulse width		200	-	-	ns
Advance pulse width		3	-	-	μs
Timing resistor at EXTRC		0.01	-	10	MΩ
Timing capacitor at EXTRC		100	-	-	pF
Delay time variation relative to T0*		-	-	±5	%
Vil at $\overline{BRAKE}$	VBEMF = 5V	0	-	0.3	V
Vih at $\overline{BRAKE}$	VBEMF = 5V	1.5	-	-	V
Output voltage swing at PROP & INTEGRAL	I_{out}<0.1mA	0	-	VBIAS±5%	V
DAC step size at PROP & INTEGRAL		32	-	39	mV
Output impedance at PROP & INTEGRAL	0.5V<V_{out}<2.0V I_{out}=0.1mA	-	-	300	Ω

Spindle Motor Speed Control (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Kp,proportional gain**		0.31	-	0.38	V/rad/s
Ki,integral gain		7.00	-	8.55	V/rad
VBIAS output w.r.t. VREF		-50	-	25	mV
Input voltage at VIN & VLIM		0	-	2.35	V
Input leakage current at VIN & VLIM		-	-	±1	µA
Output resistance at OUTUPA,B,C & OUTCT	Output in HIGH state, pulled to VBEMF	5	-	20	kΩ
Vol at OUTUPA,B,C & OUTCT	I_{out}<3mA VBEMF=13.2V	-	-	1.0	V
Output resistance at OUTA,B,C	Output in HIGH state, pulled to VBEMF	5	-	20	kΩ
Vol at OUTA,B,C	I_{out}<5mA	-	-	1.0	V
Input voltage at SENSE	A_V=2	0.0	-	1.0	V
Input voltage at SENSEREF		0.0	-	0.05	V
Input leakage current at SENSE	0.0V<V_{in}<1.0V	-	-	±10	µA
Input leakage current at SENSEREF	0.0V<V_{in}<0.05V	-200	-	10	µA
Input capacitance at SENSE & SENSEREF		-	-	20	pF
Gain variation***	A_V=2,4,8,16	-	-	±10	%
Input impedance at BEMFA,B,C	-0.3V<V_{in}<15V	100 -	- -	- 10	kΩ pF
Input impedance at CTSENSE		30 -	- -	- 10	kΩ pF
LOCK indication range		5384.9	-	5415.1	RPM
Speed resolution		-	-	±0.018	%

*T0 is the commutation delay and is given by the relationship T0 = 0.56RC. Suggested value for C would be 470 to 1000 pF. An external R and C must be provided such that T0 is greater than 10 µs (R=22 kΩ, C=470 pF).
**The motor speed control loop can be described as: $H(s)=K_p+K_i/s$
***The transconductance gain from VIN or VLIM to the steady-state current flowing through the motor is given by $G = 1/(R_{SENSE} \cdot A_V)$

DATA ACQUISITION

A/D Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ADCIN full-scale swing w.r.t. VREF	X4=LOW	-	±(VREF/2)	-	V
	X4-HIGH	-	±(VREF/8)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	4.0	-	µs
LSB voltage	X4=LOW	-	VREF/256	-	mV
	X4=HIGH	-	VREF/1024	-	mV
Differential linearity error		-	-	±0.75	LSB
Relative accuracy**		-	-	±1.0	LSB
Power supply sensitivity		-	-	±0.5	LSB

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the A/D transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Error D/A Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ERRDAC full-scale voltage swing w.r.t ERREF		-	±(VREF/2)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	4.0		µs
LSB voltage		-	VREF/256	-	mV
Output voltage at ERREF		1.56	1.61	1.66	V
ERRDAC offset w.r.t. ERREF		-	-	±5	mV
Differential linearity error		-	-	±0.5	LSB
Relative accuracy**		-	-	±1.0	LSB
Power supply sensitivity		-	-	±0.5	LSB

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the D/A transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH. Timing measurements are defined in Figure 5 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Pulse width, ALE HIGH	t_{ALPW}	45	-	-	ns
Muxed address valid time to ALE fall	t_{AS}	7.5	-	-	ns
Muxed address hold time from ALE fall	t_{AH}	20	-	-	ns
Read data delay time from $\overline{RD}$ fall	t_{DDR}	-	-	149	ns
Read data hold time from $\overline{RD}$ rise	t_{DHR}	0	-	55	ns
Pulse width, $\overline{RD}$ LOW	t_{RDPW}	200	-	-	ns
Write data set up time to $\overline{WR}$ rise	t_{DSW}	70	-	-	ns
Write data hold time from $\overline{WR}$ rise	t_{DHW}	10	-	-	ns
Pulse width, $\overline{WR}$ LOW	t_{WRPW}	100	-	-	ns
$\overline{RD}$ or $\overline{WR}$ delay time from ALE fall	t_{RWD}	25	-	-	ns
$\overline{CS}$ valid time to ALE fall	t_{CSS}	0	-	-	ns
$\overline{CS}$ hold time from $\overline{RD}$ or $\overline{WR}$ rise	t_{CSH}	0	-	-	ns
$\overline{ASE}$ valid time to ALE fall	t_{ASES}	45	-	-	ns
$\overline{ASE}$ hold time from ALE fall	t_{ASEH}	0	-	-	ns

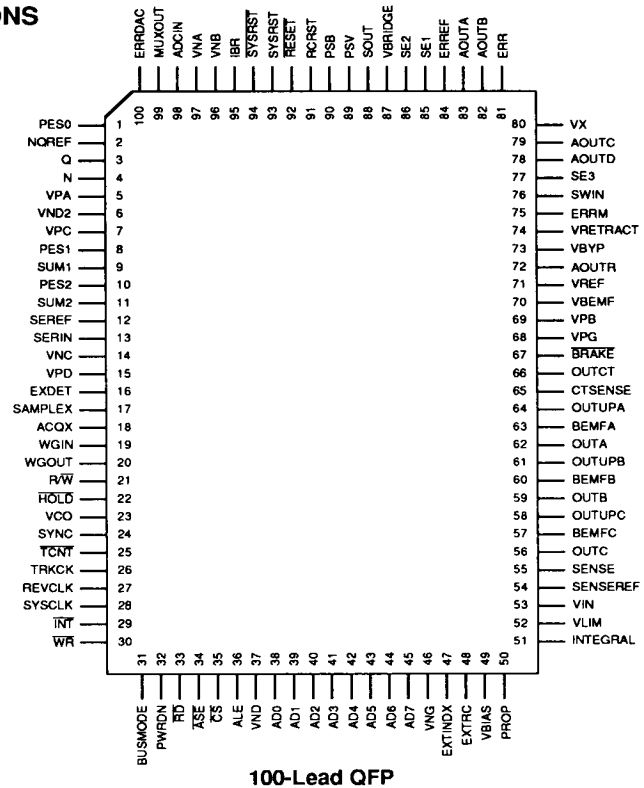
Motorola Microprocessor Interface Timing

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW. Timing measurements are defined in Figure 6 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Pulse width, AS HIGH	t_{ASPW}	45	-	-	ns
Muxed address valid time to AS fall	t_{AS}	10	-	-	ns
Muxed address hold time from AS fall	t_{AH}	20	-	-	ns
Read data delay time from DS rise	t_{DDR}	-	-	180	ns
Read data hold time from DS fall	t_{DHR}	0	-	80	ns
Pulse width, DS HIGH during READ	t_{DSPWR}	200	-	-	ns
Write data setup time to DS fall	t_{DSW}	70	-	-	ns
Write data hold time from DS fall	t_{DHW}	10	-	-	ns
Pulse width, DS HIGH during WRITE	t_{DSPWW}	100	-	-	ns
DS delay time from AS fall	t_{ASDS}	25	-	-	ns
R/$\overline{W}$ delay time from AS fall during WRITE	t_{ASRW}	25	-	-	ns
R/$\overline{W}$ hold time from DS fall during WRITE	t_{RWH}	0	-	-	ns
$\overline{CS}$ valid time to AS fall	t_{CSS}	0	-	-	ns
$\overline{CS}$ hold time from DS fall	t_{CSH}	0	-	-	ns
$\overline{ASE}$ valid time to AS fall	t_{ASES}	45	-	-	ns
$\overline{ASE}$ hold time from AS fall	t_{ASEH}	0	-	-	ns

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H4633 100-Lead QFP	32H4633-CG	32H4633-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914