

DESCRIPTION

The HYM532512 is a 512K x 32-bit Fast page mode CMOS DRAM module consisting of sixteen HY534256 in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM532512M is a Tin-Lead plated and HYM532512MG is a Gold plated socket type Single In-Line Memory Module suitable for easy interchange and addition of 2M byte memory.

FEATURES

- Low power dissipation
Max. CMOS standby 88.0mW
Max. TTL standby 176.0mW
Max. operating

Speed	Power
60	4.05W
70	3.61W
80	3.17W

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

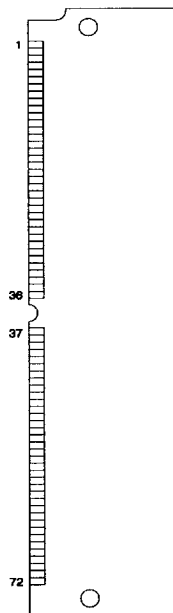
Speed	tRAC	tCAC	tPC
60	60ns	20ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	45ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh
- 512 refresh cycles / 8ms

PIN DESCRIPTION

RAS0-RAS3	Row Address Strobe
CAS0-CAS3	Column Address Strobe
WE	Write Enable
A0-A8	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground

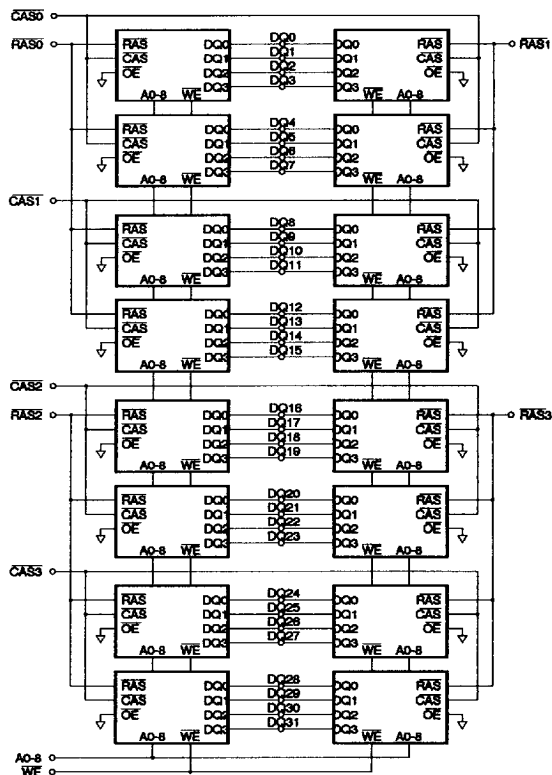
PIN CONNECTION



PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	CAS0
5	DQ17	41	CAS2
6	DQ2	42	CAS3
7	DQ18	43	CAS1
8	DQ3	44	RAS0
9	DQ19	45	RAS1
10	VCC	46	NC
11	NC	47	WE
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	NC	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	VCC
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	VCC	66	NC
31	A8	67	PD1
32	NC	68	PD2
33	RAS3	69	PD3
34	RAS2	70	PD4
35	NC	71	NC
36	NC	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-60	-70	-80
PD1	NC	NC	NC
PD2	Vss	Vss	Vss
PD3	NC	Vss	NC
PD4	NC	NC	Vss

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	9.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS≤VIN≤VCC+1.0, All other pins not under test = VSS		-160	160	μA	
ILO	Output Leakage Current (High Impedance State)	VSS≤VOUT≤VCC, RAS & CAS at VIH		-20	20	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	60 70 80	- - -	736 656 576	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs≥VSS		-	32	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	60 70 80	- - -	736 656 576	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	60 70 80	- - -	576 496 416	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V		-	16	mA	
ICC6	VCC Supply Current, CAS-before-RAS refresh	trc = trc (min.)	60 70 80	- - -	736 656 576	mA	1,3
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIL and CAS = VIH.

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532512M/MG						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	120	-	130	-	150	-	ns	
2	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	45	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	35	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	50	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRAS P	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	20	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	20	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	40	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	50	-	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	20	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	45	-	50	-	55	-	ns	
39	tREF	Refresh Period (512 cycles)	-	8	-	8	-	8	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

		HYM532512M/MG						UNIT	NOTE	
#	SYMBOL	PARAMETER	-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.			MAX.
41	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	15	-	15	-	15	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	40	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY534256 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. $twcs$ is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $twcs \geq twcs(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

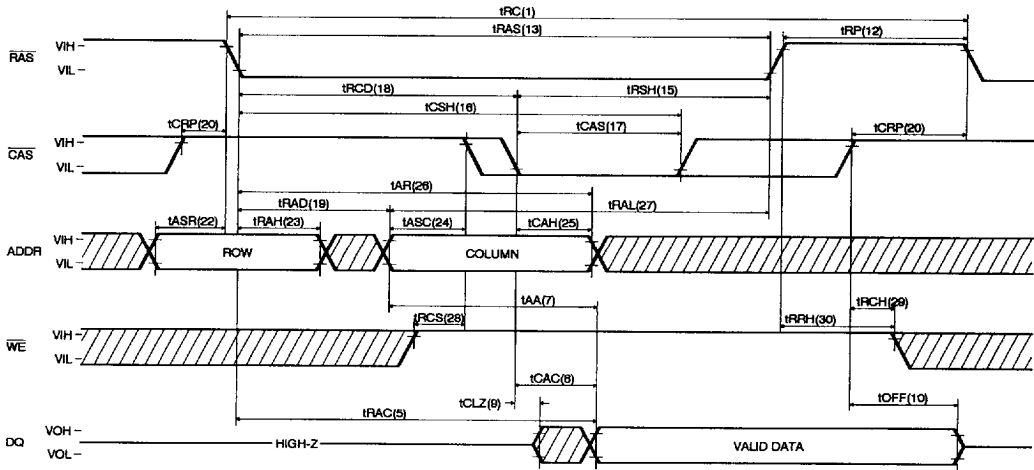
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $f = 1\text{MHz}$, unless otherwise noted.)

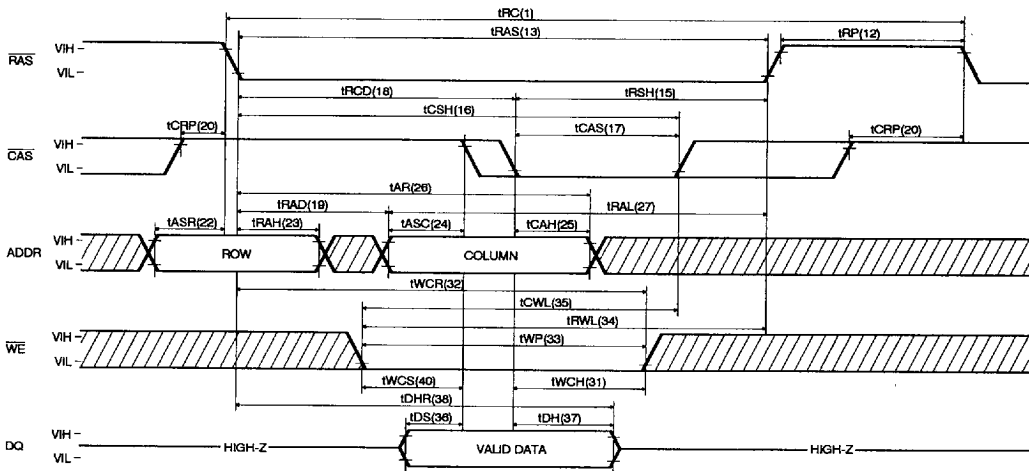
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A8)	-	121	pF
C_{IN2}	Input Capacitance (WE)	-	137	pF
C_{IN3}	Input Capacitance (RAS0-RAS3)	-	48	pF
C_{IN4}	Input Capacitance (CAS0-CAS3)	-	48	pF
C_{DQ}	Data Input/Output Capacitance (DQ0-DQ31)	-	29	pF

TIMING DIAGRAM

READ CYCLE



EARLY WRITE CYCLE

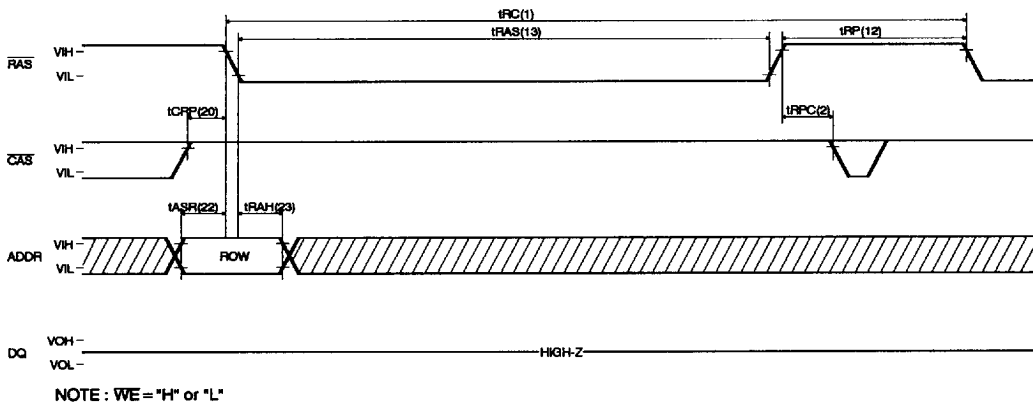


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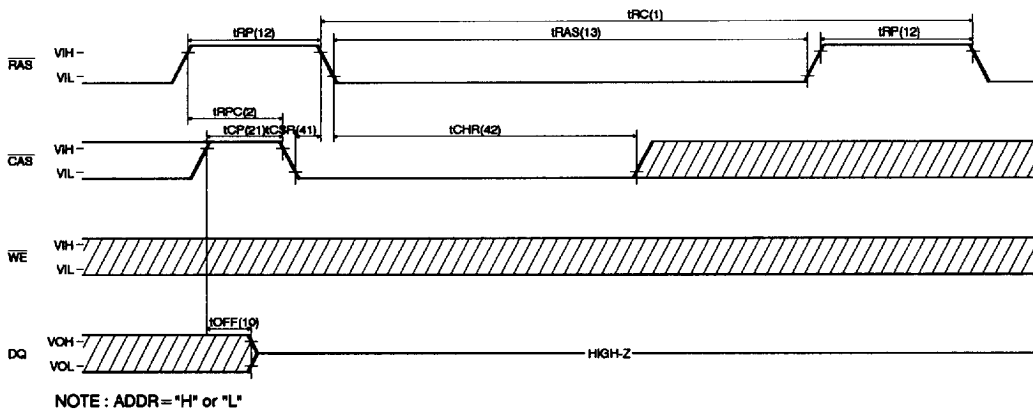
The timing diagram illustrates the relationship between the RAS, CAS, ADDR, WE, and DQ signals. Key timing parameters are defined as follows:

- RAS:** $t_{RASP}(14)$ (RAS pulse width), $t_{CRP}(20)$ (RAS to CAS setup), $t_{RHP}(4)$ (RAS hold).
- CAS:** $t_{CSH}(18)$ (CAS setup), $t_{RCD}(18)$ (RAS to CAS delay), $t_{CAS}(17)$ (CAS pulse width), $t_{CP}(21)$ (CAS to RAS delay), $t_{CAS}(17)$ (CAS hold), $t_{CRP}(20)$ (CAS to RAS setup).
- ADDR:** $t_{ASR}(22)$ (Address setup), $t_{RAH}(23)$ (Row Address hold), $t_{ASC}(24)$ (Address to CAS delay), $t_{CAH}(25)$ (Column Address hold), $t_{ASC}(24)$ (Address to CAS delay), $t_{CAH}(25)$ (Column Address hold), $t_{ASC}(24)$ (Address to CAS delay), $t_{CAH}(25)$ (Column Address hold).
- WE:** $t_{WCH}(31)$ (Write Enable setup), $t_{WCR}(32)$ (Write Enable to CAS delay), $t_{WCH}(31)$ (Write Enable hold), $t_{WCR}(32)$ (Write Enable to CAS delay).
- DQ:** $t_{DS}(36)$ (Data Setup), $t_{DHS}(37)$ (Data Hold), $t_{DHS}(37)$ (Data Hold), $t_{DS}(36)$ (Data Setup), $t_{DHS}(37)$ (Data Hold).

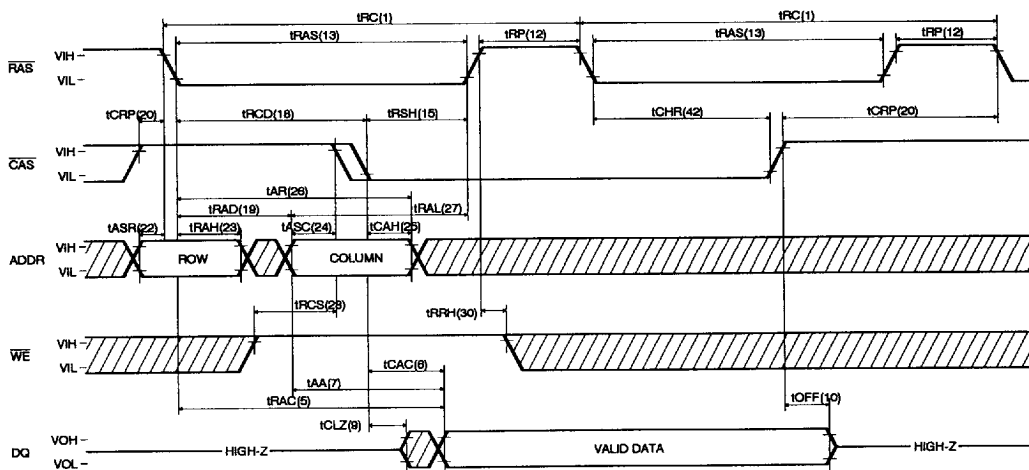
RAS-ONLY REFRESH CYCLE



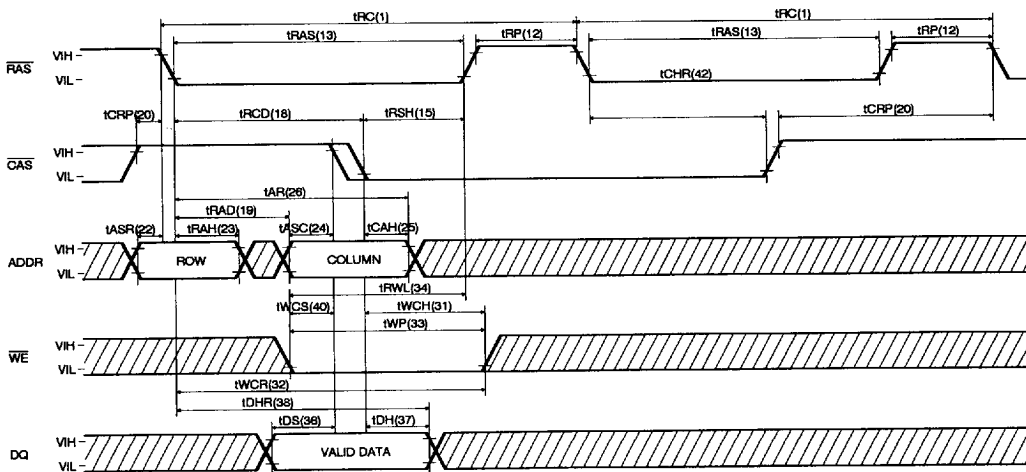
CAS-BEFORE-RAS REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)



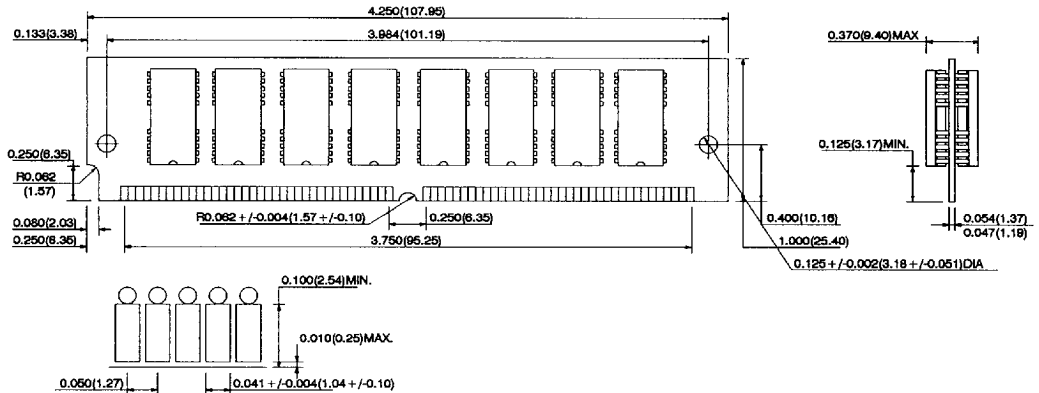
HIDDEN REFRESH CYCLE (WRITE)



PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532512M	60/70/80		SIMM	Tin-Lead
HYM532512MG	60/70/80		SIMM	Gold