CDK2307

Dual, 20/40/65/80MSPS, 12/13-bit Analog-to-Digital Converters

FEATURES

- 13-bit resolution
- 20/40/65/80MSPS maximum sampling rate
- Ultra-low power dissipation: 30/55/85/102mW
- SNR 72dB at 80MSPS and 8MHz F_{IN}
- Internal reference circuitry
- 1.8V core supply voltage
- 1.7V – 3.6V I/O supply voltage
- Parallel CMOS output
- 64-pin QFN package (TQFP-64 package option also available)
- Dual channel
- Pin compatible with CDK2308

APPLICATIONS

- Handheld Communication, PMR, SDR
- Medical Imaging
- Portable Test Equipment
- Digital Oscilloscopes
- Baseband / IF Communication
- Video Digitizing
- CCD Digitizing

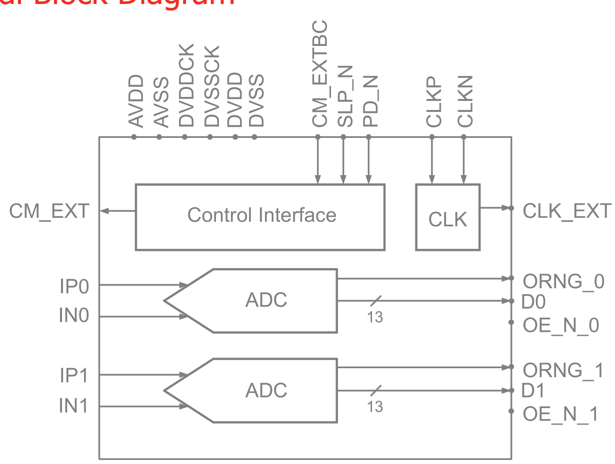
General Description

The CDK2307 is a high performance, low power dual Analog-to-Digital Converter (ADC). The ADC employs internal reference circuitry, a CMOS control interface and CMOS output data, and is based on a proprietary structure. Digital error correction is employed to ensure no missing codes in the complete full scale range.

Several idle modes with fast startup times exist. Each channel can be independently powered down and the entire chip can either be put in Standby Mode or Power Down mode. The different modes are optimized to allow the user to select the mode resulting in the smallest possible energy consumption during idle mode and startup.

The CDK2307 has a highly linear THA optimized for frequencies up to 70MHz. The differential clock interface is optimized for low jitter clock sources and supports LVDS, LVPECL, sine wave and CMOS clock inputs.

Functional Block Diagram



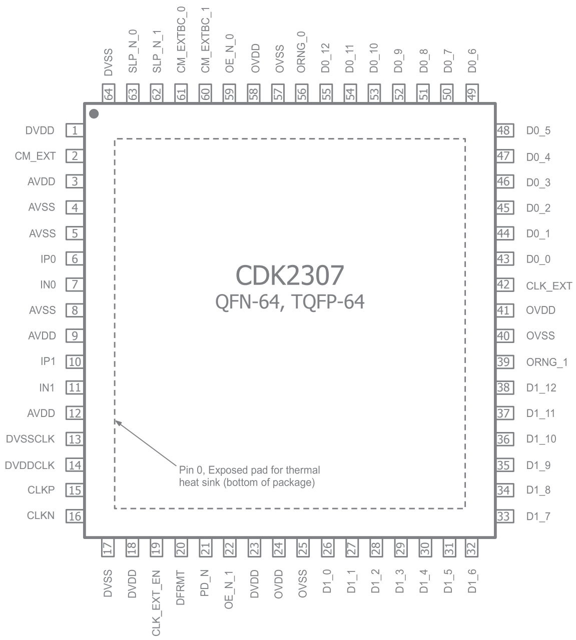
Ordering Information

Part Number	Speed	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CDK2307AILP64	20MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307BILP64	40MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307CILP64	65MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307DILP64	80MSPS	QFN-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307AITQ64	20MSPS	TQFP-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307BITQ64	40MSPS	TQFP-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307CITQ64	65MSPS	TQFP-64	Yes	Yes	-40°C to +85°C	Tray
CDK2307DITQ64	80MSPS	TQFP-64	Yes	Yes	-40°C to +85°C	Tray

Moisture sensitivity level for all parts is MSL-2A.

Pin Configuration

QFN-64, TQFP-64



Pin Assignments

Pin No.	Pin Name	Description
1, 18, 23	DVDD	Digital and I/O-ring pre driver supply voltage, 1.8V
2	CM_EXT	Common Mode voltage output
3, 9, 12	AVDD	Analog supply voltage, 1.8V
4, 5, 8	AVSS	Analog ground
6, 7	IP0, IN0	Analog input Channel 0 (non-inverting, inverting)
10, 11	IP1, IN1	Analog input Channel 1 (non-inverting, inverting)
13	DVSSCLK	Clock circuitry ground
14	DVDDCLK	Clock circuitry supply voltage, 1.8V
15	CLKP	Clock input, non-inverting (Format: LVDS, PECL, CMOS/TTL, Sine Wave)
16	CLKN	Clock input, inverting. For CMOS input on CLKP, connect CLKN to ground
17, 64	DVSS	Digital circuitry ground
19	CLK_EXT_EN	CLK_EXT signal enabled when low (zero). Tristate when high.
20	DFRMT	Data format selection. 0: Offset Binary, 1: Two's Complement
21	PD_N	Full chip Power Down mode when Low. All digital outputs reset to zero. After chip power up, always apply Power Down mode before using Active Mode to reset chip.
22	OE_N_1	Output Enable Channel 0. Tristate when high.
24, 41, 58	OVDD	I/O ring post-driver supply voltage. Voltage range 1.7V to 3.6V.
25, 40, 57	OVSS	Ground for I/O ring
26	D1_0	Output Data Channel 1 (LSB, 13-bit output or $1V_{pp}$ full scale range)
27	D1_1	Output Data Channel 1 (LSB, 12-bit output $2V_{pp}$ full scale range)
28	D1_2	Output Data Channel 1
29	D1_3	Output Data Channel 1

Pin Assignments *(Continued)*

Pin No.	Pin Name	Description
30	D1_4	Output Data Channel 1
31	D1_5	Output Data Channel 1
32	D1_6	Output Data Channel 1
33	D1_7	Output Data Channel 1
34	D1_8	Output Data Channel 1
35	D1_9	Output Data Channel 1
36	D1_10	Output Data Channel 1
37	D1_11	Output Data Channel 1 (MSB for $1V_{PP}$ full scale range, see Reference Voltages section)
38	D1_12	Output Data Channel 1 (MSB for $2V_{PP}$ full scale range)
39	ORNG_1	Out of Range flag Channel 1. High when input signal is out of range
42	CLK_EXT	Output clock signal for data synchronization. CMOS levels.
43	D0_0	Output Data Channel 0 (LSB, 13 bit output or 1Vpp full scale range)
44	D0_1	Output Data Channel 0 (LSB, 12 bit output 2Vpp full scale range)
45	D0_2	Output Data Channel 0
46	D0_3	Output Data Channel 0
47	D0_4	Output Data Channel 0
48	D0_5	Output Data Channel 0
49	D0_6	Output Data Channel 0
50	D0_7	Output Data Channel 0
51	D0_8	Output Data Channel 0
52	D0_9	Output Data Channel 0
53	D0_10	Output Data Channel 0
54	D0_11	Output Data Channel 0 (MSB for $1V_{PP}$ full scale range, see Reference Voltages section)
55	D0_12	Output Data Channel 0 (MSB for $2V_{PP}$ full scale range)
56	ORNG_0	Out of Range flag Channel 0. High when input signal is out of range.
59	OE_N_0	Output Enable Channel 0. Tristate when low.
60, 61	CM_EXTBC_1, CM_EXTBC_0	Bias control bits for the buffer driving pin CM_EXT 00: Off 01: 50uA 10: 500uA 11: 1mA
62, 63	SLP_N_1, SLP_N_0	Sleep Mode 00: Sleep Mode 01: Channel 0 active 10: Channel 1 active 11: Both channels active

Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
AVDD, AVSS	-0.3	+2.3	V
DVDD, DVSS	-0.3	+2.3	V
AVSS, DVSSCLK, DVSS, OVSS	-0.3	+0.3	V
OVDD, OVSS	-0.3	+3.9	V
CKP, CKN, DVSSCLK	-0.3	+3.9	V
Analog inputs and outpts (IPx, INx, AVSS)	-0.3	+2.3	V
Digital inputs	-0.3	+3.9	V
Digital outputs	-0.3	+3.9	V

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature	-40		85	°C
Storage Temperature Range	-60		+150	°C
Lead Temperature (Soldering, 10s)	J-STD-020			

ESD Protection

Product	QFN-64	TQFP-64
Human Body Model (HBM)	2kV	2kV

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C

Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 20/40/65/80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy						
	No Missing Codes			Guaranteed		
	Offset Error	Midscale offset		1		LSB
	Gain Error	Full scale range deviation from typical	-6		6	%FS
	Gain Matching	Gain matching between channels. ±3 sigma value at worst case conditions.		±0.5		%FS
DNL	Differential Non-Linearity	12-bit level		±0.2		LSB
INL	Integral Non-Linearity	12-bit level		±0.6		LSB
V_{CMO}	Common Mode Voltage Output			VAVDD/2		V
Analog Input						
V_{CMI}	Input Common Mode	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
V_{FSR}	Full Scale Range, Normal	Differential input voltage range,		2.0		Vpp
	Full Scale Range, Option	Differential input voltage range, 1V (see section Reference Voltages)		1.0		Vpp
	Input Capacitance	Differential input capacitance		2.0		pF
	Bandwidth	Input bandwidth, full power	500			MHz
Power Supply						
AVDD, DVDD	Core Supply Voltage	Supply voltage to all 1.8V domain pins. See Pin Configuration and Description	1.7	1.8	2.0	V
OVDD	I/O Supply Voltage	Output driver supply voltage (OVDD). Must be higher than or equal to Core Supply Voltage (VOVDD ≥ VDVDD)	1.7	2.5	3.6	V

Electrical Characteristics - CDK2307A

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 20MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 2MHz		72.5		dBFS
		F_{IN} = 8MHz	71.5	72.2		dBFS
		$F_{IN} \simeq$ FS/2		72.1		dBFS
		F_{IN} = 20MHz		71.6		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 2MHz		72.4		dBFS
		F_{IN} = 8MHz	71	72		dBFS
		$F_{IN} \simeq$ FS/2		71.7		dBFS
		F_{IN} = 20MHz		71.3		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 2MHz		87		dBc
		F_{IN} = 8MHz	75	85		dBc
		$F_{IN} \simeq$ FS/2		80		dBc
		F_{IN} = 20MHz		80		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 2MHz		-90		dBc
		F_{IN} = 8MHz	-85	-95		dBc
		$F_{IN} \simeq$ FS/2		-95		dBc
		F_{IN} = 20MHz		-95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 2MHz		-87		dBc
		F_{IN} = 8MHz	-75	-85		dBc
		$F_{IN} \simeq$ FS/2		-80		dBc
		F_{IN} = 20MHz		-80		dBc
ENOB	Effective number of Bits	F_{IN} = 2MHz		11.7		bits
		F_{IN} = 8MHz	11.5	11.7		bits
		$F_{IN} \simeq$ FS/2		11.6		bits
		F_{IN} = 20MHz		11.6		bits
X_{TALK}	Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-105		dB
Power Supply						
AIDD	Analog Supply Current			11.6		mA
DIDD	Digital Supply Current	Digital core supply		1.8		mA
OIDD	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz		2.9		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		2.4		mA
	Analog Power Dissipation			20.9		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		9.2		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		30.1		mW
	Power Down Dissipation			9.9		µW
	Sleep Mode 1	Power Dissipation, Sleep mode one channel		20.5		mW
	Sleep Mode 2	Power Dissipation, Sleep mode both channels		9.2		mW
Clock Inputs						
	Max. Conversion Rate		20			MSPS
	Min. Conversion Rate			15		MSPS

Electrical Characteristics - CDK2307B

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 40MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 2MHz		72.5		dBFS
		F_{IN} = 8MHz	71.9	72.7		dBFS
		F_{IN} ≃ FS/2		72		dBFS
		F_{IN} = 30MHz		70.8		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 2MHz		71.7		dBFS
		F_{IN} = 8MHz	71	72.1		dBFS
		F_{IN} ≃ FS/2		71.5		dBFS
		F_{IN} = 30MHz		71.2		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 2MHz		81		dBc
		F_{IN} = 8MHz	75	81		dBc
		F_{IN} ≃ FS/2		80		dBc
		F_{IN} = 30MHz		80		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 2MHz		-90		dBc
		F_{IN} = 8MHz	-85	-95		dBc
		F_{IN} ≃ FS/2		-95		dBc
		F_{IN} = 30MHz		-90		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 2MHz		-81		dBc
		F_{IN} = 8MHz	-75	-81		dBc
		F_{IN} ≃ FS/2		-80		dBc
		F_{IN} = 30MHz		-80		dBc
ENOB	Effective number of Bits	F_{IN} = 2MHz		11.6		bits
		F_{IN} = 8MHz	11.5	11.7		bits
		F_{IN} ≃ FS/2		11.6		bits
		F_{IN} = 30MHz		11.5		bits
X_{TALK}	Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-100		dB
Power Supply						
AIDD	Analog Supply Current			21.1		mA
DIDD	Digital Supply Current	Digital core supply		3.3		mA
OIDD	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz		5.3		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		4.4		mA
	Analog Power Dissipation			38.0		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		16.9		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		54.9		mW
	Power Down Dissipation			9.7		µW
	Sleep Mode 1	Power Dissipation, Sleep mode one channel		36.1		mW
	Sleep Mode 2	Power Dissipation, Sleep mode both channels		14.2		mW
Clock Inputs						
	Max. Conversion Rate		40			MSPS
	Min. Conversion Rate			20		MSPS

Electrical Characteristics - CDK2307C

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 65MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	71.6	72.6		dBFS
		F_{IN} = 20MHz		71.8		dBFS
		$F_{IN} \simeq$ FS/2		71.5		dBFS
		F_{IN} = 40MHz		70.4		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	70.5	71.7		dBFS
		F_{IN} = 20MHz		71.7		dBFS
		$F_{IN} \simeq$ FS/2		71.7		dBFS
		F_{IN} = 40MHz		70		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	75	81		dBc
		F_{IN} = 20MHz		84		dBc
		$F_{IN} \simeq$ FS/2		79		dBc
		F_{IN} = 40MHz		77		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	-85	-95		dBc
		F_{IN} = 20MHz		-95		dBc
		$F_{IN} \simeq$ FS/2		-95		dBc
		F_{IN} = 40MHz		-95		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	-75	-81		dBc
		F_{IN} = 20MHz		-84		dBc
		$F_{IN} \simeq$ FS/2		-79		dBc
		F_{IN} = 40MHz		-79		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz	11.4	11.6		bits
		F_{IN} = 20MHz		11.6		bits
		$F_{IN} \simeq$ FS/2		11.5		bits
		F_{IN} = 40MHz		11.3		bits
X_{TALK}	Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-95		dB
Power Supply						
AIDD	Analog Supply Current			32.8		mA
DIDD	Digital Supply Current	Digital core supply		5.0		mA
OIDD	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz		8.2		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		6.6		mA
	Analog Power Dissipation			59.0		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		25.5		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		84.5		mW
	Power Down Dissipation			9.3		µW
	Sleep Mode 1	Power Dissipation, Sleep mode one channel		55.3		mW
	Sleep Mode 2	Power Dissipation, Sleep mode both channels		20.4		mW
Clock Inputs						
	Max. Conversion Rate		65			MSPS
	Min. Conversion Rate			40		MSPS

Electrical Characteristics - CDK2307D

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Performance						
SNR	Signal to Noise Ratio	F_{IN} = 8MHz	70.4	72		dBFS
		F_{IN} = 20MHz		71.7		dBFS
		F_{IN} = 30MHz		71.2		dBFS
		F_{IN} ≃ FS/2		70.7		dBFS
SINAD	Signal to Noise and Distortion Ratio	F_{IN} = 8MHz	69.5	70.5		dBFS
		F_{IN} = 20MHz		70.5		dBFS
		F_{IN} = 30MHz		70.4		dBFS
		F_{IN} ≃ FS/2		70.3		dBFS
SFDR	Spurious Free Dynamic Range	F_{IN} = 8MHz	74	77		dBc
		F_{IN} = 20MHz		78		dBc
		F_{IN} = 30MHz		78		dBc
		F_{IN} ≃ FS/2		78		dBc
HD2	Second order Harmonic Distortion	F_{IN} = 8MHz	-80	-95		dBc
		F_{IN} = 20MHz		-90		dBc
		F_{IN} = 30MHz		-90		dBc
		F_{IN} ≃ FS/2		-85		dBc
HD3	Third order Harmonic Distortion	F_{IN} = 8MHz	-74	-77		dBc
		F_{IN} = 20MHz		-78		dBc
		F_{IN} = 30MHz		-78		dBc
		F_{IN} ≃ FS/2		-78		dBc
ENOB	Effective number of Bits	F_{IN} = 8MHz	11.3	11.4		bits
		F_{IN} = 20MHz		11.4		bits
		F_{IN} = 30MHz		11.4		bits
		F_{IN} ≃ FS/2		11.4		bits
X_{TALK}	Crosstalk	Signal crosstalk between channels, F_{IN1} = 8MHz, F_{IN0} = 9.9MHz		-95.0		dB
Power Supply						
AIDD	Analog Supply Current			39.7		mA
DIDD	Digital Supply Current	Digital core supply		6.0		mA
OIDD	Output Driver Supply	2.5V output driver supply, sine wave input, F_{IN} = 1MHz		9.4		mA
		2.5V output driver supply, sine wave input, F_{IN} = 1MHz, CLK_EXT disabled		7.7		mA
	Analog Power Dissipation			71.5		mW
	Digital Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		30		mW
	Total Power Dissipation	OVDD = 2.5V, 5pF load on output bits, F_{IN} = 1MHz, CLK_EXT disabled		101.5		mW
	Power Down Dissipation			9.1		µW
	Sleep Mode 1	Power Dissipation, Sleep mode one channel		66.4		mW
	Sleep Mode 2	Power Dissipation, Sleep mode both channels		24.1		mW
Clock Inputs						
	Max. Conversion Rate		80			MSPS
	Min. Conversion Rate			65		MSPS

Digital and Timing Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 50 MSPS clock, 50% clock duty cycle, -1 dBFS input signal, 5pF capacitive load, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Clock Inputs						
	Duty Cycle		20		80	% high
	Compliance		CMOS, LVDS, LVPECL, Sine Wave			
	Input Range	Differential input swing	400			mVpp
		Differential input swing, sine wave clock input	1.6			Vpp
	Input Common Mode Voltage	Keep voltages within ground and voltage of OVDD	0.3		VOVDD -0.3	V
	Input Capacitance	Differential		2		pF
Timing						
T_{PD}	Start Up Time Active Mode	From Power Down Mode to Active Mode			900	clk cycles
T_{SLP}	Start Up Time Mode	From Sleep Mode to Active			20	clk cycles
T_{OVR}	Out Of Range Recovery Time			1		clk cycles
T_{AP}	Aperture Delay			0.8		ns
ε_{RMS}	Aperture Jitter			<0.5		psrms
T_{LAT}	Pipeline Delay			12		clk cycles
T_D	Output Delay (see timing diagram)	5pF load on output bits	3		10	ns
T_{DC}	Output Delay (see timing diagram)	Relative to CLK_EXT	1		6	ns
Logic Inputs						
V_{HI}	High Level Input Voltage	VOVDD ≥ 3.0V	2			V
		VOVDD = 1.7V – 3.0V	0.8 • VOVDD			V
V_{LI}	Low Level Input Voltage	VOVDD ≥ 3.0V	0		0.8	V
		VOVDD = 1.7V – 3.0V	0		0.2 • VOVDD	V
I_{HI}	High Level Input Leakage Current		-10		10	µA
I_{LI}	Low Level Input Leakage Current		-10		10	µA
C_I	Input Capacitance			3		pF
Logic Outputs						
V_{HO}	High Level Output Voltage		VOVDD-0.1			V
V_{LO}	Low Level Output Voltage				0.1	V
C_L	Max Capacitive Load	Post-driver supply voltage equal to pre-driver supply voltage VOVDD = VDVDD			5	pF
		Post-driver supply voltage above 2.25V (1)		10		pF

Note:

(1) The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum.

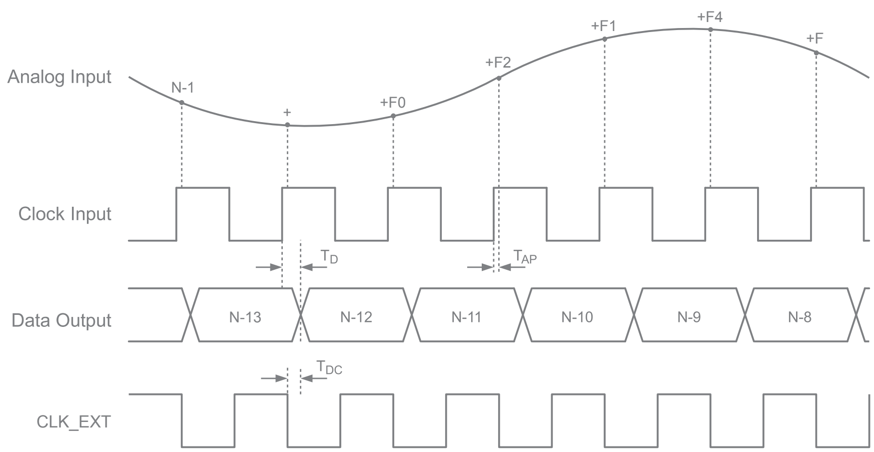


Figure 1. Timing Diagram

Recommended Usage

Analog Input

The analog input to the CDK2307 is done through a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at mid supply common mode voltage is recommended even if performance will be good for the ranges specified. The CM_EXT pin provides a voltage suitable for a common mode voltage reference. The internal buffer for the CM_EXT voltage can be switched off, and driving capabilities can be changed by using the CM_EXTBC control input.

Figure 2 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22Ω) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

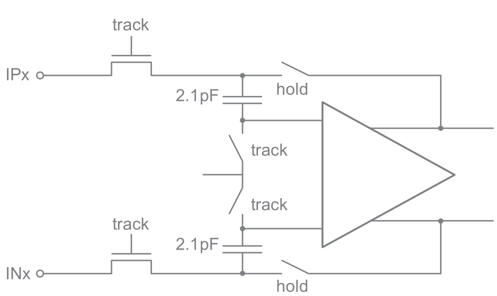


Figure 2. Input Configuration

DC-Coupling

Figure 3 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the CM_EXT output should be used as a reference to set the common mode voltage.

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the CDK2307 input specifications.

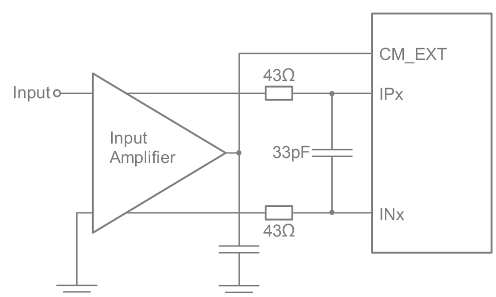


Figure 3. DC-Coupled Input

Detailed configuration and usage instructions must be found in the documentation of the selected driver.

AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 4 shows a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to keep phase mismatch between the differential ADC inputs small for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must hence be taken into account during PCB layout.

If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in Figure 6 can be used.

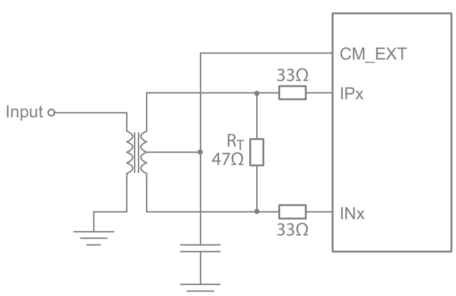


Figure 4. Transformer-Coupled Input

Figure 5 shows AC-coupling using capacitors. Resistors from the CM_EXT output, RCM, should be used to bias the differential input signals to the correct voltage. The series capacitor, CI, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

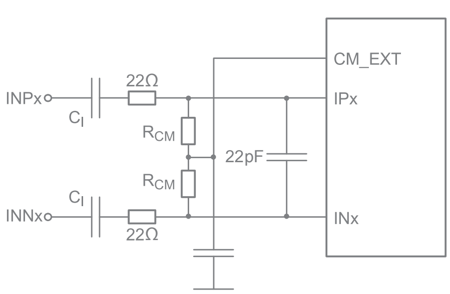


Figure 5. AC-Coupled Input

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of Figure 6 can be used. The configuration is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the energy traveling towards the source. However, the impedance match seen into the transformer will become worse.

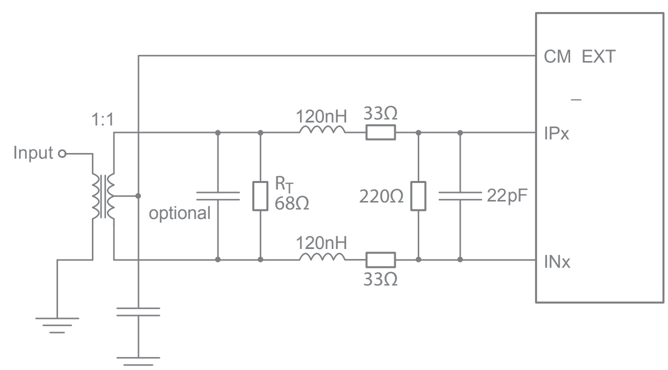


Figure 6. Alternative Input Network

Clock Input And Jitter Considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the CDK2307 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% are acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally, and hence a wide common mode voltage range is accepted. Differential clock sources such as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. For differential sine wave clock input the amplitude must be at least ±800mV$_{pp}$.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1.

$$SNR_{jitter} = 20 \cdot \log (2 \cdot \pi \cdot F_{IN} \cdot \varepsilon_t)$$

where F_{IN} is the signal frequency, and ε_t is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be retimed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Digital Outputs

Digital output data are presented in a parallel CMOS form. The voltage on the OVDD pin sets the levels of the CMOS outputs. The output drivers are dimensioned to drive a wide range of loads for OVDD above 2.25V, but it is recommended to minimize the load to ensure as low transient switching currents and resulting noise as possible. In applications with a large fanout or large capacitive loads, it is recommended to add external buffers located close to the ADC chip.

The timing is described in the Timing Diagram section. Note that the load or equivalent delay on CLK_EXT always should be lower than the load on data outputs to ensure sufficient timing margins.

The digital outputs can be set in tristate mode by setting the OE_N signal high.

Note that the out of range flags (ORNG) will behave differently for 12-bit and 13-bit output. For 13-bit output ORNG will be set when digital output data are all ones or all zeros. For 12-bit output the ORNG flags will be set when all twelve bits are zeros or ones and when the thirteenth bit is equal to the rest of the bits.

The CDK2307 employs digital offset correction. This means that the output code will be 4096 with the positive and negative inputs shorted together(zero differential). However, small mismatches in parasitics at the input can cause this to alter slightly. The offset correction also results in possible loss of codes at the edges of the full scale range. With "NO" offset correction, the ADC would clip in one end before the other, in practice resulting in code loss at the opposite end. With the output being centered digitally, the output will clip, and the out of range flags will be set, before max code is reached. When out of range flags are set, the code is forced to all ones for over-range and all zeros for under-range.

Data Format Selection

The output data are presented on offset binary form when DFRMT is low (connect to OVSS). Setting DFRMT high (connect to OVDD) results in 2's complement output format. Details are shown in Table 1 on page 14.

The data outputs can be used in three different configurations.

Normal mode:

All 13-bits are used. MSB is Dx_12 and LSB is Dx_0. This mode gives optimum performance due to reduced quantization noise.

12-bit mode:

The LSB is left unconnected such that only 12 bits are used. MSB is Dx_12 and LSB is Dx_1. This mode gives slightly reduced performance, due to increased quantization noise.

Reduced full scale range mode:

The full scale range is reduced from $2V_{pp}$ to $1V_{pp}$ which is equivalent to 6dB gain in the ADC frontend. MSB is Dx_11 and LSB is Dx_0. Note that the codes will wrap around when exceeding the full scale range, and that out of range bits should be used to clamp output data. See section Reference Voltages for details. This mode gives slightly reduced performance.

Table 1: Data Format Description for $2V_{pp}$ Full Scale Range

Differential Input Voltage (IPx - INx)	Output data: Dx_12 : Dx_0 (DFRMT = 0, offset binary)	Output Data: Dx_12 : Dx_0 (DFRMT = 1, 2's complement)
1.0 V	1 1111 1111 1111	0 1111 1111 1111
+0.24mV	1 0000 0000 0000	0 0000 0000 0000
-0.24mV	0 1111 1111 1111	1 1111 1111 1111
-1.0V	0 0000 0000 0000	1 0000 0000 0000

Reference Voltages

The reference voltages are internally generated and buffered based on a bandgap voltage reference. No external decoupling is necessary, and the reference voltages are not available externally. This simplifies usage of the ADC since two extremely sensitive pins, otherwise needed, are removed from the interface.

If a lower full scale range is required the 13-bit output word provides sufficient resolution to perform digital scaling-with an equivalent impact on noise compared to adjusting the reference voltages.

A simple way to obtain $1.0V_{pp}$ input range with a 12-bit output word is shown in the table on page 10. Note that only 2's complement output data are available in this mode and that out of range conditions must be determined based on a two bit output. The output code will wrap around when the code goes outside the full scale range. The out of range bits should be used to clamp the output data for overrange conditions.

Operational Modes

The operational modes are controlled with the PD_N and SLP_N pins. If PD_N is set low, all other control pins are overridden and the chip is set in Power Down mode. In this mode all circuitry is completely turned off and the internal clock is disabled. Hence, only leakage current contributes to the Power Down Dissipation. The startup time from this mode is longer than for other idle modes as all references need to settle to their final values before normal operation can resume.

The SLP_N bus can be used to power down each channel independently, or to set the full chip in Sleep Mode. In this mode internal clocking is disabled, but some low bandwidth circuitry is kept on to allow for a short startup time. However, Sleep Mode represents a significant reduction in supply current, and it can be used to save power even for short idle periods.

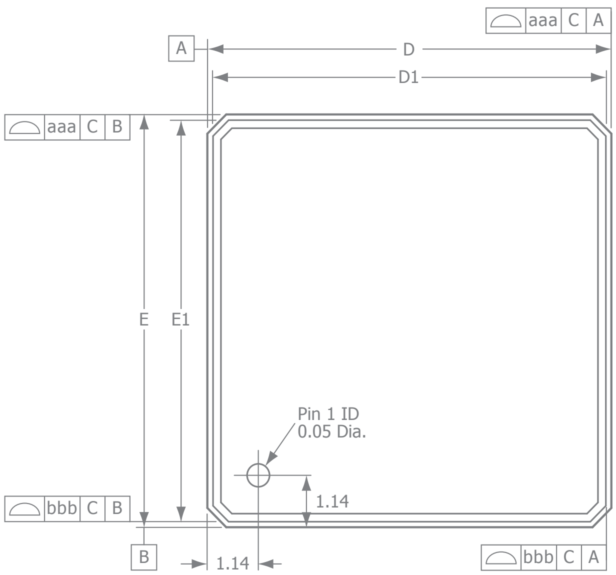
The input clock could be kept running in all idle modes. However, even lower power dissipation is possible in Power Down mode if the input clock is stopped. In this case it is important to start the input clock prior to enabling active mode.

Table 2: Data Format Description for $1V_{pp}$ Full Scale Range

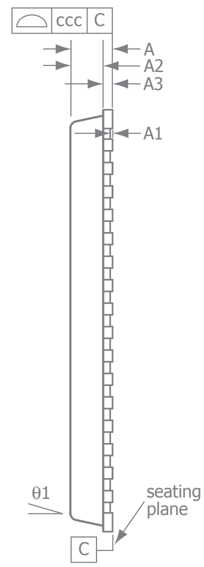
Differential Input Voltage (IPx - INx)	Output data: Dx_11: Dx_0 (DFRMT = 0) (2's Complement)	Out of Range (Use Logical AND Function for &)	Output Data: Dx_11: Dx_0 (DFRMT = 1) (2's Complement)	Out of Range (Use Logical AND Function for &)
> 0.5V	0111 1111 1111	Dx_12 = 1 & Dx_11 = 1	0111 1111 1111	D_12 = 0 & D_11 = 1
0.5V	0111 1111 1111		0111 1111 1111	
+0.24mV	0000 0000 0000		0000 0000 0000	
-0.24mV	1111 1111 1111		1111 1111 1111	
-0.5V	1000 0000 0000		1000 0000 0000	
< -0.5V	1000 0000 0000	Dx_12 = 0 & Dx_11 = 0	1000 0000 0000	Dx_12 = 1 & Dx_11 = 0

Mechanical Dimensions

QFN-64 Package



TOP VIEW

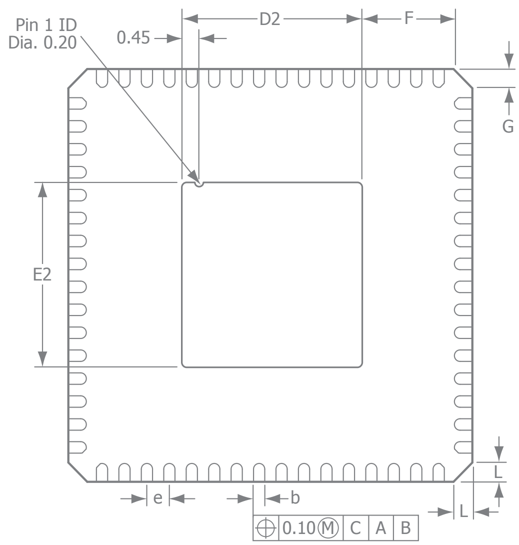


SIDE VIEW

	Inches			Millimeters		
Symbol	Min	Typ	Max	Min	Typ	Max
A	–	–	0.035	–	–	0.9
A_1	0.00	0.0004	0.002	0.00	0.01	0.05
A_2	–	0.026	0.028	–	0.65	0.7
A_3		0.008 REF			0.2 REF	
b	0.008	0.010	0.012	0.2	0.25	0.30
D		0.354 BSC			9.00 BSC	
D_1		0.354 BSC			8.75 BSC	
D_2	0.197	0.205	0.213	5.0	5.2	5.4
E		0.354 BSC			9.00 BSC	
E_1		0.344 BSC			8.75 BSC	
E_2	0.197	0.205	0.213	5.0	5.2	5.4
F	0.05	–	–	1.3	–	–
G	0.0096	0.0168	0.024	0.24	0.42	0.6
L	0.012	0.016	0.020	0.3	0.4	0.5
e		0.020 BSC			0.50 BSC	
θ_1	0°	–	12°	0°	–	12°
Tolerance of Form and Position						
aaa		0.10			0.004	
bbb		0.10			0.004	
ccc		0.05			0.002	

NOTES:

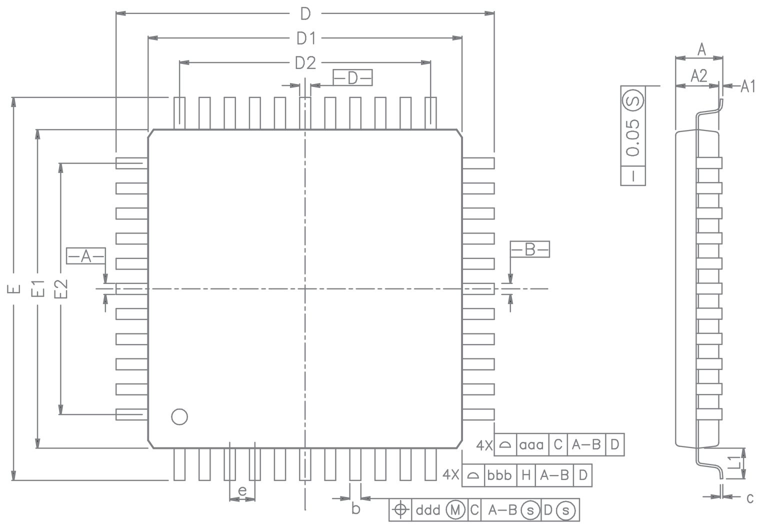
1. All dimensions are in millimeters.
2. Die thickness allowable is 0.305mm maximum (.012 inches maximum)
3. Dimensioning & tolerances conform to ASME y14.5m. -1994.
4. Dimension applies to plated terminal and is measured between 0.20 and 0.25mm from terminal tip.
5. The pin #1 identifier must be placed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max 0.08mm.
8. Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.
9. Applied only to terminals.
10. Package corners unless otherwise specipied are r0.175±0.025mm.



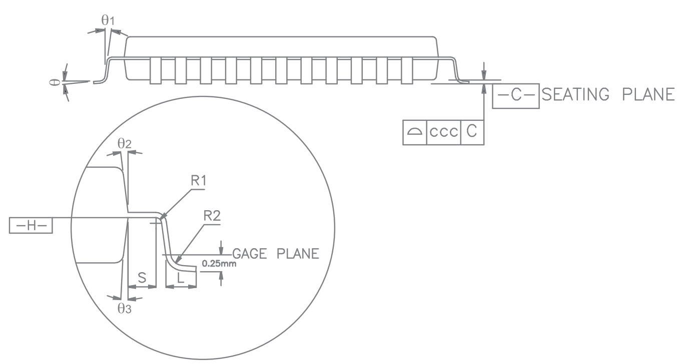
BOTTOM VIEW

Mechanical Dimensions (Continued)

TQFP-64 Package



TOP VIEW SIDE VIEW



DETAIL SIDE VIEW

	Inches			Millimeters		
Symbol	Min	Typ	Max	Min	Typ	Max
A	–	–	0.047	–	–	1.2
A_1	0.002	–	0.006	0.05	–	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
D		0.472 BSC			12.00 BSC	
D_1		0.393 BSC			10.00 BSC	
E		0.472 BSC			12.00 BSC	
E_1		0.393 BSC			10.00 BSC	
R_2	0.003	–	0.008	0.08	–	0.20
R_1	0.003	–	–	0.08	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	–	–	0°	–	–
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
c	0.004	–	0.008	0.09	0.20	
L	0.018	0.24	0.030	0.45	0.75	
L_1		0.039 REF			1.00 REF	
S	0.008	–	–	0.20	–	–
b	0.007	0.008	0.011	0.17	0.20	0.27
e		0.020 BSC			0.520 BSC	
D_2		0.295			7.50	
E_2		0.295			7.50	
aaa		0.008			0.20	
bbb		0.008			0.20	
ccc		0.003			0.08	
ddd		0.003			0.08	

NOTES:

1. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maxmum plastic body size dimensions including mold mismatch.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.
3. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.

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