REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
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SHEET	22	23	24	25	26	27																		
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21		

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Kenneth S. Rice

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
24 MAY 1990

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS UV ERASABLE ASYNCHRONOUS REGISTERED PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90754
A	67268	

SHEET 1

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1674

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6). Two product assurance classes, military high reliability (device classes B, Q, or M) and space application (device classes S or V) and a choice of case outlines and lead finishes are available and are reflected in the complete part number. Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the complete part number.

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962	-	90754	01	M	X	X
Federal stock class designator	RHA designator (1.2.1)		Device type (1.2.2)	Device class designator (1.2.3)	Case outline (1.2.4)	Lead finish (1.2.5)
Drawing number						

1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, or S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q or V devices shall meet or exceed the electrical performance characterictics specified in table I herein after exposure to the specified irradiation levels specified in the absolute maximum ratings herein and the RHA marked device shall be marked in accordance with MIL-I-38535. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	CY7C331-40	Asynchronous Registered PLD	40 ns
02	CY7C331-30	Asynchronous Registered PLD	30 ns
03	CY7C331-25	Asynchronous Registered PLD	25 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level (see 6.7 herein) as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outlines. Device classes M, B, or S case outlines shall meet the requirements in appendix C of MIL-M-38510 and as listed below. Device classes Q or V case outlines shall meet the requirements of MIL-I-38535, appendix C of MIL-M-38510, and as listed below.

Outline letter	Case outline
X	See figure 1, (28-lead, 1.485" x .310" x .200"), dual-in-line package 1/
Y	F-11 (28-lead, .740" x .380" x .090"), flat package 1/
Z	See figure 2, (28-lead, .458" x .458" x .180"), J-leaded chip carrier 1/
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package 1/

1/ Lid shall be transparent to permit ultraviolet light erasure.

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, or S or MIL-I-38535 for classes Q or V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, or C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 2/

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation 3/	1.2 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines Y and 3	See MIL-M-38510, appendix C
Case outline X	26°C/W 4/
Case outline Z	20°C/W 4/
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q or V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
4/ When the thermal resistance for this case is specified in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.
5/ When a QML source exists, a value shall be provided.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B or S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B or S a full electrical characterization table for each device type shall be included in this SMD when a qualified source exists. The individual item requirements for device classes Q or V shall be in accordance with MIL-I-38535 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, or S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figures 1 and 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Truth table. The truth table shall be as specified on figure 4.

3.2.3.1 Unprogrammed or erased devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 4. When required in groups A, C, or D (see 4.4), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless therwise specified, the electrical performance characteristics and post irradiation parameter imits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the part number listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103. Marking for device classes B or S shall be in accordance with MIL-M-38510. Marking for device classes Q or V shall be in accordance with MIL-I-38535.

3.5.1 Quality mark. The quality mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The quality mark for device classes B or S shall be a "J" or "JAN" as required in MIL-M-38510. The quality mark for device classes Q or V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). For device classes Q or V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein) or, for device classes Q or V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B or S in MIL-M-38510 or for device classes Q or V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECS of hange of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, or S. Device classes M, B, or S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

3.12 Processing EPLDs. All testing requirements and qaulity assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.12.1 Erasure of EPLDs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.

3.12.2 Programmability of EPLDs. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.6.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA, $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA, $V_{IN} = V_{IH}, V_{IL}$	1, 2, 3	All		0.5	V
Input high voltage 1/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 1/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-40	40	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0.5 V	1, 2, 3	All	-30	-90	mA
Power supply current at frequency 3/	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND, f = max	1, 2, 3	All		200	mA
Standby power supply current	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA, V_{IN} = GND	1, 2, 3	All		150	mA
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.4.1c)	4	All		7	pF
Output capacitance 3/	C_{OUT}	V_{CC} = 5.0 V T_A = +25°C, f = 1 MHz (see 4.4.1c)	4	All		8	pF
Functional tests		See 4.4.1d	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input to output propagation delay 5/	t_{PD}		9, 10, 11	01		40	ns
				02		30	
				03		25	
Input register clock to output delay 6/	t_{ICO}		9, 10, 11	01		65	ns
				02		50	
				03		45	
Output data stable time from input clock 6/	t_{IOH}		9, 10, 11	All	5		ns
Input or feedback setup time to input register clock 6/	t_{IS}		9, 10, 11	All	5		ns
Input register hold time from input clock 6/	t_{IH}		9, 10, 11	01	20		ns
				02	15		
				03	13		
Input to input register asynchronous reset delay 6/	t_{IAR}		9, 10, 11	01		65	ns
				02		50	
				03		45	
Input register reset width 3/ 6/	t_{IRW}		9, 10, 11	01	65		ns
				02	50		
				03	45		
Input register reset recovery time 3/ 6/	t_{IRR}		9, 10, 11	01	65		ns
				02	50		
				03	45		
Input to input register asynchronous set delay 6/	t_{IAS}		9, 10, 11	01		65	ns
				02		50	
				03		45	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input register set width 3/ 6/	t_{ISW}		9, 10, 11	01	65		ns
				02	50		
				03	45		
Input register set recovery time 6/	t_{ISR}		9, 10, 11	01	65		ns
				02	50		
				03	45		
Input and output clock width high 3/ 6/ 7/ 8/	t_{WH}		9, 10, 11	01	25		ns
				02	20		
				03	15		
Input and output clock width low 3/ 6/ 7/ 8/	t_{WL}		9, 10, 11	01	25		ns
				02	20		
				03	15		
Maximum frequency with feedback in input registered mode ($1/(t_{ICO} + t_{IS})$) 3/ 9/	f_{MAX1}		9, 10, 11	01	14.2		MHz
				02	18.1		
				03	20.0		
Maximum frequency data path in input registered mode (Lower of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$ or $1/(t_{IS} + t_{IH})$) 3/ 6/	f_{MAX2}		9, 10, 11	01	15.3		MHz
				02	20.0		
				03	22.2		
Output data stable from input clock minus input register input hold time 10/ 11/	t_{IOH}-t_{IH}		9, 10, 11	All	0		ns
Output register clock to output delay 7/	t_{CO}		9, 10, 11	01		40	ns
				02		30	
				03		25	

See footnotes at end of table.

☆ U. S. GOVERNMENT PRINTING OFFICE: 1988—549-904

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output data stable time from output clock 3/ 7/	t_{OH}		9, 10, 11	All	3		ns
Output register input set up time to output clock 7/	t_S		9, 10, 11	01	20		ns
				02,03	15		
Output register input hold time from output clock 7/	t_H		9, 10, 11	01	12		ns
				02,03	10		
Input to output register asynchronous reset delay 7/	t_{OAR}		9, 10, 11	01		40	ns
				02		30	
				03		25	
Output register reset width 3/ 7/	t_{ORW}		9, 10, 11	01	40		ns
				02	30		
				03	25		
Output register reset recovery time 3/ 7/	t_{ORR}		9, 10, 11	01	40		ns
				02	30		
				03	25		
Input to output register asynchronous set delay 7/	t_{OAS}		9, 10, 11	01		40	ns
				02		30	
				03		25	
Output register set width 3/ 7/	t_{OSW}		9, 10, 11	01	40		ns
				02	30		
				03	25		
Output register set recovery time 3/ 7/	t_{OSR}		9, 10, 11	01	40		ns
				02	30		
				03	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 4/ $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Input to output enable delay 12/ 13/	t_{EA}		9, 10, 11	01		40	ns
				02		30	
				03		25	
Input to output disable delay 3/ 12/ 13/	t_{ER}		9, 10, 11	01		40	ns
				02		30	
				03		25	
Pin 14 to output enable delay 12/ 13/	t_{PZX}		9, 10, 11	01		35	ns
				03		25	
				04		20	
Pin 14 to output disable delay 3/ 12/ 13/	t_{PXZ}		9, 10, 11	01		35	ns
				03		25	
				04		20	
Maximum frequency with feedback in output registered mode $(1/(t_{CO} + t_S))$ 3/ 14/ 15/	f_{MAX3}		9, 10, 11	01	16.6		MHz
				02	22.2		
				03	25.0		
Maximum frequency data path in output registered mode (Lowest of $1/t_{CO}$, $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$) 3/ 7/	f_{MAX4}		9, 10, 11	01	20.0		MHz
				02	25.0		
				03	33.3		
Output data stable from output clock minus input register input hold time 3/ 11/ 16/	t_{OH}-t_{IH}		9, 10, 11	All	0		ns
Maximum frequency pipelined mode 3/ 8/ 15/	f_{MAX5}		9, 10, 11	01	18.5		MHz
				02	23.5		
				03	28.0		

See footnotes on next page.

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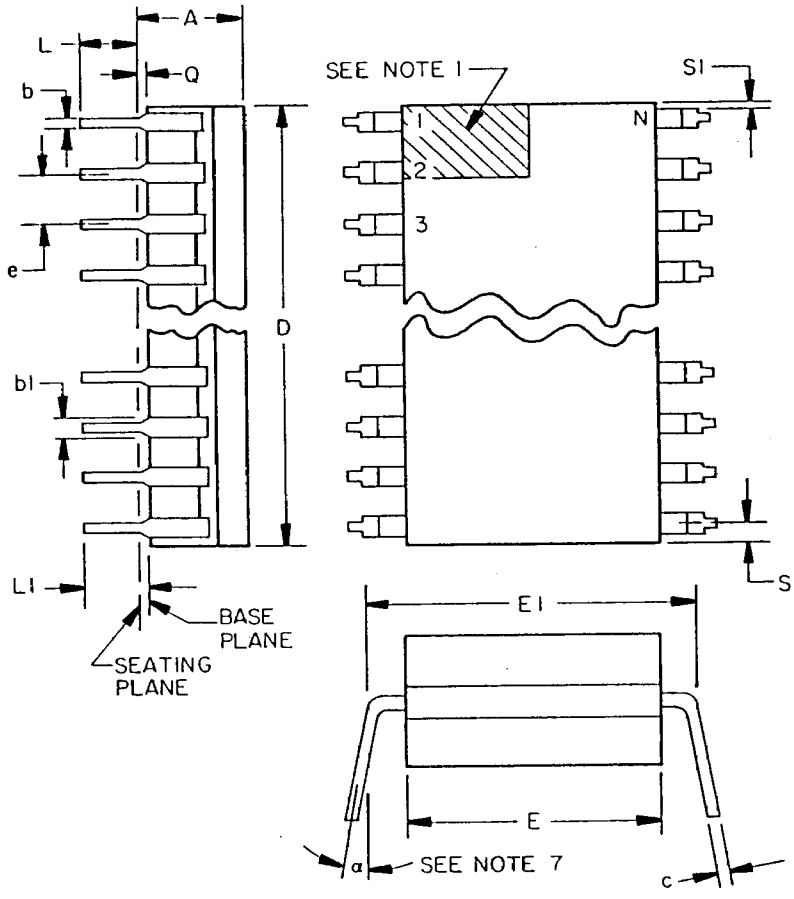
1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load on figure 5, circuit A. See figure 6 for switching waveforms.
5/ Refer to figure 7, configuration 1.
6/ Refer to figure 7, configuration 2.
7/ Refer to figure 7, configuration 3.
8/ Refer to figure 7, configuration 6.
9/ Refer to figure 7, configuration 7.
10/ Refer to figure 7, configuration 9.
11/ This specification is intended to guarantee interface compatibility of the other members of the device family, contact the manufacturer for compatibility information.
12/ Refer to figure 7, configuration 4.
13/ Measured at the point to which a previous high level has fallen to 0.5 V below V_{OH} minimum or a previous low level has risen to 0.5 V above V_{OL} maximum with the load on figure 5, circuit B. See figure 6 for enable and disable test waveforms.
14/ Refer to figure 7, configuration 8.
15/ This specification is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source.
16/ Refer to figure 7, configuration 10.

3.12.3 Verification of erasure or programmed EPLDs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B or S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q or V, sampling and inspection procedures shall be in accordance with MIL-I-38535.



Configuration 1

FIGURE 1. Case X (28-pin, 1.485" x 0.310" x 0.200"), dual-in-line package.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90754
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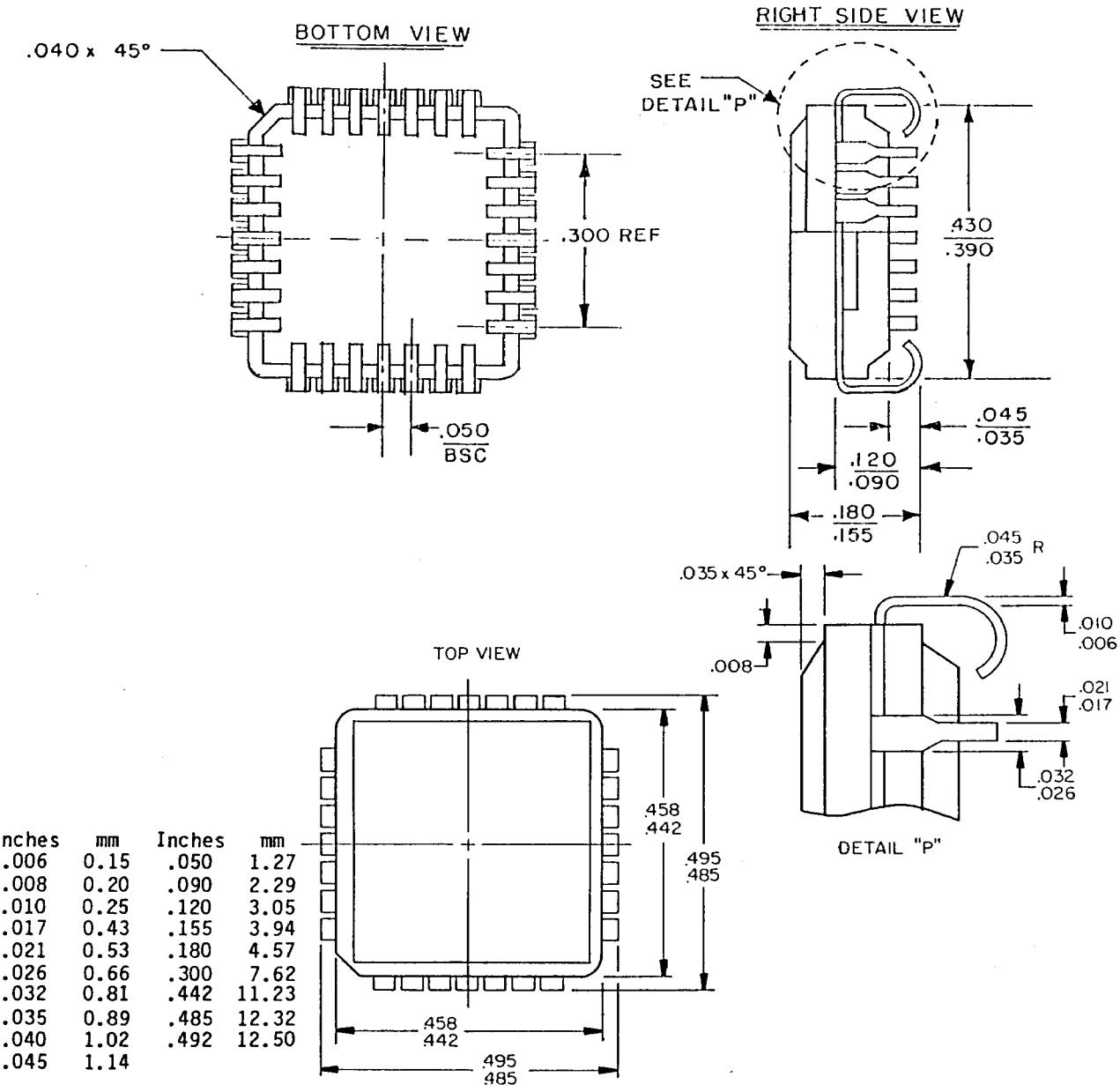
Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	---	.200	---	5.08	
b	.014	.023	0.36	0.58	3
b_1	.038	.065	0.96	1.65	3,4
c	.008	.015	0.20	0.38	3
D	1.430	1.485	36.33	37.72	5
E	.220	.310	5.59	7.87	5
E_1	.300	.320	7.62	8.13	6

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
e	.100 BSC		2.54 BSC		7
L	.125	.200	3.18	5.08	
L_1	.150	---	3.81	---	
Q	.015	.060	0.38	1.52	8
S	---	.100	---	2.54	9
S_1	.005	---	0.13	---	9
α	0°	15°	0°	15°	

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when lead finish A or B is applied.
4. The minimum limit for dimension b_1 may be .023 (0.58 mm) for leads number 1, 14, 15, and 28 only.
5. This dimension allows for off-center lid, meniscus and glass overrun.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 28.
8. Dimension Q shall be measured from the seating plane to the base plane.
9. Applies to all four corners (leads number 1, 14, 15, and 28) shall apply.

FIGURE 1. Case X (28-pin, 1.485" x 0.310" x 0.200"), dual-in-line package - Continued.



Inches	mm	Inches	mm
.006	0.15	.050	1.27
.008	0.20	.090	2.29
.010	0.25	.120	3.05
.017	0.43	.155	3.94
.021	0.53	.180	4.57
.026	0.66	.300	7.62
.032	0.81	.442	11.23
.035	0.89	.485	12.32
.040	1.02	.492	12.50
.045	1.14		

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 2. Case Z (28-lead, .458" x .458" x .180"), J-leaded chip carrier package.

Device types	All
Case outlines	X, Y, Z, and 3
Terminal number	Terminal symbol
1	I_0
2	I_1
3	I_2
4	I_3
5	I_4
6	I_5
7	I_6
8	GND
9	I_7
10	I_8
11	I_9
12	I_{10}
13	$\overline{I_{11}}$
14	$\overline{OE}/I_{12}$
15	I/O_{11}
16	I/O_{10}
17	I/O_9
18	I/O_8
19	I/O_7
20	I/O_6
21	GND
22	V_{CC}
23	I/O_5
24	I/O_4
25	I/O_3
26	I/O_2
27	I/O_1
28	I/O_0

FIGURE 3. Terminal connections.

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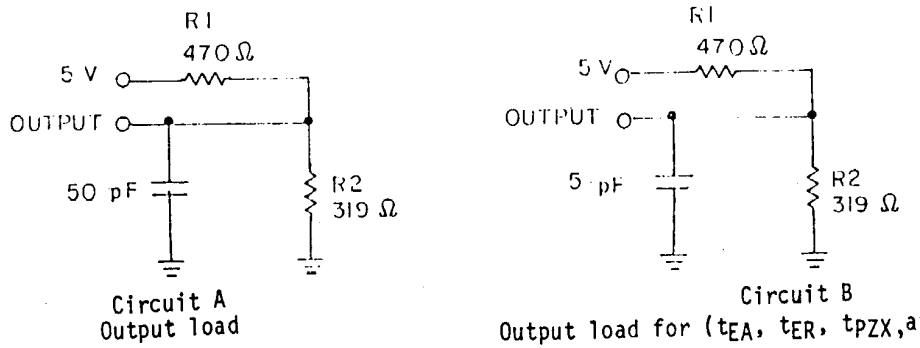
Truth table																							
Input pins													Output pins										
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	$\overline{OE}/I$	I/O_{11}	I/O_{10}	I/O_9	I/O_8	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
X	X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = High impedance.
2. X = Don't care.

FIGURE 4. Truth table (unprogrammed).



*Including scope and jig (minimum values).

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	≤ 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

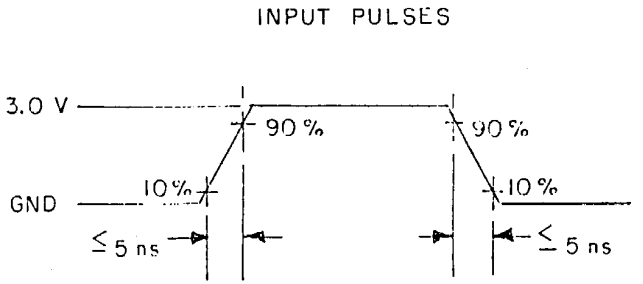
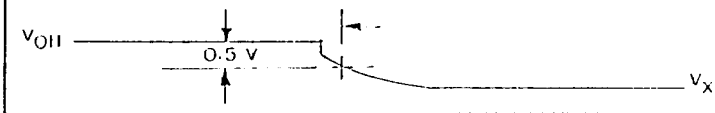
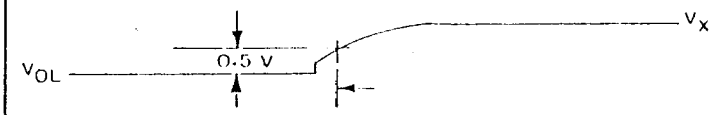
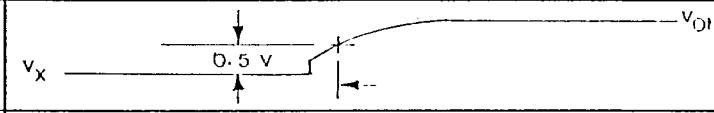
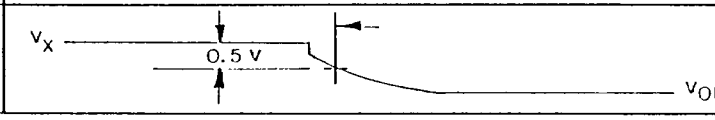


FIGURE 5. Output load circuit and test conditions.

Output control switching waveform

PARAMETER	V_X	OUTPUT WAVEFORM - MEASUREMENT LEVEL
$t_{PXZ(-)}$ $t_{ER(-)}$	1.5 V	
$t_{PXZ(+)}$ $t_{ER(+)}$	2.6 V	
$t_{PZX(+)}$ $t_{EA(+)}$	2.02 V	
$t_{PZX(-)}$ $t_{EA(-)}$	2.02 V	

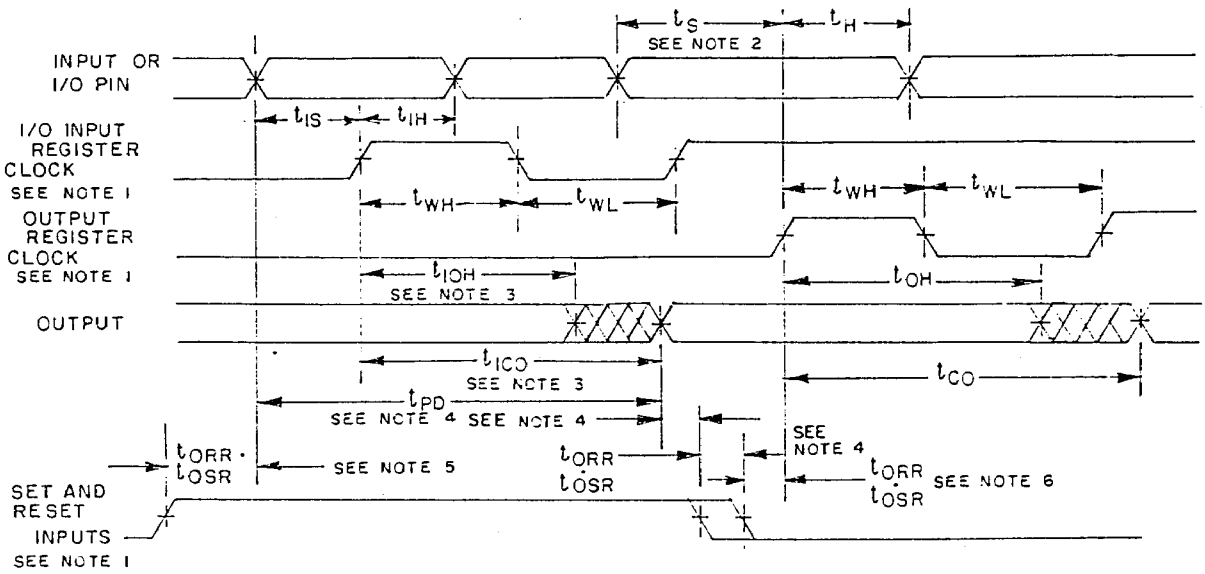
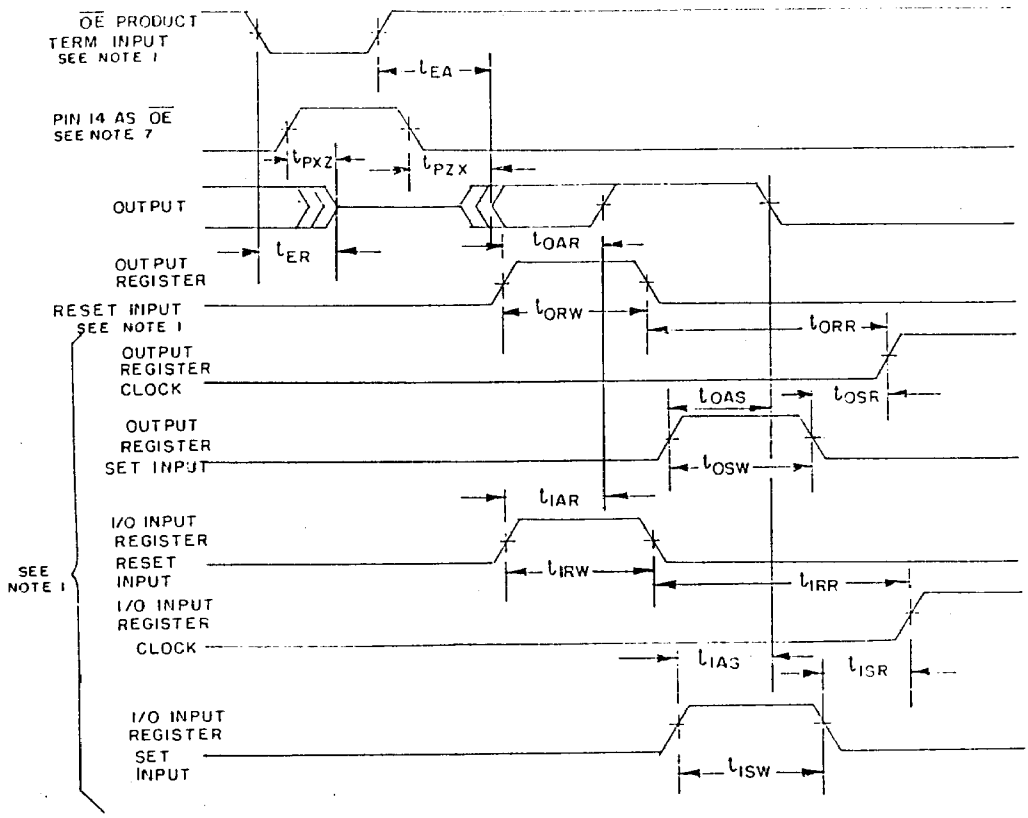


FIGURE 6. Switching waveforms.



NOTES:

1. As these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.
2. Dedicated input or input register set in transparent mode. Input register set and reset inputs are in a high state.
3. Output register is set in transparent mode. Output register set and reset inputs are in a high state.
4. Combinatorial mode. Reset and set inputs of the input and output registers should remain in a high state at least until the output responds at t_{PD}. When returning set and reset inputs to a low state, one of these signals should go low a minimum of t_{OSR} (set input) or t_{ORR} (reset input) prior to the other. This guarantees predictable register states upon exit from combinatorial mode.
5. When entering the combinatorial mode, input and output register set and reset inputs must be stable in a high state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to application of logic input signals.
6. When returning to the input and/or output registered mode, register set and reset inputs must be stable in a low state a minimum of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to the application of the register clock input.
7. Refer to figure 7, configuration 5.

FIGURE 6. Switching waveforms - Continued.

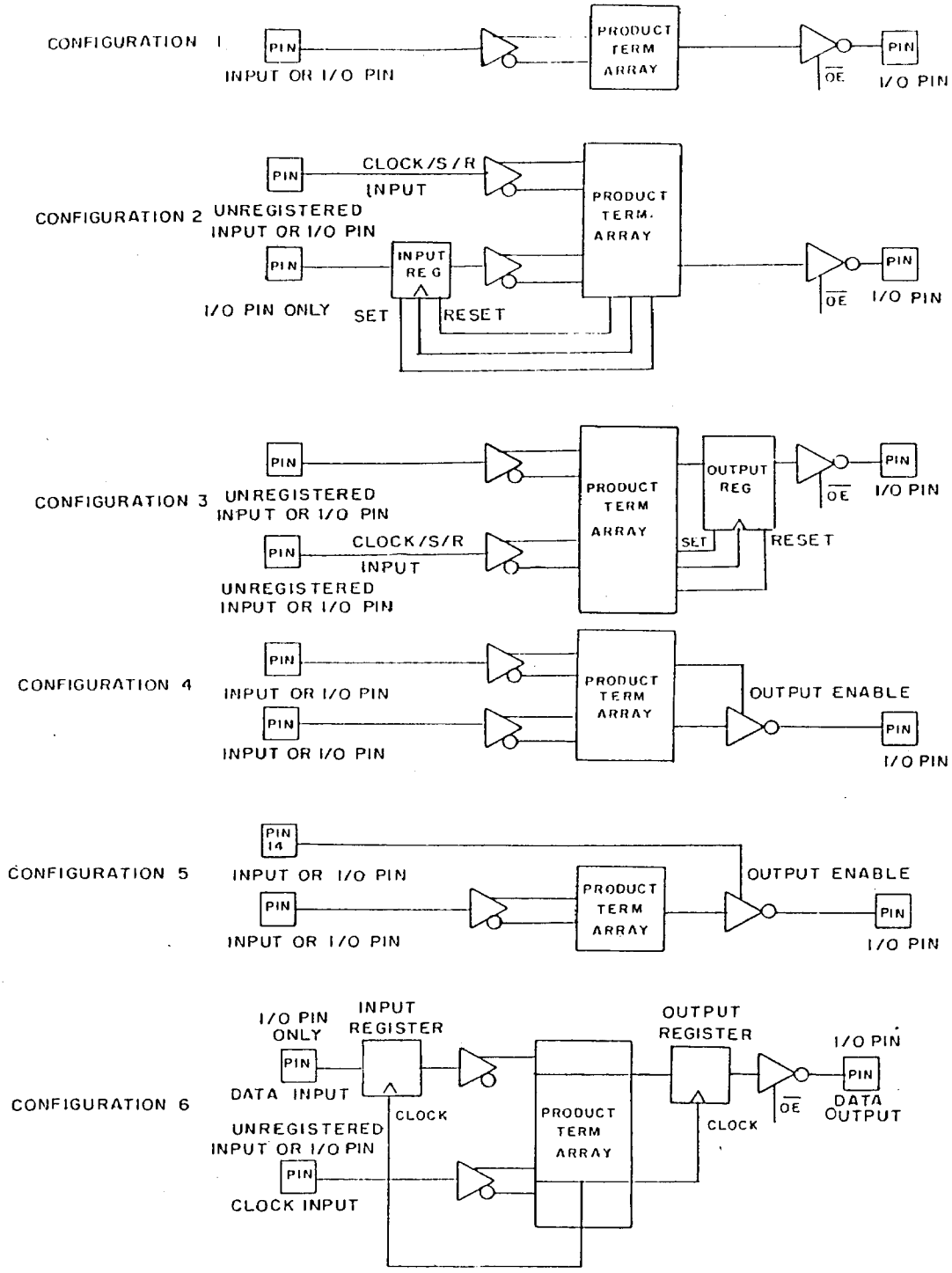


FIGURE 7. Timing configurations.

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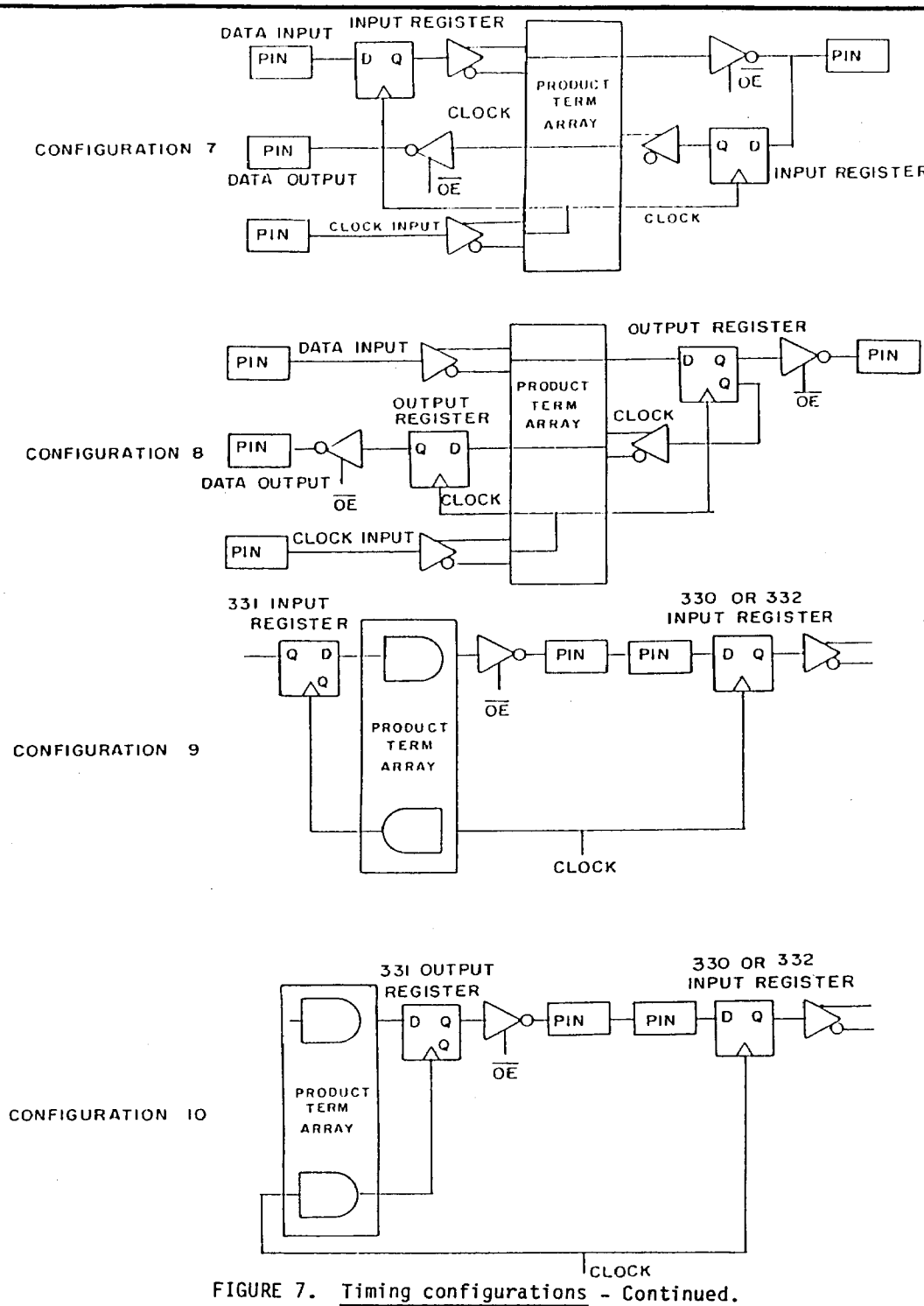

FIGURE 7. Timing configurations - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B or S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q or V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. The following additional criteria shall apply.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Dynamic burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B or S, the test circuit shall be submitted to the qualifying activity. For device classes Q or V, the test circuit shall be submitted to DESC-ECS with the certificate of compliance and under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

(2) T_A = +125°C, minimum.

c. Static burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A.

(2) T_A = +125°C minimum, test duration for the static test shall be 48 hours minimum for class S. The 48-hour burn-in shall be broken into two sequences of 24 hours each (static I and static II) followed by interim electrical measurements.

(3) All inputs and common inputs/outputs shall be connected through R_1 to V_{CC}, separate outputs may be open or connected to $V_{CC}/2$ ±0.5 V. Resistor R_1 is optional on both inputs and open outputs when V_{CC} is not applied, and required on outputs connected to $V_{CC}/2$. R_1 = 2 kΩ ±5 percent, V_{CC} = 5.75 V ±0.25 V.

(4) For static II burn-in, change input connections to V_{SS}.

d. Interim and final electrical test parameters shall be as specified in table IIA herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

e. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.)

Margin test method.

(1) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.12.2).

(2) Bake, unbiased, for 72 hours at +140°C or for 48 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.

(3) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(4) Erase (see 3.12.1).

(5) Program a minimum of 50 percent of the total number of cells, including the slowest programming cell (see 3.12.2).

(6) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(7) Perform dynamic burn-in (see 4.2a).

(8) Perform margin test using V_m = +5.7 V at +25°C using loose timing (i.e., t_{ACC} = 1 µs).

(9) Perform electrical tests (see 4.2b).

(10) Erase (see 3.12.1). Devices may be submitted for groups A, B, C, and D testing.

(11) Verify erasure (see 3.12.3).

4.2.1 Additional screening for device class V. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein. These additional screens may be used to satisfy space system requirements and shall be reflected in the complete part number (see 6.7).

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B or S. Qualification inspection for device classes B or S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q or V. Qualification inspection for device classes Q or V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B or S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, or S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q or V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial characterization and after any process or design changes which may affect input or output capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B or S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q or V, subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. Steady-state life test conditions; method 1005 of MIL-STD-883:

(1) Test condition D. For device class M, the test circuit shall be submitted to DESC-ECS for review with the certificate of compliance. For device classes B or S, the test circuit shall be submitted to the qualifying activity. For device classes Q or V, the test circuit shall be submitted to DESC-ECS with the certificate of compliance and under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.4 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B or S shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the level specified in the purchase order. RHA tests for device classes Q or V shall be performed in accordance with MIL-I-38535 and 1.2.1 herein.

a. RHA tests for device classes B or S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, or S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the post irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5%, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

(1) Inputs tested high, V_{CC} = 6/ volts dc, R_{CC} = 6/ Ω +5%, V_{IN} = 6/ volts dc, R_{IN} = 6/ Ω +20%, and all outputs are open.

(2) Inputs tested low V_{CC} = 6/ volts dc, R_{CC} = 6/ Ω +5%, V_{IN} = 0.0 V dc, and all outputs are open.

f. For device classes M, B, or S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

6/ When a QPL or QML source exists, values will be inserted as applicable.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (per method 5005 table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9 or 2,8A,10		
2	Static burn-in method 1015	Not required	Not required	Required	Not required	Not required
3	Same as line 1			1 Δ 7/		
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1 Δ 7/		
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9	1*,2,3,7*, 8A,8B,9	1*,2,3,7*, 8A,8B,9	1*,2,3,7*, 8A,8B,9	1*,2,3,7*, 8A,8B,9
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 Δ		1,2,3,7, 8A,8B,9, 10,11
9	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B Δ		2,3,7, 8A,8B	
10	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7, 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

See footnotes on next page.

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table IIA).
4/ * Indicates PDA applies to subgroups 1 and 7.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (line 1).
7/ The device manufacturer may at his option, either complete subgroup 1 electrical parameter measurements, including delta measurements, within 96 hours after burn-in completion (removal of bias); or may complete subgroup 1 electrical measurements without delta measurements within 24 hours after burn-in completion (removal of bias).

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100 percent
Internal visual	2010, condition A or approved alternate	100 percent
Nondestructive bond pull	2023	100 percent
Reverse bias burn-in	1015	100 percent
Burn-in parameters	1015, total of 240 hours at +125°C	100 percent
Radiographic	2012	100 percent

TABLE IIC. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IX} standby	±10 μA
I_{OZ} standby	±10 μA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta (Δ).

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4.5 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (A). The intergrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12000 $\mu W/cm^2$ power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12000 $\mu W/cm^2$). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, or S and MIL-I-38535 for device classes Q or V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B or Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1695, Engineering Change Proposal (Short Form).

6.3 Approved sources of supply. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.5 Symbols, definitions and functional descriptions.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique part numbers. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique part number. By establishing a one part number system covering all four documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B or S. Sources of supply for device classes B or S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q or V. Sources of supply for device classes Q or V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 24 MAY 1990

Approved sources of supply for SMD 5962-90754 are listed below for immediate procurement only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-9075401MXX	65786	CY7C331-40WMB
5962-9075401MYX	65786	CY7C331-40TMB
5962-9075401MZX	65786	CY7C331-40HMB
5962-9075401M3X	65786	CY7C331-40QMB
5962-9075402MXX	65786	CY7C331-30WMB
5962-9075402MYX	65786	CY7C331-30TMB
5962-9075402MZX	65786	CY7C331-30HMB
5962-9075402M3X	65786	CY7C331-30QMB
5962-9075403MXX	65786	CY7C331-25WMB
5962-9075403MYX	65786	CY7C331-25TMB
5962-9075403MZX	65786	CY7C331-25HMB
5962-9075403M3X	65786	CY7C331-25QMB

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.