March 2001

8 - Bit Micro-controller

64KB ISP flash & 1KB RAM embedded

Product List

SM2965C40, 40 MHz 64KB internal flash MCU

Description

The SM2965 series product is an 8 - bit single chip microcontroller with 64KB flash & 1K byte RAM embedded. It has In-System Programming (ISP) function and is a derivative of the 80C52 microcontroller family. With its hardware features and powerful instruction set, it's straight forward to make it a versatile and cost effective controller for those applications which demand up to 32 I/O pins for PDIP package or up to 36 I/O pins for PLCC/QFP package, or applications which need up to 64K byte flash memory either for program or for
data or mixed.
To program the on-chip flash memory, a commercial writer is available to do it in parallel programming method. The on-chip flash memory can be programmed in either serial or parallel interface with its ISP feature.

Ordering Information

SM2965ihhk (blank chip)
SM2965ihh - yyyk

i: process identifier {C}.
hh: working clock in MHz {40}.
yyy: production code {001,...,999}
k: package type postfix {as below table}

Postfix	Package	Pin/Pad Configuration	Dimension
P	40L PDIP	page 2	page 19
J	44L PLCC	page 2	page 20
Q	44L QFP	page 2	page 21

Features

- Working voltage:4.5V through 5.5V
- program voltage:5V
- General 80C52 family compatible
- 12 clocks per machine cycle
- 64K byte on chip flash memory with In-System Programming (ISP) capability
- 1024 byte on chip data RAM
- Three 16 bit Timers/Counters
- One Watch Dog Timer
- Four 8-bit I/O ports for PDIP package
- Four 8-bit I/O ports + one 4-bit I/O ports for PLCC or QFP package
- Full duplex serial channel
- Bit operation instruction
- Page free jumps
- 8-bit Unsigned Division
- 8-bit Unsigned Multiply
- BCD arithmetic
- Direct Addressing
- Indirect Addressing
- Nested Interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:
  Idle mode and Power down mode
- Code protection function
- Low EMI (inhibit ALE)
- Reset with address $00 blank initiate ISP service program
- ISP service program space configurable in N*512byte (N=0 to 8) size

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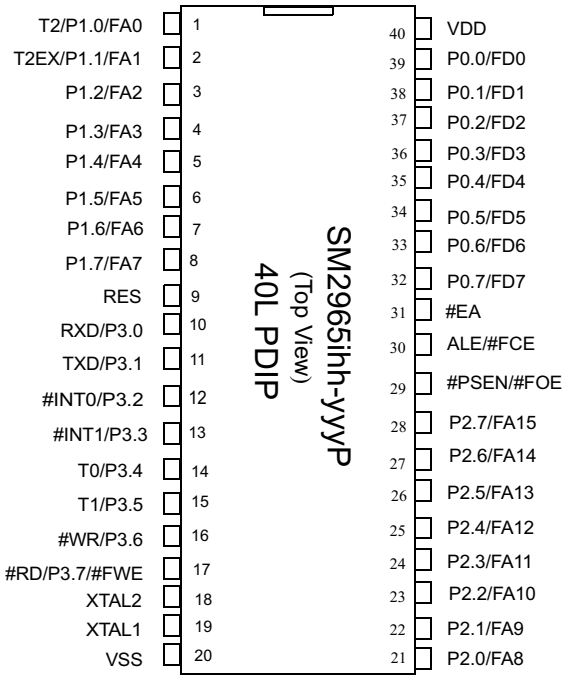
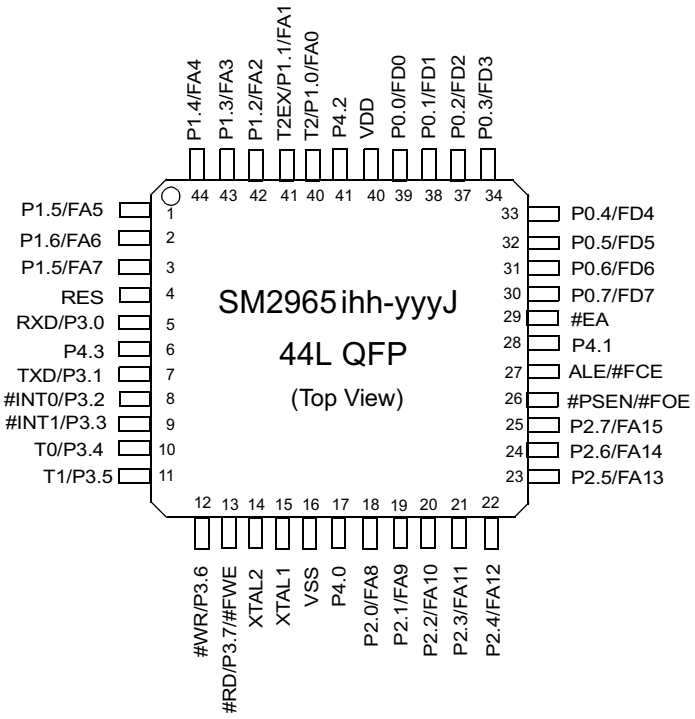
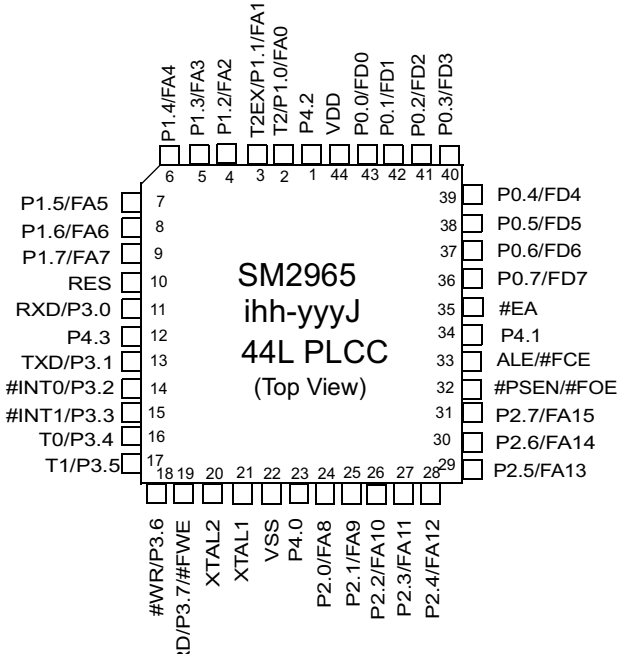
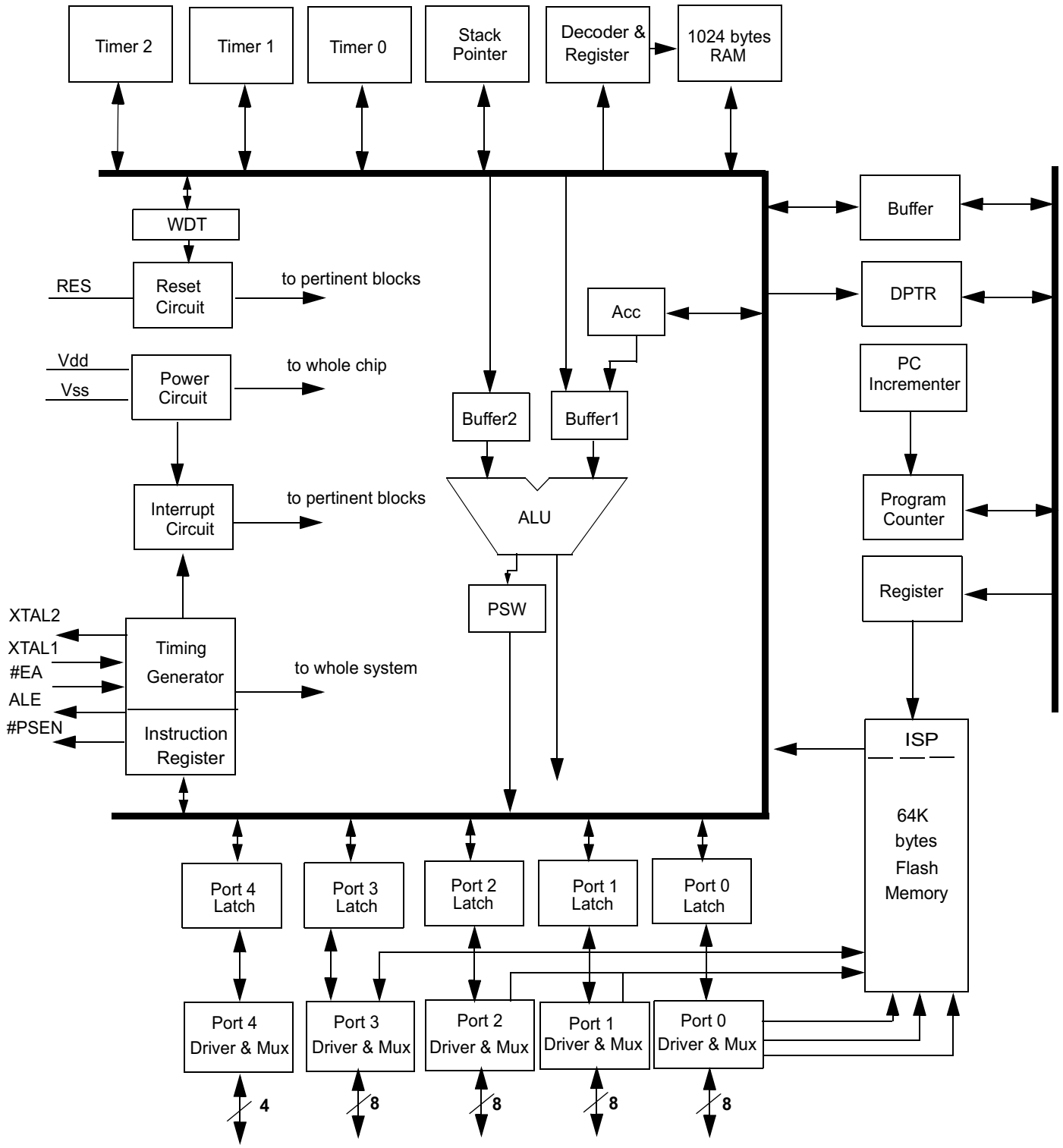
Pin Configurations







Block Diagram



Pin Descriptions

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	T2/P1.0/FA0		i/o	bit 0 of port 1 & timer 2 & bit 0 of flash block address
2	41	3	T2EX/P1.1/FA1		i/o	bit 1 of port 1 & timer control, bit 1 of flash/ext. mem.address
3	42	4	P1.2/FA2		i/o	bit 2 of port 1 & bit 2 of flash/ext. memory address
4	43	5	P1.3/FA3		i/o	bit 3 of port 1 & bit 3 of flash/ext. memory address
5	44	6	P1.4/FA4		i/o	bit 4 of port 1 & bit 4 of flash/ext. memory address
6	1	7	P1.5/FA5		i/o	bit 5 of port 1 & bit 5 of flash/ext. memory address
7	2	8	P1.6/FA6		i/o	bit 6 of port 1 & bit 6 of flash/ext. memory address
8	3	9	P1.7/FA7		i/o	bit 7 of port 1 & bit 7 of flash/ext. memory address
9	4	10	RES	H	i	Reset
10	5	11	RXD/P3.0	- / - /L	i/o	bit 0 of port 3 & Receive data & flash block enable
11	7	13	TXD/P3.1		i/o	bit 1 of port 3 & Transmit data
12	8	14	#INT0/P3.2	L/ -	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	#INT1/P3.3	L/ - /L	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	T0/P3.4	- / - /L	i/o	bit 4 of port 3 & Timer 0
15	11	17	T1/P3.5	- / - /L	i/o	bit 5 of port 3 & Timer 1
16	12	18	#WR/P3.6	L/ -	i/o	bit 6 of port 3 & ext. memory write
17	13	19	#RD/P3.7/#FWE	L/ -	i/o	bit 7 of port 3 & ext. mem. read & write enable to flash block
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/FA8		i/o	bit 0 of port 2 & bit 8 of flash/ext. memory address
22	19	25	P2.1/FA9		i/o	bit 1 of port 2 & bit 9 of flash/ext. memory address
23	20	26	P2.2/FA10		i/o	bit 2 of port 2 & bit 10 of flash/ext. memory address
24	21	27	P2.3/FA11		i/o	bit 3 of port 2 & bit 11 of flash/ext. memory address
25	22	28	P2.4/FA12		i/o	bit 4 of port 2 & bit 12 of flash/ext. memory address
26	23	29	P2.5/FA13		i/o	bit 5 of port 2 & bit 13 of flash/ext. memory address
27	24	30	P2.6/FA14		i/o	bit 6 of port 2 & bit 14 of flash/ext. memory address
28	25	31	P2.7/FA15	L/L	i/o	bit 7 of port 2 & bit 15 of flash/ext. memory address
29	26	32	#PSEN/#FOE	- /L	o/i	program storage enable & o/p enable to flash block
30	27	33	ALE/#FCE	L	o/i	address latch enable & chip enable to flash block
31	29	35	#EA		i	external access
32	30	36	P0.7/FD7		i/o	bit 7 of port 0 & data bit 7 of flash/ext. memory
33	31	37	P0.6/FD6		i/o	bit 6 of port 0 & data bit 6 of flash/ext. memory
34	32	38	P0.5/FD5		i/o	bit 5 of port 0 & data bit 5 of flash/ext. memory
35	33	39	P0.4/FD4		i/o	bit 4 of port 0 & data bit 4 of flash/ext. memory
36	34	40	P0.3/FD3		i/o	bit 3 of port 0 & data bit 3 of flash/ext. memory
37	35	41	P0.2/FD2		i/o	bit 2 of port 0 & data bit 2 of flash/ext. memory
38	36	42	P0.1/FD1		i/o	bit 1 of port 0 & data bit 1 of flash/ext. memory
39	37	43	P0.0/FD0		i/o	bit 0 of port 0 & data bit 0 of flash/ext. memory
40	38	44	VDD			Drive Voltage, +5 Vcc
	17	23	P4.0		i/o	bit 0 of Port 4
	28	34	P4.1		i/o	bit 1 of Port 4
	39	1	P4.2		i/o	bit 2 of Port 4
	6	12	P4.3		i/o	bit 3 of Port 4

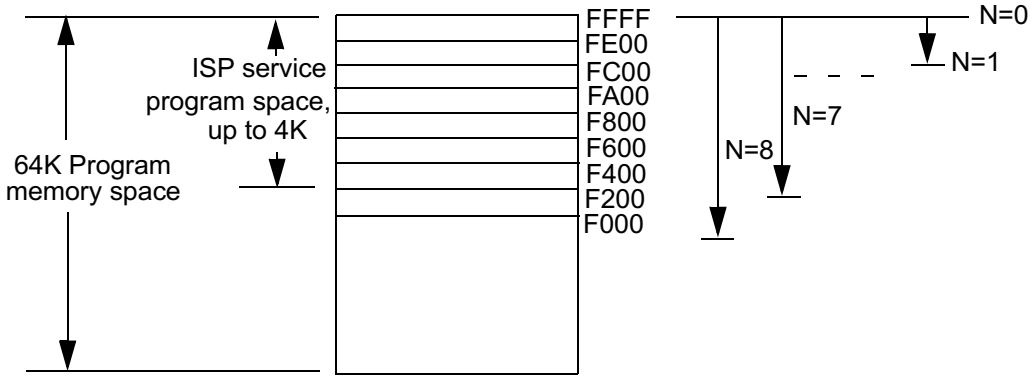
Extension Function Description

Memory Structure

The SM2965 is the general 80C52 hardware core to integrate the ISP function module as a single chip microcontroller. Its memory structure follows general 80C52 structure.

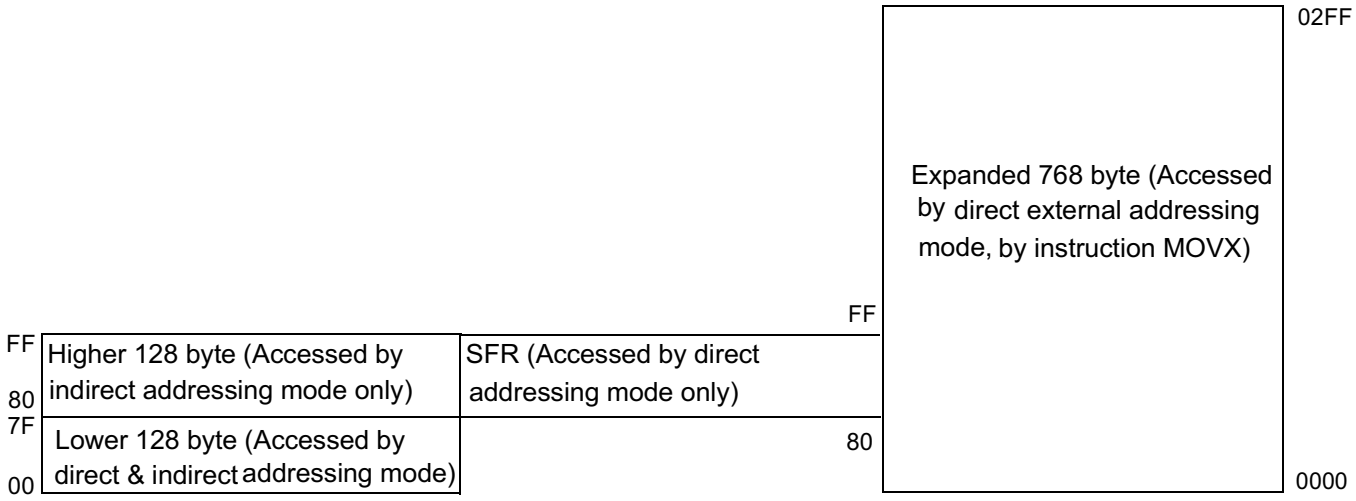
Program Memory

The SM2965 has 64K byte on-chip flash memory which used as general program memory, on which include up to 4K byte specific ISP service program memory space. The address range for the 64K byte is $0000 to $FFFF. The address range for the ISP service program is $F000 to $FFFF. The ISP service program size can be partitioned as N blocks of 512 byte (N=0 to 8). When N=0 means no ISP service program space available, total 64K byte memory used as program memory. When N=1 means memory address $FE00 to $FFFF reserved for ISP service program. When N=2 means memory address $FC00 to FFFF reserved for ISP service program,...etc. Value N can be set and programmed into SM2965 by writer.



Data Memory

The SM2965 has 1K byte on-chip RAM, 256 byte of it are the same as general 80C52 internal memory structure while the expanded 768 byte on-chip RAM can be accessed by external memory addressing method. (by instruction MOVX)



Data Memory - Lower 128 byte

Data memory $00 to $FF is the same as 80C52
The address $00 to $7F can be accessed by direct and indirect addressing mode.
Address $00 to $1F is register area.
Address $20 to $2F is memory bit area.
Address $30 to 7F is for general memory area.

Data memory - Higher 128 byte

The address $80 to $FF can be accessed by indirect addressing mode only.
Addressing $80 to $FF is data area.

Data Memory - Expanded 768 byte

From external address $0000 to $02FF is the on-chip expanded RAM area, total 768 byte. This area can be accessed by external direct addressing mode only (by instruction MOVX).

If the address of instruction MOVX @DPTR is larger than $02FF then SM2965 will generate the external memory control signal automatically.The bit 1 (OME) of special function register $BF (SCONF) can enable or disable this expanded 768 byte RAM. The defaut setting of OME bit is 1 (enable).

The address space of instruction MOVX @Rn is determined by bit 1 & bit 0 (PS1, PS0) of special function register $85 (IMPSR). The default setting of PS1, PS0 bits is 00 (page 0).

One page of data RAM is 256 byte.

PS1, PS0=00, Rn of instruction MOVX @Rn mapping to expanded RAM address $0000 to $ 00FF (page 0)
PS1, PS0=01, Rn of instruction MOVX @Rn mapping to expanded RAM address $0100 to $ 01FF (page 1)
PS1, PS0=10, Rn of instruction MOVX @Rn mapping to expanded RAM address $0200 to $ 02FF (page 2)
PS1, PS0=11, Rn of instruction MOVX @Rn mapping to expanded RAM address $XY00 to $ XYFF which high byte address specified by port 2. (SM2965 will generate the external memory control signal automatically).

Special Function Register (SFR)

The address $80 to $FF can be accessed by direct addressing mode only.
Address $80 to $FF is SFR area.
The next table lists the SFRs which is identical to general 80C52 as well as SM2965 Extension SFRs.

$F8									$FF
$F0	B				**FAH**	**FAL**	**FDAT**	**FCR**	$F7
$E8									$EF
$E0	ACC								$E7
$D8	**P4**								$DF
$D0	PSW								$D7
$C8	T2CON		RC2H	RC2L	TL2	TH2			$CF
$C0									$C7
$B8	IP							**SCONF**	$BF
$B0	P3								$B7
$A8	IE								$AF
$A0	P2								$A7
$98	SCON	SBUF						**WDTC**	$9F
$90	P1								$97
$88	TCON	TMOD	TL0	TL1	TH0	TH1			$8F
$80	P0	SP	DPL	DPH	(Reserved)	**IMPSR**		PCON	$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for SM2965

Description of SM2965 Extension SFRs

Port4 (P4, $D8)

	0	0	0	0	P4.3	P4.2	P4.1	P4.0
Reset value	0	0	0	0	1	1	1	1
	MSB							LSB

The bit 3, bit 2, bit 1, bit 0 output the setting to pin P4.3, P4.2, P4.1, P4.0 respectively.

Internal Memory Page Select Register (IMPSR, $85)

	R	R	R	R	R	R	PS1	PS0
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

Note: "R" means reserved

SM2965 has 768 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX)
The address space of instruction MOVX @Rn is determined by bit 1 & bit 0 (PS1, PS0) of IMPSR. The default setting of PS1, PS0 bits is 00 (page 0).

System Control Register (SCONF,&BF)

	WDR	R	R	R	R	ISPE	OME	ALE1
Reset value	0	0	0	0	0	0	1	0
	MSB							LSB

WDR : Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1
ISPE : ISP function enable bit
OME : 768 byte on-chip RAM enable bit
ALE1 : ALE output inhibit bit, to reduce EMI

Watch Dog Timer Register (WDTC, $9F)

	WDTE	0	CLEAR	0	0	PS2	PS1	PS0
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS2 ~ PS0 : clock source divider selection bit

Flash Control Register (FCR, $F7)

	START	R	R	R	R	R	F1	F2
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

START : ISP function start bit
F1 ~F0 : ISP function select bit

Flash Address-High Register (FAH, $F4)

	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

FA15 ~FA8: flash address-high for ISP function

Flash Address-Low Register (FAL, $F5)

	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

FA7 ~ FA0: flash address-low for ISP function

Flash Data Register (FDAT, $F6)

	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset value	0	0	0	0	0	0	0	0
	MSB							LSB

FD7 ~FD0: flash data for ISP function

In-System Programming (ISP) Function

The SM2965 can generate flash control signal by internal hardware circuit. User utilize flash control register, flash address register and flash data register to perform the ISP function without removing the SM2965 from the system.

The SM2965 provided internal flash control signal which can do flash progam.chip erase/page erase/protect functions. User need to design and use any kind of interface which SM2965 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

ISP Service Program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM2965 for the ISP purpose.

The ISP service program were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM2965 and host device which output data to the SM2965. For example, if user utilize UART interface to receive/transmit data between SM2965 and host device, the ISP service program should include baut rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under SM2965 active or idle mode. It can not be initiated under power down mode.

Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range $F000 to $FFFF. It can be divided as blocks of N*512 byte. (N=0 to 8). When N=0 means no ISP function, all of 64K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 512 byte while the rest of 63.5K byte flash memory can be used as program memory. The maximum ISP service program allowed is 4K byte when N=8. Under such configuration, the usable program memory space is 60K byte.

After N determined, SM2965 will reserve the ISP service program space downward from the top of the program address $FFFF. The start address of the ISP service program located at $Fx00 while is x is an even number, depending on the lock bit N. Please see page 5 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not been protected, the content of ISP service program still can be read. If the flash been protected, the overall content of flash program memory space including ISP service program space can not be read.

Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user need to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when SM2965 was in system.

Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are two ways to do so:
(1) Blank reset. Hardware reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program.
(2) Execute jump instruction can load the start address of the ISP service program to PC.

User can initiate general 80C52 INT function to initiate the ISP service program. After ISP service program executed, user need to reset the SM2965, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

ISP Registers-Flash Address-High Register (FAH,$F4) and Flash Address-Low Register (FAL,$F5)

The FAH & FAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by FAH & FAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

ISP Registers - Flash Data Register (FDAT,&F6)

The FDAT provide the 8-bit data for ISP function.

ISP Registers - Flash Control Register (FCR,& $F7)

START	R	R	R	R	R	F1	F0

START: ISP function start bit
1: start ISP function which indicated by bit 1, bit 0 (F1, F0)
0: no operation

After START bit set to 1 then the SM2965 hardware circuit will latch address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. User does not need to check START bit status by software method.

F1 ~ F0: ISP function select bit

F [1:0]	ISP function
00	Byte program
01	Chip protect
10	Page erase
11	Chip erase

One page of flash memory is 512 byte.

To perform byte program/page erase ISP function, user need to specify flash address at first. When performing page erase function, SM2965 will erase entire page which flash address indicated by FAH & FAL registers located within the page.
e.g. flash address: $XYMN
page erase function will erase from $XY00 to $X(Y+1)FF (Y:even number), or
page erase function will erase from $X(Y-1) 00 to $XYFF (Y:odd number)

To perform the chip erase ISP function, SM2965 will erase all the flash program memory except the ISP service program space, also, SM2965 will un-protect the flash memory automatically. To perform chip protect ISP function, the SM2965 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV $BF,#04H      ; enable SM2965 ISP function
MOV $F4,#10H      ; set flash address-high, 10H
MOV $F5,#05H      ; set flash address-low, 05H
MOV $F6,#22H      ; set flash data to be programmed, data = 22H
MOV $F7,#80H      ; start to program #22H to the flash address $1005H
                  ; after byte program finished, START bit of FCR will be reset to 0 automatically
                  ; program counter then point to the next instruction
```

ISP Register - System Control Register (SCONF,$BF)

WDR	R	R	R	R	ISPE	OME	ALE1

The bit 2 (ISP) of SCONF is ISP enable bit. User can enable overall SM2965 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0.

The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally.

Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate a reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0,Timer1 and Timer2 of general 80C52. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The SM2965 WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) of Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDT. After WDTE set to 1, The 16-bit counter starts to count with the selected time base source clock which set by PS2 ~ PS0. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when SM2965 been reset, either hardware rest or WDT reset.

To reset the WDT is done by setting 1 to the bit 5 (CLEAR) of WDT. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

Watch Dog Timer Registers -WDT Control Register (WDTC,$9F)

WDTE	0	CLEAR	0	0	PS2	PS1	PS0

WDTE : Watch Dog Timer enable bit
CLEAR : Watch Dog Timer reset bit
PS2 ~ PS0 : clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

Watch Dog Timer Register - System Control Register (SCONF,$BF)

WDR	R	R	R	R	R	OME	ALEI

The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever unpredicted reset happened.

Reduce EMI Function

The SM2965 allows user to reduce the EMI emission by setting 1 to the bit 0 (ALEI) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.

Operating Conditions

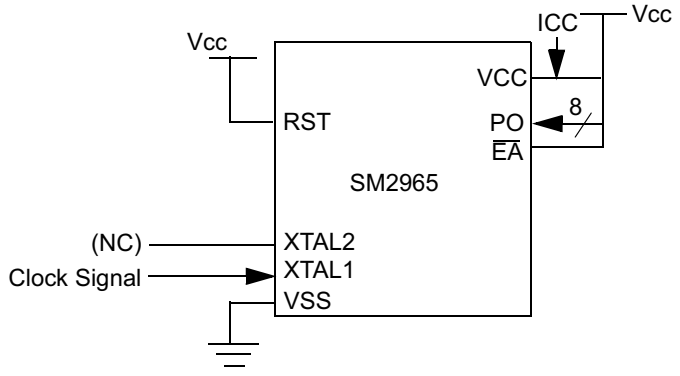
Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Ambient temperature under bias	0	25	70	degree C	
VCC5	Supply voltage	4.5	5.0	5.5	V	SM2965C
Fosc 16	Oscillator Frequency	3.0	16	16	MHz	SM2965C16
Fosc 25		16	25	25	MHz	SM2965C25
Fosc 40		25	40	40	MHz	SM2965C40

DC Characteristics

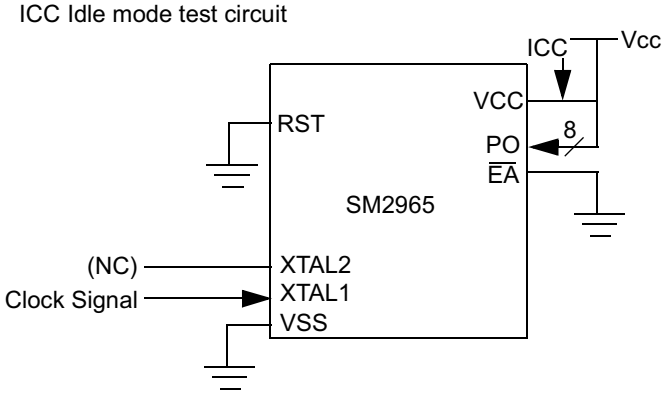
(16/25/40 MHZ, typical operating conditions, valid for SM89516 series)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,4,#EA	-0.5	0.8	V	Vcc=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	"
VIH1	Input High Voltage	port 0,1,2,3,4,#EA	2.0	Vcc+0.5	V	"
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	"
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=3.2mA
VOL2	Output Low Voltage	port 1,2,3,4		0.45	V	IOL=1.6mA
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		± 10	uA	0.45V<Vin<Vcc
R RES	Reset Pulldown Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25°C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 40MHz
				15	mA	Active mode, 25MHz
				10	mA	Active mode, 16MHz
				10	mA	Idle mode, 40MHz
				7.5	mA	Idle mode, 25MHz
				6	mA	Idle mode, 16MHz
				150	uA	Power down mode

ICC Active mode test circuit



ICC Idle mode test circuit

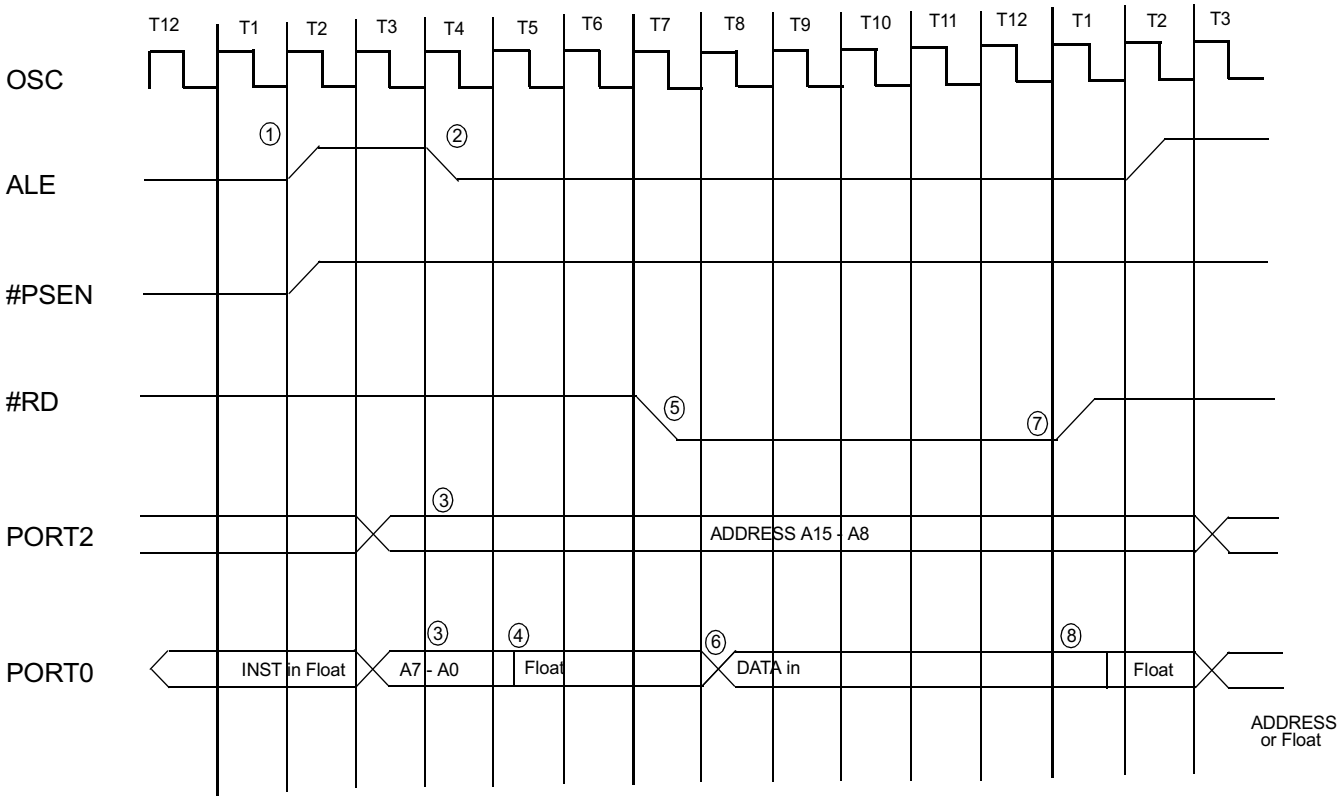


AC Characteristics

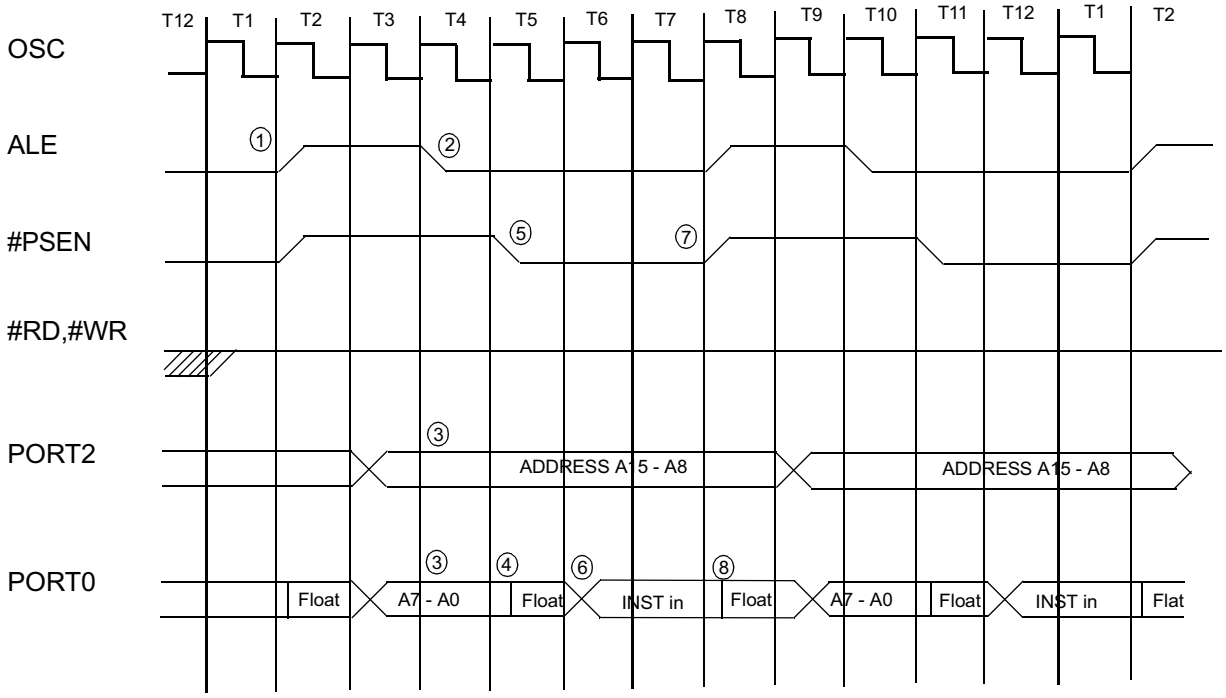
(16/25/40 MHZ, operating conditions; CL for Port 0, ALE and PSEN Outputs=150uF; CL for all Other Output=80pF)

Symbol	Parameter	Valid Cycle	f osc 16			Variable f osc			Unit	Remarks
			Min.	Typ.	Max	Min.	Typ.	Max		
T LHLL	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T AVLL	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T LLAX	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T LLIV	ALE low to Valid Instruction In	RD			240			4xT - 10	nS	
T LLPL	ALE low to #PSEN low	RD	53			T - 10			nS	
T PLPH	#PSEN pulse width	RD	173			3xT - 15			nS	
T PLIV	#PSEN low to Valid Instruction In	RD			177			3xT - 10	nS	
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS	
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS	
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS	
T PLAZ	#PSEN low to Address Float	RD			10			10	nS	
T RLRH	#RD pulse width	RD	365			6xT - 10			nS	
T WLWH	#WR pulse width	WRT	365			6xT - 10			nS	
T RLDV	#RD low to Valid Data In	RD			302			5xT - 10	nS	
T RHDX	Data Hold after #RD	RD	0			0			nS	
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS	
T LLDV	ALE low to Valid Data In	RD			590			8xT - 10	nS	
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS	
T LLYL	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT + 10	nS	
T AVYL	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T QVWX	Data Valid to #WR transition	WRT	38			T - 25			nS	
T WHQX	Data hold after #WR	WRT	73			T + 10			nS	
T RLAZ	#RD low to Address Float	RD						5	nS	
T YALH	#WR or #RD high to ALE high	RD/WRT	53		72	T -10		T + 10	nS	
T CHCL	clock fall time								nS	
T CLCX	clock low time								nS	
T CLCH	clock rise time								nS	
T CHCX	clock high time								nS	
T, TCLCL	clock period			63			1/fosc		nS	

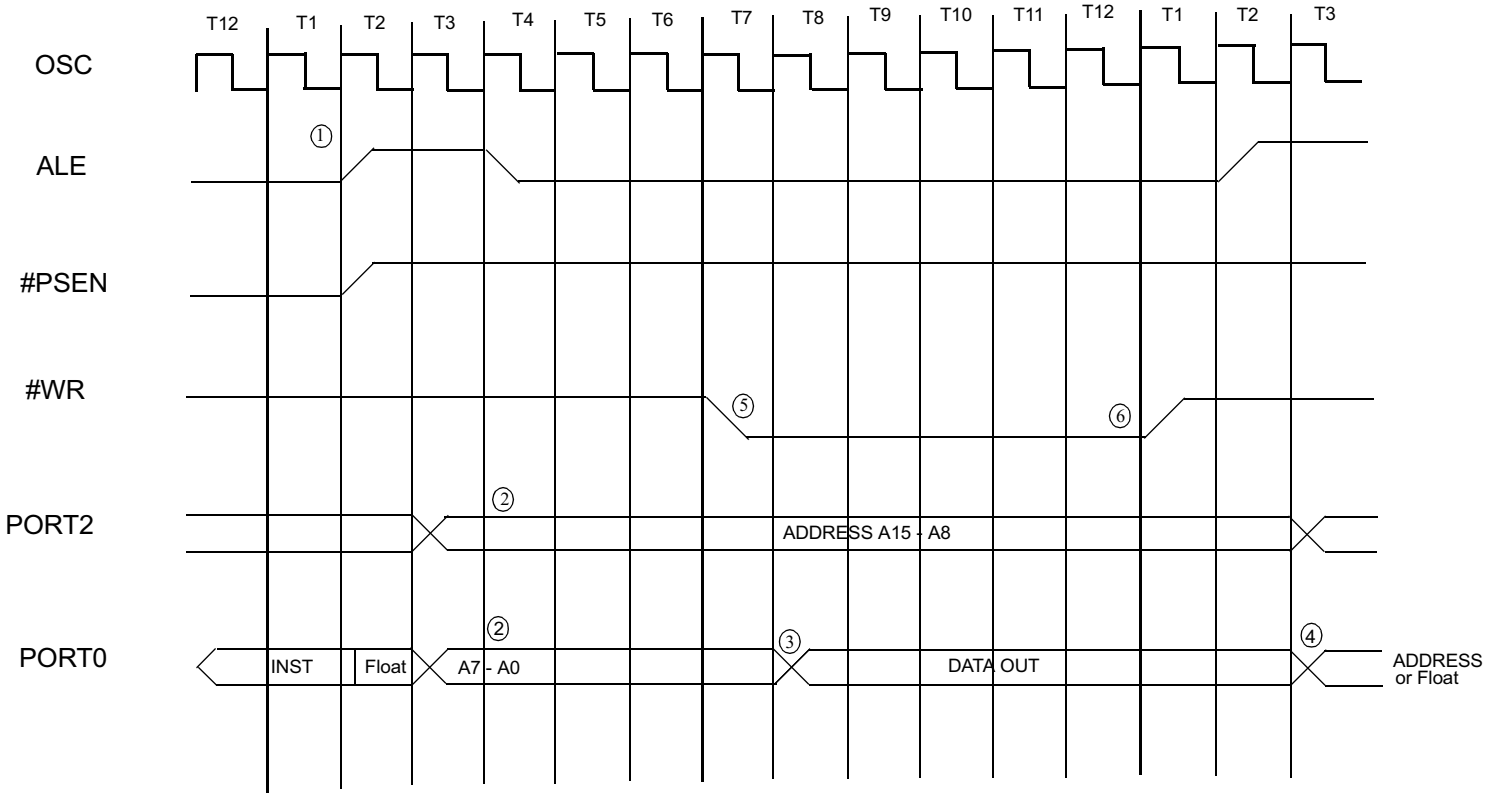
Data Memory Read Cycle Timing



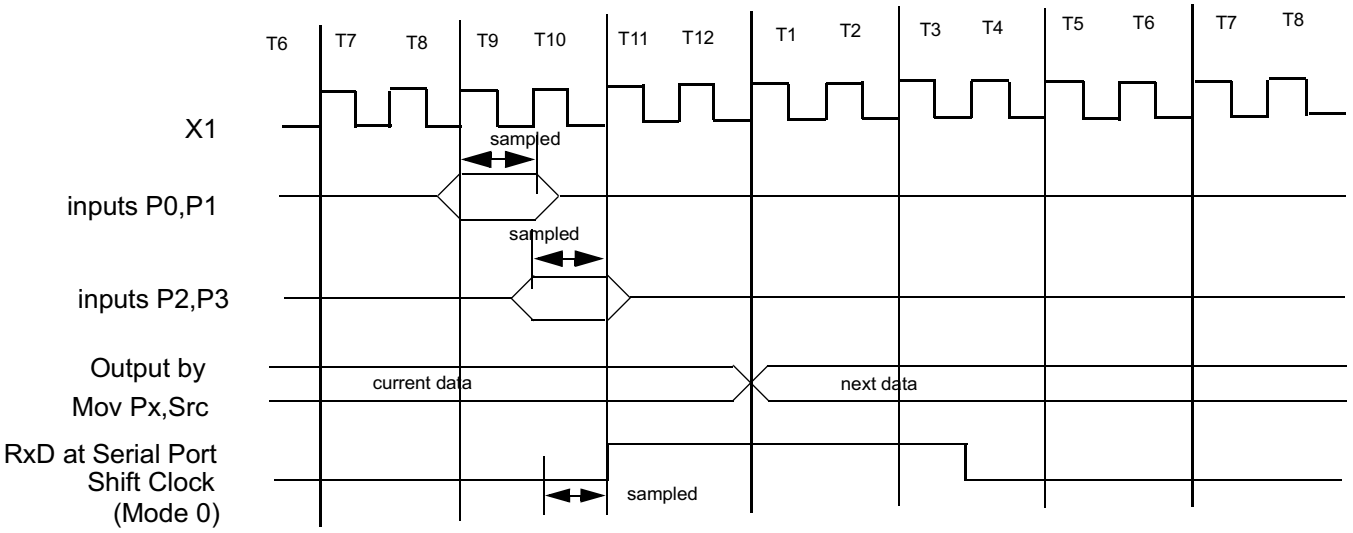
Program Memory Read Cycle Timing



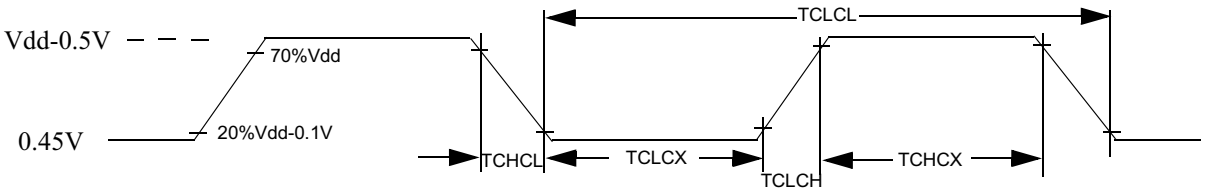
Data Memory Write Cycle Timing



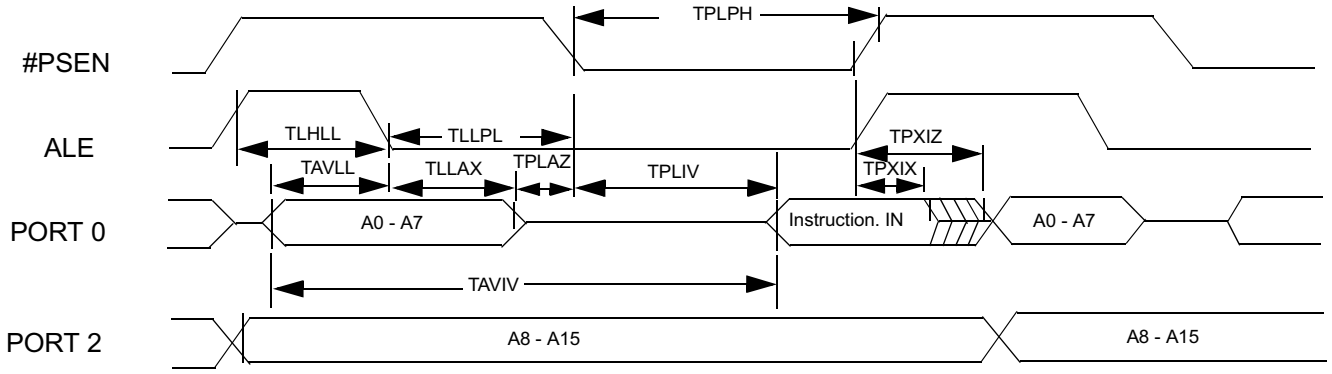
I/O Ports Timing



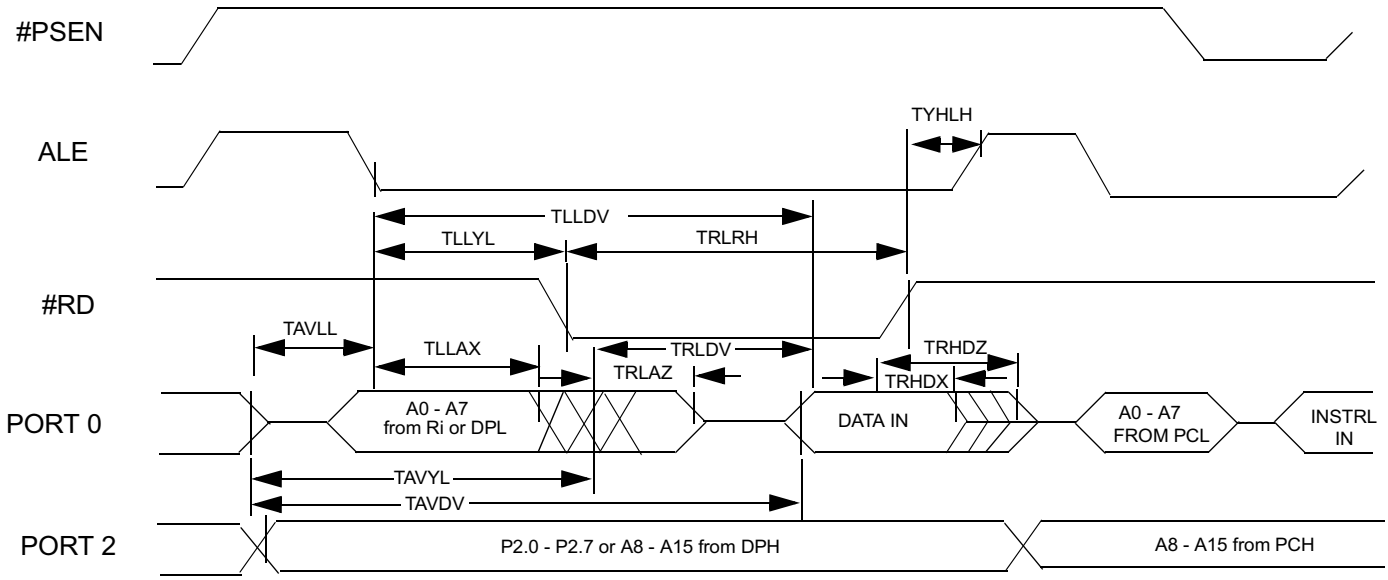
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



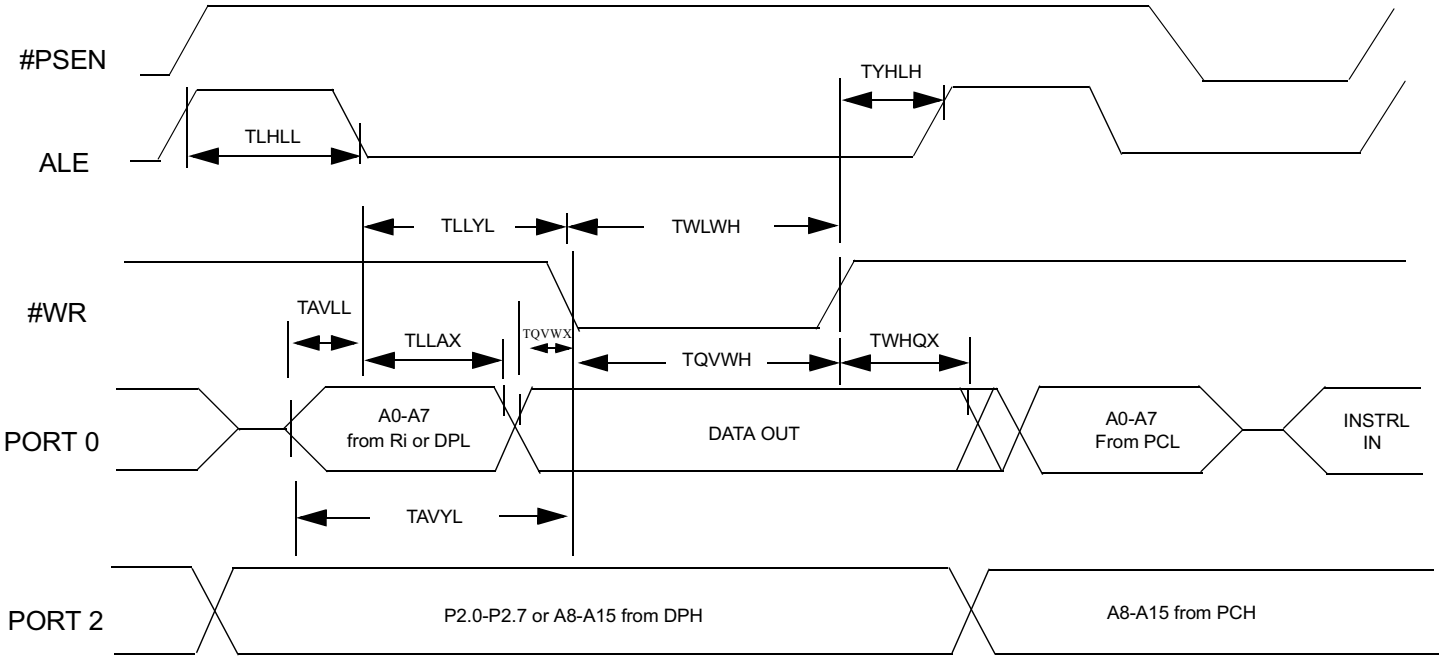
Tm.I External Program Memory Read Cycle



Tm.II External Data Memory Read Cycle

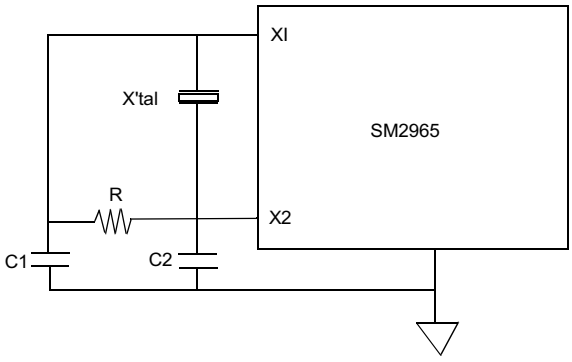


Tm.III External Data Memory Write Cycle



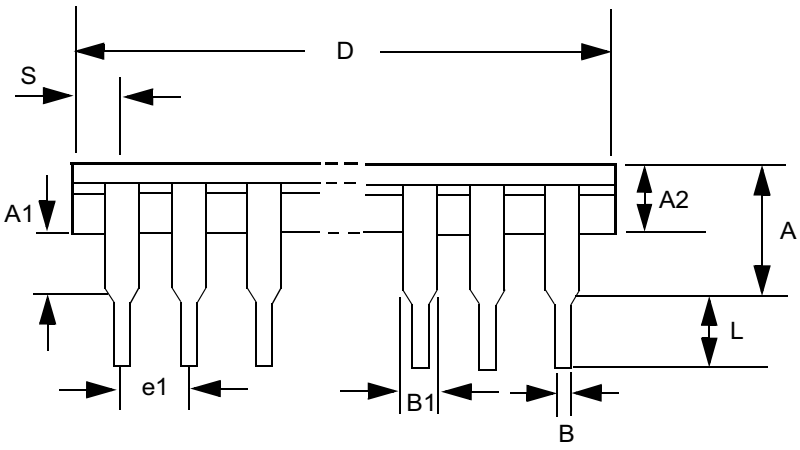
Application Reference

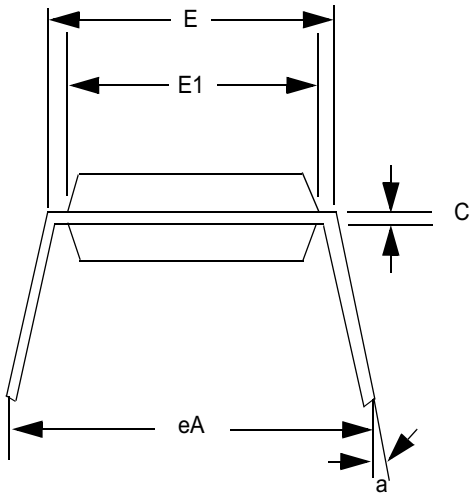
Valid for SM2965				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 p	30 p	30 p	30 p
C2	30 p	30 p	30 p	30 p
R	open	open	open	open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	10 pF	2 pF
C2	30 pF	15 pF	10 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ



NOTE:Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

40L 600mil PDIP Information



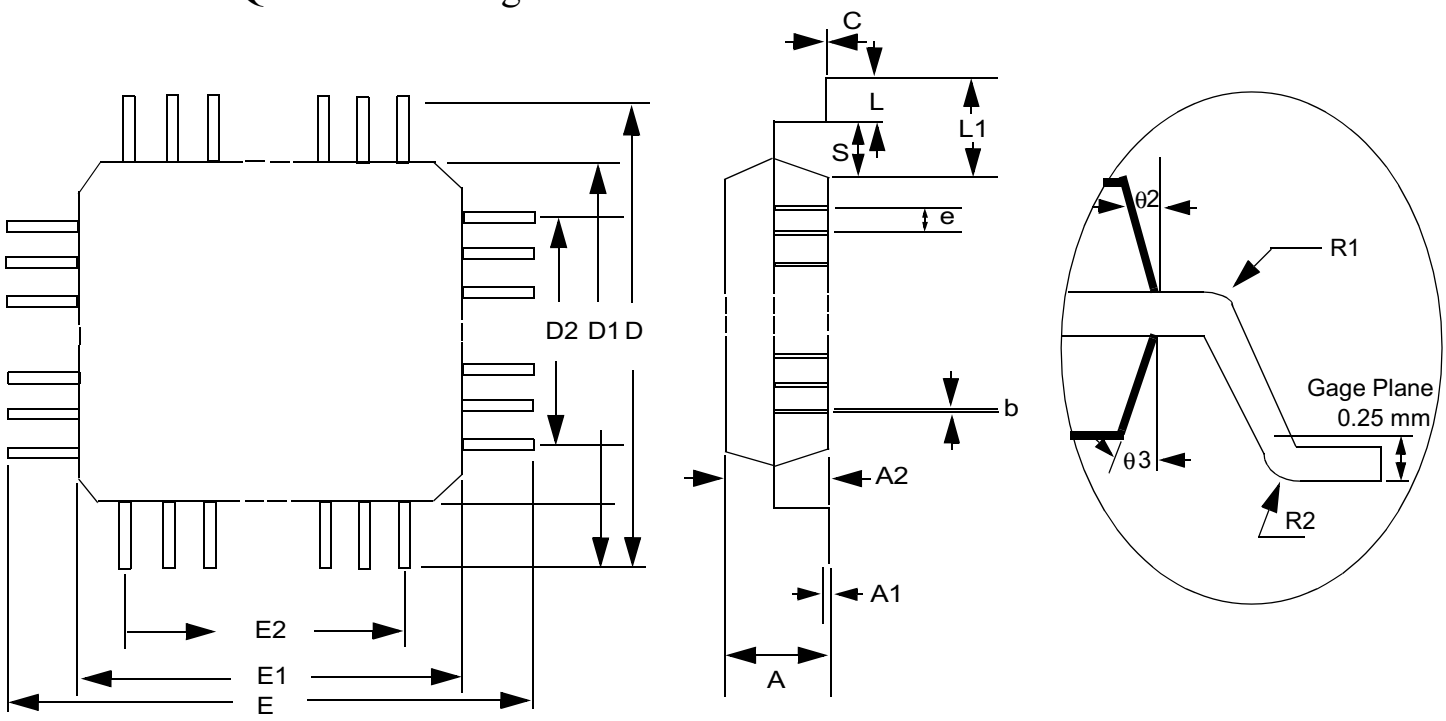


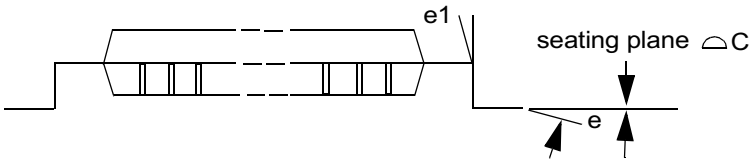
Note:

1.Dimension D Max & include mold flash or tie bar burrs.
2.Dimension E1 does not include interlead flash.
3.Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4.Dimension B1 does not include dambar protrusion/ infrusion.
5.Controlling dimension is inch.
6.General appearance spec. should base on final visual inspection spec.

Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.210	- / 5.33
A1	0.010 / -	0.25 / -
A2	0.150 / 0.160	3.81 / 4.06
B	0.016 / 0.022	0.41 / 0.56
B1	0.048 / 0.054	1.22 / 1.37
C	0.008 / 0.014	0.20 / 0.36
D	- / 2.070	- / 52.58
E	0.590 / 0.610	14.99 / 15.49
E1	0.540 / 0.552	13.72 / 14.02
e1	0.090 / 0.110	2.29 / 2.79
L	0.120 / 0.140	3.05 / 3.56
a	0° / 15°	0° / 15°
eA	0.630 / 0.670	16.00 / 17.02
S	- / 0.090	- / 2.29

44L Plastic Quad Flat Package

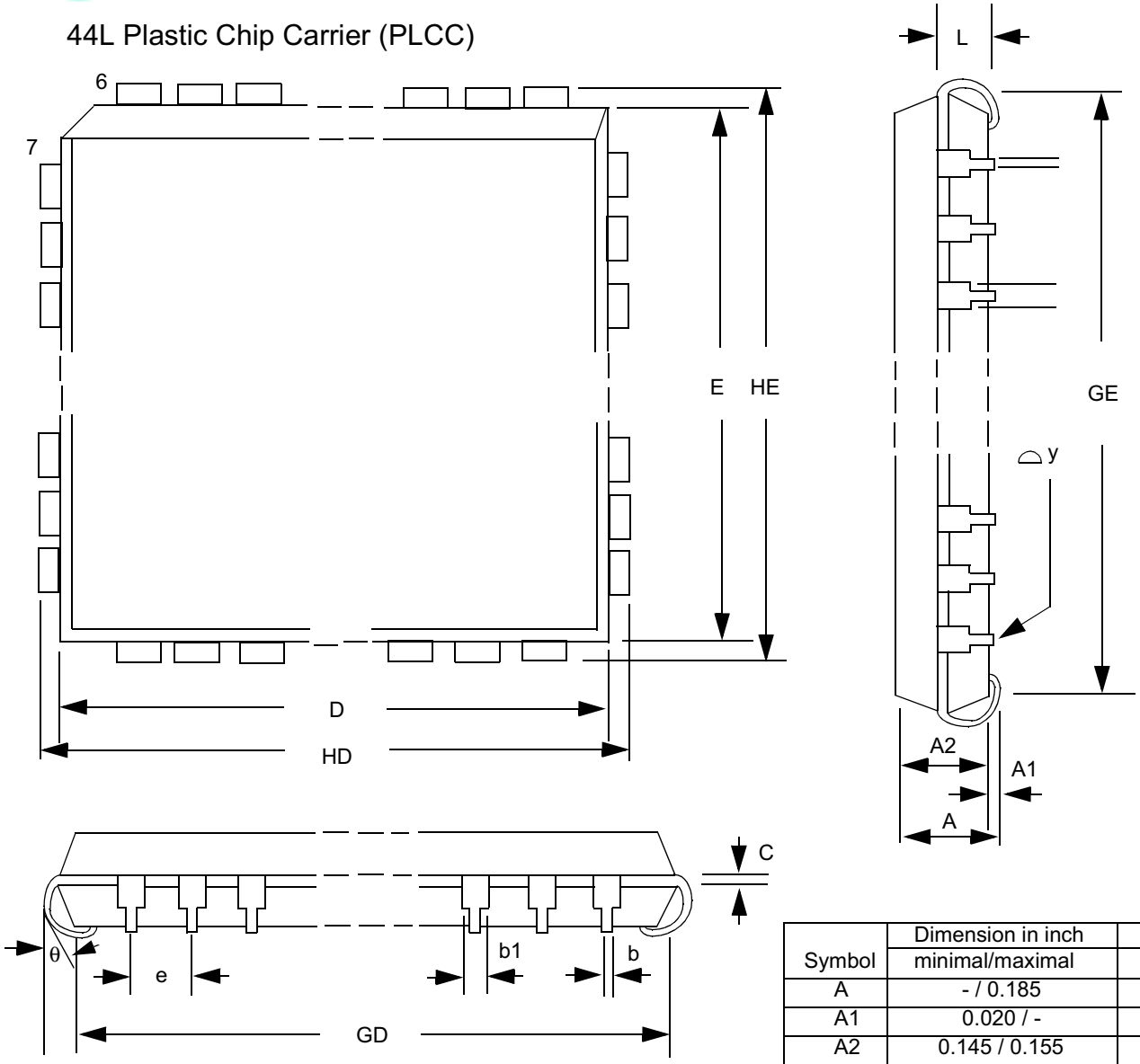




Note:
Dimension D1 and E1 do not include mold protrusion.
Allowance protrusion is 0.25mm per side.
Dimension D1 and E1 do include mold mismatch and are determined datum plane.
Dimension b does not include dambar protrusion.
Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot.

Symbol	Dimension in Inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.100	- / 2.55
A1	0.006 / 0.014	0.15 / 0.35
A2	0.071 / 0.087	1.80 / 2.20
b	0.012 / 0.018	0.30 / 0.45
c	0.004 / 0.009	0.09 / 0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73 / 1.03
L1	0.063	1.60
R1	0.005 / -	0.13 / -
R2	0.005 / 0.012	0.13 / 0.30
S	0.008 / -	0.20 / -
θ	0° / 7°	as left
θ1	0° / -	as left
θ2	10° REF	as left
θ3	7° REF	as left
⌓C	0.004	0.10

44L Plastic Chip Carrier (PLCC)



Symbol	Dimension in inch minimal/maximal	Dimension in mm minimal/maximal
A	- / 0.185	- / 4.70
A1	0.020 / -	0.51 / -
A2	0.145 / 0.155	3.68 / 3.94
b1	0.026 / 0.032	0.66 / 0.81
b	0.016 / 0.022	0.41 / 0.56
C	0.008 / 0.014	0.20 / 0.36
D	0.648 / 0.658	16.46 / 16.71
E	0.648 / 0.658	16.46 / 16.71
e	0.050 BSC	1.27 BSC
GD	0.590 / 0.630	14.99 / 16.00
GE	0.590 / 0.630	14.99 / 16.00
HD	0.680 / 0.700	17.27 / 17.78
HE	0.680 / 0.700	17.27 / 17.78
L	0.090 / 0.110	2.29 / 2.79
θ	- / 0.004	- / 0.10
⌓ y	/	/

Note:

1.Dimension D & E does not include interlead flash.

2.Dimension b1 does not include dambar protrusion/ intrusion.

3.Controlling dimension:Inch

4.General appearance spec. should base on final visual inspection spec.

eMCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Website: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	LabTool - 48 (1 * 1) LabTool - 848 (1*8)
Caprilion P.O. Box 461 KaoHsiung, Taiwan, ROC Website: http://www.market.net.tw/ ~ cap/	Tel:07-3865061 Fax:07-3865421 E-mail: cap@market.net.tw	UNIV2000
Hi-Lo 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Website: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mai: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8)
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Website: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	ChipStation (1*1) SU - 2000 (1*8)
System General 5F, No. 9 Alley 6, Lane 45 Bao Shing Rd. Shin - Tien, Taipei, Taiwan, ROC Website: http://www.sg.com.tw	Tel:02-29173005 Fax:02-29111283 E-mail: sales@sg.com.tw	Multi - Apro (1*1)
BP Microsystems 1000 N. Post Oak Road, Suite 225 Houston, Tx, U.S.A 77055-7237 Website: http://www.bpmicro.com	Tel:1-800-225-2102(US only) 713-688-4600 Fax:713-688-0920 E-mail: Tech@BPMicro.com	BP - 1200 (1*1)
Stag Programmers LTD Silver Court, Watchmead, Welwyn Garden, City, Hertfordshire, AL7 1LT. United Kingdom Website: http://www.stag.co.uk	Tel:44(0)1707 332148 Fax:+44(0)1707 371503 E-mail: sales@sg.com.tw	P803 (1*8)
Xeltek Electronic Co., Ltd 338 Hongwu Road, Nanjing, China 210002 Website: http://www.xeltek-cn.com	Tel:+86-25-4408399, 4543153-206 E-mail: xelclw@jlonline.com, xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/680 (1*1) Superpro/280 (1*1) Superpro/L+(1*1)

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Description: