FM24C04 FRAM® Serial Memory

Product Specification

1

Features

- 4,096-Bit Nonvolatile Ferroelectric RAM Organized as 512w x 8b
- Very Low Power CMOS Technology
  - 100µA Active (Read or Write)
  - 25µA Standby Over Commercial Temperature Range
- Reliable Thin Film Ferroelectric Technology
  - 10 Billion (10^{10}) Cycle Read/Write Endurance
  - 10 Year Data Retention
- High Performance
  - No Write Delay
  - 512 Byte Sequential Write
  - 47ms Full Chip Write
- Two Wire I²C Serial Interface
  - Direct Replacement for Xicor X24C04
- Hardware Write Protection
- True 5V Only Operation
- 8 Pin Mini-DIP and SOIC Packages
- -40° to +85°C Operating Range

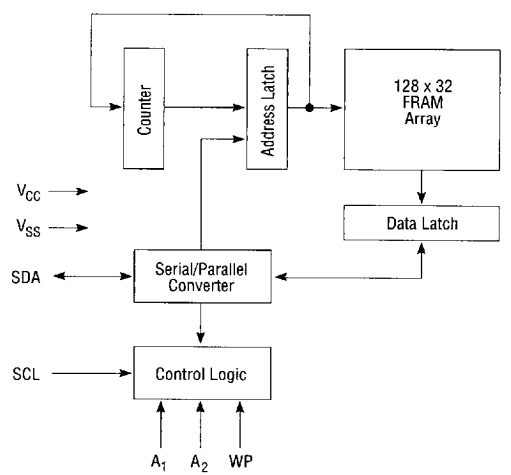
Description

The Ramtron FM24C04 ferroelectric random access memory, or FRAM® memory provides nonvolatile data integrity in a compact package. A two wire serial interface provides access to any byte within the memory while reducing the cost of the processor interface. The FM24C04 is useful in a wide variety of applications for the storage of configuration information, user programmable data/features, and calibration data.

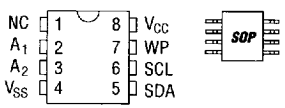
With Ramtron's ferroelectric technology, all writes are nonvolatile, eliminating long delays, extra page mode control, or high voltage pins. The technology is designed for highly reliable operation, offering extended endurance and 10 year data retention.

The part uses the industry standard two wire protocol for serial chip communication and is pin compatible with a number of parts from other vendors. Up to 16Kbits of FRAM memory may be connected on a single bus, comprised of multiple 24C04 parts. It is available in 300 mil mini-DIP and 150 mil SOP packages.

Functional Diagram



Pin Configurations



Pin Names	Function
A_1 - A_2	Device Address
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{SS}	Ground
V_{CC}	Supply Voltage

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R6 June 1994

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Absolute Maximum Ratings

Description	Ratings
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	-40°C to +85°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
D.C. Output Current	5mA
Lead Temperature (Soldering, 10 Seconds)	300°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Operating Conditions

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Typ(1)	Max	Units	Test Conditions
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	V_{CC} Supply Current		60	100	µA	SCL @ 100KHz, Read or Write SCL CMOS Levels, All Other Inputs = V_{SS} or V_{CC} - 0.3V
I_{SB}(2)	Standby Current 0°C to 70°C		8	25	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{SB}(2)	Standby Current -40°C to 85°C		16	60	µA	SCL = SDA = V_{CC}, All Other Inputs = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}	Input Low Voltage	-1.0		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3mA

(1) Typical values are measured at 25°C, 5.0V.
(2) Must perform a stop command prior to measurement.

Endurance and Data Retention

Parameter	Min	Max	Units
Endurance	10 Billion		R/W Cycles
Data Retention	10		Years

Power-Up Timing (3)

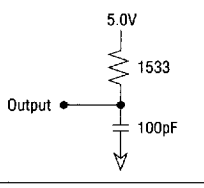
Symbol	Parameter	Max	Units
t_{PUR}(3)	Power Up to Read Operation	1	µs
t_{PUW}(3)	Power Up to Write Operation	1	µs

(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

AC Conditions of Test

AC Conditions	Test
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Levels	V_{CC} x 0.5

Equivalent AC Load Circuit



Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Test	Max	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (A_{1-2}, SCL, WP)	6	pF	V_{IN} = 0V

(4) This parameter is periodically sampled and not 100% tested.

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Pin Descriptions

SCL — Serial Clock

When high, the SCL clocks data into and out of the FM24C04. It is an input only.

SDA — Serial Data Address

This bi-directional pin is used to transfer addresses to the FM24C04 and data to or from the FM24C04. It is an open drain output and intended to be wire-ORed with all other devices on the serial bus using an external pull-up resistor.

A_1, A_2 — Address Bits 1 and 2

The A_1 and A_2 inputs set the device address for this particular FM24C04. If the state of A_1 and A_2 matches that within the slave address, then this FM24C04 will respond to the command. These pins must be connected to either V_{CC} or V_{SS}.

WP — Write Protect

If tied to V_{CC}, write operations into the upper half of the memory (bank select A_0 set to 1 in the slave address) will be disabled. Read and write operations to the lower portion of memory will proceed normally. If the write protection feature is not desired, this pin must be tied to V_{SS}.

Bus Protocol

The FM24C04 employs a bi-directional two wire bus protocol designed to support multiple bus slaves with a minimum of processor I/O pins. Figure 1 shows a typical system configuration connecting a microcontroller with two FM24C04 devices. Up to four FM24C04 devices can be connected on a single bus.

By convention, any device sending data onto the bus is the transmitter, while the device that is getting the data is the receiver. The device controlling the bus is the master and provides the clock signal for all operations. Devices being controlled are the slaves. The FM24C04 is always a slave device.

Transitions or states on the SDA and SCL lines denote one of four conditions: a *start, stop, data bit,* or *acknowledge*. Figure 2 shows the signaling for these conditions, while the following four sections describe their function.

Figure 3 shows the detailed timing specifications for the bus. Note that all SCL specifications and the *start* and *stop* specifications apply to both read and write operations. They are shown on one or the other for clarity. Also, the write timing specifications apply to all transmissions to the FM24C04, including the slave and word address, as well as write data sent to the FM24C04 from the bus master.

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Figure 1. Typical System Configuration

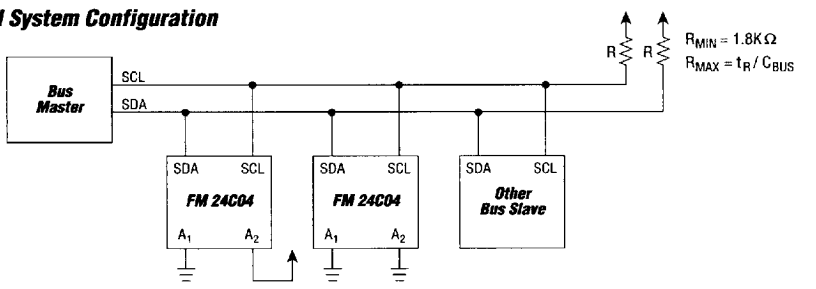

Figure 2. Data Transfer Protocol

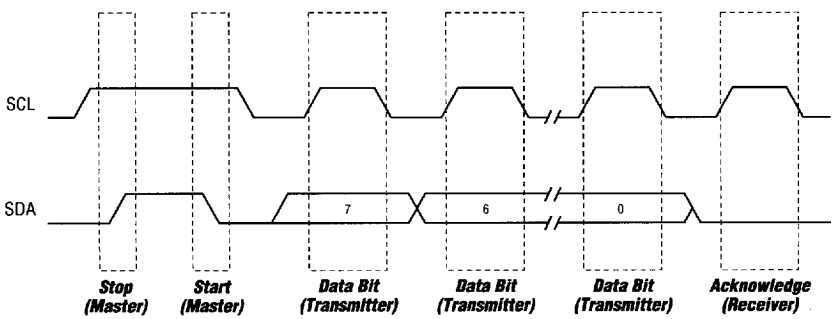

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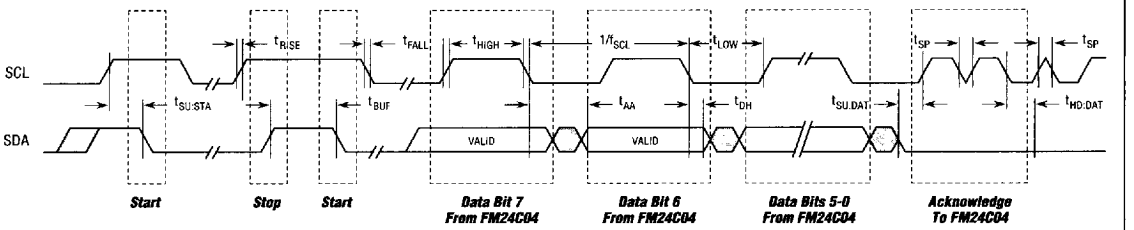
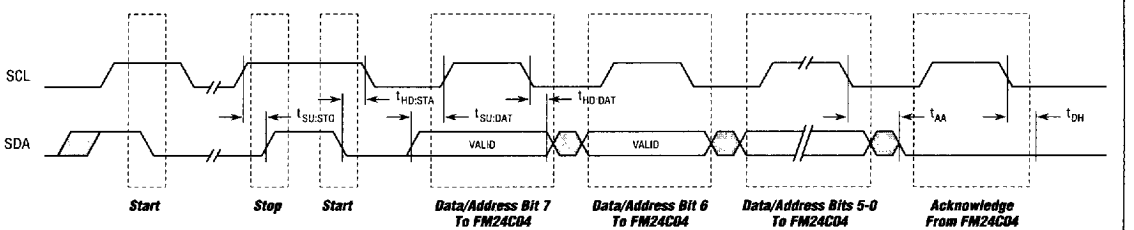
Figure 3. Bus Timing

Read



Write



Notes:

All start and stop timings apply to both read and write cycles identically.

Clock specifications same for both read and write.

Write timing specifications apply to slave address, word address, and write data.

These timing diagrams provide representative timing relationships of the signals. They are not intended to provide functional relationships between the signals. These are provided in Figures 5 through 9.

Read and Write Cycle AC Parameters

T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%, Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
t_{SP}	Noise Suppression Time Constant at SCL, SDA Inputs		50	ns
t_{AA}	SCL Low to SDA Data Out Valid		3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		ns
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_{RISE} (4)	SDA and SCL Rise Time		1	µs
t_{FALL} (4)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.0		µs
t_{DH}	Data Out Hold Time (From SCL @ V_{IL})	0		ns

(4) This parameter is periodically sampled and not 100% tested.

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Start Condition

A *start* condition is indicated to the FM24C04 when there is a high to low transition of SDA while SCL is high. All commands to the FM24C04 must be preceded by a *start*. In addition, a *start* condition occurring at any point within an operation will abort that operation and ready the FM24C04 to start a new one.

Stop Condition

A *stop* condition is indicated to the FM24C04 when there is a low to high transition of SDA while SCL is high. All operations to the FM24C04 must end with a *stop*. In addition, any operation will be aborted at any point when this condition occurs.

Data/Address Transfers

Data/address transfers take place during the period when SCL is high. Except under the two conditions described above, the state of the SDA line may not change while SCL is high. Address transfers are always sent to the FM24C04, while data transfers may either be sent to the FM24C04 (for a write) or to the bus master (for a read).

Acknowledge

Acknowledge transfers take place on the ninth clock cycle after each eight-bit address or data transfer. During this clock cycle, the transmitter will release the SDA bus to allow the receiver to drive the bus low to acknowledge receipt of the byte.

Device Operation

Low Voltage Protection

When powering up, the FM24C04 will automatically perform an internal reset and await a *start* signal from the bus master. The bus master should wait T_{PUR} (or T_{PUW}) after V_{CC} reaches 4.5V before issuing the *start* for the first read or write access. Additionally, whenever V_{CC} falls below 3.5V (typical), the part goes into its low voltage protection mode. In this mode, all accesses to the part are inhibited and the part performs an internal reset. If an access was in progress when the power supply fails, it will be automatically aborted by the FM24C04. When power rises back above 4.5V, a *start* signal must be issued by the bus master to initiate an access.

Slave Address

Following a *start*, the FM24C04 will expect a slave address byte to appear on the bus. This byte consists of four parts as shown in Figure 4.

- Bits 7 through 4 are the device type identifier which must be binary 1010 as shown.
- Bits 2 and 3 are the device address. If bit 2 matches the state of the A_1 pin and bit 3 matches the state of the A_2 pin, then the part will be selected.
- Bit 1 is the page select. If set to 1, then the upper 256 bytes of memory (addresses hex 100 through 1ff) will be accessed, while the lower block will be accessed if it is 0.
- Bit 0 is the read/write bit. If set to a 1, a read operation is being performed by the master; otherwise, a write is intended.

Word Address

After a slave device *acknowledges* the slave address on a write operation, the master will place the word address on the bus. This byte, in addition to the page select bit from the slave address, forms the address of the byte within the memory that is to be written. This nine-bit value is latched in the internal address latch. There is no word address specified during a read operation.

During the transmission of each data byte and before the acknowledge cycle, the address in the internal latch is incremented to allow the following byte to be accessed immediately. When the last byte in the memory is accessed (at address hex 1ff), the address is reset to 0. There is no alignment requirement for the first byte of a block cycle — any address may be specified. There is also no limit to the number of bytes that may be accessed in a single read or write operation.

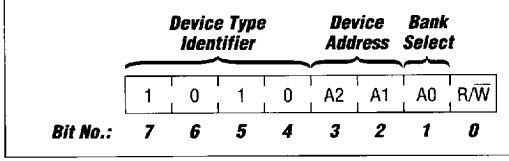
Data Transfer

After all address bytes have been transmitted, data will be transferred between the FM24C04 and the bus master. In the case of a read, the FM24C04 will place each of the eight bits on the bus and then wait for an acknowledge from the bus master before performing a read on the subsequent address. For a write operation, the FM24C04 will accept eight bits from the bus master and then drive the acknowledge on the bus.

All data and address bytes are transmitted most significant bit (bit 7) first.

After the acknowledge of a data byte transfer, the bus master may either begin another read or write on the subsequent byte, issue a *stop* command to terminate the block operation, or issue a *start* command to terminate the current operation and start a new one.

Figure 4. Slave Address



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Write Operations

All write operations start with a slave and word address transmission to the FM24C04. In the slave address, bit 0 should be set to a 0 to denote a write operation. After they are acknowledged, the bus master transmits each data byte(s) to the FM24C04. After each byte, the FM24C04 will generate an acknowledge signal. Any number of bytes may be written in a single write sequence. After the last byte in the memory (address hex 1ff) is written, the address counter wraps around to zero so that the subsequent byte written will be the first (address 0).

There is no write delay on the FM24C04. Any operation, either a read or write to some other address, may immediately follow a write. Acknowledge polling, a sequence used with EEPROM devices to let the bus master know when a write cycle is complete, will return done immediately (the FM24C04 will acknowledge the first correct slave address).

If a write cycle must be aborted (with a *start* or *stop* condition), this should take place *before* the transmission of the eighth bit in order that the memory not be altered.

The write protect (WP) pin on the FM24C04 allows the upper half of the memory array (addresses hex 100 through 1ff) to be protected against accidental modification. When the pin is tied to V_{CC}, slave and word addresses targeted at the FM24C04 will still be acknowledged, but no acknowledge will occur on the data cycle if the address is in the upper half. In addition, no address incrementing occurs when writes are attempted to this half of the memory. If the write protection feature is not desired, this pin must be tied to V_{SS}.

Figure 5. Byte Write

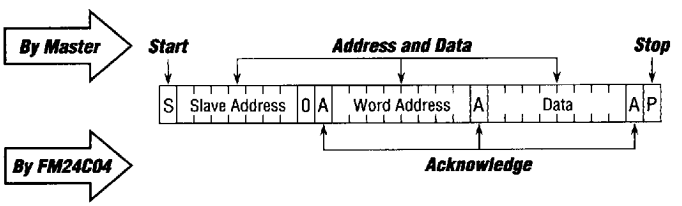
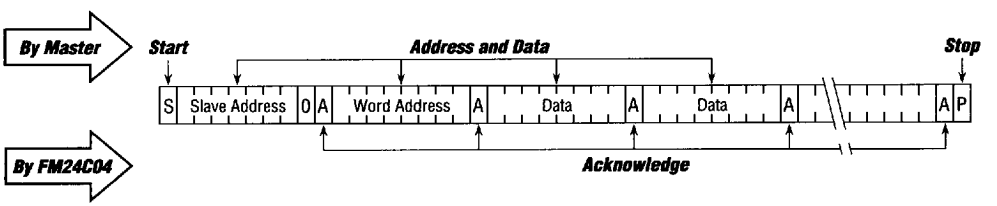


Figure 6. Multiple Byte Write



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Read Operations

Current Address or Sequential Read

Sequential read operations take place from the address currently held in the internal address latch, and so require only that the bus master provide a slave address transfer before the FM24C04 begins the transfer of data to the master. In this slave address, bit 0 should be set to a 1 to denote a read operation. Note that the MSB of the nine-bit internal address latch is specified by the slave address word, and is therefore *always* set during a read, regardless of which page the previous access referenced.

One or multiple bytes may be read from the FM24C04 in a single read operation. In a multi-byte read, each acknowledge from the bus master indicates to the slave that another byte is being requested.

The read operation must be properly terminated after the final 8-bit byte has been read. The bus master can end the read sequence in one of four ways:

(1) The first and recommended way is for the bus master to issue a no acknowledge in the ninth clock cycle and a stop in the tenth clock cycle. This is shown in Figures 7 through 9.
(2) The second method is for the bus master to issue a no acknowledge in the ninth clock cycle and a start in the tenth clock cycle.
(3) The bus master issues a stop in the ninth clock cycle.
(4) The bus master issues a start in the ninth clock cycle.

After the last byte in the memory (address hex 1ff) is read, the address counter wraps around to zero so that the subsequent byte to be read will be the first location in the memory (address 0). These sequences are shown below in Figures 7 and 8.

Selective (Random) Read

Selective, or random, read operations are possible on the FM24C04 by using the first two bytes of the *write* operation to load the internal address. The slave address for the part is sent out with bit 0 ($R/\overline{W}$) set to 0 to denote a write operation, and the word address is set to specify the least significant 8 bits of the desired address.

After the FM24C04 acknowledges this word address, the bus master should abort the *write* and begin the read with a *start* command. A new slave address is then sent out, this time with the $R/\overline{W}$ bit set to 1. Following the slave address and acknowledge, the FM24C04 will immediately begin transmission of the requested data. Figure 9 shows this operation.

Figure 7. Current Address Read

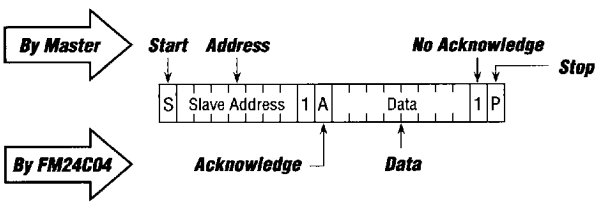


Figure 8. Sequential Read

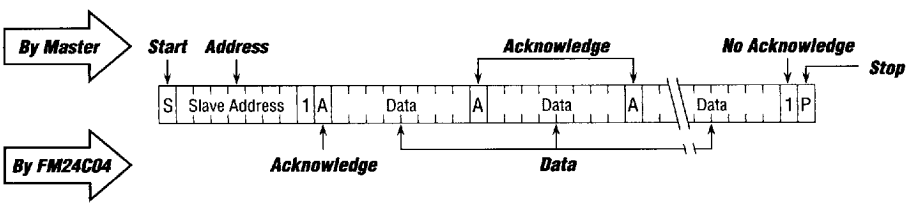
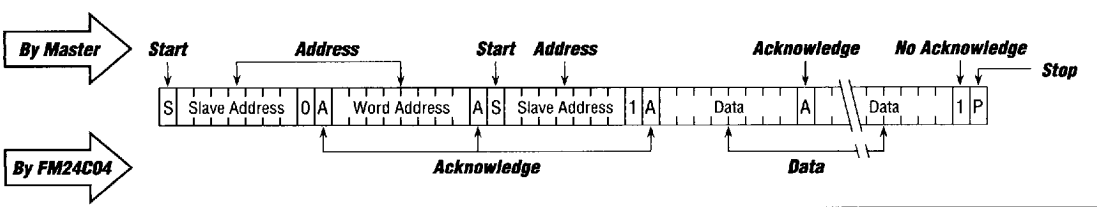


Figure 9. Selective Read



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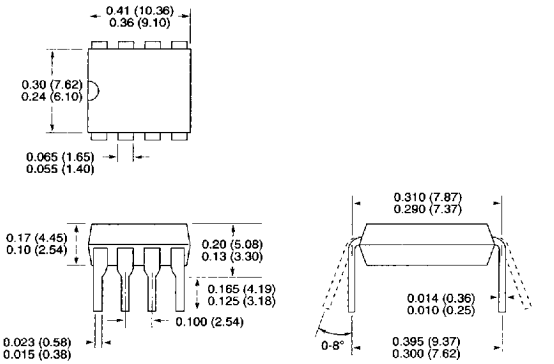
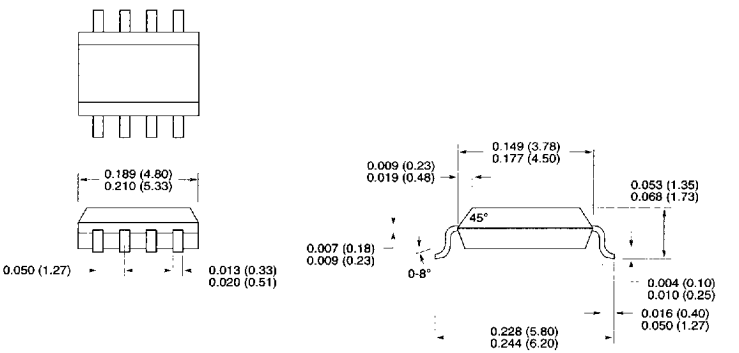
Packaging Information

8-Pin Plastic or Ceramic DIP



8-Pin SO (JEDEC)



Ordering Information

FM 24C04 - PS

Package Type (8-Pin)
PS - Plastic Skinny DIP
PT - Thin Plastic Skinny DIP
S - Plastic SOP
C - CERDIP

4K Serial FRAM Memory

Ramtron Ferroelectric Memory

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