PENTIUM® III XEON™ PROCESSOR AT 700 MHz and 900 MHz.

Datasheet

Product Features

- Binary compatible with applications running on previous members of the Intel microprocessor family
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Dynamic Independent Bus architecture: separate dedicated external 100 MHz System Bus and dedicated internal cache bus operating at full processor core speed
- Power Management capabilities
- System Management mode
- Multiple low-power states
- Single Edge Contact (S.E.C.) cartridge packaging technology; the S.E.C. cartridge delivers high performance processing and bus technology to mid range to high end servers and workstations
- 100 MHz system bus speeds data transfer between the processor and the system
- Integrated high performance16k instruction and 16k data, non-blocking, level-one cache
- Available in 1MB (700 MHz) or 2MB (900 MHz and 700 MHz) unified, non-blocking level-two cache
- Enables systems which are scaleable up to two processors and 64GB of physical memory
- SMBus interface to advanced manageability features
- Streaming SIMD Extensions for enhanced video, sound and 3D performance

The Intel® Pentium® III Xeon™ Processor at 700 MHz with 1MB or 2MB L2 cache and 900 MHz with 2MB L2 cache is designed for mid-range to high-end servers and workstations, and is binary compatible with previous Intel® Architecture processors. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz provides the best performance available for applications running on advanced operating systems such as Microsoft* Windows* 98, Microsoft* Windows* NT*, and UNIX*. The processor is scalable to four processors in a multiprocessor system and extends the power of the Pentium® Pro processor with new features designed to make this processor the right choice for powerful workstation, advanced server management, and mission-critical applications. Pentium® III Xeon™ processor at 700 MHz and 900 MHz-based workstations offer the memory architecture required by the most demanding workstation applications and workloads. Specific features of the processor address platform manageability to meet the needs of a robust IT environment, maximize system up time and ensure optimal configuration and operation of servers. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz enhances the ability of server platforms to monitor, protect, and service the processor and its environment.

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1. INTRODUCTION

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz, like the Pentium® Pro, Pentium® II, Pentium® II Xeon™ and previous Pentium® III Xeon™ processors, implements a Dynamic Execution micro-architecture, a unique combination of multiple branch prediction, data flow analysis, and speculative execution. The Pentium® III Xeon™ processor at 700 MHz will be available in 1MB and 2MB L2 cache sizes whereas the Pentium® III Xeon™ processor at 900 MHz will only be available in the 2MB L2 cache size.

The Pentium® III Xeon™ processor improves upon previous generations of Intel® processors by adding Streaming SIMD Extensions. The Single Instruction Multiple Data (SIMD) extensions significantly accelerate performance of 3D graphics. Besides 3D graphics improvements, the extensions also include additional integer and cacheability instructions that improve other aspects of performance. In addition, the Pentium® III Xeon™ processor utilizes a variation of the S.E.C. (Single Edge Contact) package technology first introduced on the Pentium® II processor. The SEC packaging technology allows the Pentium® III Xeon™ processor at 700 MHz and 900 MHz to implement the Dual Independent Bus Architecture and have up to 2MB of level 2 cache. The level 2 cache is integrated in the processing unit and communication occurs at the full speed of the processor core.

As with previous members of the Pentium® II Xeon™ processor family, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz features built-in direct multiprocessing support. For systems with up to four processors, it is important to consider the additional power requirements and signal integrity issues of supporting multiple loads on a high-speed bus. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz supports both uni-processor and multiprocessor implementations with support for up to four processors on each local processor bus, or *system bus*.

The processor system bus I/O buffers operate using *Assisted Gunning Transistor Logic, or AGTL+.* The processor uses the S.E.C. cartridge package supported by the SC330 Connector (See Chapter 7 for the processor mechanical specifications.)

The Pentium® III Xeon™ processor includes an SMBus interface that allows access to several processor features, including two memory components (referred to as the Processor Information ROM and the Scratch EEPROM) and a thermal sensor on the processor substrate.

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz system bus definition uses the SC330.1 interface. The SC330.1 interface is an electrical only enhancement to the SC330 (formerly Slot2) interface that allows supporting for a 4-way Pentium® III Xeon™ processor at 700 MHz and 900 MHz-based system running at 100 MHz system bus frequency. The SC330.1 specification adds the required flexibility to accommodate control and monitoring signals for an OCVR (On Cartridge Voltage Regulator). The OCVR provides the necessary high precision regulation used by Intel's latest silicon technology. This document provides information regarding the design of a system using the Pentium® III Xeon™ processor at 700 MHz and 900 MHz with the new SC330.1 bus specification.

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz is designed to be compatible with previous SC330-compliant baseboards given that an existing platform meets the signal integrity and timing requirements of Intel's latest silicon technology as specified in this document. For details on system compatibility requirements refer to the *Pentium III Xeon Processor System Compatibility Guidelines*. Certain versions of the processor are designed to be compatible with the existing VRM 8.3 Guidelines, allowing an easy transition for Flexible Mother Board designs. The 2.8V version of the processor (regardless of frequency and cache size) is designed for compatibility with the VRM 8.3 Guidelines. The 5V/12V version of the processor adds flexibility to operate at either 5 Volts or 12 Volts. The new flexible motherboard specification that incorporates the SC330.1 interface uses the same form factor and pin definition of the existing SC330 (formerly Slot 2) processors, but adds signals to control an OCVR and remote sensing capabilities. The SC330.1 enhancement is electrically and mechanically compatible with baseboards designed for the SC330 interface.

2. TERMINOLOGY

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a non-maskable interrupt has occurred. In the case of lines where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D [3:0] # = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term 'system bus' refers to the interface between the processor, system core logic and other bus agents. The system bus is a multiprocessing interface to processors, memory and I/O. Cache coherency is maintained with other agents on the system bus through the MESI cache protocol as supported by the HIT# and HITM# bus signals. The term "processor" refers to the cartridge package that interfaces to a host system board through the SC330.1 interface specification. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz includes one processor core with integrated L2 cache, an On-Cartridge Voltage Regulator (OCVR), system bus termination and various system management features. In addition, the processor includes a thermal plate for cooling solution attachment and a protective cover.

2.1 S.E.C. CARTRIDGE TERMINOLOGY

The following terms are used in this document and are defined here for clarification:

- **Cover** — The processor casing on the opposite side of the thermal plate.
- **Core pin** — The most external feature of the core package contained within the S.E.C. cartridge used to connect the core to an internal cartridge substrate trace. For measurement and specification purposes, the cartridge vias used to connect the core package to the cartridge substrate traces may be considered the core pins.
- **Core pad** — A feature of a processor die contained within the core package used to connect the die to the core package. A core pad is defined in the processor signal integrity models and is only observable in simulation.
- **Pentium® III Xeon™ processor at 700 MHz and 900 MHz** — The SC330 processor including internal components, substrate, thermal plate and cover, with either 1MB or 2MB of on-die L2 cache, a 100 MHz system bus, and support for up to 4-way configurations.
- **FMB** (**Flexible Motherboard Specification)** — A set of specifications to which a design is targeted to allow forward compatibility with existing and future processors.
- **L1 cache** — Integrated static RAM used to maintain recently used information. Due to code locality, maintaining recently used information can significantly improve system performance in many applications. The L1 cache is integrated directly on the processor core.
- **L2 cache** — The L2 cache is integrated directly on the processor core.
- **OCVR** — On Cartridge Voltage Regulator, a new feature that provides the necessary regulated power to the processor core and Integrated L2 cache and is located on the Pentium® III Xeon™ processor at 700 MHz and 900 MHz substrate.
- **2.8V version** — refers to a Pentium® III Xeon™ processor at 700 MHz and 900 MHz that can be powered with +2.8 volts applied to its VCC_CORE pins.
- **5V/12V version** — refers to a Pentium® III Xeon™ processor at 700 MHz and 900 MHz that can be powered with either +5.0 or +12.0 volts applied to its VCC_CORE pins.
- **HV_EN#** — pin added to the SC330.1 definition as a way of differentiating a 5V/12V version Pentium® III Xeon™ processor at 700 MHz and 900 MHz from a 2.8V version. HV_EN# is tied to V_{ss} (ground) on the 5V/12V version, and is high impedance (floating) on the 2.8V version. This is a reserved (no connect) pin on Pentium® III Xeon™ processors.
- **Processor substrate** — The structure on which components are mounted inside the S.E.C. cartridge (with or without components attached).
- **Processor core** — The processor's execution engine.
- **S.E.C. cartridge** — The processor packaging technology used for the Pentium® II Xeon™ processor family. S.E.C. is short for "Single Edge Contact" cartridge.
- **Streaming SIMD Extensions —** A new set of instructions supported by Intel® processors beginning with the Pentium® III Xeon™ processor. Single Instruction Multiple Data (SIMD) extensions significantly accelerate performance of 3D graphics. Besides 3D graphics improvements, the extensions also include additional integer and cacheability instructions that improve other aspects of performance.
- **Thermal plate** — The surface used to connect a heatsink or other thermal solution to the processor.

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Additional terms referred to in this and other related documentation:

- **SC330.1** — An enhanced electrical and mechanical interface based on the SC330 (formerly Slot2) interface that defines additional signals and electrical requirements to support an OCVR (On Cartridge Voltage Regulator), a processor core and a System Bus frequency of 100 MHz for 4-way designs. Refer to Chapter 10 for details.
- **Retention mechanism** — A mechanical component designed to hold the processor in a SC330 connector.

2.2 State of Data

The data contained within this document is subject to change. It is the best information that Intel® is able to provide by the publication date of this document.

2.3 References

The reader of this specification should also be familiar with material and concepts presented in the following documents:

- *CPU-ID Instruction Application Note* (Order Number 241618)
- *Pentium® III Xeon™ Processor at 700 MHz and 900 MHz Signal Integrity Models,* IBIS Format (www.developer.intel.com)
- *Intel® Pentium® III Xeon™ Processor Specification Update* (Order Number 244460)
- *S330 Processor Enabling Technology Vendor List* (www.developer.intel.com)
- *Intel Architecture Software Developer's Manual* (Order Number 243193)
  - *Volume I: Basic Architecture* (Order Number 243190)
  - *Volume II: Instruction Set Reference* (Order Number 243191)
  - *Volume III: System Programming Guide* (Order Number 243192)
- *330-Contact Slot Connector (SC330) Design Guidelines*
  (http://developer.intel.com/design/pentiumii/xeon/designgd/index.htm)
- *VRM 8.3 Specification*
  (http://developer.intel.com/design/pentiumii/xeon/designgd/index.htm)
- *Pentium® II Xeon™ processor/Intel® 450NX PCIset AGTL+ Layout Guidelines* (Order Number 243790)

3. ELECTRICAL SPECIFICATIONS

3.1 System Bus and VREF

The Pentium® III Xeon™ processor signals use a variation of the Pentium® Pro processor GTL+ signaling technology. The Pentium® III Xeon™ processor differs from the Pentium® II processor and Pentium® Pro processor in its output buffer implementation. The buffers that drive most of the system bus signals on the Pentium® III Xeon™ processor are actively driven to V_{TT} for one clock cycle after the low to high transition to improve rise-times and reduce noise. These signals should still be considered open-drain and require termination to a supply that provides the high signal level. Because this specification is different from the standard GTL+ specification, it is referred to as *Assisted Gunning Transistor Logic* (AGTL+) in this document. AGTL+ logic and GTL+ logic are compatible with each other and may both be used on the same system bus. For more information on the GTL+ specification, see the *Pentium II Processor Developer's Manual* (Order Number 243502).

AGTL+ inputs use differential receivers that require a reference signal (V_{REF}). The receivers use V_{REF} to determine if a signal is a logical 0 or a logical 1. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz generates its own version of V_{REF}. V_{REF} must be generated on the baseboard for other devices on the AGTL+ system bus. Termination is used to pull the bus up to the high voltage level and to control signal integrity on the transmission line. The processor contains termination resistors, but additional termination on the baseboard may be necessary to maintain proper signal quality and timing for the processor and any additional system bus devices. Some of the electrical specifications assume a specific effective termination resistance. See test conditions described with each specification.

Due to the existence of termination on each of up to 4 processors in a Pentium® III Xeon™ processor at 700 MHz and 900 MHz, the AGTL+ bus is typically not a daisy chain topology as in previous P6 Family processor systems. Like the Pentium® II Xeon™ processor, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz timing specifications are defined to points internal to the processor cartridge. Analog signal simulation of the system bus is required when developing Pentium® III Xeon™ processor at 700 MHz and 900 MHz-based systems to ensure proper operation over all conditions.

3.2 Power and Ground Pins

By implementing an On Cartridge Voltage Regulator (OCVR), the Pentium® III Xeon™ processor at 700 MHz and 900 MHz eliminates the need for high precision regulation from the flexible baseboard. A Pentium® III Xeon™ processor at 700 MHz and 900 MHz platform could be implemented to supply operating voltages of the processor die and of the L2 cache die for compatibility with previous generations of the Pentium® III Xeon™ processor. These voltages may differ from each other. Note that the Pentium® III Xeon™ processor at 700 MHz and 900 MHz does not require a dedicated L2 supply and that VID logic will assume L2 supply is not required. (*Please refer to the VRM 8.3 specification for details*). The Pentium® III Xeon™ processor at 700 MHz and 900 MHz FMB allows compatibility with previous Pentium® III Xeon™ processors. In an FMB that supports Pentium® III Xeon™ processor, there must be two groups of power inputs to support the voltage difference between the components in the package. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz will not use the voltage identification (VID) pins for L2 Cache (VID_L2), but a system that supports the previous generation of Pentium® III Xeon™ processors must use those pins to supply the correct voltages to the processor L2 cache.

In a FMB design, there are five pins defined on the package for core voltage identification (VID_CORE), and five pins defined on the package for L2 cache voltage identification (VID_L2). These pins specify the voltage required by the processor core and L2 cache respectively. A Pentium® III Xeon™ processor at 700 MHz and 900 MHz relies on the VID identification pins for the V_{CC_CORE} required voltage level ONLY and does not require a separate L2 voltage supply.

For signal integrity improvement and clean power distribution within the S.E.C. package, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz FMB has 65 V_{CC} (power) and 55 V_{SS} (ground) inputs (see section 7.3 for a complete edge finger signal listing). The 65 V_{CC} pins are further divided to provide the different voltage levels to the components. V_{CC_CORE} inputs for the processor core account for 35 of the V_{CC} pins, while 8 V_{TT} inputs (1.5V) are used to provide an AGTL+ termination voltage to the processor. The 20 V_{CC_L2} inputs are not connected on the Pentium® III Xeon™ processor at 700 MHz and 900 MHz). One V_{CC_SMB} pin is provided for use by the SMBus, and one V_{CC_TAP}. The V_{CC_SMB}, V_{CC_TAP}, V_{CC_L2} (on previous versions of the Pentium® III Xeon™ only), and V_{CC_CORE} must remain electrically separated from each other. V_{CC_SMB} must be connected to a 3.3V power supply (even if the SMBus features are not used) in order for the processor to function properly. On the baseboard, all V_{CC_CORE} pins must be connected to a voltage plane. Similarly, all V_{SS} pins must be connected to a system ground plane.

ELECTRICAL SPECIFICATIONS

For a summary of the power and ground pins listed above, see Table 50 and Table 51 in section 7.3 of this document for signal listings by Pin Number and Pin Name.

3.3 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This causes voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or a reduced lifetime of the component.

3.3.1 VCC_CORE

The power input should provide bulk capacitance with a low Effective Series Resistance (ESR) and the system designer must also control the interconnect resistance from the regulator (or VRM pins) to the SC330 connector. Simulation is required for first and second order characterization. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, is provided on the voltage regulation module (VRM) defined in the *VRM 8.3 DC–DC Converter Design Guidelines*. The input to VCC_CORE should be capable of delivering a recommended minimum $dI_{CC_{CORE}}/dt$ defined in Table 6 while maintaining the required tolerances defined in Table 5.

3.3.2 LEVEL 2 CACHE DECOUPLING

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz **does not** require the VccL2 pins for power, however for systems that are designed to support this processor as well as previous Pentium® II Xeon™ and Pentium® III Xeon™ processors, the regulator solutions need to implement and provide bulk capacitance with a low Effective Series Resistance (ESR) in order to meet the tolerance requirements for $V_{CC_{L2}}$ of previous processors. Use similar design practices as those recommended for VCC_CORE.

3.3.3 SYSTEM BUS AGTL+ DECOUPLING

The processor contains high frequency decoupling capacitance on the cartridge substrate; the system baseboard must provide bulk decoupling for proper AGTL+ bus operation. High frequency decoupling may be necessary at the SC330 connector to further improve signal integrity if noise is introduced at the connector interface.

3.4 Clock Frequencies and System Bus Clock Ratios

The Pentium® III Xeon™ processor uses a clock ratio design in which the bus clock is multiplied by a ratio to produce the processors internal (“core”) clock. The Pentium® III Xeon™ processor at 700 MHz begins sampling A20M#, IGNNE#, LINT[0], and LINT[1] on the inactive-to-active transition of RESET# to determine the core-frequency to bus-frequency relationship, and the PLL immediately begins to lock on to the input clock. However, the Pentium® III Xeon™ processor at 900 MHz ignores the logic states presented to the core/bus ratio pins at the de-assertion of the RESET# signal, and will operate only with a 9:1 core/bus ratio. On the active-to-inactive transition of RESET#, the Pentium® III Xeon™ processor at 700 MHz internally latches the inputs to allow the pins to be used for normal functionality. Effectively, these pins must meet a large setup time (1ms) to the active-to-inactive transition of RESET# (see RESET# and PWRGD relationship in Figure 41). These pins should then be held static for at least 2 bus clocks, but no longer than 20 bus clocks.

Table 1 System Bus-to-Core Frequency Ratio Configuration[1]

Ratio of BCLK to Core Frequency	100 MHz Target Frequency	EBL PWRUP Reg[27, 25:22]	LINT[1]	LINT[0]	IGNNE#	A20M#
1/4 (Safe-LLLL)		0 0011	L	L	L	L
1/7	700 MHz	0 1001	H	L	H	L
2/18[2]	900 MHz	1 0000	X	X	X	X
1/4(Safe-HHHH)		0 1100	H	H	H	H

NOTES:

1. The frequency multipliers supported are shown in Table 1; other combinations will not be validated nor supported by Intel. Also, each multiplier is only valid for use on the product of the frequency indicated in Table 1.
2. The Pentium® III Xeon™ processor at 900 MHz with 2MB of L2 cache will ignore the logic states presented to the core/bus ratio pins (A20M#, IGNNE#, LINT0, and LINT1) at the de-assertion of the RESET# signal, and will operate only with a 9:1 core/bus ratio.

Clock multiplying within the processor is provided by the internal PLL, requiring a constant frequency BCLK input. The BCLK frequency ratio cannot be changed dynamically during normal operation or any low power modes. The BCLK frequency ratio for the Pentium® III Xeon™ processor at 700 MHz can be changed when RESET# is active, assuming that all RESET# specifications are met.

See Figure 1 for the timing relationship between the system bus multiplier signals, RESET#, and normal processor operation. Using CRESET# (CMOS Reset) and the timing shown in Figure 1, the circuit in Figure 2 can be used to share these configuration signals. The component used as the multiplexer must not have outputs that drive higher than 2.5V in order to meet the processor's 2.5V tolerant buffer specifications.

As shown in Figure 2, the pull-up resistors between the multiplexer and the processor (1KΩ) force a "safe" ratio into the processor in the event that the processor powers up before the multiplexer and/or core logic. This prevents the processor from ever seeing a ratio higher than the final ratio.

If the multiplexer were powered by $V_{CC2.5}$, a pull-down resistor could be used on CRESET# instead of the four pull-up resistors between the multiplexer and the processor. In this case, the multiplexer must be designed such that the compatibility inputs are truly ignored, as their state is unknown.

In any case, the compatibility inputs to the multiplexer must meet the input specifications of the multiplexer. This may require a level translation before the multiplexer inputs unless the inputs and the signals driving them are already compatible.

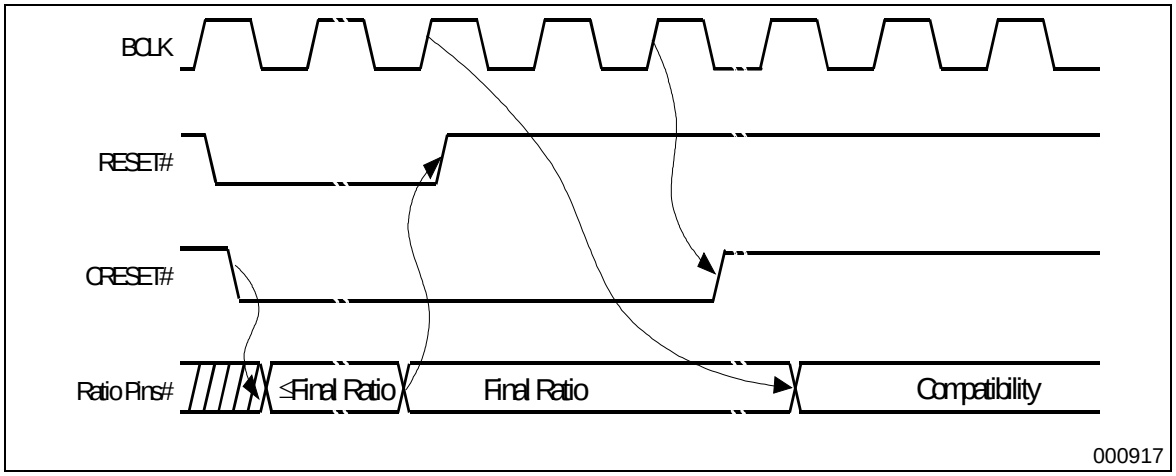

Figure 1. Timing Diagram of Clock Ratio Signals

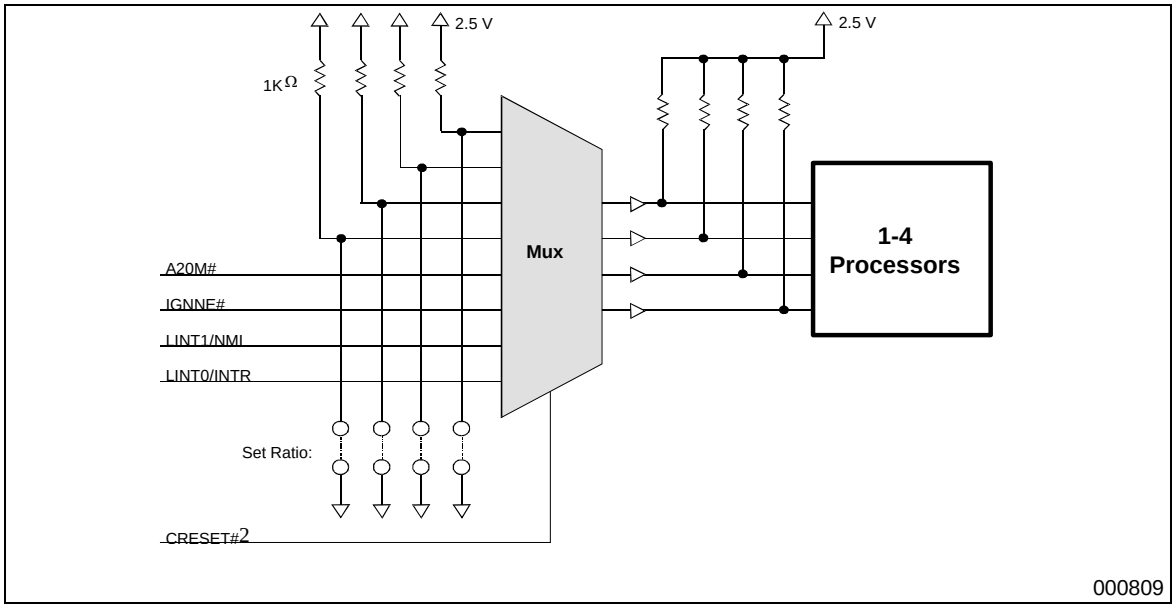

Figure 2. Logical[1] Schematic for Clock Ratio Pin Sharing

NOTES:
1. Signal Integrity issues may require this circuit to be modified
2. Current Intel® 840 chipsets do not implement the CRESET# signal.

3.4.2 MIXING PROCESSORS OF DIFFERENT FREQUENCIES

Mixing components of different internal clock frequencies is not supported and has not been validated by Intel. Operating system support for multi-processing with mixed frequency components should also be considered.

Also, Intel® does not support or validate operation of processors with different cache sizes. Intel® only supports and validates multi-processor configurations where all processors operate with the same system bus and core frequencies and have the same L1 and L2 cache sizes. Since the Pentium® III Xeon™ processor at 900 MHz with 2MB of L2 cache will operate only with a 9:1 core/bus ratio, this processor should only be used in systems containing identical processors. Intel® does not support or validate the mixing of Pentium® III Xeon™ processors at 500 MHz and 550 MHz, Pentium® III Xeon™ processors at 700 MHz and 900 MHz, Pentium® III Xeon™ processors at 600 MHz to 1 GHz with 256KB L2 cache, and Pentium® II Xeon™ processors on the same system bus, regardless of frequency or L2 cache sizes.

3.5 Voltage Identification

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz FMB guidelines enable compatibility with systems originally designed for previous members of the Pentium® II Xeon™ and Pentium® III Xeon™ processor family. To provide power delivery flexibility, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz is available in two different input voltage versions; one version operates at 2.8 Volts and the other at 5 Volts or 12 Volts. As in previous versions of Pentium® II Xeon™ and Pentium® III Xeon™ processors, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz contains five voltage identification (VID) pins, which are used by the processor for OCVR voltage selection in combination with pin A3, which incorporates added functionality for power delivery schemes.

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz incorporates a new pin (A3, HV_EN#) as a method to identify its ability to be powered by a 5V or 12V power supply. The HV_EN# signal is used as a way of differentiating a 5V/12V version processor cartridge from a 2.8V version. HV_EN# is tied to Vss (ground) on the 5V/12V version, and is high impedance (floating) on the 2.8V version. This is a reserved (no connect) pin on previous versions of the Pentium® III Xeon™ processor.

Since the L2 cache is integrated in the core, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz does not require a VID code to specify cache voltage. Pentium® III Xeon™ processor at 700 MHz and 900 MHz FMB designs could be implemented to provide the additional five voltage identification pins for L2 cache voltage selection if Pentium® II Xeon™ processor and previous versions of Pentium® III Xeon™ processor compatibility are desired. These pins may be used to support automatic selection of both power supply voltages as required by a specific cartridge.

VID_CORE[4:0] controls the voltage supply to the processor core and VID_L2[4:0] controls the voltage supply to the L2 cache (in the case of the Pentium® II Xeon™ processor and Pentium® III Xeon™ processor at 500 MHz and 550 MHz). Both core and L2 use the same encoding as shown in Table 2. They are not driven *signals*, but are either an open circuit or a short circuit to V_{SS}. The combination of opens and shorts defines the voltage required by the processor core (and L2 cache for the Pentium® II Xeon™ processor and Pentium® III Xeon™ processor at 500 MHz and 550 MHz), the VID_L2 lines on the Pentium® III Xeon™ processor at 700 MHz and 900 MHz are all left open (pulled high on the baseboard). The VID pins support variations in processor core voltages and L2 cache implementations among processors in the SC330 processor family. Table 2 shows the recommended range of values to support for both the processor core and the L2 cache. A '1' in this table refers to an open pin and '0' refers to a short to ground. The definition provided below is a superset of the definition previously defined for the Pentium® Pro processor (VID4 was not used by the Pentium® Pro processor) and is common to the Pentium® III Xeon™ processor at 700 MHz and 900 MHz (for V_{CC_CORE} only), Pentium® II Xeon™ and previous Pentium® III Xeon™ processors. The power supply must supply the voltage that is requested *or* it must disable itself.

To ensure the system is capable of supporting Pentium® III Xeon™ processor at 700 MHz and 900 MHz, Pentium® II Xeon™ processors and previous Pentium® III Xeon™ processors, a system should support those voltages indicated with a bold **x** in Table 2.

Table 2. FMB Core and L2 Voltage Identification Definition [1, 2]

Processor pins							
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**Vcc**	**Core**[3]	**L2**[3,5]
00110b – 01111b					Reserved **2**		
0	0	1	0	1	**1.80**	**X**	**X**
0	0	1	0	0	**1.85**	**X**	**X**
0	0	0	1	1	**1.90**	**X**	**X**
0	0	0	1	0	**1.95**	**X**	**X**
0	0	0	0	1	**2.00**	**X**	**X**
0	0	0	0	0	**2.05**	**X**	**X**
1	1	1	1	0	**2.1**	**X**	**X**
1	1	1	0	1	**2.2**		**X**
1	1	1	0	0	**2.3**		**X**
1	1	0	1	1	**2.4**		**X**
1	1	0	1	0	**2.5**		**X**
1	1	0	0	1	**2.6**		**X**
1	1	0	0	0	**2.7**		**X**
1	0	1	1	1	**2.8**[6]	**X**	**X**
1	0	1	1	0	**2.9**		
1	0	1	0	1	**3.0**		
1	0	1	0	0	**3.1**		
1	0	0	1	1	**3.2**		
1	0	0	1	0	**3.3**		
1	0	0	0	1	**3.4**		
1	0	0	0	0	**3.5**		
1	1	1	1	1	**No core**[7]		**Core** [4]

NOTES:

1. 0 = processor pin connected to VSS, 1 = Open on processor; may be pulled up to TTL V_{IH} on baseboard. See the *VRM 8.3 DC–DC Converter Design Guidelines* and/or the *VRM 8.3 DC–DC Converter Design Guidelines*.
2. VRM output should be disabled for VCC_{CORE} values less than 1.80V.
3. **X =** Required.
4. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz does not require an L2 voltage supply. The VCC_L2 and L2 VID lines are ”open” on the processor cartridge.
5. Required for FMB compatibility, not necessary for the Pentium® III Xeon™ processor at 700 MHz and 900 MHz.
6. This VID setting can be used in combination with HV_EN# pin (A3) for differentiating 2.8V version from 5V/12V version cartridges.
7. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz incorporates an integrated L2 cache, which eliminates the requirement of a VRM to power the L2 cache. Legacy systems provide L2 VRMs for Pentium® II Xeon™ processor or Pentium® III Xeon™ processor at 500 MHz and 550 MHz support. In these legacy systems, the Pentium® III Xeon™ processor at 700 MHz and 900 MHz will pass VID[4:0] = 11111 to the L2 VRM, instructing it to disable its output voltage. Certain VRM designs will also de-assert their VRM_PWRGD output. VRM_PWRGD signals are generally used to derive a SYS_PWRGD signal. With VRM_PWRGD de-asserted, the SYS_PWRGD is likely to be de-asserted, and the system will not boot. OEMs should examine legacy system and VRM designs intended to support the Pentium® III Xeon™ processor at 700 MHz and 900 MHz to ensure that there is no adverse impact to SYS_PWRGD derivation. See Figures 41 and 42.

The VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator only if required by the regulator or external logic monitoring the VID[4:0] signals. The power source chosen to drive/pull up VIDs must be guaranteed to be stable whenever the supply to the voltage regulator is non-zero and the OCVR is enabled. An invalid VID while the output is coming up could lead to and incorrect voltage above VCC_{CORE} max. This will prevent the possibility of the processor supply going above VCC_{CORE} in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line

pull-ups. A resistor of greater than or equal to 10KΩ may be used to connect the VID signals to the converter input. See the *VRM 8.3 DC–DC Converter Design Guidelines* for further information.

3.6 System Bus Unused Pins and Test Pins

Unless otherwise specified, All RESERVED_XXX pins must remain unconnected. Note that pins that are newly marked as RESERVED in this document may be tied to a power rail in existing baseboards. See Chapter 7 for a pin listing of the processor edge connector for the location of each reserved pin.

NOTE: Pentium® III Xeon™ processor at 700 MHz and 900 MHz pin A11 (RESERVED_A11) may be pulled-down to VSS for legacy compatibility.

The TEST_2.5_A62 pin must be connected to 2.5 Volts via a pull-up resistor between 1K and 10KΩ.

For the Pentium® III Xeon™ processor at 700 MHz and 900 MHz 5V/12V version only, it is recommended that pins that were previously specified as TEST_VCC_CORE_XX (now specified TEST_2.5_XX), be connected to the VCC_2.5 supply through separate 10KΩ resistors on the baseboard. However, there will be no damage to cartridges if existing platforms provide 2.8 Volts to the pull-up resistors. All TEST_VTT pins must be connected to the Vtt supply through individual 150Ω resistors. All TEST_VSS pins must be connected individually to the Vss supply through individual 1KΩ resistors.

PICCLK must always be driven with a valid clock input. and the PICD[1:0] lines must be pulled-up to 2.5V even when the APIC will not be used. A separate pull-up resistor to 2.5V (keep trace short) is required for each PICD line.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused AGTL+ inputs should be left as no connects; AGTL+ termination on the processor provides a high level. Unused active low CMOS inputs should be connected to 2.5V with a ~10KΩ resistor. Unused active high CMOS inputs should be connected to ground (V_{SS}). Unused outputs may be left unconnected. A resistor must be used when tying bi-directional signals to power or ground. When tying *any* signal to power or ground, a resistor will also allow for system testability. For correct operation when using a logic analyzer interface, refer to Chapter 8 for design considerations.

3.7 System Bus Signal Groups

In order to simplify the following discussion, the system bus signals have been combined into groups by buffer type. *All system bus outputs should be treated as open drain* and requires a high-level source provided externally by the termination or pull-up resistor.

AGTL+ input signals have differential input buffers, which use 2/3 V_{TT} as a reference level. AGTL+ output signals require termination to 1.5V. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. The AGTL+ buffers employ active negation for one clock cycle after assertion to improve rise times.

The CMOS, Clock, APIC, and TAP inputs can each be driven from ground to 2.5V. The CMOS, APIC, and TAP outputs are open drain and should be pulled high to 2.5V. This ensures correct operation for the processor. Timings are specified into the load resistance as defined in the AC timing tables. See Chapter 8 for design considerations for debug equipment.

The SMBus signals should be driven using standard 3.3V CMOS logic levels.

Table 3. Processor pin Groups

Group Name	Signals
AGTL+ Input	BPRI#, BR[3:1]#[1], DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[35:03]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[1], D[63:00]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGD[2], SMI#, SLP#[2], STPCLK#
CMOS Output	FERR#, IERR#, THERMTRIP#[2]
System Bus Clock	BCLK
APIC Clock	PICCLK
APIC I/O[3]	PICD[1:0]
TAP Input[3]	TCK, TDI, TMS, TRST#
TAP Output[3]	TDO
SMBus Interface	SMBDAT, SMBCLK, SMBALERT#, WP
Power/Other[4]	VCC_CORE, Vcc_TAP, Vcc_SMB, VTT, VSS, RESERVED_XXX, SA[2:1], SELFSB[0:1], OCVR_EN, OCVR_OK, VIN_SENSE, CORE_AN_VSENSE, HV_EN#

NOTES:

1. The BR0# pin is the only BREQ# signal that is bi-directional. The internal BREQ# signals are mapped onto BR# pins based on a processor's agent ID. See Chapter 10 for more information.
2. For information on these signals, see Chapter 10.
3. These signals are specified for 2.5V operation.
4. V_{TT} is used for the AGTL+ termination.
   V_{SS} is system ground.
   V_{CC_TAP} is the TAP supply.
   V_{CC_SMB} is the SM bus supply.
   Reserved pins must be left unconnected. Do not connect to each other.

3.7.2 ASYNCHRONOUS VS. SYNCHRONOUS FOR SYSTEM BUS SIGNALS

All AGTL+ signals are synchronous to BCLK. All of the CMOS, Clock, APIC, and TAP signals can be applied asynchronously to BCLK.

All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK. All SMBus signals are synchronous to SMBCLK. TCK and SMBCLK can be asynchronous to all other clocks.

3.8 Access Port (TAP) Connection

Depending on the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor be first in the TAP chain and followed by any other components within the system. A voltage translation buffer should be used to drive the next device in the chain unless a component is used that is capable of accepting a 2.5V input. Similar considerations must be made for TCK, TMS, and TRST#. Multiple copies of each TAP signal may be required if multiple voltage levels are needed within a system.

NOTE

TDI is pulled up to V_{CCTAP} with ~150Ω on the processor cartridge. An open drain signal driving this pin must be able to deliver sufficient current to drive the signal low. Also, no resistor should exist in the system design on this pin, as it would be in parallel with this resistor.

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A Debug Port is described in Chapter 8. The Debug Port must be placed at the start and end of the TAP chain with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. In an MP system, be cautious when including an empty SC330 connector in the scan chain. All connectors in the scan chain must have a processor or termination card installed to complete the chain between TDI and TDO or the system must support a method to bypass the empty connectors. SC330 terminator substrates should tie TDI directly to TDO. (See Chapter 8 for more details.)

3.9 Maximum Ratings

Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	3
V_{CC_CORE}	Supply voltage with respect to V_{SS} seen at the input of the OCVR	–0.5	Operating voltage + 1.0	V	1,2
V_{SMBus}	Any processor SM supply voltage with respect to V_{SS}	-0.3	Operating voltage + 1.0	V	
V_{CCTAP}	Any processor TAP supply voltage with respect to V_{SS}	-0.3	3.3	V	1
V_{inGTL}	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.3	+ 1.65	V	
V_{inCMOS}	CMOS & APIC buffer DC input voltage with respect to V_{SS}	–0.3	3.3	V	
$V_{inSMBus}$	SMBus buffer DC input voltage with respect to V_{SS}	-0.1	7.0	V	
I_{PWR_EN}	Max PWR_EN[1:0] pin current		100	mA	

NOTES:

1. Operating voltage is the voltage to which the component is designed to operate. See Table 5.
2. V_{CC_CORE} is the voltage input seen at the input of the OCVR device which may be 2.8V for one product version or 5V (or 12V) for another product version.
3. Please contact Intel® for storage requirements in excess of one year.

3.10 Processor DC Specifications

The voltage and current specifications provided in Table 5 and Table 6 are defined at the processor edge fingers. The processor signal DC specifications in Tables 7, 8 and 9 are defined at the processor core. Each signal trace between the processor edge finger and the processor core carries a small amount of current and has a finite resistance. The current produces a voltage drop between the processor edge finger and the core. Simulations should therefore be run versus these specifications to the processor core.

See Chapter 1 for the processor edge finger signal definitions and Table 3 for the signal grouping.

Most of the signals on the processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to V_{TT}. The DC specifications for these signals are listed in Table 7.

To ease connection with other devices, the Clock, CMOS, APIC, SMBus and TAP signals are designed to interface at non-AGTL+ levels. The processor contains a voltage clamp device on the cartridge substrate between the core and edge fingers. This device “clamps” the 2.5V level CMOS, TAP, and APIC signals to 1.5V levels, which helps reduce overshoot levels at the processor core. All CMOS, TAP, Clock, and APIC signals interface with the voltage clamp, with the exception of BCLK, PICCLK and PWRGOOD. The DC specifications for these pins are listed in Table 8 and Table 9.

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NOTE

Unless otherwise noted, each specification applies to all Pentium® III Xeon™ processor at 700 MHz and 900 MHz. Where differences exist between processors, look for the table entries identified by "**FMB**" in order to design a Flexible Mother Board (FMB) capable of accepting the Pentium® III Xeon™ processor at 700 MHz and 900 MHz as well as the Pentium® II Xeon™ processor and previous versions of the Pentium® III Xeon™ processor.

Specifications are only valid while meeting specifications for case temperature, clock frequency and input voltages. Care should be taken to read all notes associated with each parameter.

Table 5. Voltage Specifications [1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCCORE} **(2.8V version)**	V_{CC} for 2.8V version processor		2.8		V	2,3,4
V_{CCCORE} (2.8V version) Tolerance, Static	Processor core voltage static tolerance at edge fingers	-0.085		0.085	V	6
V_{CCCORE} (2.8V version) Tolerance, Transient	Processor core voltage transient tolerance at edge fingers	-0.130		0.130	V	6
V_{CCCORE} **(5V/12Vversion)**	V_{CC} for 5V/12V version processor	4.75 11.4	5.0 12.0	5.25 12.6	V	4,6,7,8
V_{TT}	AGTL+ Bus Termination voltage	1.365	1.50	1.635	V	1.5V ±9%, 5
V_{CC_SMB}	SMBus supply voltage	3.135	3.3	3.465	V	3.3V ±5%, 9
V_{CC_TAP}	TAP supply voltage	2.375	2.50	2.625	V	2.5V ±5%

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes. "FMB" is a suggested design guideline for flexible motherboard design. Failure to adhere to the FMB guidelines may impact system upgradeability.
2. V_{CC_CORE} supplies the processor core. FMB refers to the range of set points for all Pentium® III Xeon™ processors.
3. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 3.5 for more information. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz does not require a separate V_{CC_L2} voltage.
4. Use the Typical Voltage specification along with the tolerance specifications to provide correct voltage regulation to the processor.
5. Vtt is 1.5 +/- 9**%** (AC & DC) when the measurement is bandwidth limited to 20 MHz and measured at the SC 330 connector pin on the back (solder tail) side of the baseboard. This parameter is measured at the processor edge fingers. The SC330 connector is specified to have a pin self-inductance of 6.0 nH maximum, a pin-to-pin capacitance of 2 pF (maximum at 1 MHz), and an average contact resistance over the 6 V_{TT} pins of 15 mΩ maximum Z.
6. These are the tolerance requirements, across a 20 MHz bandwidth, **at the processor edge fingers.** The requirements at the processor edge fingers account for voltage drops (and impedance discontinuities) at the processor edge fingers and to the processor core. Voltage must return to within the static voltage specification within 100 us after the transient event. The SC330 connector is specified to have a pin self-inductance of 6.0 nH maximum, a pin-to-pin capacitance of 2 pF (maximum at 1 MHz), and an average contact resistance of 15mΩ maximum in order to function with the Intel® specified voltage regulator module (VRM 8.3). Contact Intel® for testing details of these parameters. Not 100% tested. Specified by design characterization.
7. Pentium® III Xeon™ processor at 700 MHz and 900 MHz 5V/12V version is to be operated by 5V or 12V, and is available for new designs that do not provide compatibility with previous versions of the Pentium® III Xeon™ processor.
8. 5V and 12V are specified at ±5%. This parameter includes both static (noise & ripple) and transient tolerances at the edge fingers.
9. Vcc_SMB must be connected to 3.3V power supply (even if the SMBus features are not used) in order for the processor to function properly.

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Table 6. Current Specifications [1,10]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Icc_core @ 2.74V VCC_CORE	700 MHz 900 MHz			13.9 17.0	A	2
Icc_core @ 4.75V VCC_CORE	700 MHz 900 MHz			8.4 10.3	A	2
Icc_core @ 11.4V VCC_CORE	700 MHz 900 MHz			3.5 4.3	A	2
Icc_core FMB	2.74V 4.75V 11.4V			19.0 11.0 5.0	A	1, 2, 10
IV_{TT}	Termination voltage supply current	0	0.3	1.2	A	4
I_{SGnt}	I_{CC} Stop Grant for processor core 2.8V 5.0V 12.0V	-	-	10.0 5.6 2.3	A	3,5
I_{CCSLP}	I_{CC} Sleep for processor core 2.8V 5.0V 12.0V	-	-	10.0 5.6 2.3	A	3
$DIcc_{CORE}/dt$	Current slew rate			10	A/µs	6,7
DI_{CCVTT}/dt	Termination current slew rate			5	A/µs	7
I_{CCTAP}	I_{CC} for TAP power supply			100	mA	
$I_{CCSMBus}$	I_{CC} for SMBus power supply		3	22.5	mA	8

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes. “FMB” is a suggested design guideline for flexible motherboard design.
2. Vcc_core/Icc_core supplies the processor core, integrated L2 cache and OCVR.
3. Max I_{CC} measurements are measured at V_{CC} minimum voltage (at VRM or system power supply output) under maximum signal loading conditions.
4. This is the current required for a single processor. A similar current is drawn through the termination resistors of each load on the AGTL+ bus. V_{TT} is decoupled on the SC330 cartridge such that negative current flow due to the active pull-up to V_{CC_CORE} in the processor will not be seen at the processor fingers.
5. The current specified is also for AutoHALT state.
6. Maximum values are specified by design/characterization at nominal V_{CC} and at the SC330 edge fingers.
7. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.

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8. VCC_SMB must be connected to 3.3V power supply (even if the SMBus features are not used) in order for the processor to function properly.
9. A disabled processor OCVR draws approximately 46 mA at 2.8V V_{CC_CORE} from the motherboard VRM. If your system needs to maintain VRM regulation with a disabled processor (OCVR_EN inactive), the VRM output minimum load specification should be 46 mA or less.
10. The FMB specification is applicable to 2.8V OCVR processors where a VRM is used as the power source.

Table 7. AGTL+ Signal Groups, DC Specifications at the processor Core

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.150	0.9	V	4,7
V_{IH}	Input High Voltage	1.15V	V_{TT}	V	1,4,7
R_{ON_N}	nMOS On Resistance		12.5	Ohm	5, 6
R_{ON_P}	pMOS On Resistance		85	Ohm	5, 8
$V_{OH_{TS}}$	Output High Voltage Tri-state		V_{TT}	V	1, 4
I_L	Leakage current for the Inputs, Outputs and I/O		±15	µA	2, 3

NOTES:

1. Processor core parameter correlated into a 25Ω resistor to a V_{TT} of 1.5V.
2. $0 \leq Vin \leq 1.5 +3\%$.
3. $0 \leq Vout \leq 2 +5\%$.
4. The processor core drives high for only one clock cycle. It then drives low or tri-states its outputs. V_{TT} is specified in Table 5.
5. Not 100% tested. Specified by design characterization.
6. This R_{ON} specification corresponds to a V_{OL_MAX} of 0.5V when taken into an effective 25Ω load to V_{TT} of 1.5V.
7. Vil/Vih are not guaranteed with respect to AC parameters.
8. Specified under no load conditions at an I-V operating point of zero current and V=VTT conditions.

Table 8. CMOS, TAP, Clock and APIC Signal Groups, DC Specifications at the processor edge fingers

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.150	0.7	V	6
V_{IH}	Input High Voltage	1.7	2.625	V	2.5V + 5% maximum, 7
(PICCLK & PWRGD only)		2.0	2.625	V	2.5V + 5% maximum, 4, 5
V_{OL}	Output Low Voltage		0.5	V	Parameter measured at 14mA
(APIC only)			0.550	V	Parameter measured at 20mA
V_{OH}	Output High Voltage		2.625	V	All outputs are open-drain to 2.5V + 5%
I_{LI}	Input Leakage Current		±100	µA	1
I_{LO}	Output Leakage Current		±100	µA	2
Con	I/O Pin Capacitance		25	pF	3

NOTES:

1. $0 \leq V_{IN} \leq 2.625V$.
2. $0 \leq V_{OUT} \leq 2.625V$.
3. Total capacitance of processor core and voltage clamp device. Does not include cartridge trace capacitance. Applies to all CMOS, TAP, Clock, and APIC signals except BCLK, PICCLK and PWRGOOD.
4. This parameter applies to PICCLK.
5. This parameter applies to PWRDG.

6. Maximum V_{IL} at the processor core pin is specified as 2/3 V_{TT} – 0.2V.
7. Minimum V_{IH} at the processor core pin is specified as 2/3 V_{TT} + 0.2V.

Table 9. SMBus Signal Group, DC Specifications at the processor edge fingers

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	0.3 x Vcc_{SMB}	V	
V_{IH}	Input High Voltage	0.7 x Vcc_{SMB}	3.465	V	3.3V + 5% maximum
V_{OL}	Output Low Voltage		0.4	V	
I_{OL}	Output Low Current		3	mA	Except SMBALERT#
I_{OL2}	Output Low Current	6		mA	SMBALERT# 1
I_{LI}	Input Leakage Current		10	µA	
I_{LO}	Output Leakage Current		10	µA	

NOTES:

1. SMBALERT# is an open drain signal.

Table 10. OCVR Control Signals, DC Specifications at the processor edge fingers

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL} OCVR_EN	Input Low Voltage		0.8	V	2, 3
V_{IH} OCVR_EN	Input High Voltage	2.0		V	2, 3
V_{OL} OCVR_OK	Output Low Voltage		0.4	V	-1.5mA max
V_{OH} OCVR_OK	Output High Voltage	-	-	V	1

NOTES:

1. Driver configured as open drain connected to 3.3V (Vcc_SMB) through a 10KΩ resistor.
2. Vih_max (absolute) = 5.25 VDC when the OCVR is powered.
3. If the OCVR on the processor is not operating, such as at initial system power up or if there is no power input to the processor, the input should be driven in such a way that no more than 20 mA can flow into the input (assuming it is connected to ground). This is equivalent to using a 270Ω or higher pull-up resistor tied to a typical 5V supply as the only source for driving the input high.

3.11 AGTL+ System Bus Specifications

Table 11 below lists parameters controlled within the processor to be taken into consideration. A reference voltage (V_{REF}), derived on the processor cartridge from V_{TT}, is used by the input buffers to determine the valid high and low levels. V_{REF} should be set to the same level for other AGTL+ logic using a voltage divider on the baseboard. It is important that the baseboard impedance be held as tight as possible and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. See Layout Guidelines (section 2.4) for impedance recommendations.

Table 11 Internal Parameters for the AGTL+ Bus

Symbol	Parameter	Min	Typ	Max	Units	Notes
R_{TT}	Termination Resistor		150		Ohm	1
V_{REF}	Bus Reference Voltage	0.733 V_{TT} - 100mV	0.733 V_{TT}	0.733 V_{TT} + 100mV	V	2

NOTES:

1. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz contains on-die termination resistors with +/-10% tolerance.
2. V_{REF} is generated on the processor substrate.

3.12 System Bus AC Specifications

The system bus timings specified in this section are defined at the processor core pins unless otherwise noted. Timings are tested at the processor core during manufacturing.

NOTE: Timing specifications T45-T49 are reserved for future use.

All system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to 2/3 V_{TT} for both '0' and '1' logic levels unless otherwise specified.

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Table 12. System Bus AC Specifications (Clock) at the processor Core Pins [1, 2, 3]

T#	Parameter	Min	Nom	Max	Unit	Figure	Notes
	System Bus Frequency	90		100.2	MHz		4
T1:	BCLK Period	10.0		11.11	nS	4	4, 5, 9
T2:	BCLK Period Stability			±150	pS		6, 7, 9
T3:	BCLK High Time	2.5			nS	4, 12	@>2.0V, 9
T4:	BCLK Low Time	2.5			nS	4, 12	@<0.5V, 9
T5:	BCLK Rise Time	0.50		1.5	nS	4, 12	0.5V–2.0V 8, 9
T6:	BCLK Fall Time	0.50		1.5	nS	4, 12	2.0V–0.5V 8, 9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1V at the processor core pins.
4. The internal core clock frequency is derived from the processor system bus clock. The system bus clock to core clock ratio is determined during initialization as described in 6.2. Table 1 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 nS tolerance for clock driver variation. See the *CK98WS Clock Synthesizer/Driver Specification* for further information.
6. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the rising edges of adjacent BCLKs crossing 1.25V at the processor core pin. The jitter present must be accounted for as a component of BCLK timing skew between devices.
7. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the *CK98WS Clock Synthesizer/Driver Specification* for further details.
8. Not 100% tested. Specified by design characterization as a clock driver requirement.
9. This frequency range is specified by the *CK98WS Clock Synthesizer/Driver Specification*, and is guaranteed by design only (not tested).

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Table 14. AGTL+ Signal Group, System Bus AC Specifications at the Core Pins[1]

R_L = 25 ohms Terminated to 1.5V						
T#	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
T7:	AGTL+ Output Valid Delay	-0.07	2.65	nS	Figure 5	2, 8
T8:	AGTL+ Input Setup Time	1.20		nS	Figure 6	3, 4, 6, 8
T9:	AGTL+ Input Hold Time	0.62		nS	Figure 6	5
T10:	RESET# Pulse Width	1.00		mS	Figure 8	5

NOTES:

1. These specifications are tested during manufacturing.
2. Valid delay timings for these signals at the processor core assume a 25Ω termination to 1.5V.
3. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
4. RESET# can be asserted (active) asynchronously, but must be de-asserted synchronously to the bus clock.
5. After the bus ratio on A20M#, IGNNE# and LINT[1:0] are stable, V_{CC_CORE}, and BCLK are within specification, and PWRGD is asserted. See Figure 8, 40 & 41.
6. Specification is for a minimum 0.40V swing from V_{REF} - 200 mV to V_{REF} + 200 mV. This assumes an edge rate of .3V/ns.
7. Parameter specified with an AGTL+ signal crossing point of 1.0V with respect to BCLK voltage reference.
8. Parameter specified with an AGTL+ signal crossing point of 1.1V with respect to BCLK voltage reference.

Table 15. CMOS, TAP, Clock and APIC Signal Groups, AC Specifications at the processor Core [1, 2]

T#	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
T14:	CMOS Input Pulse Width, except PWRGD and LINT[1:0]	2		BCLKs	Figure 5	Active and Inactive states
T14B:	LINT[1:0] Input Pulse Width	6		BCLKs	Figure 5	3
T15:	PWRGD Inactive Pulse Width	10		BCLKs	Figure 8	4

NOTES:

1. These specifications are tested during manufacturing.
2. Valid delay timings for these signals are specified into 100Ω to 2.5V.
3. When driven inactive or after V_{CC_CORE}, and BCLK become stable. PWRGD must remain below V_{IL_MAX} from Table 8 until all the voltage planes meet the voltage tolerance specifications in Table 5 and BCLK has met the BCLK AC specifications in Table 11 for at least 10 clock cycles. PWRGD must rise glitch-free and monotonically to 2.5V.
4. If the BCLK signal meets its AC specification within 150ns of turning on then the PWRGD Inactive Pulse Width specification is waived and BCLK may start after PWRGD is asserted. PWRGD must still remain below V_{IL_MAX} until all the voltage planes meet the voltage tolerance specifications.

Table 16. System Bus AC Specifications (Reset Conditions[1])

T#	Parameter	Min	Max	Unit	Figure	Notes
T16:	Reset Configuration Signals (A[14:05]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	Figure 8	Before de-assertion of RESET
T17:	Reset Configuration Signals (A[14:05]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	Figure 8	After clock that de-asserts RESET#
T18:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time	1		mS	Figure 8	Before de-assertion of RESET#
T19:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time		5	BCLKs	Figure 8	After assertion of RESET# [1]
T20:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time	2	20	BCLKs	Figure 8 Figure 9	After clock that de-asserts RESET#

NOTES:

1. For a Reset, the clock ratio defined by these signals must be a safe value (their final or lower multiplier) within this delay unless PWRGD is being driven inactive.

Table 17. System Bus AC Specifications (APIC Clock and APIC I/O) at the processor Core Pins [1]

T#	Parameter	Min	Max	Unit	Figure	Notes
T21:	PICCLK Frequency	2.0	33.3	MHz		
T22:	PICCLK Period	30.0	500.0	nS	Figure 3	
T23:	PICCLK High Time	12.0		nS	Figure 3	
T24:	PICCLK Low Time	12.0		nS	Figure 3	
T25:	PICCLK Rise Time	0.25	3.0	nS	Figure 3	5
T26:	PICCLK Fall Time	0.25	3.0	nS	Figure 3	5
T27:	PICD[1:0] Setup Time	5.0		nS	Figure 6	2
T28:	PICD[1:0] Hold Time	2.5		nS	Figure 6	2
T29A:	PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	nS	Figure 5	2,3,4
T29B:	PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0	nS	Figure 5	2,3,4

NOTES:

1. These specifications are tested during manufacturing.
2. Referenced to PICCLK rising edge.
3. For open drain signals, valid delay is synonymous with float delay.
4. Valid delay timings for these signals are specified into a 150Ω resistor to 2.5V.
5. This data is specified at the processor core.

Table 18. System Bus AC Specifications (TAP Connection) at the processor Core [1]

T#	Parameter	Min	Max	Unit	Figure	Notes
T30:	TCK Frequency		16.667	MHz		
T31:	TCK Period	60.0		nS	Figure 3	
T32:	TCK High Time	25.0		nS	Figure 3	@1.7V 2
T33:	TCK Low Time	25.0		nS	Figure 3	@0.7V 2
T34:	TCK Rise Time		5.0	nS	Figure 3	(0.7V–1.7V) 2, 3
T35:	TCK Fall Time		5.0	nS	Figure 3	(1.7V–0.7V) 2, 3
T36:	TRST# Pulse Width	40.0		nS	Figure 10	(Asynchronous) 2
T37:	TDI, TMS Setup Time	5.0		nS	Figure 9	4
T38:	TDI, TMS Hold Time	14.0		nS	Figure 9	4
T39:	TDO Valid Delay	1.0	10.0	nS	Figure 9	5, 6
T40:	TDO Float Delay		25.0	nS	Figure 9	2, 5, 6
T41:	All Non-Test Outputs Valid Delay	2.0	25.0	nS	Figure 9	5, 7, 8
T42:	All Non-Test Inputs Setup Time		25.0	nS	Figure 9	2, 5, 7, 8
T43:	All Non-Test Inputs Setup Time	5.0		nS	Figure 9	4, 7, 8
T44:	All Non-Test Inputs Hold Time	13.0		nS	Figure 9	4, 7, 8

NOTES:

1. Unless otherwise noted, these specifications are tested during manufacturing.
2. Not 100% tested. Specified by design characterization.
3. 1 nS can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. Valid delay timing for this signal is specified to 2.5V.
7. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to TAP operations.
8. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.

ELECTRICAL SPECIFICATIONS

Table 19. SMBus Signal Group, AC Specifications at the Edge Fingers

T#	Parameter	Min	Max	Unit	Figure	Notes
T50:	SMBCLK Frequency		100	KHz		
T51:	SMBCLK Period	10		uS	Figure 4	
T52:	SMBCLK High Time	4.0		uS	Figure 4	
T53:	SMBCLK Low Time	4.7		uS	Figure 4	
T54:	SMBCLK Rise Time		1.0	uS	Figure 4	
T55:	SMBCLK Fall Time		0.3	uS	Figure 4	
T56:	SMBus Output Valid Delay		1.0	uS	Figure 5	
T57:	SMBus Input Setup Time	250		nS	Figure 6	
T58:	SMBus Input Hold Time	0		nS	Figure 6	
T59:	Bus Free Time	4.7		uS		1

NOTES:

1. Minimum time allowed between request cycles.

Table 20. OCVR Control Signals, AC Specifications at the Edge Fingers

Parameter	Min	Max	Unit	Notes
OCVR_EN High Time	10.0		uS	
OCVR_EN Rise Time		10.0	uS	
OCVR_EN Fall Time		10.0	uS	
OCVR_OK Rise Time		30.0	nS	1
OCVR_OK Fall Time		10.0	nS	1

NOTES:

1. OCVR_OK output with 5pf load and 10KΩ external pull-up to 3.3V.

Figure 3 through Figure 10 are to be used in conjunction with the DC specification and AC timings tables.

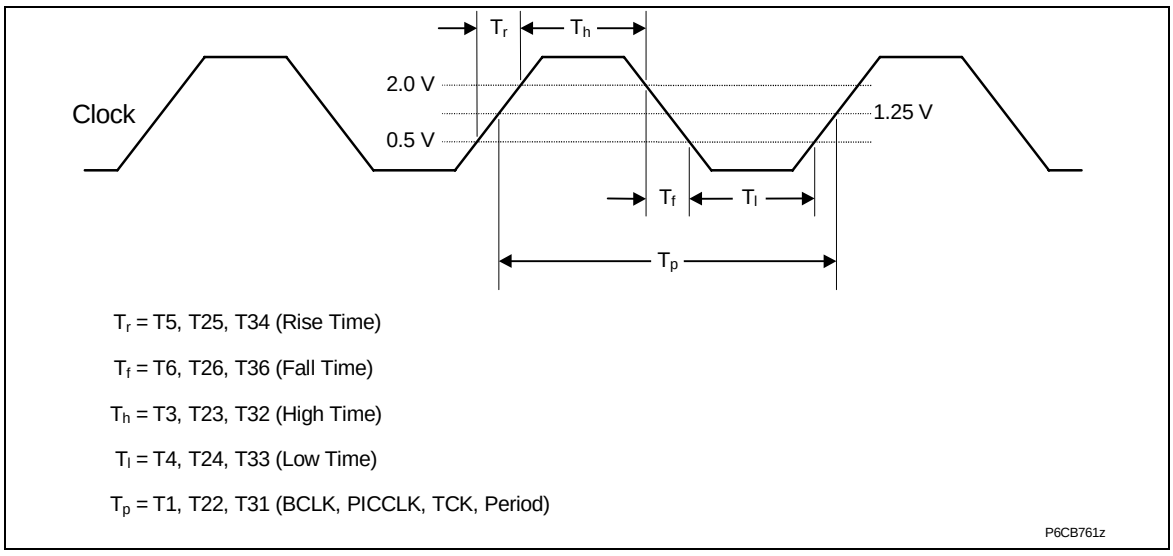


Figure 3. BCLK, PICCLK, TCK Generic Clock Waveform

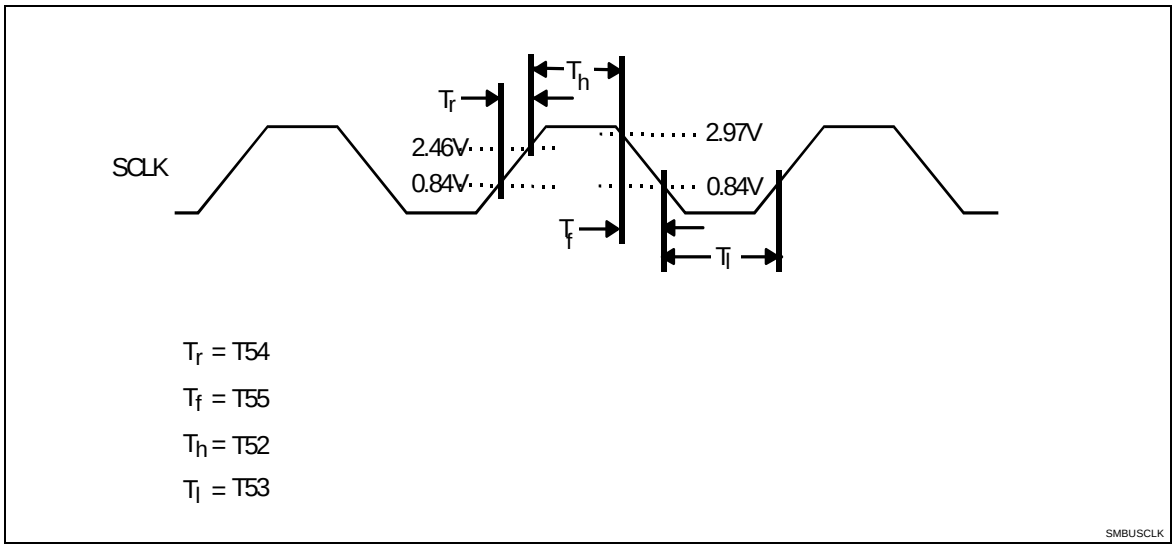


Figure 4. SMBCLK Clock Waveform

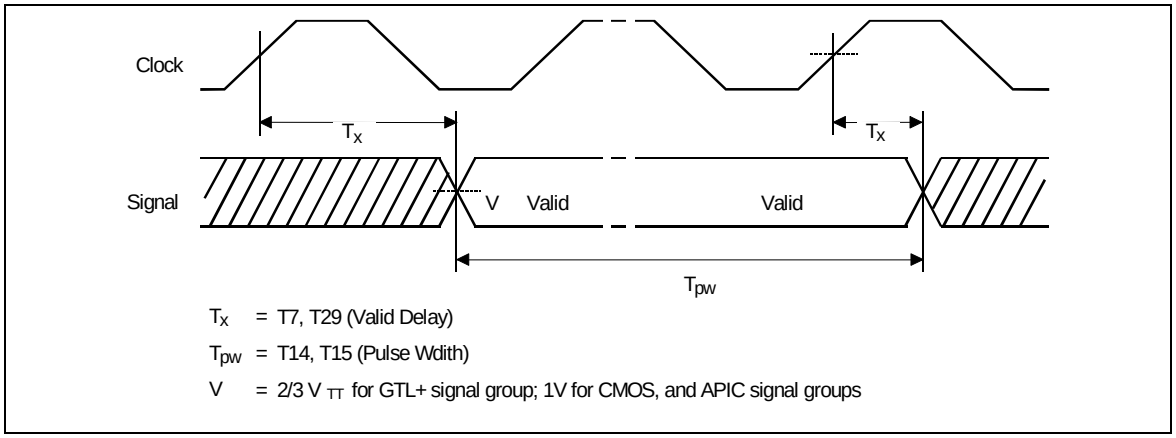


Figure 5. Valid Delay Timings

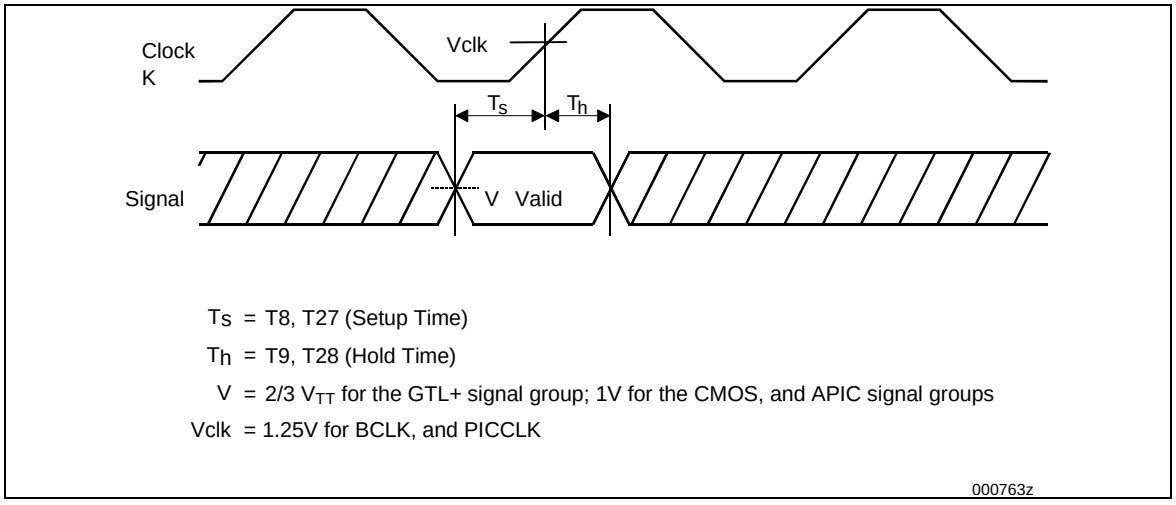
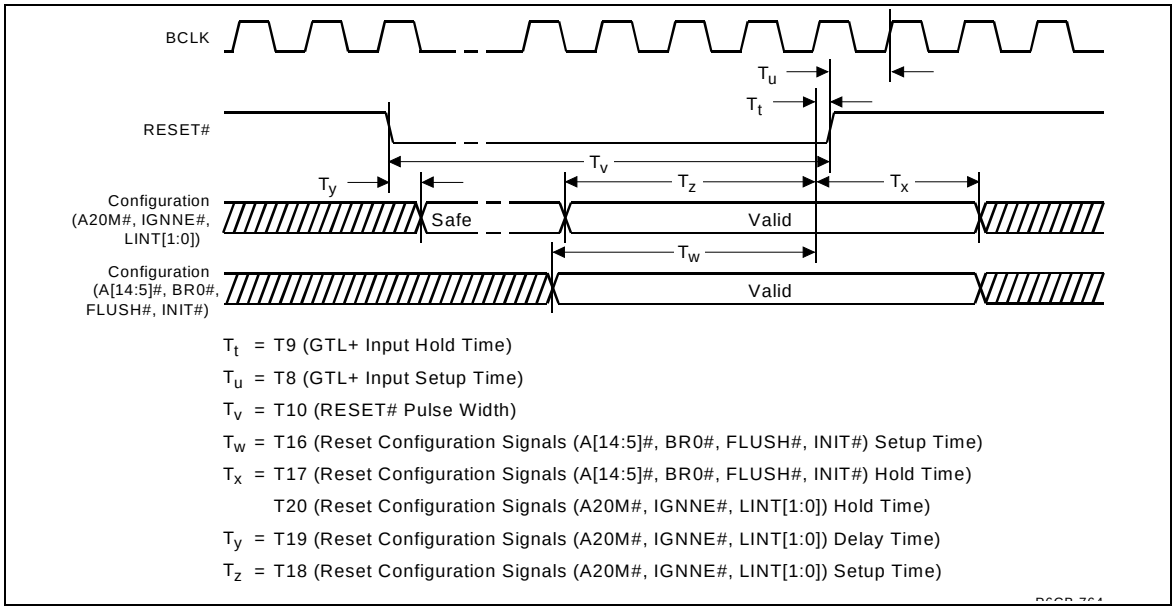


Figure 6. Setup and Hold Timings



T_t = T9 (GTL+ Input Hold Time)

T_u = T8 (GTL+ Input Setup Time)

T_v = T10 (RESET# Pulse Width)

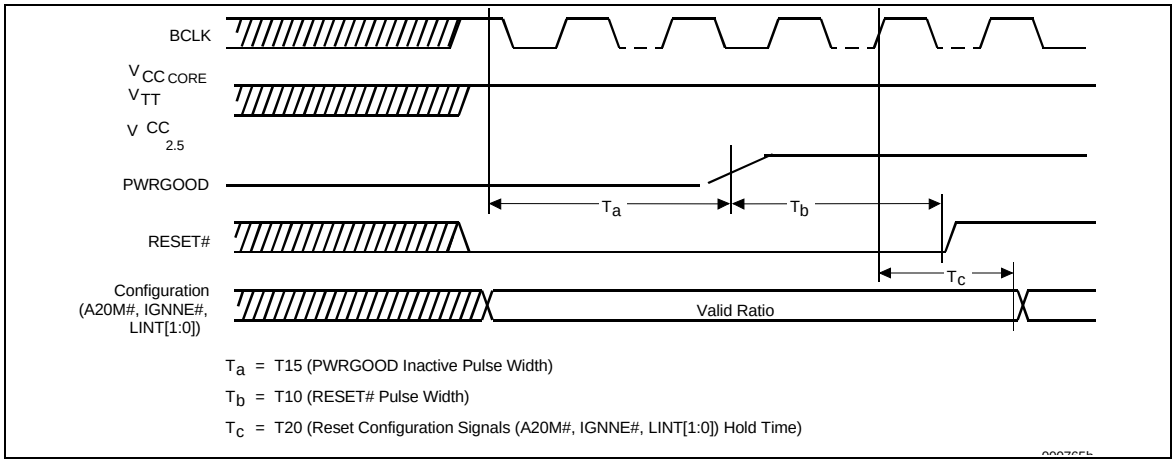
T_w = T16 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time)

T_x = T17 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time)
T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time)

T_y = T19 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time)

T_z = T18 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time)

Figure 7. System Bus Reset and Configuration Timings



T_a = T15 (PWRGOOD Inactive Pulse Width)

T_b = T10 (RESET# Pulse Width)

T_c = T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time)

Figure 8. Power-On Reset and Configuration Timings

ELECTRICAL SPECIFICATIONS

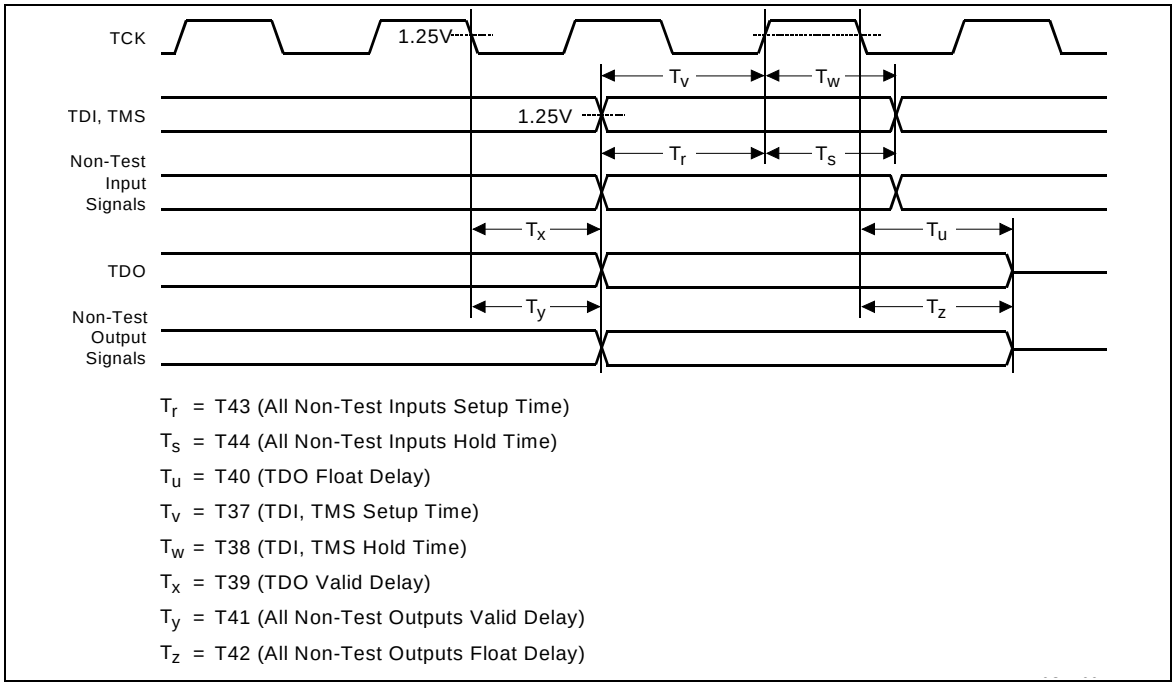


Figure 9. Test Timings (Boundary Scan)

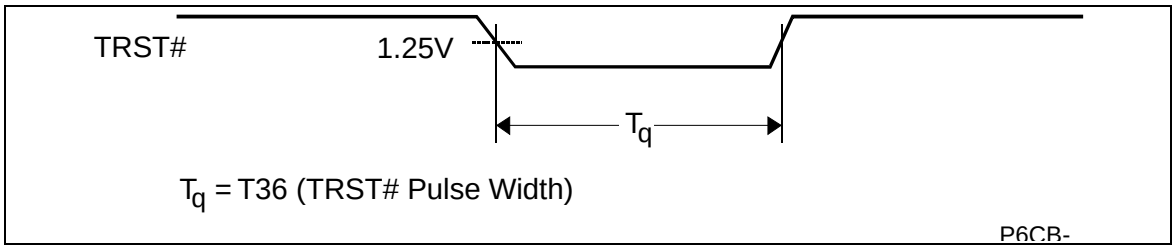


Figure 10. Test Reset Timings

4. Signal Quality

Signals driven on the system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long-term reliability of the component. Specifications are provided for simulation at the processor core. Meeting the specifications at the processor core in Table 21 through Table 27 ensures that signal quality effects will not adversely affect processor operation.

4.1 Bus Clock Signal Quality Specifications

Table 21 describes the signal quality specifications at the processor core pad for the processor system bus clock (BCLK) signal. Figure 11 shows the signal quality waveform for the system bus clock at the processor core pads.

Table 21. BCLK Signal Quality Specifications at the Processor Core Pads[1]

V#	Parameter	Min	Nom	Max	Unit	Figure	Notes
V1:	BCLK V_{IL}	-0.3		0.5	V	11	
V2:	BCLK V_{IH}	2.0		2.625	V	11	
V3:	V_{IN} Absolute Voltage Range	–0.7	2.0	3.3	V	11	
V4:	Rising Edge Ringback	2.0			V	11	2
V5:	Falling Edge Ringback			0.5	V	11	2

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

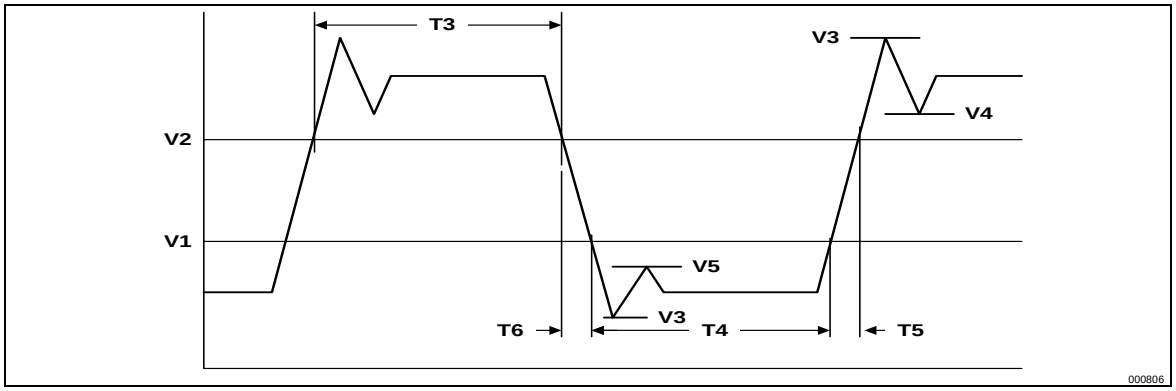


Figure 11. BCLK, TCK, PICCLK Generic Clock Waveform at the processor Core Pads

4.2 AGTL+ Signal Quality Specifications

Refer to the *Pentium II Processor Developer's Manual* (Order Number 243341) for the specification for AGTL+.

4.2.2 AGTL+ Signal Quality Specifications

Figure 12A illustrates the AGTL+ signal quality specifications for the processor for use in verifying signal quality at the processor core **pins**.

These receiver signal quality specifications do not include overdrive region, ringback threshold, edge rate, and non-monotonicity values. The receiver signal may contain ringback and non-monotonicity as long as these events do not occur inside the Setup and Hold Time windows. The Setup Time window is the shaded region, which is bounded by minimum V_{IH}, maximum V_{IL}, T8, and the BCLK 1.25V reference crossing point. The Hold Time window is the region bounded by minimum V_{IH}, maximum V_{IL}, T9, and the BCLK 1.25V reference crossing point. Note that the receiving signal at the receiver pin may contain non-ideal signal quality events within the T8 time, as long as these events occur outside the V_{IH} / V_{IL} Setup and Hold Time window boundaries.

The following conditions apply to the processor signal quality specifications:

1. A rising edge signal must cross above minimum V_{IH} prior to the Setup Time window. A falling edge signal must cross below maximum V_{IL} prior to the Setup Time window.
2. A rising edge signal in the next cycle must cross minimum V_{IL} outside the Hold Time window. A falling edge signal in the next cycle must cross maximum V_{IH} outside the Hold Time window.
3. A rising edge *flight time* uses a V_{IH} crossing point. A falling edge *flight time* uses a V_{IL} crossing point. Refer to the *Pentium III Xeon processor at 700 MHz and 900 MHz Signal Integrity Models* for a complete definition of *flight time*.
4. For purposes of receiver signal quality, a nominal value of V_{REF} (as defined in Table 10) should be used for all conditions. Therefore, the signal quality specifications given here already include sources of noise that will vary V_{IL} and V_{IH}. (e.g., V_{TT} tolerance, V_{REF} noise, V_{REF} resistor divider tolerance, etc…).
5. This receiver specification does not comprehend maximum overshoot/undershoot limits. Refer to the Section 4.2.3 for these specifications.
6. Intel® recommends signal ringback with as much margin as possible to the V_{IH}/V_{IL} levels and T8/T9 times to allow margin for other sources of system noise.

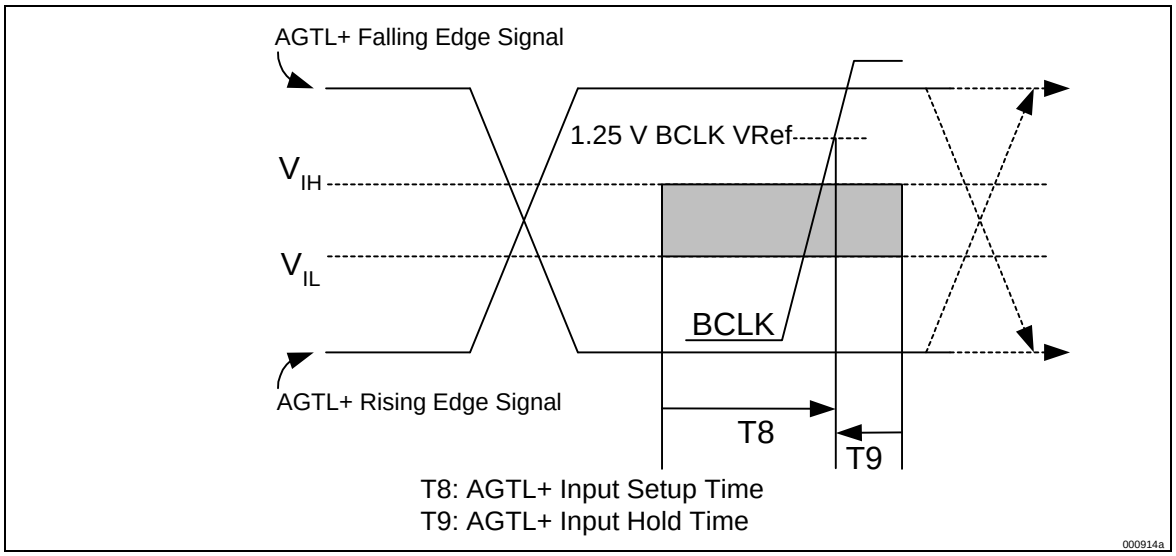


Figure 12A. Low to High AGTL+ Receiver Ringback Tolerance

4.2.3 AGTL+ OVERSHOOT/UNDERSHOOT GUIDELINES

Overshoot guidelines based on magnitude and duration of an overshoot/undershoot pulse (illustrated in Figure 13) are given in Table 23 and Table 24.

SIGNAL QUALITY

Overshoot/Undershoot is the absolute value of the maximum voltage differential across the input buffer relative to the termination voltage (V_{TT}). The overshoot/undershoot guideline limits transitions beyond VTT or VSS due to the fast signal edge rates. The processor can be damaged by repeated Overshoot/Undershoot events on 1.5 V or 2.5 V tolerant buffers if the potential is large enough (i.e., if the overshoot/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the Magnitude, the Pulse Duration, and the Activity Factor. The Overshoot/Undershoot specifications apply to the processor, regardless of whether the processor is driving or receiving the signal.

4.2.3.1 Overshoot/Undershoot Magnitude

Overshoot magnitude describes the maximum potential difference between a signal and its reference voltage level, Vss. Undershoot Magnitude describes the maximum potential difference between a signal and V_{TT} (undershoot). While overshoot can be measured relative to VSS using one probe (probe on signal and ground lead on VSS), Undershoot must be measured relative to V_{TT}. This can be accomplished by simultaneously measuring the V_{TT} plane while measuring the signal undershoot. The true waveform can then be calculated by the oscilloscope itself or by the following oscilloscope data file analysis:

$$\text{Converted Undershoot Waveform} = V_{TT} - \text{Signal}$$

Note: This Converted Undershoot Waveform appears as a positive (overshoot) signal.

Note: Overshoot (rising edge) and Undershoot (falling edge) conditions are separate and their impact must be determined independently.

After the conversion, the Overshoot/Undershoot Specifications can be applied to the Converted Undershoot Waveform using the Overshoot/Undershoot Magnitude and Pulse Duration Specifications in Tables 23, 24 and 25.

Overshoot/Undershoot Magnitude levels must also observe the Absolute Maximum Specifications. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed Pulse Durations. Provided that the magnitude of the Overshoot/Undershoot is within the Absolute Maximum Specifications, the impact of the Overshoot/Undershoot Magnitude may be determined based upon the Pulse Duration and Activity Factor.

4.2.3.2 Overshoot/Undershoot Pulse Duration

Overshoot/Undershoot Pulse Duration describes the total time that an Overshoot/Undershoot event exceeds the Overshoot/Undershoot Reference Voltage (Vos_ref = 1.635V). This total time could encompass several oscillations above the Overshoot/Undershoot Reference Voltage. Thus, multiple Overshoot/Undershoot pulses within a single Overshoot/Undershoot event must be measured to determine the total Pulse Duration.

Note: Oscillations below the Reference Voltage cannot be subtracted from the total Overshoot/Undershoot Pulse Duration.

Note: Multiple Overshoot/Undershoot events occurring within the same clock cycle must be considered together as one event. Using the worst-case Overshoot/Undershoot Magnitude, sum together the individual Pulse Durations to determine the total Overshoot/Undershoot Pulse Duration for that total event.

4.2.3.3 Overshoot/Undershoot Activity Factor

Activity Factor (AF) describes the frequency of Overshoot/Undershoot occurrence relative to a Clock. Since the highest frequency of assertion of an AGTL+ or a CMOS signal is every other clock, an AF = 1 indicates that the specific Overshoot or Undershoot waveform occurs EVERY OTHER clock cycle (e.g., 1-0-1-0… system bus switching pattern). Thus, an AF = 0.01 indicates that the specific Overshoot or Undershoot waveform occurs 1 time in every 200 CLK cycles.

The specifications provided in Tables 23, 24 and 25 show the Maximum Pulse Duration allowed for a given Overshoot/Undershoot Magnitude at a specific Activity Factor. Each Table entry is independent of all others, meaning that the Pulse Duration reflects the existence of Overshoot/Undershoot Events of that Magnitude ONLY. A platform with an overshoot/undershoot that just meets the Pulse Duration for a specific Magnitude where the AF < 1, means that there can be NO other Overshoot/Undershoot events, even of lesser Magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note: Activity Factor for AGTL+ signals is referenced to BCLK frequency.

Note: Activity Factor for CMOS signals is referenced to PICCLK frequency.

4.2.3.4 Determining if a System Meets the Overshoot/Undershoot Specifications

SIGNAL QUALITY

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that will each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

- Insure no signal (CMOS or AGTL+) ever exceed the 1.635V.
- If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables. This means that whenever the over/undershoot event occurs, it always over/undershoots to the same level.
- If multiple overshoots and/or multiple undershoots occur, measure the worst-case pulse duration for each magnitude and compare the results against the AF = 1 specifications (note: multiple overshoot/undershoot events within one clock cycle must have their pulse durations summed together to determine the total pulse duration). If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table where AF=1, then the system passes.

Table 24. AGTL+ Signal Overshoot/Undershoot Limits at the Processor Core [1, 2,3,4,5,6,7,8,9,10]

Overshoot/Undershoot Magnitude	**Max Pulse Duration (nS)**		
	AF = 0.01	**AF = 0.1**	**AF = 1**
2.3	20	2.53	0.25
2.25	20	4.93	0.49
2.2	20	9.1	0.91

NOTES:

SIGNAL QUALITY

1. Unless otherwise noted, all guidelines in this table apply to all processor frequencies.
2. Overshoot Magnitude and Undershoot Magnitude are absolute values and should never exceed 2.3V under any circumstances.
3. Overshoot is measured relative to VSS.
4. Undershoot is measured relative to VTT.
5. Overshoot/Undershoot Pulse Duration is measured relative to 1.635V.
6. Ringback below VTT cannot be subtracted from Overshoots/Undershoots.
7. Lesser Undershoot does not allocate longer or larger Overshoot. Lesser Overshoot does not allocate longer or larger Undershoot.
8. OEM's are encouraged to follow Intel provided layout guidelines.
9. All values specified by design characterization.
10. Specifications apply regardless of whether the processor is driving or receiving.

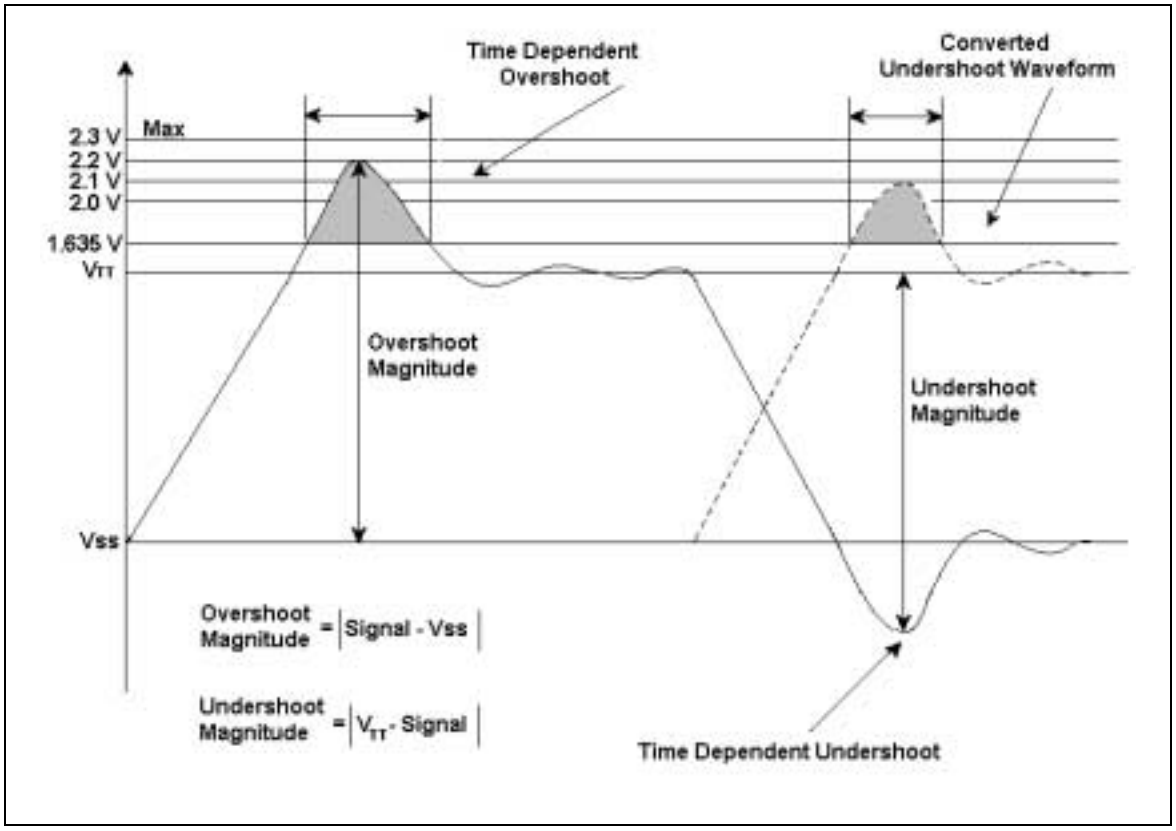


Figure 13. Maximum Acceptable Overshoot/Undershoot Waveform[1,2,3,4,5,6,7,8]

NOTES:

1. Overshoot Magnitude and Undershoot Magnitude are absolute values and should never exceed 2.3V under any circumstances.
2. Overshoot is measured relative to V_{SS}.
3. Undershoot is measured relative to V_{TT}.
4. Overshoot/Undershoot Pulse Duration is measured relative to 1.635V.
5. Ringback below V_{TT} cannot be subtracted from Overshoots/Undershoots.
6. Lesser Undershoot does not allocate longer or larger Overshoot. Lesser Overshoot does not allocate longer or larger Undershoot.
7. OEM's are encouraged to follow Intel provided layout guidelines.
8. All values specified by design characterization.

4.3 Non-GTL+ Signal Quality Specifications

There are three signal quality parameters defined for non-AGTL+ signals: Overshoot/Undershoot, Ringback, and Settling Limit. All three signal quality parameters are shown in Figure 14 for the non-AGTL+ signal group at the processor core

pads. Overshoot/Undershoot shown in Figure 14 is for illustrative purposes only to help explain Ringback and Settling Limit. Refer to Figure 13 for an illustration of Overshoot/Undershoot specifications.

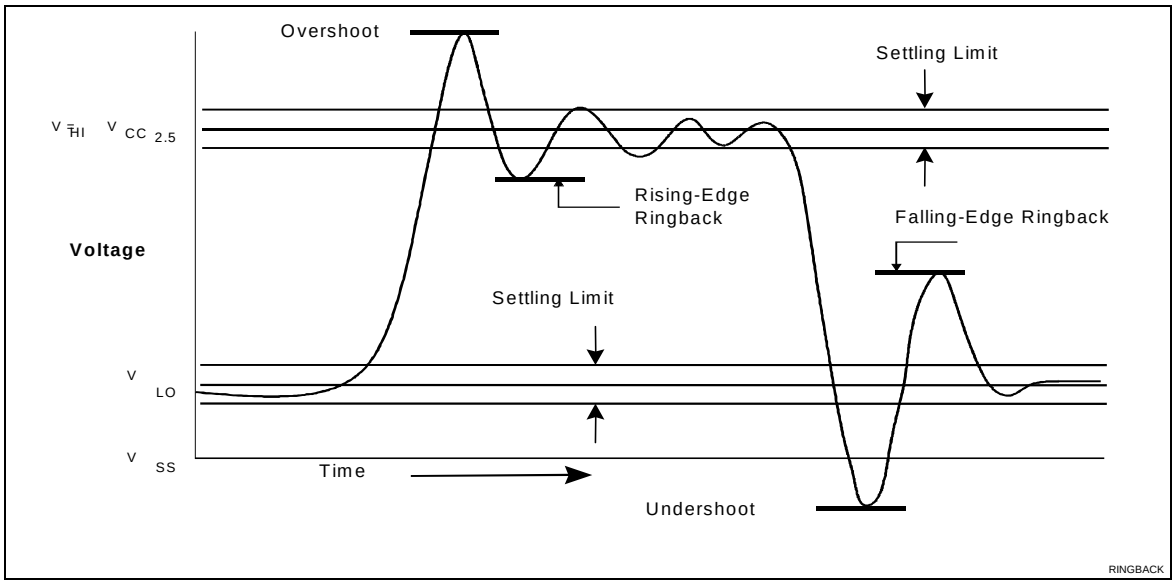


Figure 14. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback

4.3.1 2.5V Signal Overshoot/Undershoot Guidelines

The Overshoot/Undershoot guideline limits transitions beyond V_{CC} or V_{SS} due to fast signal edge rates. Refer to Figure 14 for an illustration of Overshoot/Undershoot specifications for non-AGTL+ signals. The processor may be damaged if Overshoot/Undershoot specifications are not met. The Overshoot/Undershoot specification is shown in Table 26.

Table 27. 2.5V Tolerant Signal Group Overshoot/Undershoot at the Processor Core Pins[1,2,3,4,5,6,7,8,9]

Overshoot/Undershoot Magnitude	Max Pulse Duration (nS) AF = 0.01	AF = 0.1	AF = 1
2.3	60	7.6	0.76
2.25	60	14.8	1.48
2.2	60	27.2	2.7
2.15	60	50	5
2.1	60	60	9.1
2.05	60	60	16.4
2.0	60	60	30

NOTES:

SIGNAL QUALITY

1. Activity Factor based on period equal to 30 nS.
2. Overshoot/Undershoot Magnitude = 2.3V is an Absolute value and should never be exceeded.
3. Overshoot is measured relative to VSS.
4. Undershoot is measured relative to VTT.
5. Overshoot/Undershoot Pulse Duration is measured relative to 1.635V.
6. Ringback below VTT cannot be subtracted from Overshoots/Undershoots.
7. Lesser Undershoot does not allocate longer or larger Overshoot.
8. OEM's are encouraged to follow Intel provided layout guidelines.
9. All values specified by design characterization.

4.3.2 BCLK Overshoot/Undershoot Guidelines and Specifications

Unlike AGTL+ or CMOS signals, BCLK Specifications do not provide for any relaxation due to activity factor. System designers should ensure that their platforms meet the BCLK specifications even under worst-case conditions.

Intel recommends that platforms meet the Absolute Maximum Specifications for Overshoot and Undershoot on BCLK. This ensures that the BCLK I/O buffer will meet specifications regardless of Overshoot or Undershoot Pulse Duration within a clock cycle with 50% duty cycle. For all processors, the maximum BCLK Overshoot level is 3.3V. The Absolute maximum Undershoot is –0.7V, where “maximum” is defined as the largest voltage potential below ground.

However, the Absolute Maximum Specifications can be relaxed for BCLK Undershoot if the Pulse Duration is accounted for under worst-case conditions. Thus, a system with BCLK Undershoot below -0.7V must ensure that the worst case Pulse Duration is less than or equal to the allowed Max Pulse Duration for the Worst Case Undershoot Magnitude. See the tables in this section for complete details.

Table 28. BCLK Undershoot Specifications[1,2,3,4,5,6]

Undershoot Magnitude	Max Pulse Duration (nS)
-0.85	2.13
-0.8	2.80
-0.75	3.73
-0.7	5.00
-0.65	5.00

NOTES:

1. Undershoot is measured relative to VTT.
2. Overshoot/Undershoot Pulse Duration is measured relative to 1.635V.
3. Ringback below VTT cannot be subtracted from Overshoots/Undershoots.
4. Lesser Undershoot does not allocate longer or larger Overshoot.
5. OEM's are encouraged to follow Intel provided layout guidelines.
6. All values specified by design characterization.

4.3.3 Measuring BCLK Overshoot/Undershoot

Overshoot on BCLK is measured relative to GND. By probing BCLK with an oscilloscope where the probe GND lead makes good contact to a processor GND pin, BCLK Overshoot can be accurately measured to determine if the system meets BCLK Overshoot Absolute Maximum Specifications.

Undershoot on BCLK is also measured relative to GND, again by probing BCLK with an oscilloscope where the probe GND lead makes good contact to a processor GND pin. If the system does not meet the BCLK Undershoot Absolute Maximum Specifications, then the Worst Case Undershoot Magnitude must be measured and the Pulse Duration of the Undershoot must be accounted for. Pulse Duration measurements determine the total amount of time that the BCLK signal spends below GND. Measuring from the earliest Falling Edge GND crossover to the latest Rising Edge GND crossover provides the worst-case Undershoot Pulse Duration. When compared to the Specification Table, the Pulse Duration and the Worst Case Undershoot Magnitude then determines if the system meets the BCLK Overshoot/Undershoot Specifications. Note: the measured Pulse Duration must be less than or equal to the Specified Max Pulse Duration for a given Worst Case Undershoot Magnitude.

SIGNAL QUALITY

4.3.4 2.5V TOLERANT BUFFER RINGBACK SPECIFICATION

The ringback specification is the voltage at a receiving pin that a signal rings back to after achieving its maximum absolute value. (See Figure 14 for an for an illustration of ringback.) Excessive ringback can cause false signal detection or extend the propagation delay. Violations of the signal ringback specification are not allowed for 2.5V tolerant signals.
Table 30 shows signal ringback specifications for the 2.5V tolerant signals to be used for simulations at the processor core.

Table 30. Signal Ringback Specifications for 2.5V Tolerant Signal Simulation at the processor Core

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals	$0 \rightarrow 1$	1.7	V	14
Non-AGTL+ Signals	$1 \rightarrow 0$	0.7	V	14

4.3.5 2.5V TOLERANT BUFFER SETTLING LIMIT GUIDELINE

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10% of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

5. PROCESSOR FEATURES

5.1 Low Power States and Clock Control

The processor allows the use of Auto HALT, Stop-Grant, and Sleep states to reduce power consumption by stopping the clock to specific internal sections of the processor, depending on each particular state. There is no Deep Sleep state on the processor. Refer to the following sections on low power states for the processor.

For the processor to fully realize the low current consumption of the Stop Grant, and Sleep states, an MSR bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a '1' (power on default is a '0') for the processor to stop all internal clocks during these modes. For more information, see the *Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide* (Order Number 243192). Due to not being able to recognize bus transactions during Sleep state, SMP systems are not allowed to have one or more processors in Sleep state and other processors in Normal or Stop Grant states simultaneously.

5.1.1 NORMAL STATE — STATE 1

This is the normal operating state for the processor.

5.1.2 AUTO HALT POWER DOWN STATE — STATE 2

Auto HALT is a low power state entered when the processor executes the HALT instruction. The processor will issue a normal HALT bus cycle on BE[7:0]# and REQ[4:0]# when entering this state. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

SMI# will cause the processor to execute the SMI handler. The return from the SMI handler can be to either Normal Mode or the Auto HALT Power Down state. See Chapter 11 in the *Intel Architecture Software Developer's Manual Volume 3: System Programming Guide*.

FLUSH# will be serviced during Auto HALT state. The on-chip first level caches and external second level cache will be flushed and the processor will return to the Auto HALT state.

A20M# will be serviced during Auto HALT state; the processor will mask physical address bit 20 (A20#) before any look-up in either the on-chip first level caches or external second level cache, and before a read/write transaction is driven on the bus.

The system can generate a STPCLK# while the processor is in the Auto HALT Power Down state. The processor will generate a Stop Grant bus cycle when it enters the Stop Grant state from the HALT state. If the processor enters the Stop Grant state from the Auto HALT state, the STPCLK# signal must be de-asserted before any interrupts are serviced (see below). When the system de-asserts the STPCLK# interrupt signal, the processor will return execution to the HALT state. The processor will not generate a new HALT bus cycle when it re-enters the HALT state from the Stop Grant state.

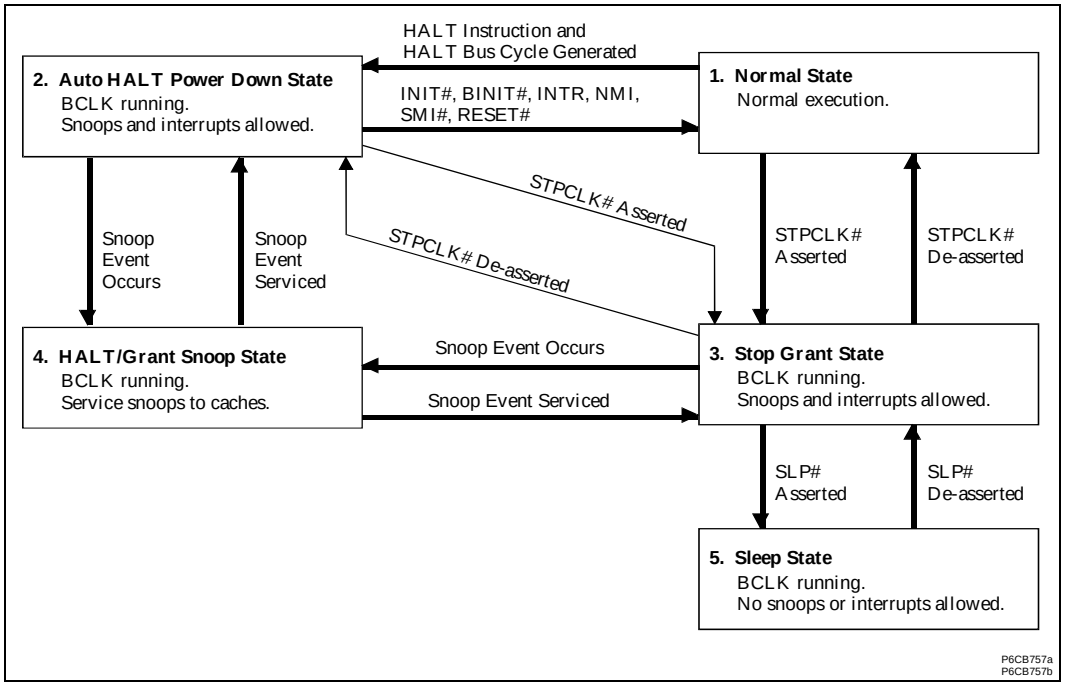


Figure 15. Stop Clock State Machine

5.1.3 STOP-GRANT STATE — STATE 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted. The processor will issue a Stop-Grant Transaction Cycle. Exit latency from this mode is 10 BLCK periods after the STPCLK# signal is de-asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from Stop-Grant state.

FLUSH# will not be serviced during Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop phase on the system bus. A transition to the Sleep state will occur with the assertion of the SLP# signal.

While in the Stop Grant State, all other interrupts will be latched by the processor, and only serviced when the processor returns to the Normal State.

5.1.4 HALT/GRANT SNOOP STATE — STATE 4

The processor will respond to snoop phase transactions (initiated by ADS#) on the system bus while in Stop-Grant state or in Auto HALT Power Down state. When a snoop transaction is presented upon the system bus, the processor will enter the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or Auto HALT Power Down state, as appropriate.

5.1.5 SLEEP STATE — STATE 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the PLL, and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state (verified by the termination of the Stop-Grant Bus transaction cycle), the SLP# pin can be asserted, causing the processor to enter the Sleep state. The system must wait 100 BCLK cycles after the completion of the Stop-Grant Bus cycle before SLP# is asserted. For an MP system, all processors must complete the Stop Grant bus cycle before the subsequent 100 BCLK wait and assertion of SLP# can occur. The processor is in Sleep state 10 BCLKs after the assertion of the SLP# pin. The latency to exit the Sleep state is 10 BCLK cycles. The SLP# pin is not recognized in the Normal, or Auto HALT States. Snoop events that occur during a transition into or out of Sleep state will cause unpredictable behavior. Therefore, transactions should be blocked by system logic during these transitions.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals immediately after the assertion of the SLP# pin (one exception is RESET# which causes the processor to re-initialize itself). The system core logic must detect these events and de-assert the SLP# signal (and subsequently de-assert the STPCLK# signal for interrupts) for the processor to correctly interpret any bus transaction or signal transition. Once in the Sleep state, the SLP# pin can be de-asserted if another asynchronous event occurs.

No transitions or assertions of signals are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal (with the exception of SLP# or RESET#) before the processor has returned to Stop Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop Grant State. If RESET# is driven active while the processor is in the Sleep State and normal operation is desired, the SLP# and STPCLK# should be de-asserted immediately after RESET# is asserted.

5.1.6 CLOCK CONTROL

During Auto HALT Power Down and Stop-Grant states, the processor will continue to process the snoop phase of a system bus cycle. The PICCLK signal should not be removed during the Auto HALT Power Down or Stop-Grant states. When the processor is in the Sleep state, it will not respond to interrupts or snoop transactions. PICCLK can be removed during the Sleep state.

The processor will not enter any low power states until all internal queues for the second level cache are empty. When re-entering Normal state, the processor will resume processing external cache requests as soon as new requests are encountered.

5.2 System Management Bus (SMBus) Interface

The processor includes an SMBus interface that allows access to several processor features, including two memory components (referred to as the processor Information ROM and the Scratch EEPROM) and a thermal sensor on the processor substrate. These devices and their features are described below.

The processor SMBus implementation uses the clock and data signals of the SMBus specification. It does not implement the SMBSUS# signals.

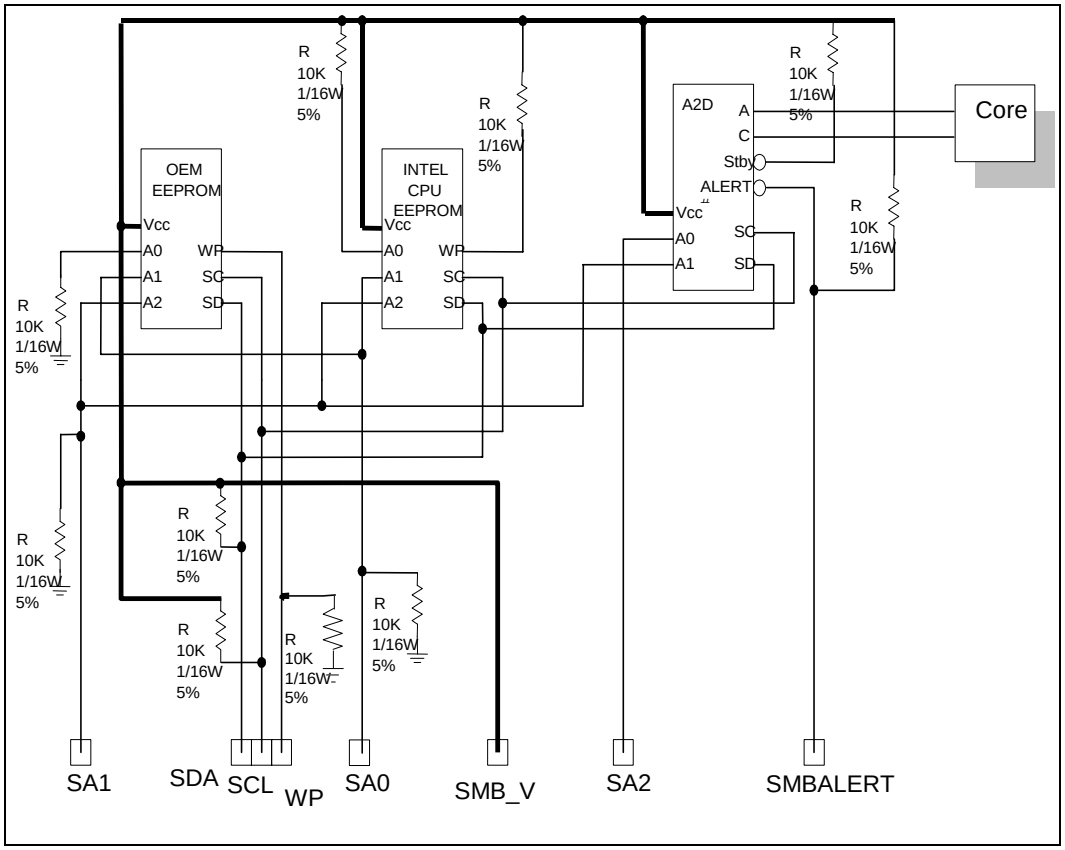


Figure 16. Logical[1] Schematic of SMBus Circuitry

NOTES:

1. Actual implementation may vary. For use in general understanding of the architecture.

5.2.1 PROCESSOR INFORMATION ROM

The processor implements previously defined fields in the processor information ROM (PI-ROM) to allow visibility of core and On Cartridge Voltage Regulation (OCVR) voltage requirements. These features are present in other SC330 processors, but are used in a different way in the Pentium® III Xeon™ processor at 700 MHz and 900 MHz. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz implements the OCVR device. This provides the flexibility to accommodate products with voltage input of 2.8V for one product version and 5V or 12V for a different product version. The 2.8V or 5V version is indicated in the PI-ROM "OCVR option 1 Input Voltage ID" field, while the 12V version is indicated in the "OCVR option 2 Input Voltage ID" PI-ROM field.

The implementation of the PI-ROM in the processor allows software to view the desired voltage outputs of the power source (VRM or Power Supply) feeding the OCVR and of the OCVR itself. Software could compare those values to actual power source/OCVR outputs (using an A/D converter), and determine if the power source and OCVR are operating correctly. The implementation of the PI-ROM gives system designers a means of determining the proper OCVR Output Voltage requirements. Without these fields, the baseboard has no way of determining the OCVR Output Voltage requirements.

The fields defined for the Pentium® III Xeon™ processor at 700 MHz and 900 MHz coincide as closely as possible with those for previous versions of the Pentium® III Xeon™ processor. The meaningless (for Pentium® III Xeon™ processor at 700 MHz and 900 MHz) "L2 Cache Voltage" field is replaced with a more useful "OCVR Output" field. The Pentium® III Xeon™ processor at 700 MHz and 900 MHz (SC330.1) has a pin defined (A56, "VIN_SENSE") that allows the baseboard to directly measure the actual OCVR input voltage, and pin (B83, "AN_CORE_VSENSE") that is an analog representation of the voltage at the OCVR output. This voltage can be compared with the desired voltage (indicated by the PIR field) to determine if the OCVR input / output voltage is varying from desired levels.

Systems implementing analog sensing should read the PIROM first, then compare that value with the measured VIN_SENSE rather than assuming any specific value. The value of AN_CORE_VSENSE is implementation dependent and cannot be assumed to be any particular value. Systems may derive benefit by monitoring its stability, but should not make assumptions about its value. In Table 31, text in **bold** represents the new defined fields for the Pentium® III Xeon™ processor at 700 MHz and 900 MHz.

Table 31. Processor Information ROM Format

Offset/Section	# of Bits	Function	Notes
HEADER: 00h	8	Data Format Revision	Two 4-bit hex digits
01h	16	EEPROM Size	Size in bytes (MSB first)
03h	8	Processor Data Address	Byte pointer, 00h if not present
04h	8	Processor Core Data Address	Byte pointer, 00h if not present
05h	8	L2 Cache Data Address	Byte pointer, 00h if not present
06h	8	SEC Cartridge Data Address	Byte pointer, 00h if not present
07h	8	Part Number Data Address	Byte pointer, 00h if not present
08h	8	Thermal Reference Data Address	Byte pointer, 00h if not present
09h	8	Feature Data Address	Byte pointer, 00h if not present
0Ah	8	Other Data Address	Byte pointer, 00h if not present
0Bh	16	Reserved	Reserved for future use
0Dh	8	Checksum	1 byte checksum
PROCESSOR: 0Eh	48	S-spec/QDF Number	Six 8-bit ASCII characters
	2	Sample/Production	00b = Sample only
	6	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
CORE: 16h	2	Processor Core Type	From CPUID
	4	Processor Core Family	From CPUID (Family 6)
	4	Processor Core Model	From CPUID (Model 8)
	4	Processor Core Stepping	From CPUID
	2	**Reserved**	
	16	**OCVR option 2 Input Voltage ID**	**Voltage in mV (0=2.8V, 12000=5V/12V**
	16	**OCVR option 2 Input Voltage Tolerance**	**Edge finger tolerance in mV, +/- (0=2.8V, 600=5V/12V)**
	8	**Reserved**	**Reserved for future use**
	16	Maximum Core Frequency	16-bit binary number (in MHz)
	16	**OCVR option 1 Input Voltage ID**	**Voltage in mV (2800=2.8V, 5000=5V/12V)**
	16	**OCVR option 1 Input Voltage Tolerance**	**Edge finger tolerance in mV, +/- (130=2.8V, 250=5V/12V)**
	8	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
L2 CACHE: 25h	32	Reserved	Reserved

	16	L2 Cache Size	16-Bit binary number (in Kbytes)
	8	Reserved	
	16	**OCVR Output Voltage ID**[1]	**Voltage in mV**
	8	**OCVR Output Voltage Tolerance, High**	**Core tolerance in mV, +**
	8	**OCVR Output Voltage Tolerance, Low**	**Core tolerance in mV, -**
	8	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
CARTRIDGE: 32h	32	Cartridge Revision	Four 8-bit ASCII characters
	2	Substrate Rev. Software ID	2-bit revision number
	6	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
PART NUMBERS: 38h	56	Processor Part Number	Seven 8-bit ASCII characters
	112	Processor BOM ID	Fourteen 8-bit ASCII characters
	64	Processor Electronic Signature	64-bit identification number
	208	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
THERMAL REF.: 70h	8	Thermal Reference Byte	See below
	16	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
FEATURES: 74h	32	Processor Core Feature Flags	From CPUID
	24	Cartridge Feature Flags	
	1	**OCVR Present**	1= Present 0= Not Present
	1	**Serial Signature**	1= Present 0= Not Present
	1	**Electronic signature present**	1= Present 0= Not Present
	1	**Thermal Sense Device Present**	1= Present 0= Not Present
	1	**Thermal Reference Byte Present**	1= Present 0= Not Present
	1	**OEM EEPROM Present**	1= Present 0= Not Present
	1	**Core VID present**	1= Present 0= Not Present
	1	**L2 Cache VID present**	Always Zero
	4	Number of Devices in TAP Chain	One 4-bit hex digit
	4	Reserved	Reserved for future use
	8	Checksum	1 byte checksum
OTHER: 7Eh	16	Reserved	Reserved for future use

NOTES:

1. OCVR Output Voltage not tested. Programmed per design target.

5.2.2 SCRATCH EEPROM

Also available on the SMBus is an EEPROM that may be used for other data at the system or processor vendor's discretion. This device has a pull-down on the WP control pin through a 10KΩ resistor, as implemented on all previous Pentium® II Xeon™ and Pentium® III Xeon™ processors. This will allow the OEM EEPROM to be programmed in systems with no manipulation of this signal. Once programmed, the data in this OEM EEPROM can be write protected by asserting the active-high WP signal. The Scratch EEPROM is a 1024 bit part.

5.2.3 PROCESSOR INFORMATION ROM AND SCRATCH EEPROM SUPPORTED SMBUS TRANSACTIONS

Four SMBus packet types are associated with the PIROM and Scratch EEPROM. Each of these packet transfers provides a device select address and read/write bit. The remaining parts of the transfer vary. Two of the packets, *Send Byte* and *Receive Byte*, transfer one additional byte after the device select. The other two packets, *Write Byte* and *Read Byte*, transfer two additional bytes after the device select. By using these four transfer types, complete access to the EEPROMs is possible.

Send Byte loads an address into the memory device that is used for subsequent access. Send Byte does not change the contents of the EEPROM, just the address pointer within it. See Table 32 and explanation below.

Receive Byte gets a byte of data from the memory device. It uses an address already loaded into the EEPROM device and returns the byte at that address. Repetitive use of Receive Byte to access an address range is possible. See Table 33 and explanation below. *Write Byte* transfers both an address and data byte into the memory device. It is a stand-alone write cycle. See Table 34. *Read Byte* transfers an address and gets a byte of data from the memory device. It is a stand alone read cycle. See Table 35.

Both ROMs respond to SMBus packet types Send Byte, Receive Byte, and Read Byte. The Scratch EEPROM additionally responds to the packet type Write Byte.

The EEPROM devices perform sequential read and page write modes that are not covered by the SMBus specification. However, by use of the four transfers described above, all transfer requirements to these devices can be achieved.

NOTE: In Tables 32 - 35 below:

S indicates a start condition (SDA falling while SCK high)

P indicates a stop condition (SDA rising while SCK high)

R/W* indicates a read/write not signal (1 = read, 0 = write)

A* indicates an acknowledge* signal, (0 = acknowledge, 1 = not acknowledge).

The selected SMBus slave device drives the shaded portions, while the SMBus master device under control of the host drives the clear portions.

Table 32. Send Byte SMBus Packet

S	Device Address	R/ W*	A*	Data	A*	P
1	7 bits	0	0	8 bits	0	1

Table 32 outlines the Send Byte packet, which provides an address to the device for later use. A device select field and a write bit, which are acknowledged by the device, follow the start condition. The following data byte is really an address, which is also acknowledged by the device. Finally the stop condition is signaled.

Table 33. Receive Byte SMBus Packet

S	Device Address	R/ W*	A*	Data	A*	P
1	7 bits	1	0	8 bits	1	1

Table 33 diagrams the Receive Byte packet that performs as a current address read. A device select address field and a read flag follow the start condition. The device decodes its address and drives acknowledge low. The data is returned by the device and the transfer is terminated by the controller providing negative acknowledge and a stop. Note that there is no data address provided, only the device address. The EEPROM internal address counter keeps track of the address accessed during the last read or write operation, incremented by one. Repeated current address reads will receive data from consecutive addresses. Address roll over will occur when the last byte of the device has been read. In this event it will roll over to the first byte of the device.

Table 34. Write Byte SMBus Packet

S	Device Address	R/ W*	A*	Data Address	A*	Data	A*	P
1	7 bits	0	0	8 bits	0	8 bits	0	1

Table 34 diagrams the Write Byte packet. This is effectively a Random Address Write function. The device select address, data offset address and write data are provided within the packet. A write flag follows the device address. Each of the three acknowledge pulses is driven by the EEPROM device. After the Write Byte packet is received the Scratch EEPROM device enters a timed writing mode during which it will not respond to further transfers. This timed writing mode will last approximately 10 milliseconds.

Table 35. Read Byte SMBus Packet

S	Device Address	R/ W*	A*	Data Address	A *	S	Device Address	R/ W*	A*	Data	A*	P
1	7 bits	0	0	8 bits	0	1	7 bits	1	0	8 bits	1	1

Table 35 illustrates the Read Byte packet. This is effectively a Random Address Read function. This is actually two consecutive SMBus transfers, an address write followed by a current address read from the same device. In the address write portion, both device address and data address are acknowledged by the EEPROM. A second start condition then occurs, followed by a receive byte read such as diagrammed above. From the programming perspective, this may be treated as two separate transfers.

5.2.4 THERMAL SENSOR

The processor thermal sensor provides a means of acquiring thermal data from the processor with an exceptional degree of precision. The thermal sensor is composed of control logic, SMBus interface logic, a precision analog-to-digital converter, and a precision current source. The thermal sensor drives a small current through the p-n junction of a thermal diode located on the same silicon die as the processor core. The forward bias voltage generated across the thermal diode is sensed and the precision A/D converter derives a single byte of thermal reference data, or a “thermal byte reading.” System management software running on the processor or on a microcontroller can acquire the data from the thermal sensor to thermally manage the system.

Upper and lower thermal reference thresholds can be individually programmed for the thermal diode. Comparator circuits sample the register where the single byte of thermal data (thermal byte reading) is stored. These circuits compare the single byte result against programmable threshold bytes. The alert signal on the processor SMBus (SMBALERT#) will assert when either threshold is crossed.

To increase the usefulness of the thermal diode and thermal sensor, the processor PIROM includes a Thermal Reference Byte determined by Intel through a specific manufacturing procedure. This procedure determines the Thermal Reference Byte and programs it into the PIROM. The Thermal Reference Byte is

uniquely determined for each unit. The procedure causes each unit to dissipate its maximum power (which can vary from unit to unit) while at the same time maintaining the thermal plate at its maximum specified operating temperature. Correctly used, this feature permits an efficient thermal solution while preserving data integrity.

The thermal byte reading can be used in conjunction with the Thermal Reference Byte in the processor Information ROM. Byte 9 of the processor Information ROM contains the address in the ROM of this byte, described in more detail in Section 5.2.5. The thermal byte reading from the thermal sensor can be compared to this Thermal Reference Byte, to provide an indication of the difference between the temperature of the processor core at the instant of the thermal byte reading and the temperature of the processor core under the steady state conditions of high power and maximum T_{PLATE} specifications. The nominal precision of the least significant bit of a thermal byte is 1°C.

Reading the thermal sensor is explained in Section 5.2.6.

The thermal sensor feature in the processor cannot be used to measure T_{PLATE}. The T_{PLATE} specification in Chapter 6 must be met regardless of the reading of the processor's thermal sensor in order to ensure adequate cooling for the entire processor. The thermal sensor feature is only available while V_{CC_CORE} and V_{CC_SMB} are at valid levels and the processor is not in a low-power state.

5.2.5 THERMAL SENSOR SUPPORTED SMBUS TRANSACTIONS

The thermal sensor responds to five of the SMBus packet types: write byte, read byte, send byte, receive byte, and ARA (Alert Response Address). The send byte packet is used for sending one-shot commands only. The receive byte packet accesses the register commanded by the last read byte packet. If a receive byte packet was preceded by a write byte or send byte packet more recently than a read byte packet, then the behavior is undefined. Tables 36 through 40 diagram the five packet types. In these figures, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'Ack' represents an acknowledge, and '///' represents a negative acknowledge. The thermal sensor transmits the shaded bits and the SMBus host controller transmits the bits that aren't shaded. Table 41 shows the encoding of the command byte.

Table 36. Write Byte SMBus Packet

S	Address	Write	Ack	Command	Ack	Data	Ack	P
1	7 bits	1	1	8 bits	1	8 bits	1	1

Table 37. Read Byte SMBus Packet

S	Address	Write	Ack	Command	Ack	S	Address	Read	Ack	Data	///	P
1	7 bits	1	1	8 bits	1	1	7 bits	1	1	8 bits	1	1

Table 38. Send Byte SMBus Packet

S	Address	Write	Ack	Command	Ack	P
1	7 bits	1	1	8 bits	1	1

Table 39. Receive Byte SMBus Packet

S	Address	Read	Ack	Data	///	P
1	7 bits	1	1	8 bits	1	1

Table 40. ARA SMBus Packet

S	ARA	Read	Ack	Address	///	P
1	0001 100	1	1	Device Address[1]	1	1

NOTE:

1. This is an 8-bit field. The device that sent the alert will respond to the ARA Packet with its address in the seven most significant bits. The least significant bit is undefined and may return as a '1' or '0'. See Section 5.2.7 for details on the Thermal Sensor Device addressing.

Table 41. Command Byte Bit Assignments

Register	Command	Reset State	Function
RESERVED	00h	N/A	Reserved for future use
RRT	01h	N/A	Read processor core thermal data
RS	02h	N/A	Read status byte (flags, busy signal)
RC	03h	0000 0000	Read configuration byte
RCR	04h	0000 0010	Read conversion rate byte
RESERVED	05h	0111 1111	Reserved for future use
RESERVED	06h	1100 1001	Reserved for future use
RRHL	07h	0111 1111	Read processor core thermal diode T_{HIGH} limit
RRLL	08h	1100 1001	Read processor core thermal diode T_{LOW} limit
WC	09h	N/A	Write configuration byte
WCR	0Ah	N/A	Write conversion rate byte
RESERVED	0Bh	N/A	Reserved for future use
RESERVED	0Ch	N/A	Reserved for future use
WRHL	0Dh	N/A	Write processor core thermal diode T_{HIGH} limit
WRLL	0Eh	N/A	Write processor core thermal diode T_{LOW} limit
OSHT	0Fh	N/A	One shot command (use send byte packet)
RESERVED	10h – FFh	N/A	Reserved for future use

All of the commands are for reading or writing registers in the thermal sensor except the one-shot command (OSHT). The one-shot command forces the immediate start of a new conversion cycle. If a conversion is in progress when the one-shot command is received, then the command is ignored. If the thermal sensor is in standby mode when the one-shot command is received, a conversion is performed and the sensor returns to standby mode. The one-shot command is not supported when the thermal sensor is in auto-convert mode.

If the thermal sensor is in auto-convert mode and is between conversions, then the conversion rate timer resets, and the next automatic conversion takes place after a full delay elapses. The default command after reset is to a reserved value (00h). After reset, receive byte packets will return invalid data until another command is sent to the thermal sensor. This one-shot feature is currently susceptible to failure and should not be used (i.e. don't issue one-shot commands) when in auto convert mode.

5.2.6 THERMAL SENSOR REGISTERS

5.2.6.1 Thermal Reference Registers

The processor core and thermal sensor internal thermal reference registers contain the thermal reference value of the thermal sensor and the processor core thermal diodes. This value ranges from +127 to -128 decimal and is expressed as a two's complement, eight-bit number. These registers are saturating, i.e. values above 127 are represented at 127 decimal, and values below -128 are represented as -128 decimal.

5.2.6.2 Thermal Limit Registers

The thermal sensor has two thermal limit registers; they define high and low limits for the processor core thermal diode. The encoding for these registers is the same as for the thermal reference registers. If the diode thermal value equals or exceeds one of its limits, then its alarm bit in the Status Register is triggered.

5.2.6.3 Status Register

The status register shown in Table 42 indicates which (if any) thermal value thresholds have been exceeded. It also indicates if a conversion is in progress or if an open circuit has been detected in the processor core thermal diode connection. Once set, alarm bits stay set until a status register read clears them. A successful read to the status register will clear any alarm bits that may have been set, unless the alarm condition persists.

Table 42. Thermal Sensor Status Register

Bit	Name	Function
7 (MSB)	BUSY	A one indicates that the device's analog to digital converter is busy converting.
6	RESERVED	Reserved for future use
5	RESERVED	Reserved for future use
4	RHIGH	A one indicates that the processor core thermal diode high temperature alarm has activated.
3	RLOW	A one indicates that the processor core thermal diode low temperature alarm has activated.
2	OPEN	A one indicates an open fault in the connection to the processor core diode.
1	RESERVED	Reserved for future use.
0 (LSB)	RESERVED	Reserved for future use.

5.2.6.4 Configuration Register

The configuration register controls the operating mode (standby vs. auto-convert) of the thermal sensor. Table 43 shows the format of the configuration register. If the RUN/STOP bit is set (high) then the thermal sensor immediately stops converting and enters standby mode. The thermal sensor will still perform analog to digital conversions in standby mode when it receives a one-shot command. If the RUN/STOP bit is clear (low) then the thermal sensor enters auto-conversion mode.

Table 43. Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 (MSB)	RESERVED	0	Reserved for future use.
6	RUN/STOP	0	Standby mode control bit. If high, the device immediately stops converting, and enters standby mode. If low, the device converts in either one-shot mode or automatically updates on a timed basis..
5-0	RESERVED	0	Reserved for future use.

5.2.6.5 Conversion Rate Register

The contents of the conversion rate register determine the nominal rate at which analog to digital conversions happen when the thermal sensor is in auto-convert mode. Table 44 shows the mapping between conversion rate register values and the conversion rate. As indicated in Table 44, the conversion rate register is set to its default state of 02h (0.25 Hz nominally) when the thermal sensor is powered up. There is a ±25% error tolerance between the conversion rate indicated in the conversion rate register and the actual conversion rate.

Table 44. Thermal Sensor Conversion Rate Register

Register Contents	Conversion Rate (Hz)
00h	0.0625
01h	0.125
02h	0.25

03h	0.5
04h	1
05h	2
06h	4
07h	8
08h to FFh	Reserved for future use

5.2.7 SMBus Device Addressing

Of the addresses broadcast across the SMBus, the memory components claim those of the form "1010XXYZb". The "XX" and "Y" bits are used to enable the devices on the cartridge at adjacent addresses. The Y bit is hard-wired on the cartridge to V_{SS} ('0') for the Scratch EEPROM and pulled to V_{CC_SMB} ('1') for the processor Information ROM. The "XX" bits are defined by the processor slot via the SA0 and SA1 pins on the SC330 connector. These address pins are pulled down (1KΩ) to ensure that the memory components are in a known state in systems that do not support the SMBus, or only support a partial implementation. The "Z" bit is the read/write bit for the serial bus transaction.

The thermal sensor internally decodes 1 of 3 upper address patterns from the bus of the form "0011XXXZb", "1001XXXZb" or "0101XXXZb". The device's addressing, as implemented, uses SA2 and SA1 and includes a Hi-Z state for the SA2 address pin. Therefore the thermal sensor supports 6 unique resulting address ranges. To set the Hi-Z state for SA2, the pin must be left floating. The system should drive SA1 and SA0, and will be pulled low (if not driven) by the 10KΩ pull-down resistor on the processor substrate. Attempting to drive either of these signals to a Hi-Z state would cause ambiguity in the memory device address decode, possibly resulting in the devices not responding, thus timing out or hanging the SMBus. As before, the "Z" bit is the read/write bit for the serial bus transaction.

Note that addresses of the form "0000XXXXb" are reserved and should not be generated by an SMBus master.

The thermal sensor latches the SA1 and SA2 signals at power up. System designers should ensure that these signals are at valid input levels before the thermal sensor powers up. This should be done by pulling the pins to V_{CCSMB} or V_{SS} via a 1KΩ or smaller resistor. Additionally, SA2 may be left unconnected to achieve the tri-state or "Z" state. If the designer desires to drive the SA1 or SA2 pin with logic the designer must ensure that the pins are at valid input levels (see Table 9) before V_{CCSMB} begins to ramp. The system designer must also ensure that their particular system implementation does not add excessive capacitance (>50 pF) to the address inputs. Excess capacitance at the address inputs may cause address recognition problems.

Figure 16 shows a logical diagram of the pin connections. Table 45 and Table 46 describe the address pin connections and how they affect the addressing of the devices.

Table 45. Thermal Sensor SMBus Addressing

Address (Hex)	Upper Address[1]	Slot Select		8-bit Address Word on Serial Bus
		SA1	SA2	b[7:0]
3Xh	0011	0	0	0011000Xb
	0011	1	0	0011010Xb
5Xh	0101	0	Z[2]	0101001Xb
	0101	1	Z[2]	0101011Xb
9Xh	1001	0	1	1001100Xb
	1001	1	1	1001110Xb

NOTES:

1. Upper address bits are decoded in conjunction with the select pins.
2. A tri-state or "Z" state on this pin is achieved by leaving this pin unconnected.

Note that system management software must be aware of the slot number-dependent changes in the address for the thermal sensor.

Table 46. Memory Device SMBus Addressing

Address (Hex)	Upper Address[1]	Slot Select		Memory Device Select	R/W	Device Addressed
	Bits 7-4	(SA1) Bit 3	(SA0) Bit 2	Bit 1	Bit 0	
A0h/A1h	1010	0	0	0	X	Scratch EEPROM 1
A2h/A3h	1010	0	0	1	X	Processor Information ROM 1
A4h/A5h	1010	0	1	0	X	Scratch EEPROM 2
A6h/A7h	1010	0	1	1	X	Processor Information ROM 2
A8h/A9h	1010	1	0	0	X	Scratch EEPROM 3
AAh/ABh	1010	1	0	1	X	Processor Information ROM 3
ACh/ADh	1010	1	1	0	X	Scratch EEPROM 4
AEh/AFh	1010	1	1	1	X	Processor Information ROM 4

This addressing scheme is targeted for up to 4-way MP systems. More processors can be supported by using a multiplexed (or separate) SMBus implementation.

6. THERMAL SPECIFICATIONS AND DESIGN CONSIDERATIONS

The processor contains a thermal plate for heatsink attachment. The thermal plate interface is intended to provide for multiple types of thermal solutions. This chapter will provide the necessary data for a thermal solution to be developed. See Figure 17 for thermal plate location.

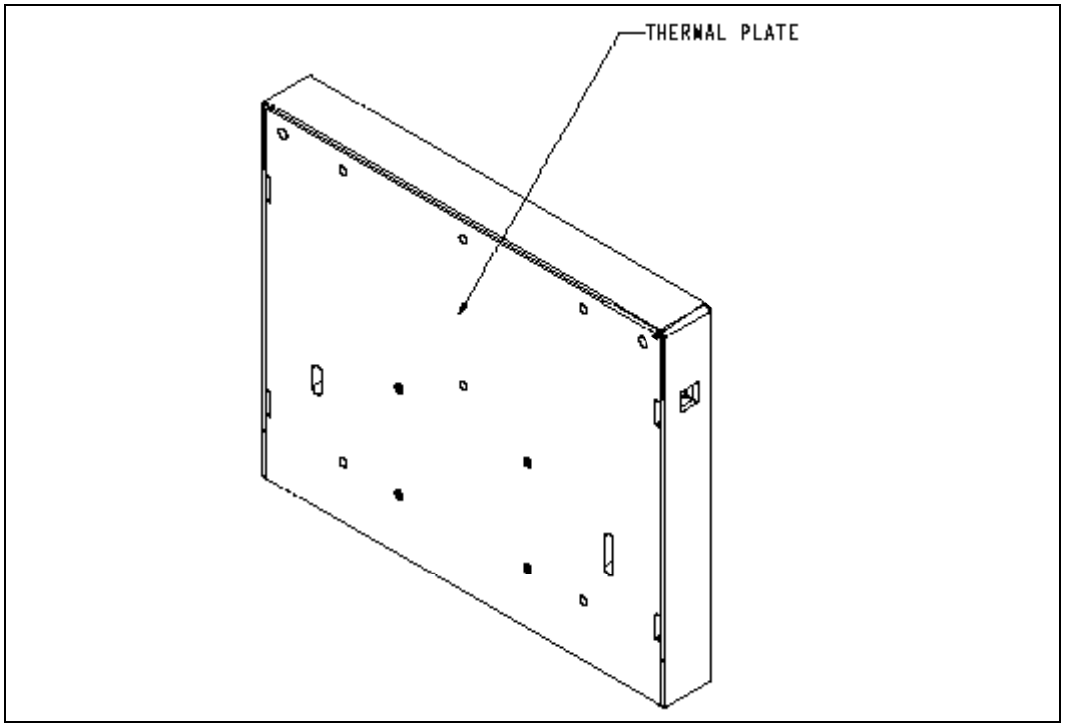


Figure 17. Thermal Plate View

6.1 Thermal Specifications

This section provides power dissipation specifications for each version of the processor. The thermal plate flatness is also specified for the S.E.C. cartridge.

6.1.1 POWER DISSIPATION

Table 47 and 48 provide the thermal design power dissipation for the processor. While the processor core dissipates the majority of the thermal power, the system designer should also be aware of the thermal power dissipated by the OCVR. Systems should design for the highest possible thermal power, even if a processor with lower frequency is planned. The thermal plate is the attach location for all thermal solutions. The maximum temperature for the entire thermal plate surface is shown in Table 47 and 48.

The processor power is dissipated through the thermal plate and other paths. The power dissipation is a combination of power from the OCVR, the processor core (with integrated L2 cache), and the AGTL+ bus termination resistors. The overall system thermal design must comprehend the Max Thermal power. The combined power from the processor core, the second level cache, and the OCVR that dissipates through the thermal plate is the Max Thermal power. The heatsink should be designed to dissipate the Max Thermal power.

The thermal sensor feature of the processor cannot be used to measure T_{PLATE}. The T_{PLATE} specification must be met regardless of the reading of the processor's thermal sensor in order to ensure adequate cooling for the entire processor.

Table 47 Power Estimates [1]

Frequency	Core Power[2] (W)	2.8V OCVR Power (W)	5V/12V OCVR Power (W)	2.8V Cartridge Power [3] (W)	5V/12V Cartridge Power [3] (W)	2.8V Thermal Power [4,8] (W)	5V/12V Thermal Power [4,8] (W)	AGTL+ Power[5]	Min T_{plate} °C	Max T_{plate} °C
700/100	25.9	6.1	7.3	32.0	33.2	28.9	29.6	2	0	65
900/100	31.8	7.5	9.0	39.3	40.8	35.5	36.3	2	0	65
FMB[6]						50	50		0	65

NOTES:

1. These values are specified at nominal V_{CC_CORE} for the processor core with integrated L2 cache.
2. Core power indicates the combined worst-case power that can be dissipated by the processor & L2 cache. This value will be determined after the product has been characterized.
3. Cartridge power indicates the worst-case power that can be dissipated by the processor, L2 cache and the OCVR. It is not possible for the AGTL+ bus, and the processor core to all be at full power simultaneously.
4. Thermal power (which OEM's should use for their thermal designs) indicates the worst-case power that can be dissipated by the processor, L2 cache and 50% of the OCVR (since the OCVR does not contact the Thermal Plate). **De-rating the thermal design power may result in exceeding the Tplate maximum temperature specification, which may result in immediate system failure or degradation of the processor's functional lifetime.**
5. AGTL+ power is the worst-case power dissipated in the termination resistors for the AGTL+ bus.
6. "FMB" is a suggested design guideline for a flexible motherboard design.
7. A disabled processor OCVR draws approximately 46 mA at 2.8V V_{CC_CORE} from the motherboard VRM. If your system needs to maintain VRM regulation with a disabled processor (OCVR_EN inactive), the VRM output minimum load specification should be 46 mA or less.
8. The Thermal Power specifications have been recently redefined. These values are based on device characterization and do not reflect any silicon design changes to lower processor power consumption. Absolute power consumption has not changed; however, the maximum thermal power specifications are being updated to reflect actual silicon performance. The Thermal Power values represent the thermal design point required to cool the processor in the platform environment.

6.1.2 PLATE FLATNESS SPECIFICATION

The thermal plate flatness for the processor is specified to 0.010” across the entire thermal plate surface, with no more than a 0.003” step anywhere on the surface of the plate, as shown in Figure 18.

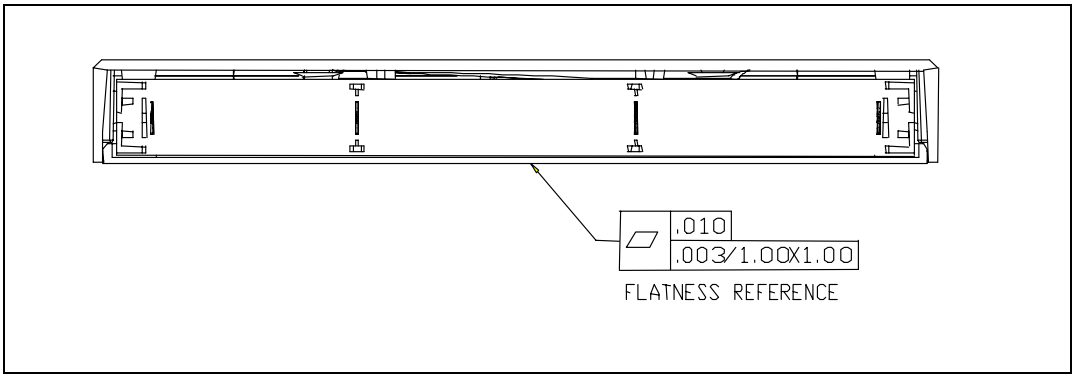


Figure 18. Plate Flatness Reference

6.2 Processor Thermal Analysis

6.2.1 THERMAL SOLUTION PERFORMANCE

Processor cooling solutions should attach to the thermal plate. The processor cover is not designed for thermal solution attachment.

The complete thermal solution must adequately control the thermal plate below the maximum and above the minimum specified in Table 47 and 48. The performance of any thermal solution is defined as the thermal resistance between the thermal plate and the ambient air around the processor (θ thermal plate to ambient). The lower the thermal resistance between the thermal plate and the ambient air, the more efficient the thermal solution is. The required *θ thermal plate to ambient* is dependent upon the maximum allowed thermal plate temperature (T_{PLATE}), the local ambient temperature (T_{LA}) and the thermal plate power (P_{PLATE}).

$$\theta \text{ thermal plate to ambient} = (T_{PLATE} - T_{LA}) / P_{PLATE}$$

The maximum T_{PLATE} and the thermal plate power are listed in Table 47 and 48. T_{LA} is a function of the system design. Table 49 provides the example of a resultant thermal solution performance for the processor at different ambient air temperatures around the processor.

Table 49. Example Thermal Solution Performance

Thermal Solution Performance	Local Ambient Temperature (T_{LA})		
FMB (50 Watts) *θ thermal plate to ambient* (°C/watt)	35°C	40°C	45°C
	0.60	0.50	0.40

Theta thermal plate to ambient value is made up of two primary components: the thermal resistance between the thermal plate and heatsink (*thetaθ thermal plate to heatsink*) and the thermal resistance between the heatsink and ambient air around the processor (*thetaθ heatsink to air*). A critical, but controllable factor to decrease the resultant value of theta thermal plate to heatsink is management of the thermal interface between the thermal plate and heatsink. The other controllable factor (*thetaθ heatsink to air*) is determined by

the design of the heatsink and airflow around the heatsink. General Information on thermal interfaces and heatsink design constraints can be found in *AP-586, Pentium II Processor Thermal Design Guidelines* (Order Number 243331).

6.2.2 THERMAL PLATE TO HEAT SINK INTERFACE MANAGEMENT GUIDE

Figure 19 shows suggested interface agent dispensing areas when using either Intel suggested interface agent. System issues in meeting the T_{PLATE} requirements will determine actual user area and interface agent selections.

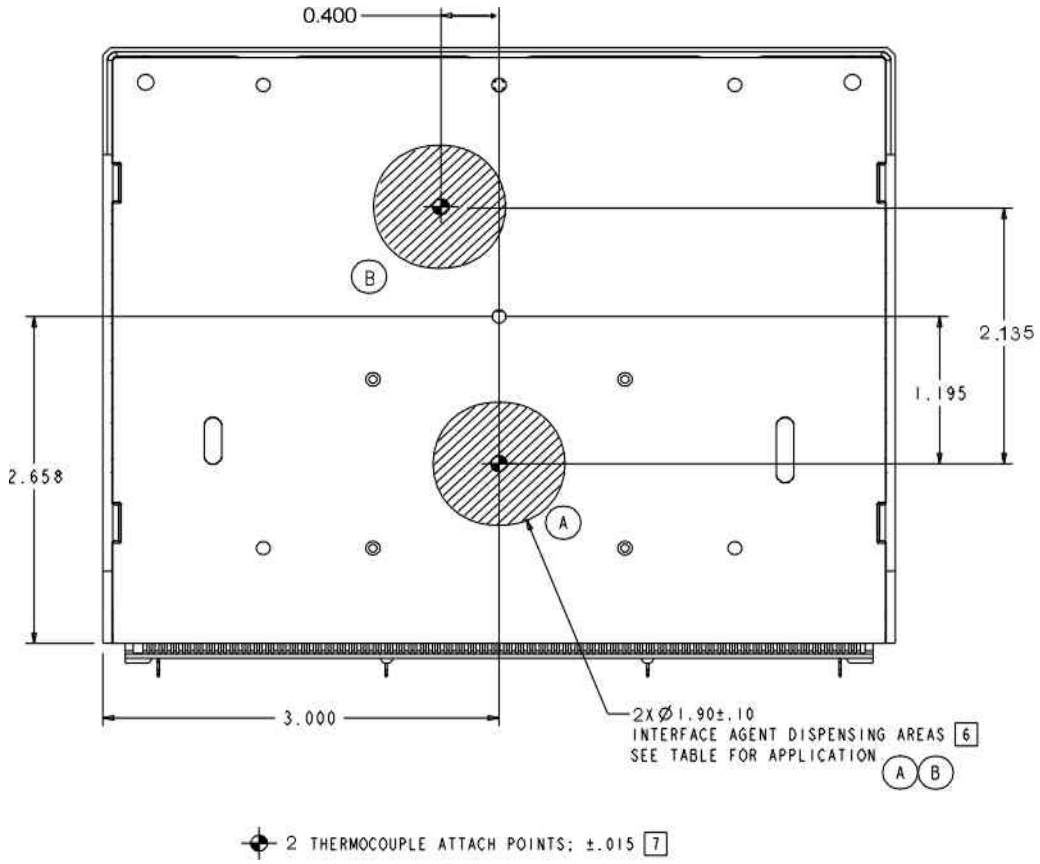


Figure 19. Interface Agent Dispensing Areas and Thermal Plate Temperature Measurement Points

NOTES:

6. Interface agent suggestions: ShinEtsu* G749 or Thermoset* TC330; Dispense volume adequate to ensure required minimum area of coverage when cooling solution is attached. Areas A and B are suggested for processor core and OCVR products. Recommended cooling solution mating surface flatness is no greater than 0.007" or flatter.
7. Temperature of the entire thermal plate surface not to exceed 65°C. Use any combination of interface agent, cooling solution, flatness condition, etc., to ensure this condition is met. Thermocouple measurement locations are the expected high temperature locations without external heat source influence. Ensure that external heat sources do not cause a violation of T_{PLATE} requirements

6.2.3 MEASUREMENTS FOR THERMAL SPECIFICATIONS

6.2.3.1 Plate Temperature Measurement

To ensure functional and reliable processor operation, the processor's thermal plate temperature (T_{PLATE}) must be maintained at or below the maximum T_{PLATE} and at or above the minimum T_{PLATE} specified in Table 47 and 48. Power from the processor core is transferred to the thermal plate at 2 locations. Figure 20 and 21 shows the locations for T_{PLATE} measurement directly above these transfer locations. Thermocouples are used to measure T_{PLATE} and special care is required to ensure an accurate temperature measurement. Before taking any temperature measurements, the thermocouples must be calibrated. When measuring the temperature of a surface, errors can be introduced in the measurement if not handled properly. Such measurement errors can be due to a poor thermal contact between the thermocouple junction and the measured surface, conduction through thermocouple leads, heat loss by radiation and convection, or by contact between the thermocouple cement and the heatsink base. To minimize these errors, the following approach is recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega* (part number: 5TC-TTK-36-36).
- Attach each thermocouple bead or junction to the top surface of the thermal plate at the locations specified in Figure 19 using high thermal conductivity cements.
- A thermocouple should be attached at a 0° angle if no heatsink is attached to the thermal plate. If a heatsink is attached to the thermal plate but the heatsink does not cover the location specified for T_{PLATE} measurement, the thermocouple should be attached at a 0° angle (refer to Figure 20).
- The thermocouple should be attached at a 90° angle if a heatsink is attached to the thermal plate and the heatsink covers the location specified for T_{PLATE} measurement (refer to Figure 21).
- The hole size through the heatsink base to route the thermocouple wires out should be smaller than 0.150" in diameter.
- Make sure there is no contact between the thermocouple cement and heatsink base. This contact will affect the thermocouple reading.

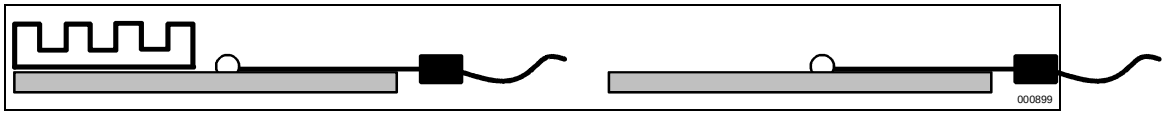


Figure 20. Technique for Measuring T_{PLATE} with 0° Angle Attachment

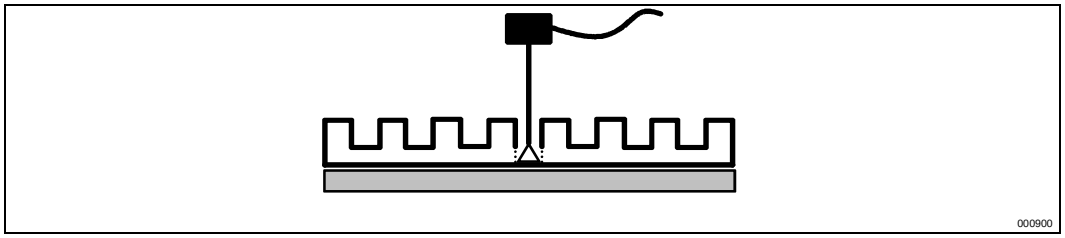


Figure 21. Technique for Measuring T_{PLATE} with 90° Angle Attachment

7. MECHANICAL SPECIFICATIONS

The processor use S.E.C. cartridge package technology. The S.E.C. cartridge contains the processor core, OCVR and other components. The S.E.C. cartridge package connects to the baseboard through an edge connector. Mechanical specifications for the processor are given in this section. See Section 1.1.1 for a complete terminology listing.

Figure 22 shows the thermal plate side view and the cover side view of the processor. Figure 23 shows the S.E.C. cartridge cooling solution attachment feature details on the thermal plate and depict package form factor dimensions and retention enabling features of the S.E.C. cartridge. The processor edge connector defined in this document is referred to as "SC330.1". This connector definition is mechanically the same as the existing SC 300 (formerly Slot 2). See the SC330 connector specifications for further details on the edge connector.

Table 50 and Table 51 provide the edge finger and SC330.1 connector signal definitions for processor. The signal locations on the SC330 edge connector are to be used for signal routing, simulation and component placement on the baseboard.

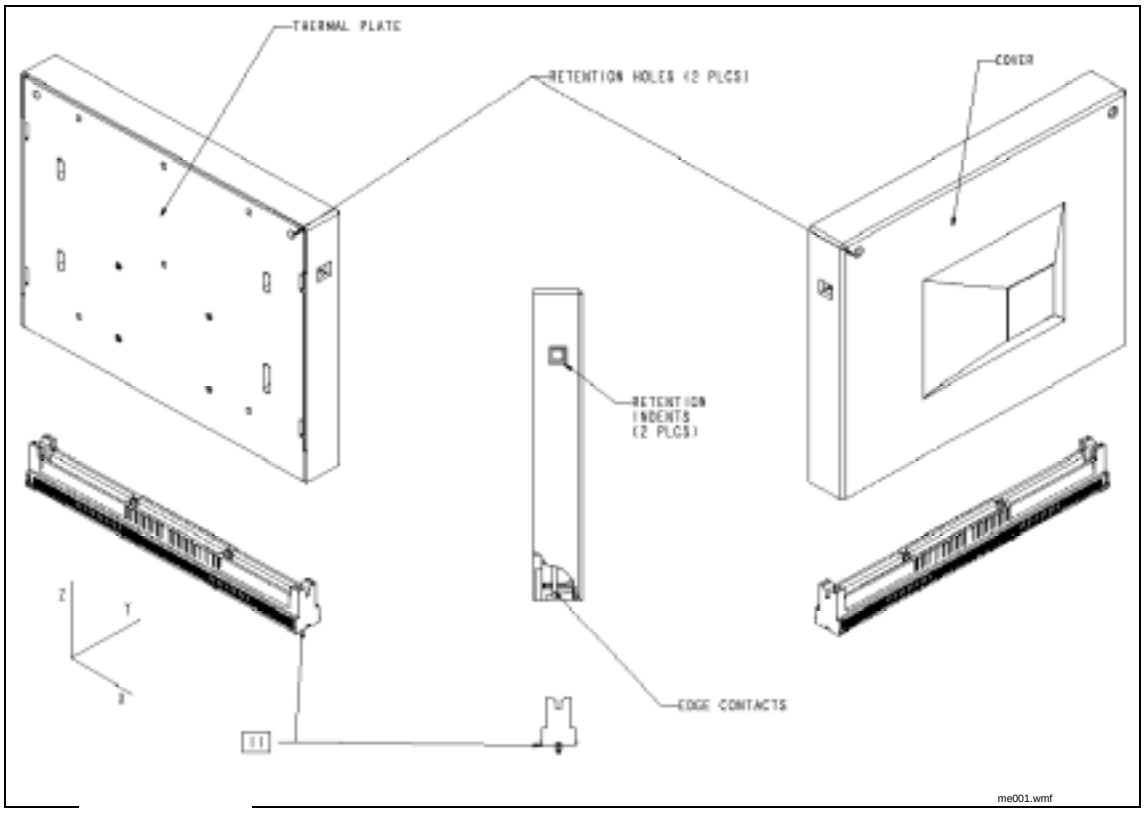


Figure 22. Isometric View of S.E.C. Cartridge

NOTES: Use of retention holes and retention indents are optional.
11. For SC330 connector specifications, see the *SC330 Connector Specification*.
12. All dimensions in inches for figures 23 thru 28.

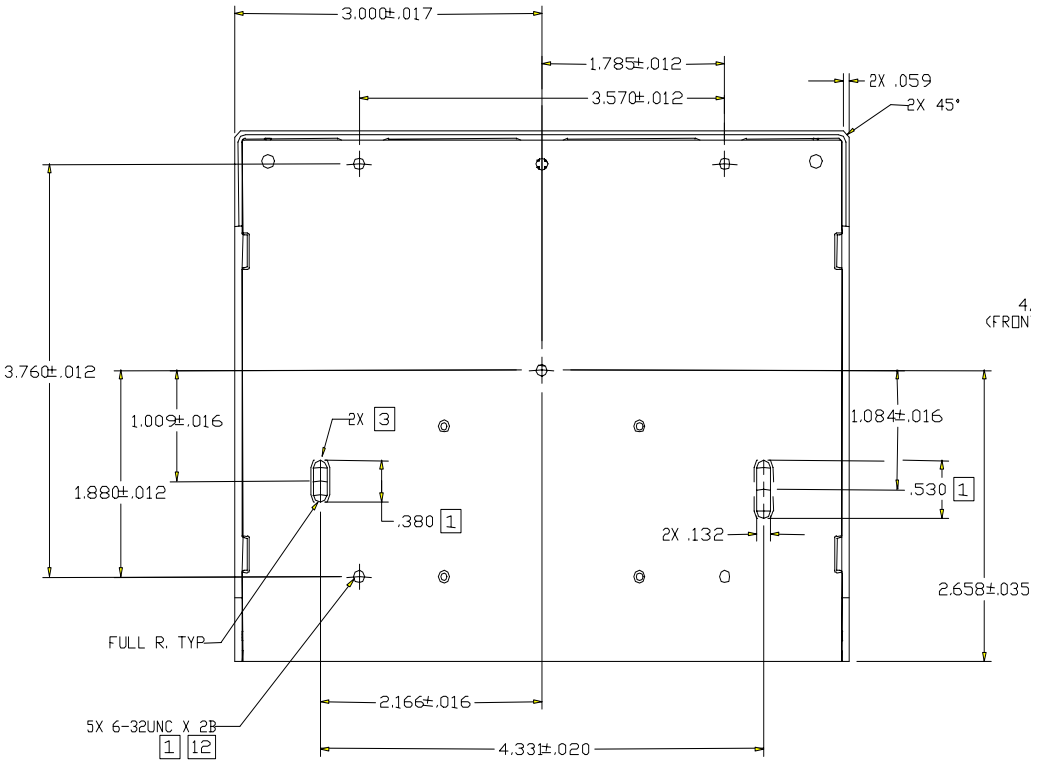


Figure 23. S.E.C. Cartridge Cooling Solution Attach Details (Notes follow)

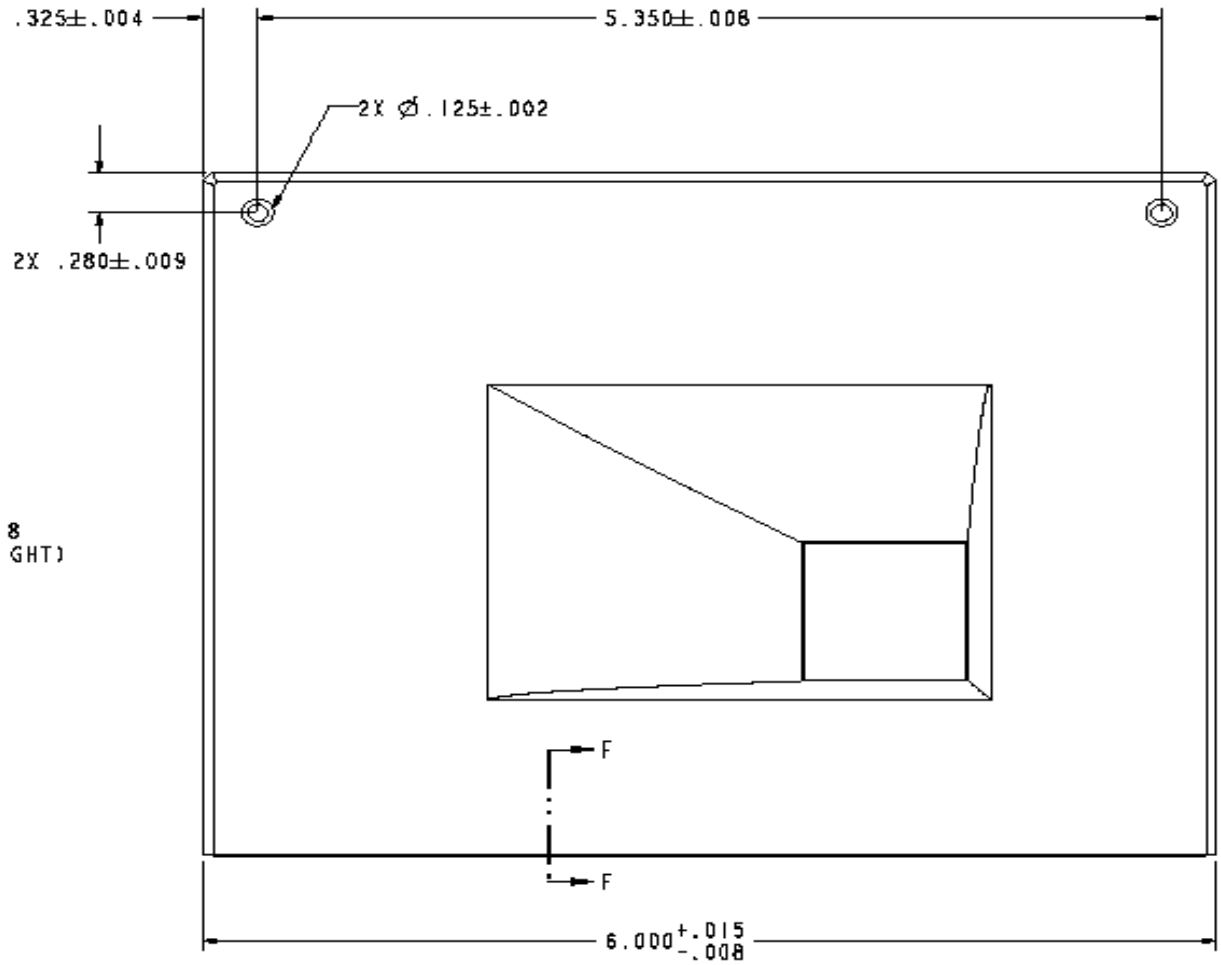


Figure 24. S.E.C. Cartridge Retention Enabling Details (Notes follow)

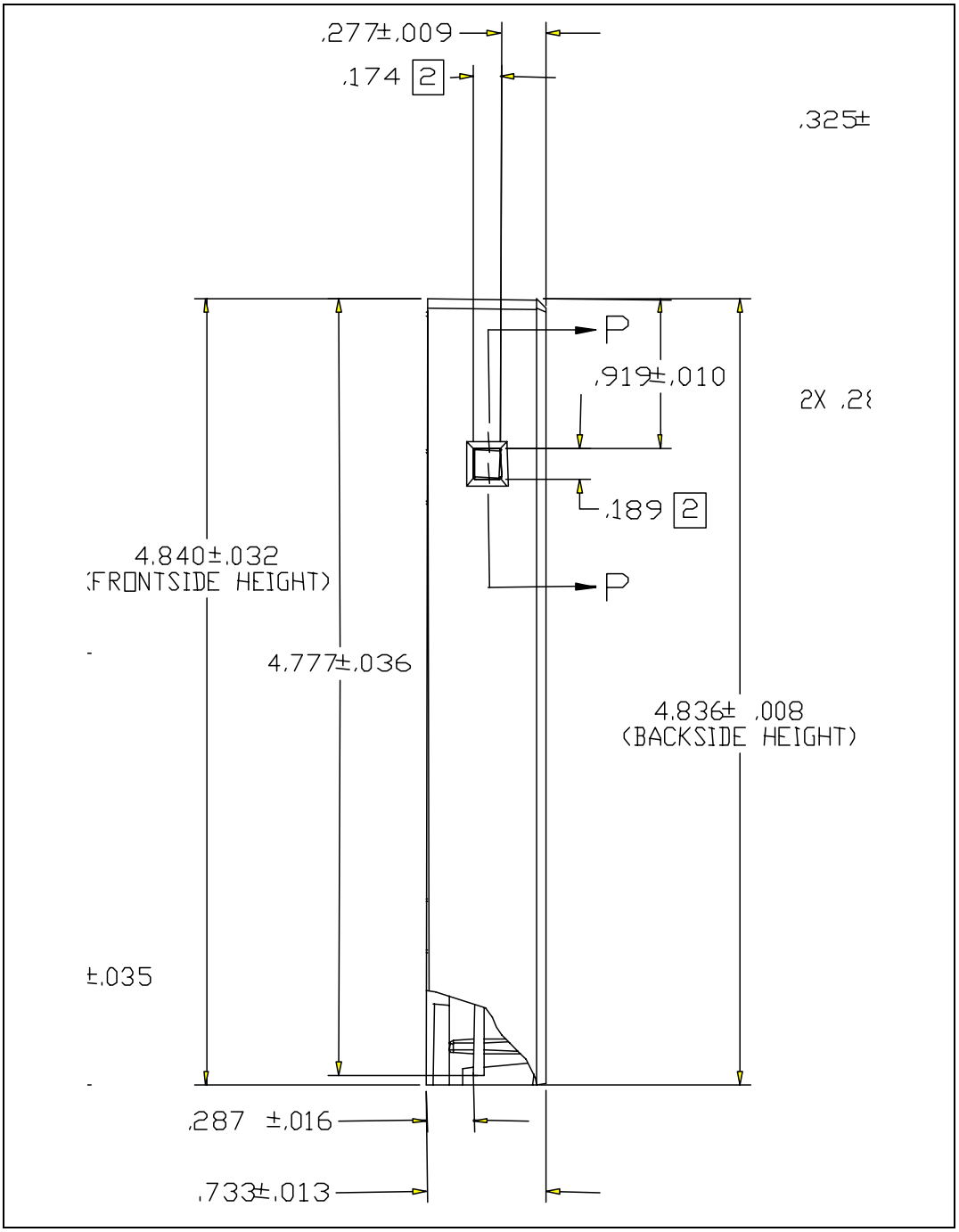


Figure 25. SEC Cartridge Retention Enabling Details

1. Maximum protrusions of the mechanical heatsink attach media into cartridge during assembly or in an installed condition not to exceed 0.160” from external face of thermal plate.
2. Specified cover retention indent dimension is at the external end of the indent. Indent walls have 1.0-degree draft, with the wider section on the external end.
3. Clip extension on internal surface of retention slots should be as little as possible and not to exceed 0.040”.
12. Tapped holes for cooling solution attach. Max torque recommendation for a screw in tapped hole is 8±1 inch-lb.

7.1 Weight

The maximum weight of a processor and thermal solution is approximately 500 grams.

7.2 Cartridge to Connector Mating Details

The staggered edge connector layout makes the processor susceptible to damage from hot socketing (inserting the cartridge while power is applied to the connector). Extra care should be taken to ensure hot socketing does not occur. The electrical and mechanical integrity of the processor edge fingers are specified for up to 50 insertion/extraction cycles.

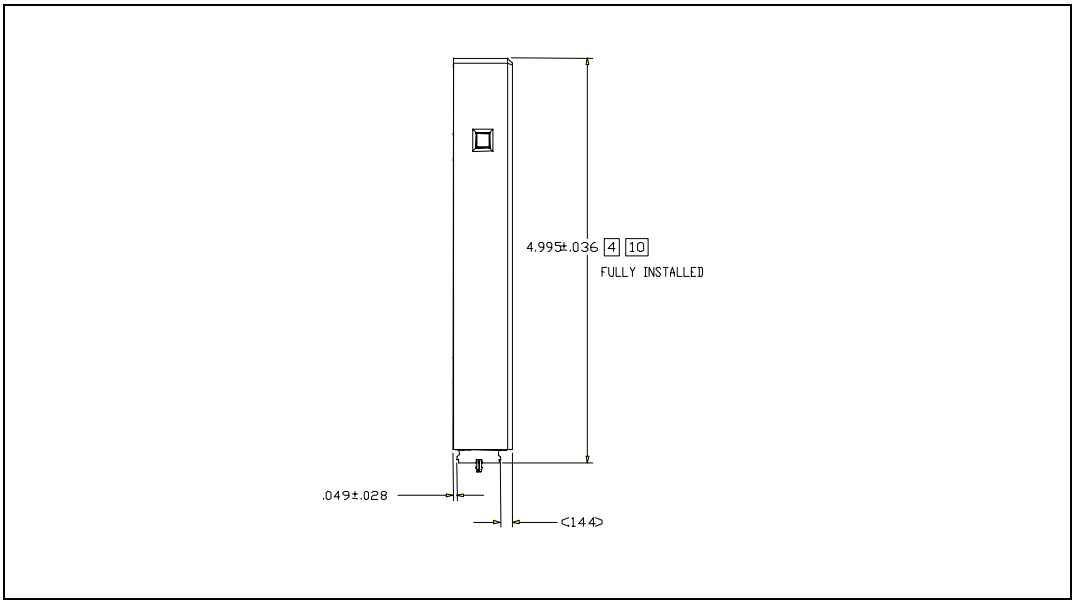


Figure 26. Side View of Connector Mating Details

NOTES:

4. Dimensional variation when cartridge is fully installed and the substrate is bottomed in the connector. Actual system installed height and tolerance is subject to the user's manufacturing tolerance of SC330 connector to the baseboard.
5. Retention devices for this cartridge must accommodate this cartridge "Float" relative to connector, without preload to the edge contacts in "X" and "Y" axes. (See figure 22 for axis orientation)
10. Fully installed dimensions must be maintained by the user's retention device. Cartridge backout from fully installed position may not exceed 0.020.

Figure 27. Top View of Cartridge Insertion Pressure Points

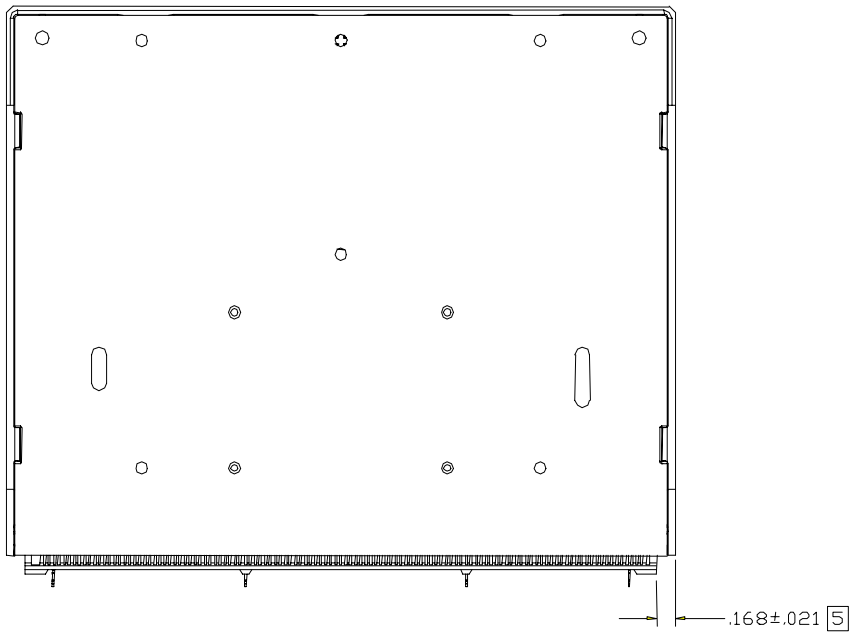


Figure 28. Front View of Connector Mating Details

NOTES:
Retention devices for this cartridge must accommodate this cartridge “Float” relative to connector, without preload to the edge contacts in “X” and “Y” axes.

7.3 Substrate Edge Finger Signal Listing

Table 50 is the processor substrate edge finger listing in order by pin number. Table 51 is the processor substrate edge connector listing in order by pin name. These tables reflect the new SC330.1 pin definition, new or changed pins definitions are shown in **bold**.

Table 50. Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A1	**RESERVED_A1**	**DO NOT CONNECT**	B1	PWR_EN[1]	Short to PWR_EN[0]
A2	VCC_TAP	TAP Supply	B2	VCC_CORE	Cartridge Vcc
A3	**HV_EN#**	**OPEN (2.8V OCVR) or SHORT TO Vss (5V/12V OCVR)**	B3	**OCVR_OK**	**Open Drain Output**
A4	VSS	Ground	B4	TEST_VSS_B4	Pull down to V_{SS}
A5	VTT	AGTL+ V_{TT} Supply	B5	VCC_CORE	Cartridge Vcc
A6	VTT	AGTL+ V_{TT} Supply	B6	VTT	AGTL+ V_{TT} Supply
A7	**SELFSB1**	**CMOS Output**	B7	VTT	AGTL+ V_{TT} Supply
A8	VSS	Ground	B8	VCC_CORE	Cartridge Vcc
A9	SELFSB0	CMOS Input	B9	RESERVED_B9	DO NOT CONNECT
A10	VSS	Ground	B10	FLUSH#	CMOS Input
A11	**RESERVED_A11**	**DO NOT CONNECT (new designs)/ or pull-down (legacy).**	B11	VCC_CORE	Cartridge Vcc
A12	IERR#	CMOS Output	B12	SMI#	CMOS Input
A13	VSS	Ground	B13	INIT#	CMOS Input
A14	A20M#	CMOS Input	B14	VCC_CORE	Cartridge Vcc
A15	FERR#	CMOS Output	B15	STPCLK#	CMOS Input
A16	VSS	Ground	B16	TCK	TAP Clock
A17	IGNNE#	CMOS Input	B17	VCC_CORE	Cartridge Vcc
A18	TDI	TAP Input	B18	SLP#	CMOS Input
A19	VSS	Ground	B19	TMS	TAP Input
A20	TDO	TAP Output	B20	VCC_CORE	Cartridge Vcc
A21	PWRGD	CMOS Input	B21	TRST#	TAP Input
A22	VSS	Ground	B22	RESERVED_B22	DO NOT CONNECT
A23	**TEST_2.5_A23**	**Pull up to 2.5V**	B23	VCC_CORE	Cartridge Vcc
A24	THERMTRIP#	CMOS Output	B24	RESERVED_B24	DO NOT CONNECT
A25	VSS	Ground	B25	RESERVED_B25	DO NOT CONNECT
A26	**OCVR_EN**	**CMOS INPUT**	B26	VCC_CORE	Cartridge Vcc
A27	LINT[0]	CMOS Input	**B27**	**TEST_2.5_B27**	**Pull up to 2.5V**
A28	VSS	Ground	B28	LINT[1]	CMOS Input
A29	PICD[0]	CMOS I/O	B29	VCC_CORE	Cartridge Vcc
A30	PREQ#	CMOS Input	B30	PICCLK	APIC Clock Input
A31	VSS	Ground	B31	PICD[1]	CMOS I/O
A32	BP#[3]	AGTL+ I/O	B32	VCC_CORE	Cartridge Vcc
A33	BPM#[0]	AGTL+ I/O	B33	BP#[2]	AGTL+ I/O
A34	VSS	Ground	B34	RESERVED_B34	DO NOT CONNECT
A35	BINIT#	AGTL+ I/O	B35	VCC_CORE	Cartridge Vcc
A36	DEP#[0]	AGTL+ I/O	B36	PRDY#	AGTL+ Output
A37	VSS	Ground	B37	BPM#[1]	AGTL+ I/O
A38	DEP#[1]	AGTL+ I/O	B38	VCC_CORE	Cartridge Vcc
A39	DEP#[3]	AGTL+ I/O	B39	DEP#[2]	AGTL+ I/O

Table 50. Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A40	VSS	Ground	B40	DEP#[4]	AGTL+ I/O
A41	DEP#[5]	AGTL+ I/O	B41	VCC_CORE	Cartridge Vcc
A42	DEP#[6]	AGTL+ I/O	B42	DEP#[7]	AGTL+ I/O
A43	VSS	Ground	B43	D#[62]	AGTL+ I/O
A44	D#[61]	AGTL+ I/O	B44	VCC_CORE	Cartridge Vcc
A45	D#[55]	AGTL+ I/O	B45	D#[58]	AGTL+ I/O
A46	VSS	Ground	B46	D#[63]	AGTL+ I/O
A47	D#[60]	AGTL+ I/O	B47	VCC_CORE	Cartridge Vcc
A48	D#[53]	AGTL+ I/O	B48	D#[56]	AGTL+ I/O
A49	VSS	Ground	B49	D#[50]	AGTL+ I/O
A50	D#[57]	AGTL+ I/O	B50	VCC_CORE	Cartridge Vcc
A51	D#[46]	AGTL+ I/O	B51	D#[54]	AGTL+ I/O
A52	VSS	Ground	B52	D#[59]	AGTL+ I/O
A53	D#[49]	AGTL+ I/O	B53	VCC_CORE	Cartridge Vcc
A54	D#[51]	AGTL+ I/O	B54	D#[48]	AGTL+ I/O
A55	VSS	Ground	B55	D#[52]	AGTL+ I/O
A56	**VIN_SENSE**	**CMOS I/O**	B56	VCC_CORE	Cartridge Vcc
A57	VSS	Ground	**B57**	**L2_SENSE**	**CMOS I/O**
A58	D#[42]	AGTL+ I/O	B58	VCC_CORE	Cartridge Vcc
A59	D#[45]	AGTL+ I/O	B59	D#[41]	AGTL+ I/O
A60	VSS	Ground	B60	D#[47]	AGTL+ I/O
A61	D#[39]	AGTL+ I/O	B61	VCC_CORE	Cartridge Vcc
A62	TEST_2.5_A62	Pull up to 2.5V	B62	D#[44]	AGTL+ I/O
A63	VSS	Ground	B63	D#[36]	AGTL+ I/O
A64	D#[43]	AGTL+ I/O	B64	VCC_CORE	Cartridge Vcc
A65	D#[37]	AGTL+ I/O	B65	D#[40]	AGTL+ I/O
A66	VSS	Ground	B66	D#[34]	AGTL+ I/O
A67	D#[33]	AGTL+ I/O	B67	VCC_CORE	Cartridge Vcc
A68	D#[35]	AGTL+ I/O	B68	D#[38]	AGTL+ I/O
A69	VSS	Ground	B69	D#[32]	AGTL+ I/O
A70	D#[31]	AGTL+ I/O	B70	VCC_CORE	Cartridge Vcc
A71	D#[30]	AGTL+ I/O	B71	D#[28]	AGTL+ I/O
A72	VSS	Ground	B72	D#[29]	AGTL+ I/O
A73	D#[27]	AGTL+ I/O	B73	VCC_CORE	Cartridge Vcc
A74	D#[24]	AGTL+ I/O	B74	D#[26]	AGTL+ I/O
A75	VSS	Ground	B75	D#[25]	AGTL+ I/O
A76	D#[23]	AGTL+ I/O	B76	VCC_CORE	Cartridge Vcc
A77	D#[21]	AGTL+ I/O	B77	D#[22]	AGTL+ I/O
A78	VSS	Ground	B78	D#[19]	AGTL+ I/O
A79	D#[16]	AGTL+ I/O	B79	VCC_CORE	Cartridge Vcc
A80	D#[13]	AGTL+ I/O	B80	D#[18]	AGTL+ I/O
A81	VSS	Ground	B81	D#[20]	AGTL+ I/O
A82	TEST_VTT_A82	Pull up to VTT	B82	VCC_CORE	Cartridge Vcc
A83	RESERVED_A83	DO NOT CONNECT	**B83**	**CORE_AN_VSENSE**	**OCVR Analog Output**
A84	VSS	Ground	B84	RESERVED_B84	DO NOT CONNECT
A85	D#[11]	AGTL+ I/O	B85	VCC_CORE	Cartridge Vcc
A86	D#[10]	AGTL+ I/O	B86	D#[17]	AGTL+ I/O
A87	VSS	Ground	B87	D#[15]	AGTL+ I/O
A88	D#[14]	AGTL+ I/O	B88	VCC_CORE	Cartridge Vcc
A89	D#[09]	AGTL+ I/O	B89	D#[12]	AGTL+ I/O
A90	VSS	Ground	B90	D#[07]	AGTL+ I/O
A91	D#[08]	AGTL+ I/O	B91	VCC_CORE	Cartridge Vcc
A92	D#[05]	AGTL+ I/O	B92	D#[06]	AGTL+ I/O
A93	VSS	Ground	B93	D#[04]	AGTL+ I/O
A94	D#[03]	AGTL+ I/O	B94	VCC_CORE	Cartridge Vcc
A95	D#[01]	AGTL+ I/O	B95	D#[02]	AGTL+ I/O

Table 50. Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A96	VSS	Ground	B96	D#[00]	AGTL+ I/O
A97	BCLK	System Bus Clock	B97	VCC_CORE	Cartridge Vcc
A98	TEST_ VSS _A98	Pull down to VSS	B98	RESET#	AGTL+ Input
A99	VSS	Ground	B99	N/C	
A100	BERR#	AGTL+ I/O	B100	VCC_CORE	Cartridge Vcc
A101	A#[33]	AGTL+ I/O	B101	A#[35]	AGTL+ I/O
A102	VSS	Ground	B102	A#[32]	AGTL+ I/O
A103	A#[34]	AGTL+ I/O	B103	VCC_CORE	Cartridge Vcc
A104	A#[30]	AGTL+ I/O	B104	A#[29]	AGTL+ I/O
A105	VSS	Ground	B105	A#[26]	AGTL+ I/O
A106	A#[31]	AGTL+ I/O	B106	VCC_L2	L2 Cache Vcc
A107	A#[27]	AGTL+ I/O	B107	A#[24]	AGTL+ I/O
A108	VSS	Ground	B108	A#[28]	AGTL+ I/O
A109	A#[22]	AGTL+ I/O	B109	VCC_L2	L2 Cache Vcc
A110	A#[23]	AGTL+ I/O	B110	A#[20]	AGTL+ I/O
A111	VSS	Ground	B111	A#[21]	AGTL+ I/O
A112	A#[19]	AGTL+ I/O	B112	VCC_L2	L2 Cache Vcc
A113	A#[18]	AGTL+ I/O	B113	A#[25]	AGTL+ I/O
A114	VSS	Ground	B114	A#[15]	AGTL+ I/O
A115	A#[16]	AGTL+ I/O	B115	VCC_L2	L2 Cache Vcc
A116	A#[13]	AGTL+ I/O	B116	A#[17]	AGTL+ I/O
A117	VSS	Ground	B117	A#[11]	AGTL+ I/O
A118	A#[14]	AGTL+ I/O	B118	VCC_L2	L2 Cache Vcc
A119	VSS	Ground	B119	A#[12]	AGTL+ I/O
A120	A#[10]	AGTL+ I/O	B120	VCC_L2	L2 Cache Vcc
A121	A#[05]	AGTL+ I/O	B121	A#[08]	AGTL+ I/O
A122	VSS	Ground	B122	A#[07]	AGTL+ I/O
A123	A#[09]	AGTL+ I/O	B123	VCC_L2	L2 Cache Vcc
A124	A#[04]	AGTL+ I/O	B124	A#[03]	AGTL+ I/O
A125	VSS	Ground	B125	A#[06]	AGTL+ I/O
A126	RESERVED_A126	DO NOT CONNECT	B126	VCC_L2	L2 Cache Vcc
A127	BNR#	AGTL+ I/O	B127	AERR#	AGTL+ I/O
A128	VSS	Ground	B128	REQ#[0]	AGTL+ I/O
A129	BPRI#	AGTL+ Input	B129	VCC_L2	L2 Cache Vcc
A130	TRDY#	AGTL+ Input	B130	REQ#[1]	AGTL+ I/O
A131	VSS	Ground	B131	REQ#[4]	AGTL+ I/O
A132	DEFER#	AGTL+ Input	B132	VCC_L2	L2 Cache Vcc
A133	REQ#[2]	AGTL+ I/O	B133	LOCK#	AGTL+ I/O
A134	VSS	Ground	B134	DRDY#	AGTL+ I/O
A135	REQ#[3]	AGTL+ I/O	B135	VCC_L2	L2 Cache Vcc
A136	HITM#	AGTL+ I/O	B136	RS#[0]	AGTL+ Input
A137	VSS	Ground	B137	HIT#	AGTL+ I/O
A138	DBSY#	AGTL+ I/O	B138	VCC_L2	L2 Cache Vcc
A139	RS#[1]	AGTL+ Input	B139	RS#[2]	AGTL+ Input
A140	VSS	Ground	B140	RP#	AGTL+ I/O
A141	BR2#	AGTL+ Input	B141	VCC_L2	L2 Cache Vcc
A142	BR0#	AGTL+ I/O	B142	BR3#	AGTL+ Input
A143	VSS	Ground	B143	BR1#	AGTL+ Input
A144	ADS#	AGTL+ I/O	B144	VCC_L2	L2 Cache Vcc
A145	AP#[0]	AGTL+ I/O	B145	RSP#	AGTL+ Input
A146	VSS	Ground	B146	AP#[1]	AGTL+ I/O
A147	VID_CORE[2]	Open or Short to VSS	B147	VCC_L2	L2 Cache Vcc
A148	VID_CORE[1]	Open or Short to VSS	B148	WP	SMBus Input
A149	VSS	Ground	B149	VID_CORE[3]	Open or Short to VSS

Table 50. Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Pin No.	Pin Name	Signal Buffer Type
A150	VID_CORE[4]	Open or Short to VSS	B150	VCC_L2	L2 Cache Vcc
A151	SMBALERT#	SMBus Alert	B151	VID_CORE[0]	Open or Short to VSS
A152	VSS	Ground	B152	VID_L2[0]	Open or Short to VSS
A153	VID_L2[2]	Open or Short to VSS	B153	VCC_L2	L2 Cache Vcc
A154	VID_L2[1]	Open or Short to VSS	B154	VID_L2[4]	Open or Short to VSS
A155	VSS	Ground	B155	VID_L2[3]	Open or Short to VSS
A156	V_{TT}	AGTL+ V_{TT} Supply	B156	VCC_L2	L2 Cache Vcc
A157	V_{TT}	AGTL+ V_{TT} Supply	B157	VTT	AGTL+ V_{TT} Supply
A158	VSS	Ground	B158	VTT	AGTL+ V_{TT} Supply
A159	SA2	SMBus Input	B159	VCC_L2	L2 Cache Vcc
A160	VCC_SM	SMBus Supply	B160	SMBCLK	SMBus Clock
A161	VSS	Ground	B161	SMBDAT	SMBus Data
A162	SA1	SMBus Input	B162	VCC_L2	L2 Cache Vcc
A163	SA0	SMBus Input	B163	RESERVED_B163	DO NOT CONNECT
A164	VSS	Ground	**B164**	**RESERVED_B164**	**DO NOT CONNECT**
A165	PWR_EN[0]	Short to PWR_EN[1]	**B165**	**RESERVED_B165**	**DO NOT CONNECT**

Table 51. Signal Listing in Order by Pin Name

Pin No.	Pin Name	Signal Buffer Type
B124	A#[03]	AGTL+ I/O
A124	A#[04]	AGTL+ I/O
A121	A#[05]	AGTL+ I/O
B125	A#[06]	AGTL+ I/O
B122	A#[07]	AGTL+ I/O
B121	A#[08]	AGTL+ I/O
A123	A#[09]	AGTL+ I/O
A120	A#[10]	AGTL+ I/O
B117	A#[11]	AGTL+ I/O
B119	A#[12]	AGTL+ I/O
A116	A#[13]	AGTL+ I/O
A118	A#[14]	AGTL+ I/O
B114	A#[15]	AGTL+ I/O
A115	A#[16]	AGTL+ I/O
B116	A#[17]	AGTL+ I/O
A113	A#[18]	AGTL+ I/O
A112	A#[19]	AGTL+ I/O
B110	A#[20]	AGTL+ I/O
B111	A#[21]	AGTL+ I/O
A109	A#[22]	AGTL+ I/O
A110	A#[23]	AGTL+ I/O
B107	A#[24]	AGTL+ I/O
B113	A#[25]	AGTL+ I/O
B105	A#[26]	AGTL+ I/O
A107	A#[27]	AGTL+ I/O
B108	A#[28]	AGTL+ I/O
B104	A#[29]	AGTL+ I/O
A104	A#[30]	AGTL+ I/O
A106	A#[31]	AGTL+ I/O
B102	A#[32]	AGTL+ I/O
A101	A#[33]	AGTL+ I/O
A103	A#[34]	AGTL+ I/O
B101	A#[35]	AGTL+ I/O
A14	A20M#	CMOS Input
A144	ADS#	AGTL+ I/O
B127	AERR#	AGTL+ I/O
A145	AP#[0]	AGTL+ I/O
B146	AP#[1]	AGTL+ I/O
A97	BCLK	System Bus Clock
A100	BERR#	AGTL+ I/O
A35	BINIT#	AGTL+ I/O
A127	BNR#	AGTL+ I/O
B33	BP#[2]	AGTL+ I/O
A32	BP#[3]	AGTL+ I/O
A33	BPM#[0]	AGTL+ I/O
B37	BPM#[1]	AGTL+ I/O
A129	BPRI#	AGTL+ Input
A142	BR0#	AGTL+ I/O
B143	BR1#	AGTL+ Input
A141	BR2#	AGTL+ Input
B142	BR3#	AGTL+ Input
B83	**CORE_AN_VSENSE**	**OCVR Analog Output**
B96	D#[00]	AGTL+ I/O
A95	D#[01]	AGTL+ I/O
B95	D#[02]	AGTL+ I/O
A94	D#[03]	AGTL+ I/O

Pin No.	Pin Name	Signal Buffer Type
B93	D#[04]	AGTL+ I/O
A92	D#[05]	AGTL+ I/O
B92	D#[06]	AGTL+ I/O
B90	D#[07]	AGTL+ I/O
A91	D#[08]	AGTL+ I/O
A89	D#[09]	AGTL+ I/O
A86	D#[10]	AGTL+ I/O
A85	D#[11]	AGTL+ I/O
B89	D#[12]	AGTL+ I/O
A80	D#[13]	AGTL+ I/O
A88	D#[14]	AGTL+ I/O
B87	D#[15]	AGTL+ I/O
A79	D#[16]	AGTL+ I/O
B86	D#[17]	AGTL+ I/O
B80	D#[18]	AGTL+ I/O
B78	D#[19]	AGTL+ I/O
B81	D#[20]	AGTL+ I/O
A77	D#[21]	AGTL+ I/O
B77	D#[22]	AGTL+ I/O
A76	D#[23]	AGTL+ I/O
A74	D#[24]	AGTL+ I/O
B75	D#[25]	AGTL+ I/O
B74	D#[26]	AGTL+ I/O
A73	D#[27]	AGTL+ I/O
B71	D#[28]	AGTL+ I/O
B72	D#[29]	AGTL+ I/O
A71	D#[30]	AGTL+ I/O
A70	D#[31]	AGTL+ I/O
B69	D#[32]	AGTL+ I/O
A67	D#[33]	AGTL+ I/O
B66	D#[34]	AGTL+ I/O
A68	D#[35]	AGTL+ I/O
B63	D#[36]	AGTL+ I/O
A65	D#[37]	AGTL+ I/O
B68	D#[38]	AGTL+ I/O
A61	D#[39]	AGTL+ I/O
B65	D#[40]	AGTL+ I/O
B59	D#[41]	AGTL+ I/O
A58	D#[42]	AGTL+ I/O
A64	D#[43]	AGTL+ I/O
B62	D#[44]	AGTL+ I/O
A59	D#[45]	AGTL+ I/O
A51	D#[46]	AGTL+ I/O
B60	D#[47]	AGTL+ I/O
B54	D#[48]	AGTL+ I/O
A53	D#[49]	AGTL+ I/O
B49	D#[50]	AGTL+ I/O
A54	D#[51]	AGTL+ I/O
B55	D#[52]	AGTL+ I/O
A48	D#[53]	AGTL+ I/O
B51	D#[54]	AGTL+ I/O
A45	D#[55]	AGTL+ I/O
B48	D#[56]	AGTL+ I/O
A50	D#[57]	AGTL+ I/O
B45	D#[58]	AGTL+ I/O
B52	D#[59]	AGTL+ I/O
A47	D#[60]	AGTL+ I/O
A44	D#[61]	AGTL+ I/O
B43	D#[62]	AGTL+ I/O
B46	D#[63]	AGTL+ I/O

Pin No.	Pin Name	Signal Buffer Type
A138	DBSY#	AGTL+ I/O
A132	DEFER#	AGTL+ Input
A36	DEP#[0]	AGTL+ I/O
A38	DEP#[1]	AGTL+ I/O
B39	DEP#[2]	AGTL+ I/O
A39	DEP#[3]	AGTL+ I/O
B40	DEP#[4]	AGTL+ I/O
A41	DEP#[5]	AGTL+ I/O
A42	DEP#[6]	AGTL+ I/O
B42	DEP#[7]	AGTL+ I/O
B134	DRDY#	AGTL+ I/O
A15	FERR#	CMOS Output
B10	FLUSH#	CMOS Input
B99	N/C	
B137	HIT#	AGTL+ I/O
A136	HITM#	AGTL+ I/O
A3	**HV_EN#**	**OPEN (2.8V version) SHORT (5V/12V version)**
A12	IERR#	CMOS Output
A17	IGNNE#	CMOS Input
B13	INIT#	CMOS Input
A27	LINT[0]	CMOS Input
B28	LINT[1]	CMOS Input
B133	LOCK#	AGTL+ I/O
B57	**L2_SENSE**	**CMOS I/O**
B3	**OCVR_OK**	**Open Drain Output**
A26	**OCVR_EN**	**CMOS INPUT**
B30	PICCLK	APIC Clock Input
A29	PICD[0]	CMOS I/O
B31	PICD[1]	CMOS I/O
B36	PRDY#	AGTL+ Output
A30	PREQ#	CMOS Input
A165	PWR_EN[0]	Short to PWR_EN[1]
B1	PWR_EN[1]	Short to PWR_EN[0]
A21	PWRGOOD	CMOS Input
B128	REQ#[0]	AGTL+ I/O
B130	REQ#[1]	AGTL+ I/O
A133	REQ#[2]	AGTL+ I/O
A135	REQ#[3]	AGTL+ I/O
B131	REQ#[4]	AGTL+ I/O
A1	**RESERVED_A1**	**DO NOT CONNECT**
A11	**RESERVED_A11**	**DO NOT CONNECT**
A126	RESERVED_A126	DO NOT CONNECT
B163	RESERVED_B163	DO NOT CONNECT
B164	**RESERVED_B164**	**DO NOT CONNECT**
B165	**RESERVED_B165**	**DO NOT CONNECT**
B22	RESERVED_B22	DO NOT CONNECT
B24	RESERVED_B24	DO NOT CONNECT
B25	RESERVED_B25	DO NOT CONNECT
B34	RESERVED_B34	DO NOT CONNECT
B84	RESERVED_B84	DO NOT CONNECT
B9	RESERVED_B9	DO NOT CONNECT
B98	RESET#	AGTL+ Input
B140	RP#	AGTL+ I/O
B136	RS#[0]	AGTL+ Input
A139	RS#[1]	AGTL+ Input
B139	RS#[2]	AGTL+ Input
B145	RSP#	AGTL+ Input
A163	SA0	SMBus Input
A162	SA1	SMBus Input

Pin No.	Pin Name	Signal Buffer Type
A159	SA2	SMBus Input
A9	SELFSB0	CMOS Input
A7	**SELFSB1**	**CMOS Output**
B18	SLP#	CMOS Input
A151	SMBALERT#	SMBus Alert
B160	SMBCLK	SMBus Clock
B161	SMBDAT	SMBus I/O
B12	SMI#	CMOS Input
B15	STPCLK#	CMOS Input
B16	TCK	TAP Clock
A18	TDI	TAP Input
A20	TDO	TAP Output
A23	**TEST_2.5_A23**	**Pull up to 2.5V**
A62	TEST_2.5_A62	Pull up to 2.5V
B27	**TEST_2.5_B27**	**Pull up to 2.5V**
A98	TEST_VSS_A98	Pull down to V_{SS}
B4	TEST_VSS_B4	Pull down to V_{SS}
A82	TEST_VTT_A82	Pull up to V_{TT}
A24	THERMTRIP#	CMOS Output
B19	TMS	TAP Input
A130	TRDY#	AGTL+ Input
B21	TRST#	TAP Input
B100	VCC_CORE	Cartridge Vcc
B103	VCC_CORE	Cartridge Vcc
B11	VCC_CORE	Cartridge Vcc
B14	VCC_CORE	Cartridge Vcc
B17	VCC_CORE	Cartridge Vcc
B2	VCC_CORE	Cartridge Vcc
B20	VCC_CORE	Cartridge Vcc
B23	VCC_CORE	Cartridge Vcc
B26	VCC_CORE	Cartridge Vcc
B29	VCC_CORE	Cartridge Vcc
B32	VCC_CORE	Cartridge Vcc
B35	VCC_CORE	Cartridge Vcc
B38	VCC_CORE	Cartridge Vcc
B41	VCC_CORE	Cartridge Vcc
B44	VCC_CORE	Cartridge Vcc
B47	VCC_CORE	Cartridge Vcc
B5	VCC_CORE	Cartridge Vcc
B50	VCC_CORE	Cartridge Vcc
B53	VCC_CORE	Cartridge Vcc
B56	VCC_CORE	Cartridge Vcc
B58	VCC_CORE	Cartridge Vcc
B61	VCC_CORE	Cartridge Vcc
B64	VCC_CORE	Cartridge Vcc
B67	VCC_CORE	Cartridge Vcc
B70	VCC_CORE	Cartridge Vcc
B73	VCC_CORE	Cartridge Vcc
B76	VCC_CORE	Cartridge Vcc
B79	VCC_CORE	Cartridge Vcc
B8	VCC_CORE	Cartridge Vcc
B82	VCC_CORE	Cartridge Vcc
B85	VCC_CORE	Cartridge Vcc
B88	VCC_CORE	Cartridge Vcc
B91	VCC_CORE	Cartridge Vcc
B94	VCC_CORE	Cartridge Vcc
B97	VCC_CORE	Cartridge Vcc
B106	VCC_L2 (N/C)	L2 Cache Vcc
B109	VCC_L2 (N/C)	L2 Cache Vcc

Pin No.	Pin Name	Signal Buffer Type
B112	VCC_L2 (N/C)	L2 Cache Vcc
B115	VCC_L2 (N/C)	L2 Cache Vcc
B118	VCC_L2 (N/C)	L2 Cache Vcc
B120	VCC_L2 (N/C)	L2 Cache Vcc
B123	VCC_L2 (N/C)	L2 Cache Vcc
B126	VCC_L2 (N/C)	L2 Cache Vcc
B129	VCC_L2 (N/C)	L2 Cache Vcc
B132	VCC_L2 (N/C)	L2 Cache Vcc
B135	VCC_L2 (N/C)	L2 Cache Vcc
B138	VCC_L2 (N/C)	L2 Cache Vcc
B141	VCC_L2 (N/C)	L2 Cache Vcc
B144	VCC_L2 (N/C)	L2 Cache Vcc
B147	VCC_L2 (N/C)	L2 Cache Vcc
B150	VCC_L2 (N/C)	L2 Cache Vcc
B153	VCC_L2 (N/C)	L2 Cache Vcc
B156	VCC_L2 (N/C)	L2 Cache Vcc
B159	VCC_L2 (N/C)	L2 Cache Vcc
B162	VCC_L2 (N/C)	L2 Cache Vcc
A160	VCC_SM	SMBus Supply
A2	VCC_TAP	TAP Supply
A56	**VIN_SENSE**	**CMOS I/O**
B151	VID_CORE[0]	Open or Short to V_{SS}
A148	VID_CORE[1]	Open or Short to V_{SS}
A147	VID_CORE[2]	Open or Short to V_{SS}
B149	VID_CORE[3]	Open or Short to V_{SS}
A150	VID_CORE[4]	Open or Short to V_{SS}
B152	VID_L2[0]	Open or Short to V_{SS}
A154	VID_L2[1]	Open or Short to V_{SS}
A153	VID_L2[2]	Open or Short to V_{SS}
B155	VID_L2[3]	Open or Short to V_{SS}
B154	VID_L2[4]	Open or Short to V_{SS}
A10	VSS	Ground
A102	VSS	Ground
A105	VSS	Ground
A108	VSS	Ground
A111	VSS	Ground
A114	VSS	Ground
A117	VSS	Ground
A119	VSS	Ground
A122	VSS	Ground
A125	VSS	Ground
A128	VSS	Ground
A13	VSS	Ground
A131	VSS	Ground
A134	VSS	Ground
A137	VSS	Ground
A140	VSS	Ground
A143	VSS	Ground
A146	VSS	Ground
A149	VSS	Ground
A152	VSS	Ground
A155	VSS	Ground
A158	VSS	Ground
A16	VSS	Ground
A161	VSS	Ground
A164	VSS	Ground
A19	VSS	Ground
A22	VSS	Ground
A25	VSS	Ground

Pin No.	Pin Name	Signal Buffer Type
A28	VSS	Ground
A31	VSS	Ground
A34	VSS	Ground
A37	VSS	Ground
A4	VSS	Ground
A40	VSS	Ground
A43	VSS	Ground
A46	VSS	Ground
A49	VSS	Ground
A52	VSS	Ground
A55	VSS	Ground
A57	VSS	Ground
A60	VSS	Ground
A63	VSS	Ground
A66	VSS	Ground
A69	VSS	Ground
A72	VSS	Ground
A75	VSS	Ground
A78	VSS	Ground
A8	VSS	Ground
A81	VSS	Ground
A84	VSS	Ground
A87	VSS	Ground
A90	VSS	Ground
A93	VSS	Ground
A96	VSS	Ground
A99	VSS	Ground
A156	VTT	AGTL+ V_{TT} Supply
A157	VTT	AGTL+ V_{TT} Supply
A5	VTT	AGTL+ V_{TT} Supply
A6	VTT	AGTL+ V_{TT} Supply
B157	VTT	AGTL+ V_{TT} Supply
B158	VTT	AGTL+ V_{TT} Supply
B6	VTT	AGTL+ V_{TT} Supply
B7	VTT	AGTL+ V_{TT} Supply
B148	WP	SMBus Input

8. INTEGRATION TOOLS

The integration tool set for system designs will include an In-Target Probe (ITP) for program execution control, register/memory/IO access, and breakpoint control. This tool provides functionality commonly associated with debuggers and emulators. The ITP uses the on-chip debug features of the processor to provide program execution control. Use of the ITP will not affect the high-speed operations of the processor signals, ensuring the system can operate at full speed with the ITP attached.

This document describes the ITP as well as a number of technical issues that must be taken into account when including the ITP and logic analyzer interconnect tools in a debug strategy. Although the tool description that follows is specific to early tools available from Intel, similar tools may also be provided in the future by third-party vendors. Thus, the tools mentioned should not be considered as Intel's tools, but as debug tools in the generic sense.

In general, the information in this chapter may be used as a basis for including integration tools in any Pentium® III Xeon™ processor at 700 MHz and 900 MHz-based system design. The logic analyzer interconnect tool keep-out zones described in this chapter should be used as general guidelines for Pentium® III Xeon™ processor at 700 MHz and 900 MHz system design.

8.1 In-Target Probe (ITP)

An In-Target Probe (ITP) for the processor is a debug tool that allows access to on-chip debug features via a small port on the system board called the debug port. The ITP communicates to the processor through the debug port using a combination of hardware and software. The software is a Microsoft* Windows* NT* 4.0-based application running on a host PC. The hardware consists of a PCI board in the host PC connected to the signals that make up the processor debug interface. Due to the nature of the ITP, the processor may be controlled without affecting any high-speed signals. This ensures that the system can operate at full speed with the ITP attached. **Intel will use an ITP for internal debug and system validation and recommends that all Pentium® III Xeon™ processor at 700 MHz and 900 MHz-based system designs include a debug port**. This is especially important if Intel assistance is required in debugging a system-processor interrelationship issue.

8.1.1 PRIMARY FUNCTION

The primary function of an ITP is to provide a control and query interface for one or more processors. With an ITP, one can control program execution and have the ability to access processor registers, system memory and I/O. Thus, one can start and stop program execution using a variety of breakpoints, single-step the program at the assembly code level, as well as read and write registers, memory and I/O. The on-chip debug features will be controlled from a Microsoft* Windows* NT* 4.0 software application running on a Pentium® or Pentium® Pro processor-based PC with a PCI card slot (See Figure 29).

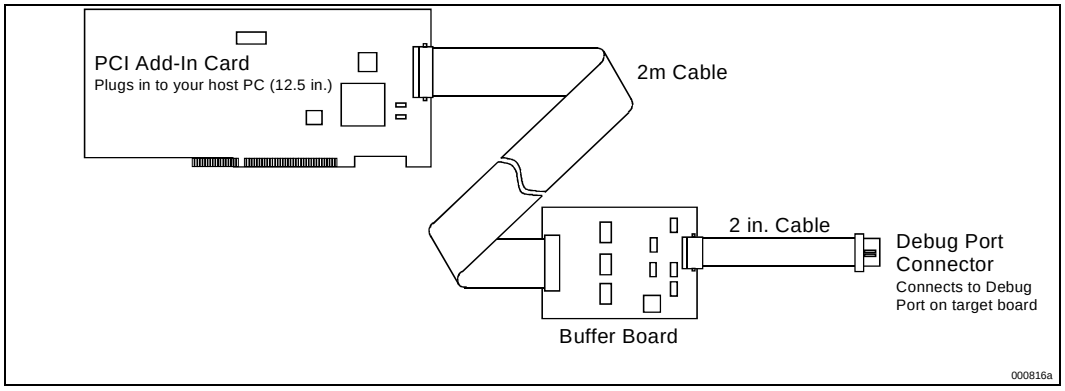


Figure 29. Hardware Components of the ITP

8.1.2 DEBUG PORT CONNECTOR DESCRIPTION

The ITP will connect to the system through the debug port. Recommended connectors, to mate the ITP cable with the debug port on the board, are available in either a vertical or right angle configuration. Both configurations fit into the same board footprint. The connectors are manufactured by AMP Incorporated and are in the AMPMODU System 50 line. Following are the AMP part numbers for the two connectors:

- Amp 30-pin shrouded vertical header: 104068-3
- Amp 30-pin shrouded right-angle header: 104069-5

NOTE

These are high density through hole connectors with pins on 0.050 in. by 0.100 in. centers. Do not confuse these with the more common 0.100 in. by 0.100 in. center headers.

The debug port must be mounted on the system baseboard; the processor does not contain a debug port.

8.1.3 KEEP OUT CONCERNS

Two keep out concerns need to be taken into account when designing a system that will support an ITP. First, system designers need to be aware that in order for the ITP cabling to egress the system under test, they must either remove the “skins” of the system under test, or, when this is not possible, design an aperture into the system.

Secondly, keep out regions will be required around the debug port connector. See Figure 30 for the keep out region required for the processor.

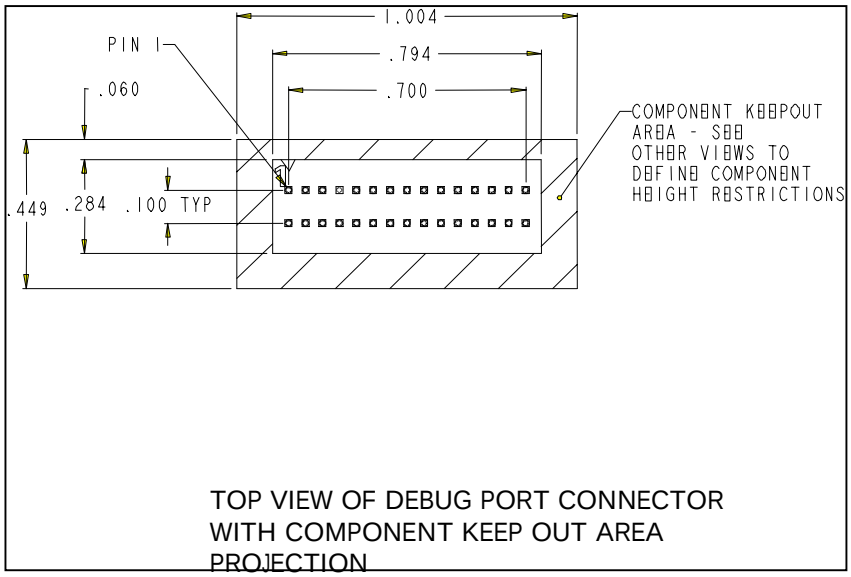


Figure 30. Debug Port Connector Keep Out Region

8.1.4 ADDITIONAL INTEGRATION TOOL MECHANICAL KEEP OUTS

Please contact your Integration Tools vendor for any additional mechanical keep out restrictions for the system design.

8.1.5 DEBUG PORT SIGNAL DESCRIPTIONS

Table 52 describes the debug port signals and provides the pin assignment.

Table 52. Debug Port Pinout Description and Requirements[1]

Name	Pin	Description	Specification Requirement	Notes
RESET#	1	Reset signal from MP cluster to ITP.	Terminate[2] signal properly at the debug port. Debug port must be at the end of the signal trace.	Connected to high-speed comparator (biased at 2/3 of the level found at the POWERON pin) on the ITP buffer board. Additional load does not change timing calculations for the processor bus agents if routed properly.
DBRESET#	3	Allows ITP to reset entire target system.	Tie signal to target system reset (recommendation): PWR_OK signal on PCIset as an ORed input). Pulled-up signal with the proper resistor (see Signal Notes section, following).	Open drain output from ITP to the target system. It will be held asserted for 100 ms; capacitance needs to be small enough to recognize assert. The pull-up resistor should be picked to (1) meet VIL of target system and (2) meet specified rise time.
TCK	5	The TAP (Test Access Port) clock from ITP to MP cluster.	Add 1.0KΩ pull-up resistor to $Vcc_{\_TAP}$ near driver. For MP systems, each processor should receive a separately buffered TCK. Add a series termination resistor or a Bessel filter on each output.	Poor routing can cause multiple clocking problems. Should be routed to all components in the boundary scan chain[3]. Simulations should be run to determine the proper value for series termination or Bessel filter, see figure 31.
TMS	7	Test mode select signal from ITP to MP cluster, controls the TAP finite state machine.	Add 1.0 KΩ pull-up resistor to $Vcc_{\_TAP}$ near driver. For MP systems, each processor should receive a separately buffered TMS. Add a series termination resistor on each output.	Operates synchronously with TCK. Should be routed to all components in the boundary scan chain[3]. Simulations should be run to determine the proper value for series termination.
TDI	8	Test data input signal from ITP to first component in boundary scan chain of MP cluster; inputs test instructions and data serially.	This signal is open-drain from the ITP. However, TDI is pulled up to $Vcc_{\_TAP}$ with ~150Ω on the processor. Add a 150 to 330Ω pull-up resistor (to $Vcc_{\_TAP}$) if TDI will not be connected directly to a processor.	Operates synchronously with TCK.
POWERON	9	Used by ITP to determine when target system power is ON and, once target system is ON, enables all debug port electrical interface activity. From target V_{TT} to ITP.	Add 1.5KΩ pull-up resistor (to V_{TT}).	If no power is applied, the ITP will not drive any signals; isolation provided using isolation gates. Voltage applied is internally used to set AGTL+ threshold (or reference) at 2/3 V_{TT}.
TDO	10	Test data output signal from last component in boundary scan chain of MP cluster to ITP; test output is read serially.	Add 150Ω pull-up resistor (to $Vcc_{\_TAP}$). Design pull-ups to route around empty processor sockets (so resistors are not in parallel).	Operates synchronously with TCK. Each processor has a 25Ω driver.
DBINST#	11	Indicates to target system that the ITP is installed.	Add ~10KΩ pull-up resistor.	Not required if boundary scan is not used in target system.
TRST#	12	Test reset signal from ITP to MP cluster, used to reset TAP logic.	Add ~680Ω pull-down. To disable TAP reset if ITP not installed.	Asynchronous input signal.

Table 52. Debug Port Pinout Description and Requirements[1]

Name	Pin	Description	Specification Requirement	Notes
BSEN#	14	Informs target system that ITP is using boundary scan.		Not required if boundary scan is not used in target system.
PREQ0#	16	PREQ0# signal, driven by ITP, makes requests to P0 to enter debug.	Add 150 to 330Ω pull-up resistor (to Vcc_{TAP}).	
PRDY0#	18	PRDY0# signal, driven by P0, informs ITP that P0 is ready for debug.	Terminate[2] signal properly at the debug port. Debug port must be at the end of the signal trace.	Connected to high-speed comparator (biased at 2/3 of the level found at the POWERON pin) on the ITP buffer board. Additional load does not change timing calculations for the processor bus agents if routed properly.
PREQ1#	20	PREQ1# signal from ITP to P1.	Add 150 to 330Ω pull-up resistor (to Vcc_{TAP})	
PRDY1#	22	PRDY1# signal from P1 to ITP.	Terminate[2] signal properly at the debug port. Debug port must be at the end of the signal trace.	Connected to high-speed comparator (biased at 2/3 of the level found at the POWERON pin) on the ITP buffer board. Additional load does not change timing calculations for the processor bus agents.
PREQ2#	24	PREQ2# signal from ITP to P2.	Add 150 to 330Ω pull-up resistor (to Vcc_{TAP}).	
PRDY2#	26	PRDY2# signal from ITP to P2.	Terminate[2] signal properly at the debug port. Debug port must be at the end of the signal trace.	Connected to high-speed comparator (biased at 2/3 of the level found at the POWERON pin) on the ITP buffer board. Additional load does not change timing calculations for the processor bus agents if routed properly.
PREQ3#	28	PREQ3# signal from ITP to P3.	Add 150 to 330Ω pull-up resistor (to Vcc_{TAP}).	
PRDY3#	30	PRDY3# signal from ITP to P3.	Terminate[2] signal properly at the debug port. Debug port must be at the end of the signal trace.	Connected to high-speed comparator (biased at 2/3 of the level found at the POWERON pin) on the ITP buffer board. Additional load does not change timing calculations for the processor bus agents if routed properly.
BCLK	29	Bus clock from the MP cluster.	Use a separate driver to drive signal to the debug port.	A separate driver should be used to avoid loading issues associated with having the ITP either installed or not installed.
GND	2, 4, 6, 13, 15, 17, 19, 21, 23, 25, 27	Signal ground.	Connect all pins to signal ground.	

NOTES:

1. Resistor values with "~" preceding them can vary from the specified value; use resistor as close as possible to the value specified.
2. Termination should include series (~240Ω) and AGTL+ termination (connected to 1.5V) resistors. See Figure 30A.
3. Signal should be at end of daisy chain and the boundary scan chain should be partitioned into two distinct sections to assist in debugging the system: one partition with only the processor(s) for system debug (i.e., used with the ITP) and another with all other components for manufacturing or system test.

8.1.6 DEBUG PORT SIGNAL NOTES

In general, all open drain AGTL+ outputs from the system must be retained at a proper logic level, whether or not the debug port is installed. RESET# from the processor system should be terminated at the debug port, as shown in Figure 30A. R_t should be a 150Ω on RESET#.

PRDYn# should have a similar layout, however R_t should be 50Ω to match board impedance rather than the normal 150Ω since there are only 2 loads on this signal.

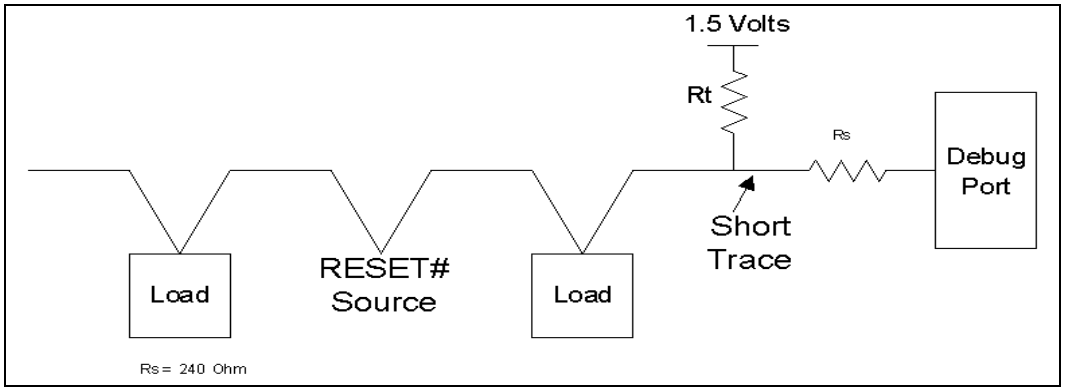


Figure 30A. AGTL+ Signal Termination

8.1.6.1 General Signal Quality Notes

Signals from the debug port are fed to the system from the ITP via a buffer board and a cable. If system signals routed to the debug port (i.e. TDO, PRDYn# and RESET#) are used elsewhere in the system, then dedicated drivers should be used to isolate the signals from reflections coming from the end of this cable. If the processor boundary scan signals are used elsewhere in the system, then the TDI, TMS, TCK, and TRST# signals from the debug port should be isolated from the system signals.

In general, no signals should be left floating. Thus, signals going from the debug port to the processor system should not be left floating. If they are left floating, there may be problems when the ITP is not plugged into the connector.

8.1.6.2 Signal Note: DBRESET#

The DBRESET# output signal from the ITP is an open drain with about 5Ω of R_{DS}. The usual implementation is to connect it to the PWROK open drain signal on the PCIset components as an OR input to initiate a system reset. In order for the DBRESET# signal to work properly, it must actually reset the entire target system. The signal should be pulled up (Intel recommends a 240Ω resistor, but system designers will need to fine tune specific system designs) to meet two considerations: (1) the signal must be able to meet V_{IL} of the system, and (2) it must allow the signal to meet the specified rise time. When asserted by the ITP, the DBRESET# signal will remain asserted for 100 ms. A large capacitance should not be present on this signal as it may prevent a full charge from building up within 100 ms.

8.1.6.3 Signal Note: TDO and TDI

The TDO signal of each processor has a 2.5V Tolerant open-drain driver. The TDI signal of each processor contains a 150Ω pull-up to Vcc_{TAP}. When connecting one processor to the next, or connecting to the TDI of the first processor, no external pull-up is required. However, the last processor of the chain does require a pull-up before passing the signal to the next device in the chain.

8.1.6.4 Signal Note: TCK and TMS

WARNING

A significant number of target systems have had signal integrity issues with the TCK signal. TCK is a critical clock signal and must be routed accordingly; make sure to observe power and ground plane integrity for this signal. Follow the guidelines below and assure the quality of the signal when beginning use of an ITP to debug your target.

Due to the number of loads on the TCK signal, special care should be taken when routing this. Poor routing can lead to multiple clocking of some agents on the debug chain, usually on the falling edge of TCK. This causes information to be lost through the chain and can result in bad commands being issued to some agents on the chain. Systems using other TCK routing schemes, particularly those with 'T' or 'Y' configurations where the trace from the source to the 'T' is long, could have signal integrity problems.

The suggested routing scheme is to drive each of the agent TCK signals individually from a buffer device. Figure 31 shows how the TCK signal should be routed to the agents in a 4-way Pentium® III Xeon™ processor-based system incorporating the Intel® 450NX PCIset. A Bessel filter is recommended over a series termination at the output of each buffer. The values shown in Figure 31 are only examples. The designer should determine the LC values appropriate for their particular application.

If it is desired to ship production systems without the 2.5V buffers installed, then pull-up resistors should be placed at the outputs to prevent TCK from floating.

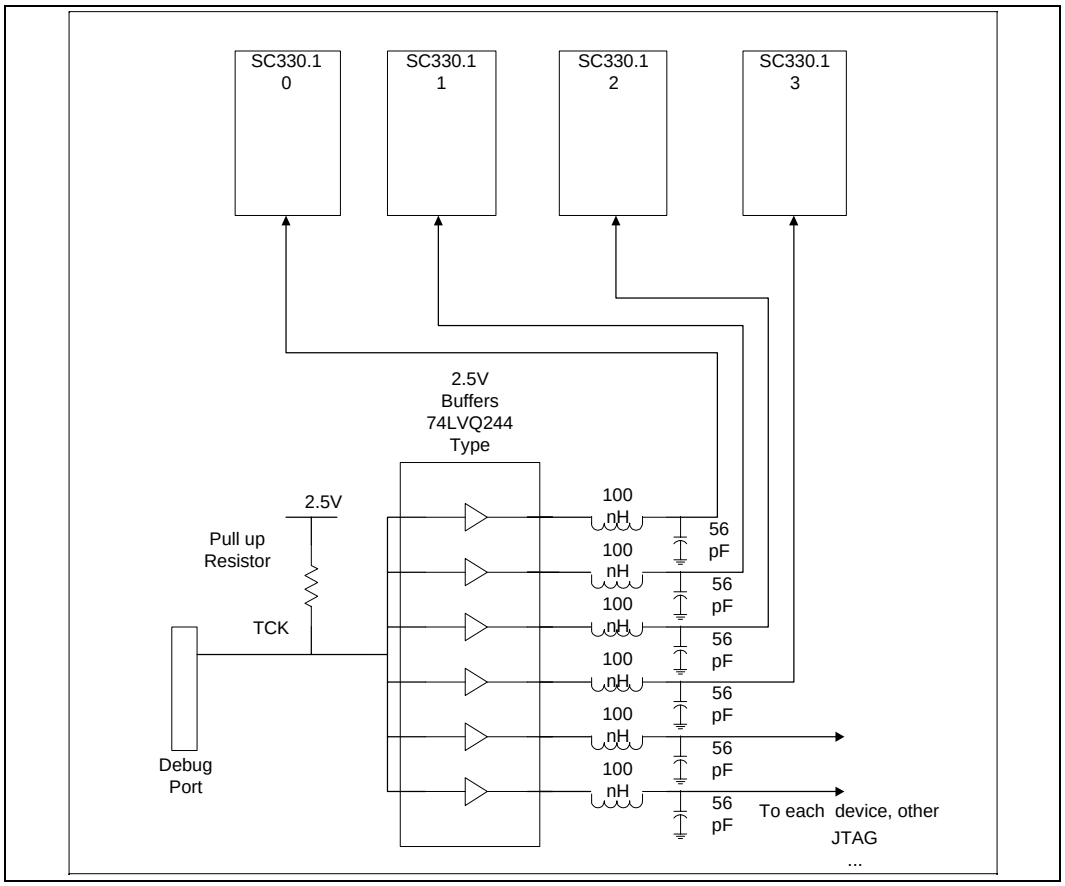


Figure 31. TCK with individual buffering scheme

The ITP buffer board drives the TCK signal through the debug port, to the buffered device(s).

NOTE

The buffer rise and fall edge rates should NOT be FASTER than 3nS. Edge rates faster than this in the system can contribute to signal reflections that endanger ITP compatibility with the target system. A low voltage buffer capable of driving 2.5V outputs such as an 74LVQ244 is suggested to eliminate the need for attenuation. Simulation should be performed to verify that the edge rates of the buffer chosen are not too fast.

The pull-up resistor to 2.5V keeps the TCK signal from floating when the ITP is not connected. The value of this resistor should be such that the ITP can still drive the signal low (1K). The trace lengths from the buffer to each of the agents should also be kept at a minimum to ensure good signal integrity.

8.1.7 Using the TAP to Communicate to the processor

An ITP communicates to the processor by stopping their execution and sending/receiving messages over boundary scan pins. As long as each processor is tied into the system boundary scan chain, the ITP can communicate with it. In the simplest case, the processors are back to back in the scan chain, with the boundary scan input (TDI) of the first processor connected up directly to the pin labeled TDI on the debug port and the boundary scan output of the last processor connected up to the pin labeled TDO on the debug port as shown in Figure 32.

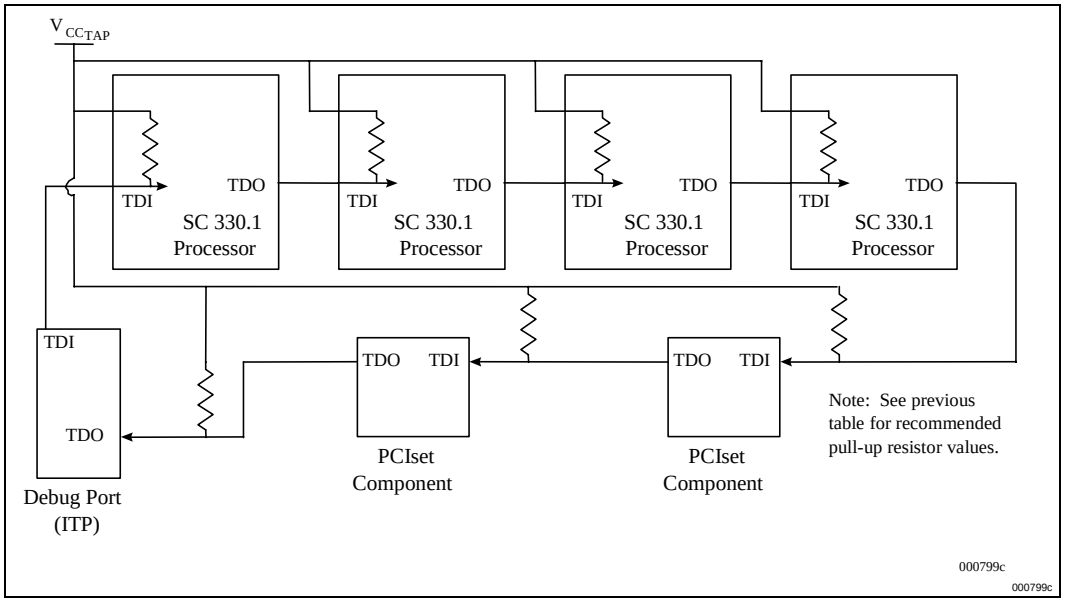


Figure 32. System Preferred Debug Port Layout

8.2 Logic Analyzer Interconnect (LAI) and Trace Capture Tool Considerations

8.2.1 LAI and Trace Capture Tool System Design Considerations

System designers must contact their third party tools vendors for Logic Analyzer Interface design considerations for the processor including electrical load models for system simulations. At this time, Hewlett-Packard, Tektronix, and American Arium are currently investigating Logic Analyzer Interconnect or trace capture tools for the processor.

8.2.2 LAI and Trace Capture tool Mechanical Keep Outs

Please contact your third party tools vendor for mechanical keep out restrictions for the Pentium® III Xeon™ processor at 700 MHz and 900 MHz.

9. BOXED PROCESSOR SPECIFICATIONS

9.1 Introduction

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz is also offered as an Intel® boxed processor. Intel® boxed processors are intended for system integrators who build systems from baseboards and off-the-shelf components. The boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz is supplied with an attached passive heatsink. This section documents baseboard and system requirements for the heatsink that will be supplied with the boxed processor. This section is particularly important for OEMs that manufacture baseboards for system integrators. Unless otherwise noted, all figures in this chapter are dimensioned in inches. Figure 33 shows a mechanical representation of the boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz.

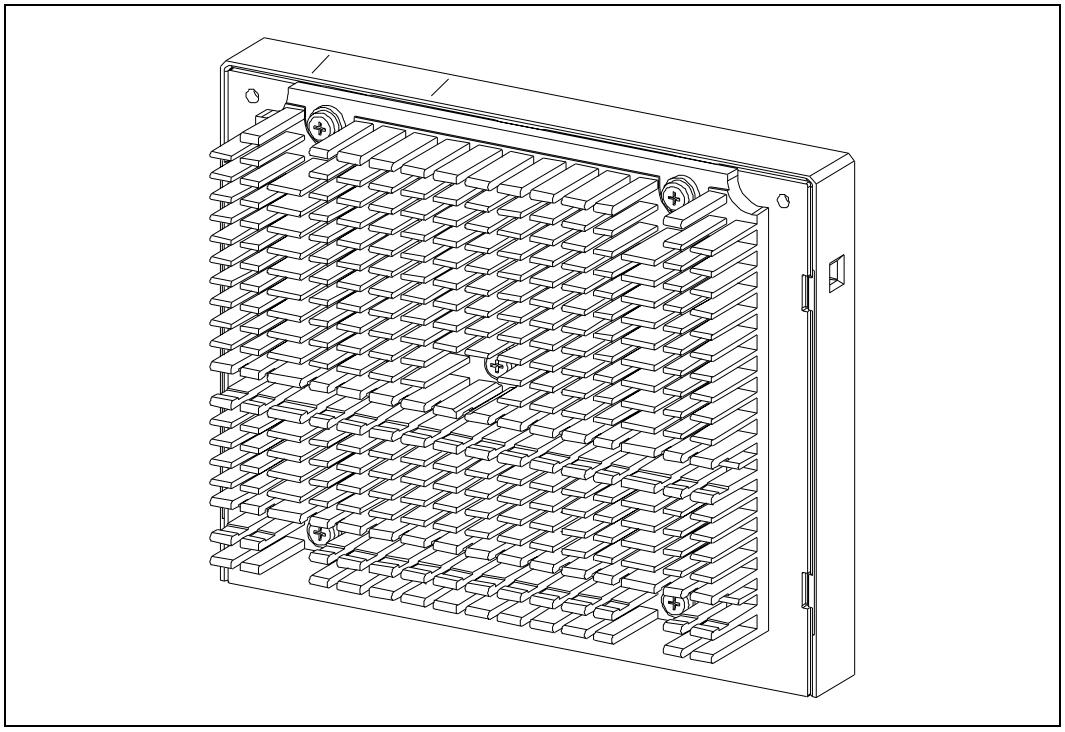


Figure 33. Boxed Pentium® III Xeon™ Processor at 700 MHz and 900 MHz

9.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz heatsink.

The boxed processor ships with an attached passive heatsink. Clearance is required around the heatsink to ensure proper installation of the processor and unimpeded airflow for proper cooling. The space requirements and dimensions for the boxed processor are shown in Figure 34 (Side View), Figure 35 (Front View), and Table 53. All dimensions are in inches.

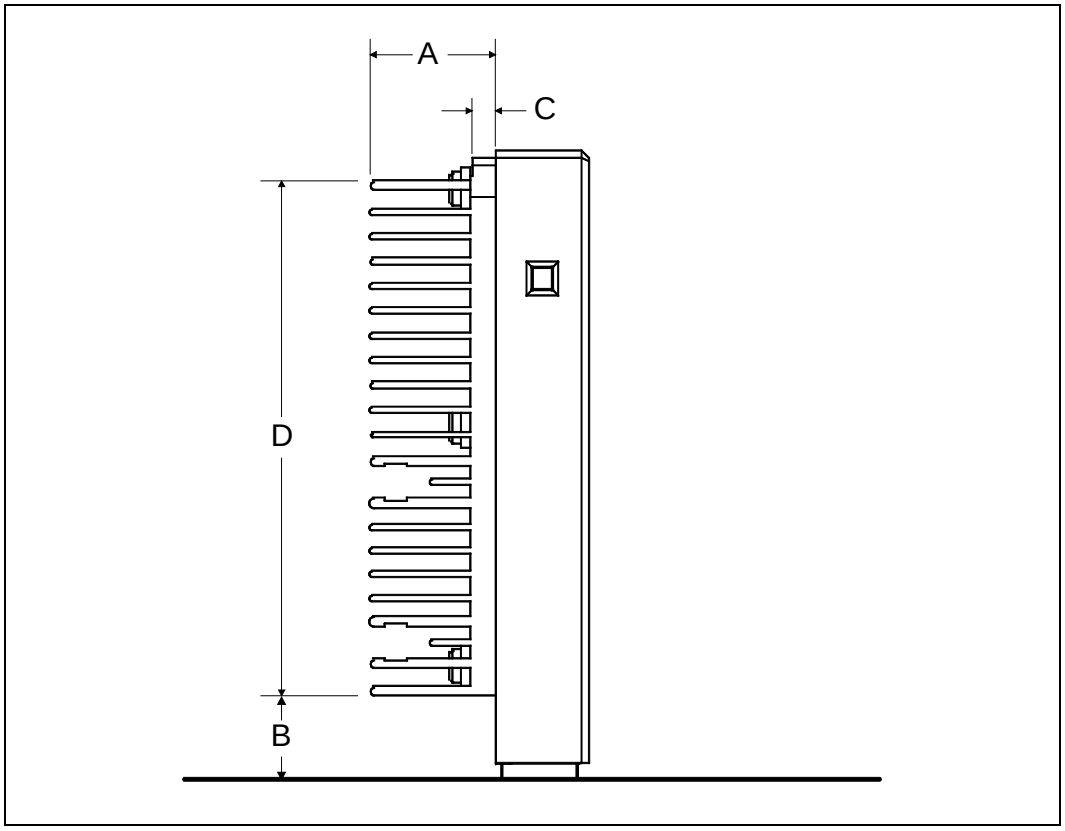


Figure 34. Side View Space Requirements for the Boxed Processor

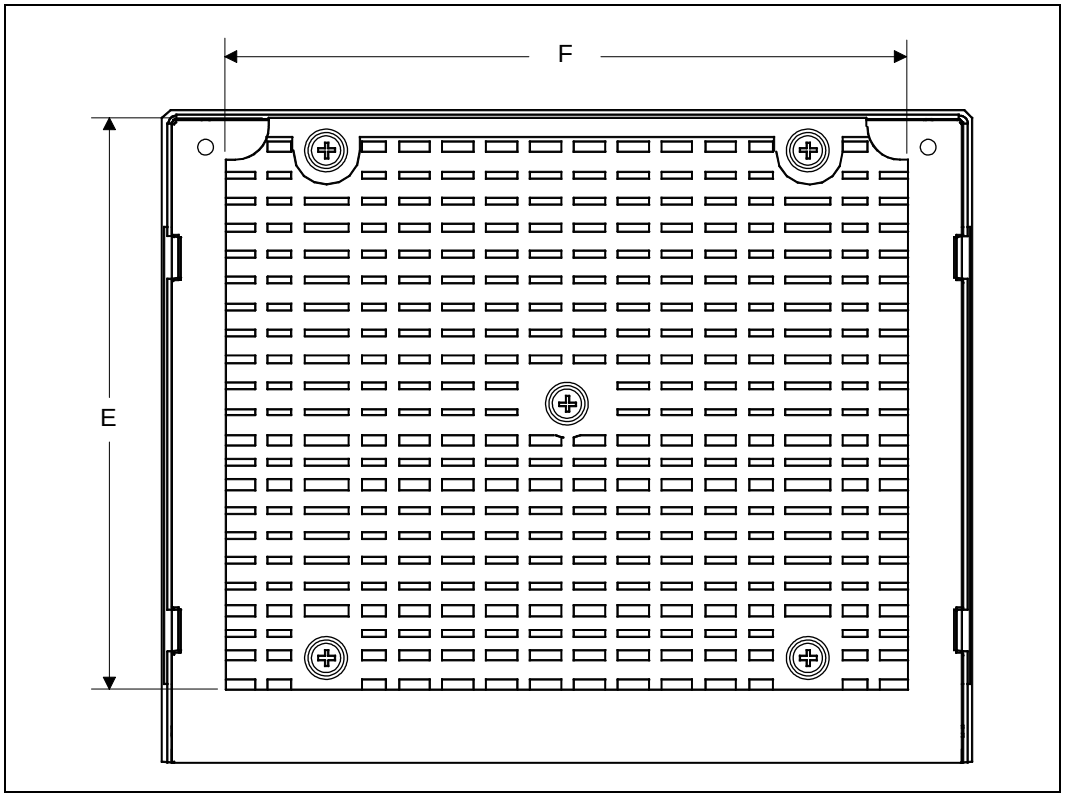


Figure 35. Front View Space Requirements for the Boxed Processor

9.2.1 BOXED PROCESSOR HEATSINK DIMENSIONS

Table 53. Boxed Processor Heatsink Dimensions

Fig. Ref. Label	Dimensions (Inches)	Min	Typ	Max
A	Heatsink Depth (off heatsink attach point)		1.03	
B	Heatsink Height (above baseboard)	0.485		
C	Heatsink Base Thickness			0.200
D	Heatsink Total Height at Fins		4.065	
E	Heatsink Total Height at Base (see front view)		4.235	
F	Heatsink Width (see front view)		5.05	

9.2.2 BOXED PROCESSOR HEATSINK WEIGHT

The boxed processor heatsink will not weigh more than 350 grams (without auxiliary fan).

9.2.3 BOXED PROCESSOR RETENTION MECHANISM

The boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz requires a retention mechanism that supports and secures the Single Edge Contact Cartridge (S.E.C.C.) in the 330-contact slot connector. An S.E.C.C. retention mechanism is not provided with the boxed processor. Baseboards designed for use by system integrators should include a retention mechanism and appropriate installation instructions. The boxed

processor does not require additional heatsink supports. Heatsink supports are not shipped with the boxed processor.

9.3 Thermal Specifications

This section describes the cooling requirements of the heatsink solution utilized by the boxed processor.

9.3.1 Boxed Processor Cooling Requirements

The boxed processor passive heatsink requires airflow horizontally across the heatsink to cool the processor. The boxed processor heatsink will keep the processor thermal plate temperature, T_{PLATE}, within the specification, provided adequate airflow is directed into the system chassis, across the heatsink and out of the system chassis. System integrators should perform thermal testing using thermocouples (see the section entitled *Processor Thermal Analysis*) to evaluate the thermal efficiency of the system.

9.3.2 Boxed Processor Passive Heatsink Performance

The boxed processor's passive heatsink is designed to provide effective heat transfer between the processor package thermal plate and the air immediately surrounding the heatsink. The direction and temperature of air flowing across the heatsink variably affects the efficiency of the heatsink. Figure 36 shows the thermal efficiency of the boxed processor heatsink, using three different directions of airflow: horizontal, top-down, and normal to the plane of the thermal plate. The performance characterization was completed in a wind tunnel, using a processor running at maximum power and at maximum thermal specification. The characterization assumes that air entering the heatsink is at constant temperature and uniformly traverses the heatsink, and that heated air is evacuated from the chassis and is not re-circulated. The characterization also assumes natural obstructions, such as the motherboard in a top-down airflow model.

To determine if a particular chassis has appropriate airflow to effectively cool the processor, measure the "upstream" temperature ($T_{AMBIENT}$, the ambient air temperature within the chassis) and the velocity of the air entering the heatsink. The Y-axis in Figure 36 represents the thermal resistance ($_{PA}$) and the X-axis represents the airflow speed in linear feet per minute (lfm). $_{PA}$ can be calculated as the difference between the thermal plate temperature and ambient air temperature (within the chassis) divided by the processor's maximum power specification.

$$\theta_{PA} = \frac{T_{PLATE} - T_{AMBIENT}}{P_{MAX}}$$

To determine if your airflow is adequate, determine the airflow speed and direction, and identify the appropriate curve in Figure 36. Calculate $_{PA}$ and determine if it falls below the graphed line at the appropriate airflow speed.

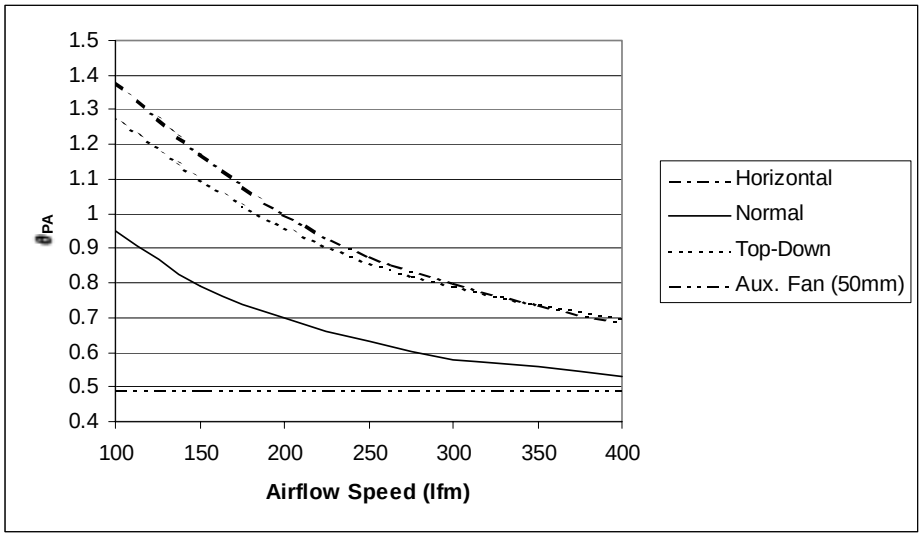


Figure 36. Boxed Processor Heatsink Performance

Figure 36 also shows the performance of the boxed processor heatsink with an attached auxiliary fan (50mm X 50mm X 15mm). In this case, the temperature of the air entering the fan is used as $T_{AMBIENT}$. $T_{AMBIENT}$ is measured just outside the fan's air intake. The presence of the auxiliary fan allows the cooling solution to perform with very little local airflow. Therefore, $_{PA}$ is virtually constant and independent of the speed and direction of airflow across the heatsink.

9.3.2 Optional auxiliary fan attachment

The boxed processor's passive heatsink includes features that allow for attachment of an auxiliary fan to improve airflow over the passive heatsink. A typical 40mm, 50mm, or 60mm fan can be attached. System integrators must evaluate the thermal performance of their system (see above) and consider the baseboard manufacturer's recommendations for thermal management before deciding if an auxiliary fan is warranted. If an auxiliary fan is needed (e.g. for the front processor in a multiprocessor system), it may be attached to the face of the boxed processor's passive heatsink. To facilitate this, the boxed processor's passive heatsink will include features in the heatsink fins onto which fan mounting hardware can be attached. The appropriate fan attach hardware will be included with the boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz if necessary. **The boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz does not ship with an auxiliary fan.**

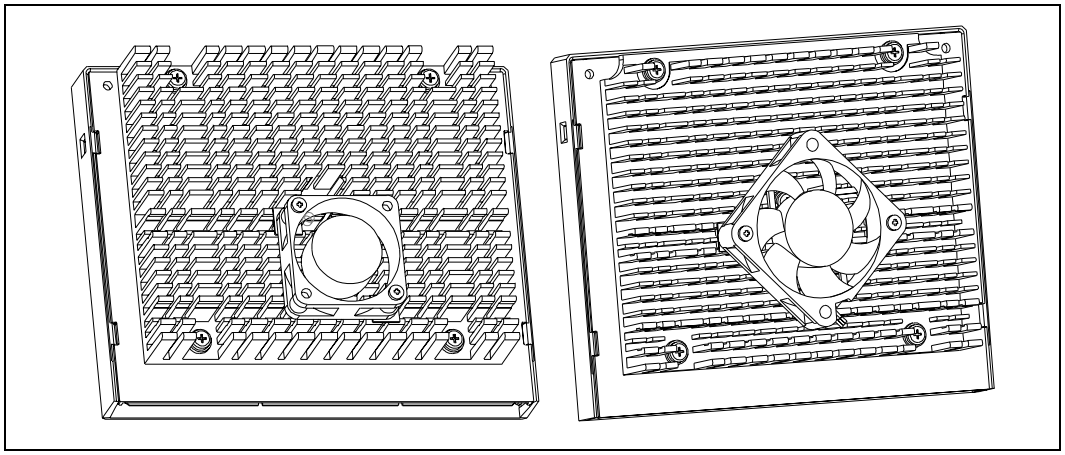


Figure 37. Conceptual Views of the Boxed Processor with Attached 40mm and 50mm Auxiliary Fan (fan not included with the Boxed Processor).

9.3.2.1 Clearance recommendations for auxiliary fan

If an auxiliary fan is used, clearance must be provided in front of the boxed processor passive heatsink to accommodate the mechanical and airflow clearance requirements of the fan and mounting hardware. Baseboard-mounted components and chassis members should not violate the clearance requirements for the auxiliary fan. Figure 38 and Figure 39 show the clearance recommended for the fan and air inlet. Required airspace clearance for fans may vary by manufacturer. Consult your fan manufacturer and/or fan documentation for specifications.

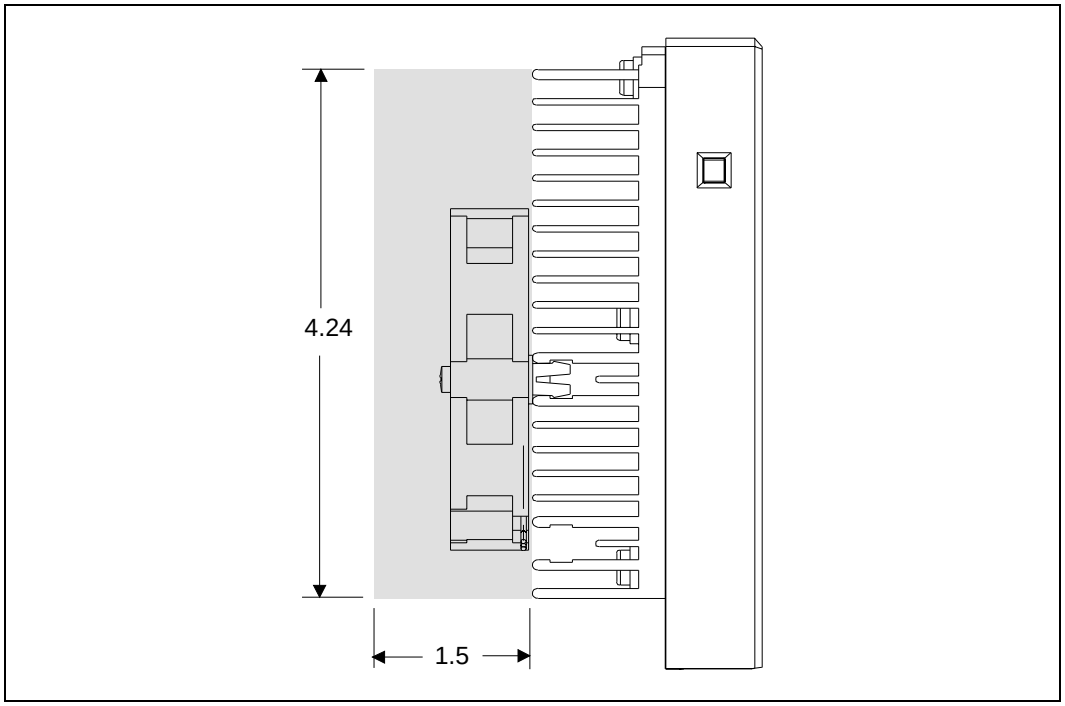


Figure 38. Side View Space Recommendation for the Auxiliary Fan

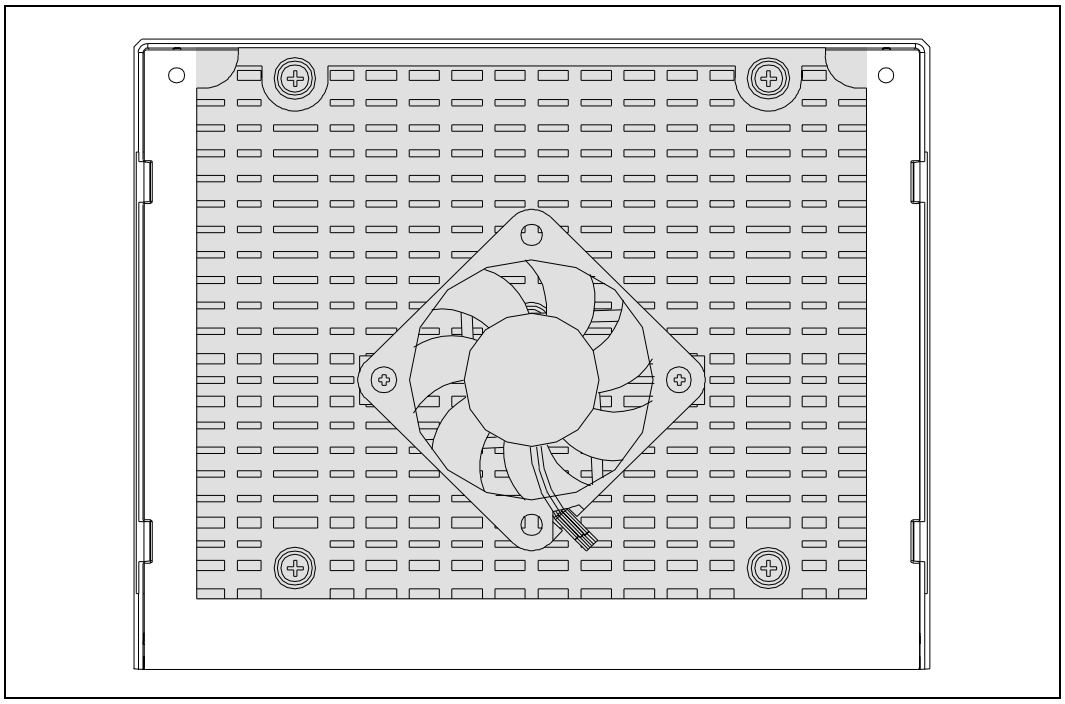


Figure 39. Front View Space Recommendation for the Auxiliary Fan

9.3.2.2 Fan power recommendations for auxiliary fan

To facilitate power to the auxiliary fan and provide fan monitoring, a fan-sense capable power header may be provided on the baseboard near every processor that may need an auxiliary fan. Although the boxed

processor does not ship with an auxiliary fan, it is highly recommended that a power header be provided. It is also recommended that the power header be consistent with the power header for other boxed processors that feature a fan-sense capable fan heatsink. Figure 40 shows the typical boxed processor fan/heatsink power cable connector. Table 54 shows the typical boxed processor fan power cable connector requirements. The actual requirements for the auxiliary fan power may vary. Consult your fan manufacturer and/or fan documentation for specifications.

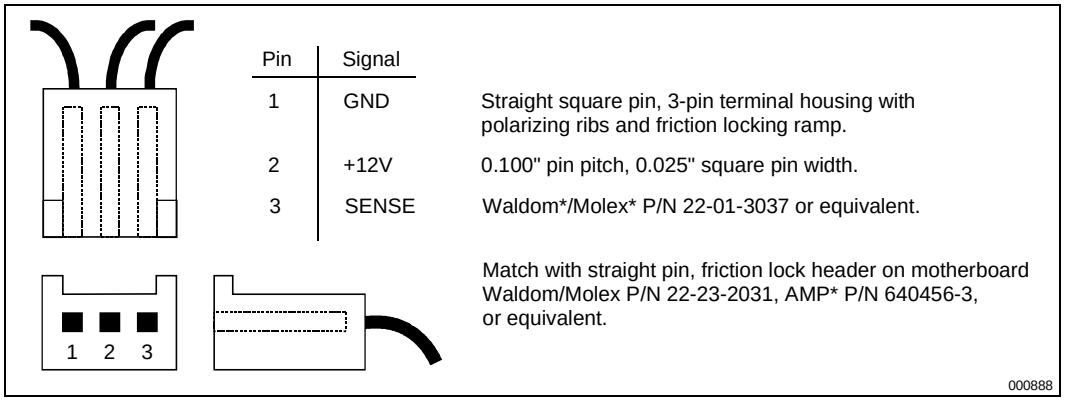


Figure 40. Standard Boxed Processor Fan/Heatsink Power Cable Connector Description

Table 54. Fan/Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12V: 12 volt fan power supply	7V	12V	13.8V
IC: Fan current draw		100mA	
SENSE: SENSE frequency (baseboard should pull this pin up to appropriate V_{CC} with resistor (typically 10 to 12 kΩ)		2 pulses per fan revolution	

9.3.2.3 Thermal evaluation for auxiliary fan

Given the complex and unique nature of baseboard layouts, and the special chassis required to support them, thermal performance may vary greatly with each baseboard/chassis combination. Baseboard manufacturers must evaluate and recommend effective thermal solutions for their specific designs, particularly designs that are proprietary. Such thermal solutions must take all system components into account. The power requirements of all processors that will be supported by the baseboard should be accommodated. The boxed Pentium® III Xeon™ processor at 700 MHz and 900 MHz is designed to provide a flexible cooling solution by incorporating features by which an auxiliary fan may be attached. *Should the system thermal evaluation warrant the requirement for an auxiliary fan, an auxiliary fan must be included with the baseboard to allow the thermal requirements of the system to be met.*

10. APPENDIX

This appendix provides an alphabetical listing of all Pentium® III Xeon™ processor at 700 MHz and 900 MHz signals and tables that summarize the signals by direction: output, input, and I/O.

10.1 Alphabetical Signals Reference

This section provides an alphabetical listing of all processor signals.

10.1.1 A[35:03]# (I/O)

The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:03]# signals are parity protected by the AP0# parity signal.

On the active-to-inactive transition of RESET#, the processors sample the A[35:03]# pins to determine their power-on configuration. See the *Pentium II Processor Developer's Manual* for details.

10.1.2 A20M# (I)

If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.

A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.

During active RESET#, each processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Figure 1. On the active-to-inactive transition of RESET#, each processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.

10.1.3 ADS# (I/O)

The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:03]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all processor system bus agents.

10.1.4 AERR# (I/O)

The AERR# (Address Parity Error) signal is observed and driven by all processor system bus agents, and if used, must connect the appropriate pins on all processor system bus agents. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction.

If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the Machine Check Architecture (MCA) of the system.

10.1.5 AP[1:0]# (I/O)

The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:03]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#, and AP0# covers A[23:03]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all processor system bus agents.

10.1.6 BCLK (I)

The BCLK (Bus Clock) is a 2.5V tolerant signal that determines the bus frequency. All processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge.

All external timing parameters are specified with respect to the BCLK signal.

10.1.7 BERR# (I/O)

The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents, and must connect the appropriate pins of all such agents, if used. However, the processor does not observe assertions of the BERR# signal.

BERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options:

- Enabled or disabled.
- Asserted optionally for internal errors along with IERR#.
- Asserted optionally by the request initiator of a bus transaction after it observes an error.
- Asserted by any bus agent when it observes an error in a bus transaction.

10.1.8 BINIT# (I/O)

The BINIT# (Bus Initialization) signal may be observed and driven by all processor system bus agents, and if used must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.

10.1.9 BNR# (I/O)

The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.

10.1.10 BP[3:2]# (I/O)

The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.

10.1.11 BPM[1:0]# (I/O)

The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

10.1.12 BPRI# (I)

The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.

10.1.13 BR0# (I/O), BR[3:1]# (I)

The BR[3:1]# (Bus Request) pins drive the BREQ[3:0]# signals on the system. The BR[3:0]# pins are interconnected in a rotating manner to other processors' BR[3:0]# pins. Table 55 gives the rotating interconnect between the processor and bus signals for 4-way processor-based systems.

Table 55. BR[3:0]# Signals Rotating Interconnect, 4-Way system

Bus Signal	Agent 0 Pins	Agent 1 Pins	Agent 2 Pins	Agent 3 Pins
BREQ0#	BR0#	BR3#	BR2#	BR1#
BREQ1#	BR1#	BR0#	BR3#	BR2#
BREQ2#	BR2#	BR1#	BR0#	BR3#
BREQ3#	BR3#	BR2#	BR1#	BR0#

Table 56 gives the interconnect between the processor and bus signals for a 2-way processor-based system.

Table 56. BR[3:0]# Signals Rotating Interconnect, 2-Way system

Bus Signal	Agent 0 Pins	Agent 1 Pins
BREQ0#	BR0#	BR3#
BREQ1#	BR1#	BR0#
BREQ2#	N/C	N/C
BREQ3#	N/C	N/C

During power-up configuration, the central agent must assert its BR0# signal. All symmetric agents sample their BR[3:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. All agents then configure their BREQ[3:0]# signals to match the appropriate bus signal protocol, as shown in Table 57.

Table 57. Agent ID Configuration

BR0#	BR1#	BR2#	BR3#	Agent ID
L	H	H	H	0
H	H	H	L	1
H	H	L	H	2
H	L	H	H	3

10.1.15 CORE_AN_SENSE (O)

This signal is tied to the Vcc seen at the processor core and represents the output of the OCVR. This signal provides the ability to monitor the stability of the OCVR in high reliability applications. The voltage seen at this pin is the actual operating voltage of the core with integrated L2 Cache minus IR drops due to trace routing in the Cartridge.

10.1.16 D[63:00]# (I/O)

The D[63:00]# (Data) signals are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.

10.1.17 DBSY# (I/O)

The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.

10.1.18 DEFER# (I)

The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of all processor system bus agents.

10.1.19 DEP[7:0]# (I/O)

The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:00]#, and must connect the appropriate pins of all processor system bus agents which use them. The DEP[7:0]# signals are enabled or disabled for ECC protection during power on configuration.

10.1.20 DRDY# (I/O)

The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.

10.1.21 FERR# (O)

The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel387™ coprocessor, and is included for compatibility with systems using DOS-type floating-point error reporting.

10.1.22 FLUSH# (I)

When the FLUSH# input signal is asserted, processors write back all data in the Modified state from their internal caches and invalidate all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted.

FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.

On the active-to-inactive transition of RESET#, each processor samples FLUSH# to determine its power-on configuration. See *Pentium II Processor Developer's Manual* for details.

10.1.23 HIT# (I/O), HITM# (I/O)

The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

10.1.24 HV_EN# (O)

The HV_EN# signal is used as a way of differentiating a 5V/12V version processor cartridge from a 2.8V version. HV_EN# is tied to Vss (ground) on the 5V/12V version, and is high impedance (floating) on the 2.8V version. This is a reserved (no connect) pin on previous versions of the Pentium® III Xeon™ processor.

10.1.25 IERR# (O)

The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the system bus. This transaction may optionally be converted to

an external error signal (e.g. NMI) by system core logic. The processor will keep IERR# asserted until it is handled in software, or with the assertion of RESET#, BINIT#, or INIT#.

10.1.26 IGNNE# (I)

The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set.

IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.

During active RESET#, the processor begins sampling the A20M#, IGNNE# , and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 1. On the active-to-inactive transition of RESET#, the processor latches these signals and freezes the frequency ratio internally. System logic must then release these signals for normal operation.

10.1.27 INIT# (I)

The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1 or L2) caches or floating-point registers. Each processor then begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents.

If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-In Self-Test (BIST).

10.1.28 INTR - see LINT[0]

10.1.29 LINT[1:0] (I)

The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous.

Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after reset, operation of these pins as LINT[1:0] is the default configuration.

During active RESET#, the Pentium® III Xeon™ processor at 700 MHz begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency (See Table 1). On the active-to-inactive transition of RESET#, the Pentium® III Xeon™ processor at 700 MHz samples these signals and latches the frequency ratio internally. System logic must then release these signals for normal operation. The Pentium® III Xeon™ processor at 900 MHz does not sample the A20M#, IGNNE#, and LINT[1:] values at the de-assertion of the RESET# signal, and will operate only with a 9:1 core/bus ratio.

10.1.30 LOCK# (I/O)

The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all Pentium® III Xeon™ processor at 700 MHz and 900 MHz system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction.

When the priority agent asserts BPRI# to arbitrate for ownership of the Pentium® III Xeon™ processor at 700 MHz and 900 MHz system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the Pentium® III Xeon™ processor at 700 MHz and 900 MHz system bus throughout the bus locked operation and ensure the atomicity of lock.

10.1.31 L2_SENSE

On Pentium® III Xeon™ processor at 500 MHz and 550 MHz cartridges, L2_SENSE is routed from the edge of the connector pin B57 to the VL2 power plane. It allows monitoring the delivery of Vcc_L2 voltage at the L2 array device for this processor. Since the Pentium® III Xeon™ processor at 700 MHz and 900 MHz does not have a separate L2 cache voltage supply, this line is NOT used and is not recommended to be connected in systems based on the Pentium® III Xeon™ processor at 700 MHz and 900 MHz only.

Systems that rely on remote sensing of Vcc_L2 need to guarantee this requirement is met at the VRM sense line regardless of core feedback.

10.1.32 OCVR_EN (I)

This signal is the output enable for the internal cartridge voltage regulator. Driving this Low will inactivate the outputs of the OCVR. This is an open drain signal referenced high to +5V through a 10KΩ resistor within the cartridge to activate the VRM when not driven low (this to satisfy legacy requirements). Refer to Figure 41 and Figure 42 For PWRGD relationships at Power up.

10.1.33 OCVR_OK(O)

This is an open drain compatible output from the On-Cartridge Voltage Regulator Module (OCVR) indicating that its outputs are enabled and operating within specifications. This signal is referenced to Vcc_SMB (+3.3V) through a 10KΩ resistor, and should be used in conjunction with an equivalent signal from the host power system to generate the CORE_PWRGD signals for the processor cores. Refer to Figure 41 and Figure 42 for PWRGD relationships at Power up. PWRGD assertion must lag OCVR_OK assertion.

10.1.34 NMI - See LINT[1]

10.1.35 PICCLK (I)

The PICCLK (APIC Clock) signal is a 2.5V tolerant input clock to the processor and core logic or I/O APIC that is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.

10.1.36 PICD[1:0] (I/O)

The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus, and must connect the appropriate pins of all processors and core logic or I/O APIC components on the APIC bus.

10.1.37 PRDY# (O)

The PRDY (Probe Ready) signal is a processor output that is used by debug tools to determine processor debug readiness.

10.1.38 PREQ# (I)

The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.

10.1.39 PWREN[1:0] (I)

These 2 pins are tied directly together on the processor. They can be used to detect processor presence by applying a voltage to one pin and observing it at the other. See 3.9 for the maximum rating for this signal.

10.1.40 PWRGOOD (I)

The (Power Good) signal is a 2.5V tolerant processor input. The processor requires this signal to be a clean indication that the clocks and power supplies (V_{CC_CORE}, V_{CC_L2}, V_{CC_TAP}, V_{CC_SMB}, $V_{CC2.5}$) are stable and within their

specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on, until they come within specification. The signal must then transition monotonically to a high (2.5V) state. Figure 41 illustrates the relationship of PWRGD to other system signals. PWRGD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGD. It must also meet the minimum pulse width specification in Table 14 and be followed by a 8 mS RESET# pulse.

The PWRGD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.

Current VRM 8.3 (on baseboard) specification requires VRM_PWRGD to be asserted when its output is within 12% of nominal value. In the Pentium® III Xeon™ processor at 700 MHz and 900 MHz, PWRGD is logically ANDed with OCVR_OK before being applied to the core (PWRGD_CORE). According to legacy datasheet documents, RESET# negation is expected 1 mS after seeing PWRGD_CORE becoming valid by the processor core. The OCVR is not expected to provide a valid OCVR_OK signal assertion within 13 mS of seeing 90% of its input voltage. The delay before the assertion of OCVR_OK may cause a race condition between RESET# and the valid PWRGD_CORE that is seen at the core. It is recommended to relax the deassertion of RESET# to meet this critical constrain. Careful analysis needs to be done in existing platforms. Refer to Figure 41 and Figure 42 below for new timing relationship requirements.

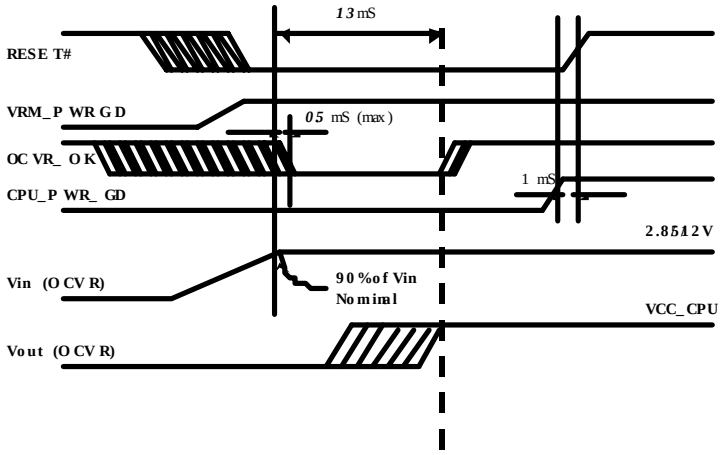


Figure 41. PWRGD Relationship at Power-On

NOTES:

1. VCC_CORE must be applied to the OCVR input before OCVR_OK can become valid (even though it could be pulled high if the VCC_SMB supply is turned on, see figure 41.
2. The OCVR_OK signal is not guaranteed to be valid until 0.5 mS (max) after Vin to the OCVR reaches 90% of it's nominal value.
3. Vin is the input to the OCVR (VCC_CORE).
4. Vout is the output from the OCVR (VCC_CPU).

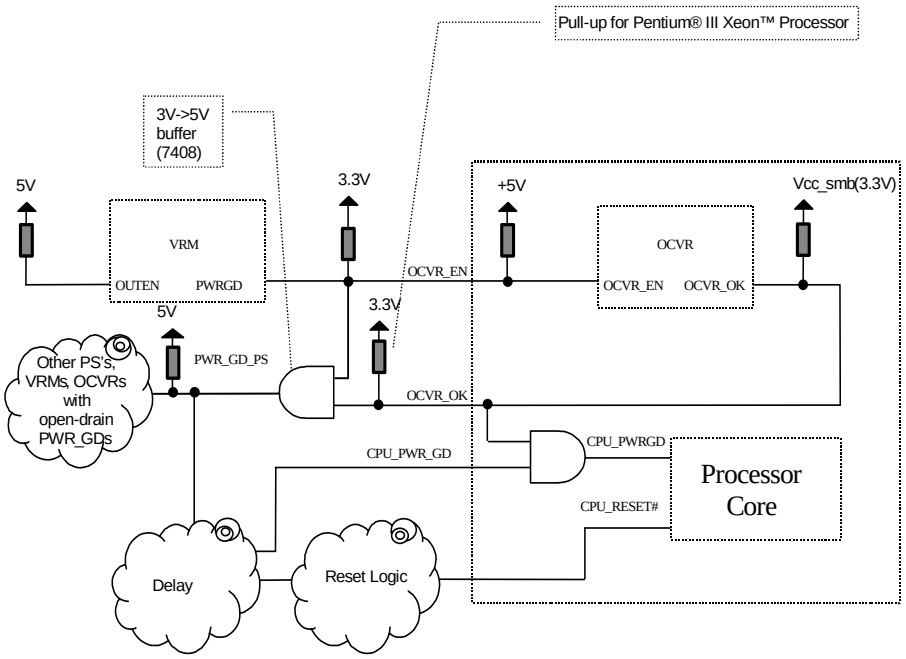


Figure 42. PWRGD Implementation

10.1.41 REQ[4:0]# (I/O)

The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.

10.1.42 RESET# (I)

Asserting the RESET# signal resets all processors to known states and invalidates their L1 and L2 caches without writing back any of their contents. RESET# must remain active for one microsecond for a "warm" reset; for a power-on reset, RESET# must stay active for at least one millisecond after the PWRGOOD input to the processor has asserted; until this de-assertion of RESET# occurs, all outputs from the processor are indeterminate unless otherwise specified. On observing active RESET#, all processor system bus agents will de-assert their outputs within two clocks.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the *Pentium II Processor Developer's Manual*.

The processor may have its outputs tri-stated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-In Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the reset-vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.

10.1.43 RP# (I/O)

The RP# (Request Parity) signal is driven by the request initiator, and provides parity protection on ADS# and REQ[4:0]#. It must connect the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

10.1.44 RS[2:0]# (I)

The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.

10.1.45 RSP# (I)

The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

10.1.46 SA[2:0] (I)

The SA (Select Address) pins are decoded on the SMBus in conjunction with the upper address bits in order to maintain unique addresses on the SMBus in a system with multiple processors. To set an SA line high, a pull-up resistor should be used that is no larger than 1KΩ. To set an SA line as low, the pin can be left unconnected. SA2 can also be tri-stated to define additional addresses for the thermal sensor. A tri-state or "Z" state on this pin is achieved by leaving this pin unconnected.

Of the addresses broadcast across the SMBus, the memory components claim those of the form "1010XXYZb". The "XX" and "Y" bits are used to enable the devices on the cartridge at adjacent addresses. The Y bit is hard-wired on the cartridge to V_{SS} ('0') for the Scratch EEPROM and pulled to V_{CCSMB} ('1') for the processor Information ROM. The "XX" bits are defined by the processor slot via the SA0 and SA1 pins on the SC330 connector. These address pins are pulled down weakly (10 k) on the cartridge to ensure that the memory components are in a known state in systems which do not support the SMBus, or only support a partial implementation. The "Z" bit is the read/write bit for the serial bus transaction.

The thermal sensor internally decodes 1 of 3 upper address patterns from the bus of the form "0011XXXZb", "1001XXXZb" or "0101XXXZb". The device's addressing, as implemented, includes a Hi-Z state for one address pin (SA2), and therefore supports 6 unique resulting addresses. The ability of the system to drive this pin to a Hi-Z state is dependent on the baseboard implementation (The pin must be left floating). The system should drive SA1 and SA0, and will be pulled low (if not driven) by the 10 k pull-down resistor on the processor substrate. Driving these signals to a Hi-Z state would cause ambiguity in the memory device address decode, possibly resulting in the devices not responding, thus timing out or hanging the SMBus. As before, the "Z" bit is the read/write bit for the serial bus transaction. For more information on the usage of these pins, see section 5.2.7.

10.1.47 SELFSB0 (I) SELFSB1 (O)

The Pentium® III Xeon™ processor at 700 MHz and 900 MHz adds a definition to the SELFSB [1:0] pins which is compatible with legacy systems as well as new platforms. The added functionality provides the means for the clock synthesizer and additional baseboard logic to auto detect the expected system bus frequency required by a specific cartridge. Table 59 and Figure 43 provide a summary of the functionality and the resistor values for an frequency auto detect circuit.

Table 59. Description of SELFSB pins

processor	Pin Location	Pin Name	Functionality
Pentium® III Xeon™ processor at 700 MHz and 900 MHz	A7	SELFSB1	Output, Frequency Detect
	A9	SELFSB0	Input, Frequency Selection.
Pentium® III Xeon™ processor at 500 MHz and 550 MHz & Pentium® II Xeon™ processor	A7	Vss	None
	A9	Reserved	None
SELFSB1: Output, (Frequency Detect). 100 MHz = GND.			
SELFSB0: **Pentium® III Xeon™ processor at 500 MHz and 550 MHz**: Not used.. **Pentium® III Xeon™ processor at 700 MHz and 900 MHz: Input; (Frequency Select).** 100 MHz= N/C or pull up to 2.5 V			

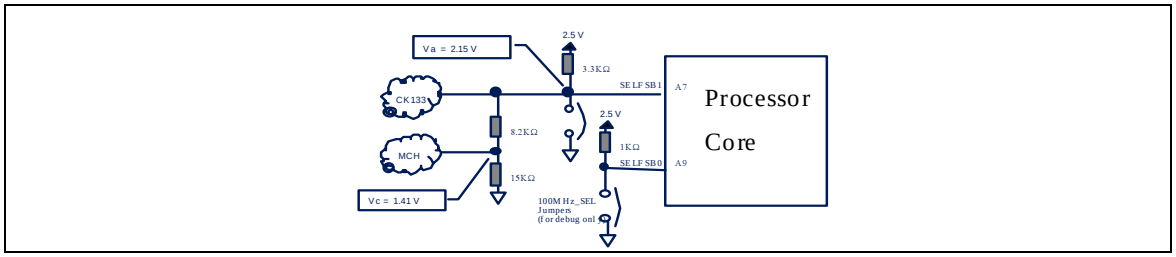


Figure 43. Recommended circuit for frequency auto detection

10.1.48 SLP# (I)

The SLP# (Sleep) signal, when asserted in Stop Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop Grant state, restarting its internal clock signals to the bus and APIC processor core units.

10.1.49 SMBALERT# (O)

SMBALERT# is an asynchronous interrupt line associated with the SMBus Thermal Sensor device.

10.1.50 SMBCLK (I)

The SMBCLK (SMBus Clock) signal is an input clock to the system management logic which is required for operation of the system management features of the Pentium® III Xeon™ processor at 700 MHz and 900 MHz. This clock is asynchronous to other clocks to the processor.

10.1.51 SMBDAT (I/O)

The SMBDAT (SMBus DATA) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices.

10.1.52 SMI# (I)

The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

10.1.53 STPCLK# (I)

The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop Grant state. The processor issues a Stop Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.

10.1.54 TCK (I)

The TCK (Test Clock) signal provides the clock input for processor Test Bus (also known as the Test Access Port).

10.1.55 TDI (I)

The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for TAP support.

10.1.56 TDO (O)

The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for TAP support.

10.1.57 TEST_2.5_[A23, A62, B27] (I)

The TEST_2.5_A62 signal must be connected to a 2.5V power source through a 1-10KΩ resistor for proper processor operation.

10.1.58 THERMTRIP# (O)

This pin indicates a thermal overload condition (thermal trip). The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will immediately stop all execution when the junction temperature exceeds approximately 135°C. This is signaled to the system by the THERMTRIP# pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself. Once the die temperature drops below the trip level, a RESET# pulse will reinitialize the processor and execution will continue at the reset vector. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped regardless of the state of RESET#.

The system designer should not act upon THERMTRIP# until after the RESET# input is de-asserted. Until this time, the THERMTRIP# output is indeterminate.

10.1.59 TMS (I)

The TMS (Test Mode Select) signal is a TAP support signal used by debug tools.

10.1.60 TRDY# (I)

The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all processor system bus agents.

10.1.61 TRST# (I)

The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. The processor self-resets during power on; therefore, it is not necessary to drive this signal during power on reset.

10.1.62 VID_L2[4:0], VID_CORE[4:0] (O)

The VID (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on the processor. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself. See section 3.9 for the maximum rating for these signals.

10.1.63 VIN_SENSE

VIN_SENSE (formerly called CPU_SENSE) is routed from edge-connector pin A56 to the VCC_{CORE} power plane. VIN_SENSE provides remote sensing capabilities for the voltage seen at the input of the OCVR.

NOTE: Pentium® III Xeon™ processor at 700 MHz and 900 MHz support either +2.8V, +5V or +12V VCC_CORE voltages depending on the version of OCVR. Therefore, any sensing logic must be capable of tolerating the selected VCC_CORE voltage (+2.8/+5V/+12V).

10.1.64 WP (I)

WP (Write Protect) can be used to write protect the scratch EEPROM. A high level write-protects the scratch EEPROM.

10.2 Signal Summaries

The following tables list attributes of the processor input, output, and I/O signals.

Table 60. Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
SMBALERT#	Low	Asynch	SMBus Output
TDO	High	TCK	TAP Output
THERMTRIP#	Low	Asynch	CMOS Output
VID_CORE[4:0]	High	Asynch	Power/Other
VID_L2[4:0]	High	Asynch	Power/Other
CPU_SENSE	High	Asynch	Power/Other
L2_SENSE	High	Asynch	Power/Other
OCVR_OK	High	Asynch	Power/Other

Table 61. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always
BPRI#	Low	BCLK	AGTL+ Input	Always
BR[3:1]#	Low	BCLK	AGTL+ Input	Always
BCLK	High	—	System Bus Clock	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always [2]
IGNNE#	Low	Asynch	CMOS Input	Always [2]
INIT#	Low	Asynch	CMOS Input	Always [2]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
RSP#	Low	BCLK	AGTL+ Input	Always
SA[2:0]	High	SMBCLK	Power/Other	
SMBCLK#	High	—	SMBus Clock	Always
SLP#	Low	Asynch	CMOS Input	During Stop Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	TAP Clock	
TDI	High	TCK	TAP Input	
TMS	High	TCK	TAP Input	
TRST#	Low	Asynch	TAP Input	
TRDY#	Low	BCLK	AGTL+ Input	
WP	High	Asynch	SMBus Input	
OCVR_EN	High	Asynch	Power/Other	

Table 62. I/O Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:03]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
AP[1:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
SELFSB0	High	—	Power/Other	

Table 62. I/O Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
SELFSB1	TBD	TBD	TBD	TBD
BR0#	Low	BCLK	AGTL+ I/O	Always
BP[3:2]#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
D[63:00]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DEP[7:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
RP#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
SMBDAT	High	SMBCLK	SMBus I/O	

Table 63. I/O Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	AGTL+ I/O	ADS#+3
BERR#	Low	BCLK	AGTL+ I/O	Always
BNR#	Low	BCLK	AGTL+ I/O	Always
BINIT#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always