SIEMENS

SIEMENS AKTIENGESELLSCHAF

T-49-19-05

8-Bit Single-Chip Microcontroller

SAB 8052/8032 Family

Preliminary

SAB 8052B Microcontroller with factory-maskprogrammable ROM (8K)
SAB 80513 Microcontroller with factory mask-programmable ROM (16 K)
SAB 8032B Microcontroller for external ROM

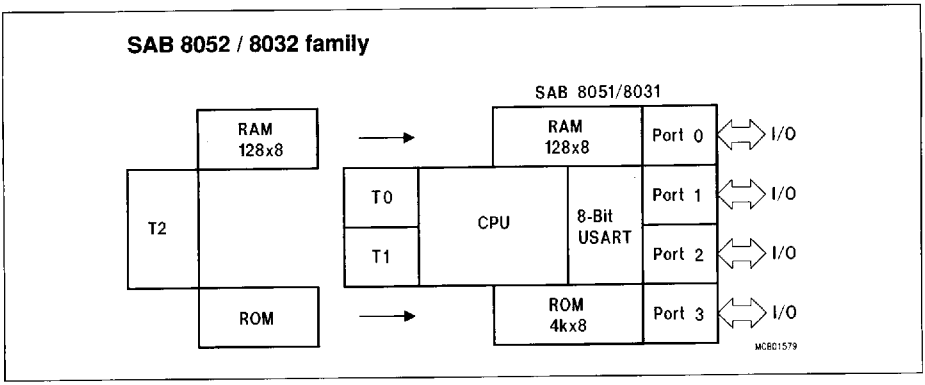
- Versions for 12 MHz / 16 MHz / 20 MHz operating frequency
- 8 K × 8 ROM (SAB 8052B only)
- 16 K × 8 ROM (SAB 80513 only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive baud rate capability
- External memory expandable up to 128 Kbytes
- Boolean processor
- Most instructions execute in:
  1 µs instruction cycle time at 12 MHz
  750 ns instruction cycle time at 16 MHz
  600 ns instruction cycle time at 20 MHz
- Multiply and divide in 4 µs/3 µs/2.4 µs
- Six interrupt vectors, two priority levels
- RAM power-down supply
- Packages P-DIP-40 and PL-CC-44
- Full backward compatibility with SAB 8051/8031
- Three temperature ranges available
  0 to 70 °C
  – 40 to 85 °C : T40/85
  – 40 to 110 °C : T40/110

The SAB 8052/8032 family are standalone, high-performance single-chip microcontrollers fabricated in + 5 V advanced N-channel, silicon-gate Siemens MYMOS technology, packaged in a 40-pin plastic dual-in-line package (P-DIP-40) or 44-pin plastic leaded chip carrier (PL-CC-44) package. It is backwardly compatible with the SAB 8051A/8031A and provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The controllers of the SAB 8052 / 8032 family contain a non-volatile 8 K × 8 read-only program memory, SAB 80513 16 K × 8 a volatile 256 × 8 read/write data memory, 32 I/O lines, three 16-bit timer/counters, a six-source, two-priority-level nested interrupt structure, a serial I/O port for either multiprocessor communications, I/O expansion, or full-duplex UART, as well as an on-chip oscillator and clock circuits.

For systems that require extra capability, the standard TTL compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals can be used to expand the SAB 8052 / 8032 family.

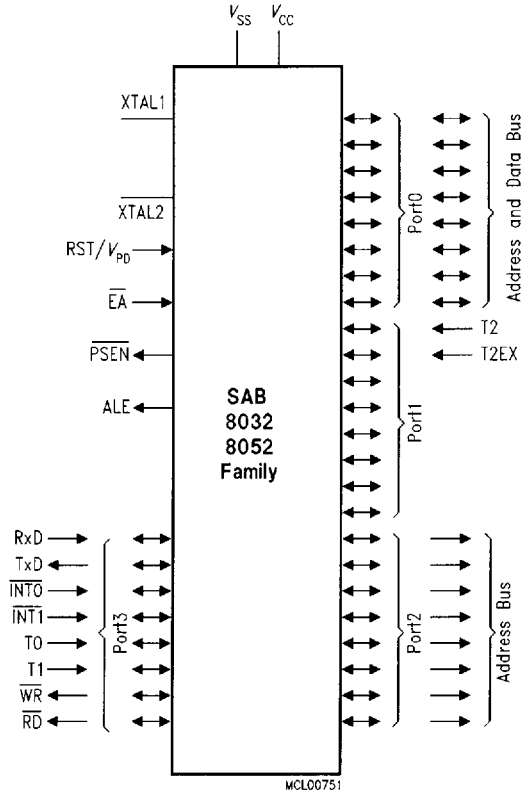
The parts are available for standard temperature range (0 to 70 °C) and extended temperature ranges (T40/85: – 40 to 85 °C and T40/110: – 40 to 110 °C).


SAB 8052 / 8032 family
SAB 8051/8031
RAM
128x8
T2
ROM
T0
T1
CPU
8-Bit
USART
RAM
128x8
ROM
4kx8
Port 0
Port 1
Port 2
Port 3
I/O
I/O
I/O
I/O
MCB01579

Ordering Information

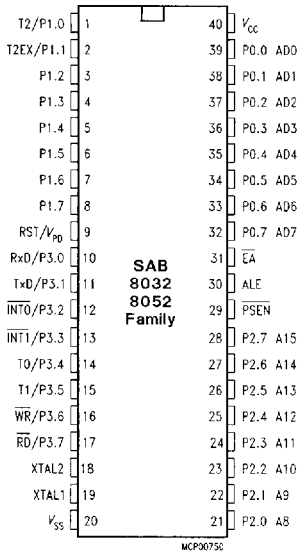
Type	Ordering code	Package	Description (8-bit single-chip microcontroller)
SAB 8032B-P	Q 67120-C419	P-DIP-40	for external memory, 12 MHz
SAB 8032B-N	Q 67120-C423	PL-CC-44	
SAB 8032B-P-T40/85	Q 67120-C427	P-DIP-40	for external memory, 12 MHz,
SAB 8032B-N-T40/85	Q 67120-C705	PL-CC-44	ext. Temp.
SAB 8032B-P-T40/110	Q 67120-C707	P-DIP-40	for external memory, 12 MHz,
SAB 8032B-N-T40/110	Q 67120-C704	PL-CC-44	ext. Temp.
SAB 8032B-16-P	Q 67120-C421	P-DIP-40	for external memory, 16 MHz
SAB 8032B-16-N	Q 67120-C425	PL-CC-44	
SAB 8032B-20-P	Q 67120-C471	P-DIP-40	for external memory, 20 MHz
SAB 8032B-20-N	Q 67120-C472	PL-CC-44	
SAB 8052B-P	Q 67120-C420	P-DIP-40	with 8-KByte mask-programmable
SAB 8052B-N	Q 67120-C424	PL-CC-44	ROM, 12 MHz
SAB 8052B-P-T40/85	Q 67120-C428	P-DIP-40	with 8-KByte mask-programmable ROM, 12 MHz, ext. Temp.
SAB 8052B-16-P	Q 67120-C422	P-DIP-40	with 8-KByte mask-programmable
SAB 8052B-16-N	Q 67120-C425	PL-CC-44	ROM, 16 MHz
SAB 80513-P	Q 67120-C383	P-DIP-40	with 16-KByte mask-programmable
SAB 80513-N	Q 67120-C384	PL-CC-44	ROM, 12 MHz
SAB 80513-P-T40/85	Q 67120-C482	P-DIP-40	with 16-KByte mask-programmable
SAB 80513-N-T40/85	Q 67120-C504	PL-CC-44	ROM, 12 MHz, ext. Temp.
SAB 80513-P-T40/110	Q 67120-C715	P-DIP-40	with 16-KByte mask-programmable
SAB 80513-N-T40/110	Q 67120-C714	PL-CC-44	ROM, 12 MHz, ext. Temp.
SAB 80513-16-P	Q 67120-C441	P-DIP-40	with 16-KByte mask-programmable
SAB 80513-16-N	Q 67120-C443	PL-CC-44	ROM, 16 MHz
SAB 80513-16-P-T40/85	Q 67120-C506	P-DIP-40	with 16-KByte mask-programmable
SAB 80513-16-N-T40/85	Q 67120-C505	PL-CC-44	ROM, 16 MHz, ext. Temp.

Logic Symbol

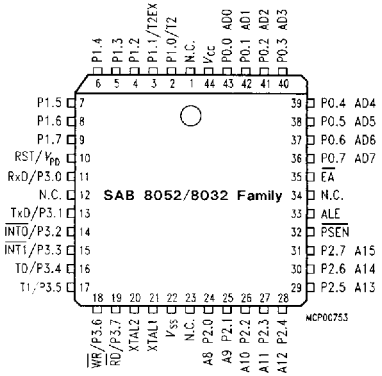


Pin Configuration

P-DIP-40



PL-CC-44



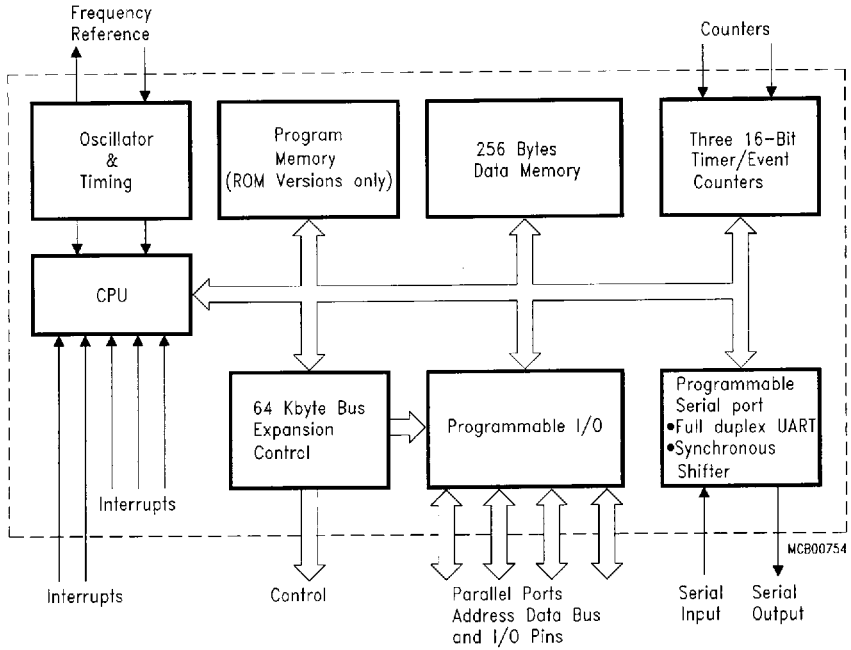
Pin Definitions and Functions

Symbol	Pins		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1-8	2-9	I/O	**PORT 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Port 1 also contains the timer 2 pins as a secondary function. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 1, as follows: – T2 (P1.0). Input to counter 2. – T2 (EX (P1.1). Capture/Reload trigger of timer 2.
RST/V_{PD}	9	10	I	**RESET** input. A high level on this pin resets the SAB 8052B. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11 13-19	I/O	**PORT 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: – RxD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TxD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	21 20		**XTAL 1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. **XTAL 2** output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**PORT 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.

Pin Definitions and Functions (continued)

Symbol	Pins		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
$\overline{PSEN}$	29	32	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	33	O	Provides **Address Latch Enable** output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	**External Access** enable. When held at a TTL high level, the ROM-versions executes instructions from the internal ROM when the PC points to the internal ROM address space. When held at a TTL low level, the ROM-versions fetch all instructions from external program memory. For the ROM-less versions this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44	–	+ 5 V **Power Supply** during operation and program verification.
V_{SS}	20	22	–	Circuit **Ground** potential
NC	–	1,12, 23,34	–	**No Connection**

Block Diagram



Instruction Set

The SAB 8052 /8032 Family has the same instruction set as the industry standard 8051 microcontroller.

A pocket guide is available which contains the complete instruction set in functional and hexadecimal order. Furtheron it provides helpful information about Special Function Registers, Interrupt Vectors and Assembler Directives.

Literature Information

Title	Ordering No.
Microcontroller Family SAB 8051 Pocket Guide	B158-H6497-X-X-7600

Absolute Maximum Ratings

Ambient temperature under bias
SAB 8052B/8032B/80513 ..... 0 to + 70 °C
SAB 8052B/8032B/80513-T40/85 ..... – 40 to 85 °C
SAB 8032B/80513-T40/110 ..... – 40 to 110 °C
Storage temperature ..... – 65 to + 150 °C
Voltage on any pin with respect to ground (V_{SS}) ..... – 0.5 to + 7 V
Power dissipation ..... 2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
T_A = 0 to 70 °C for SAB 8052B/8032B/80513
T_A = – 40 to 85 °C for SAB 8052B/8032B/80513-T40/85
T_A = – 40 to 110 °C for SAB 8032B/80513-T40/110

Symbol	Parameter	Limit Values		Unit	Test Conditions
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/V_{PD} and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/V_{PD} for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/V_{PD}	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	–	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA

DC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit	Test Conditions
		min.	max.		
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2				XTAL1 = V_{SS}
	SAB 8052B/8032B - 12/16/20	–	– 3.2	mA	V_{IL} = 0.45 V
	SAB 80513 - 12/16	–	– 3.2	mA	
	SAB 8052B/8032B - T40/85;T40/110	–	– 2.5	mA	
	SAB 80513 - 12/16 -	–	– 2.5	mA	
	T40/85;T40/110			mA	
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} - 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current				All outputs disconnected
	SAB 8052B/8032B	–	175	mA	
	SAB 8052B-16/8032B-16	–	175	mA	
	SAB 8052B-20/8032B-20	–	175	mA	
	SAB 80513	–	175	mA	
	SAB 80513-16	–	175	mA	
	SAB 80513-16-T40/85	–	200	mA	
I_{PD}	Power down current	–	15	mA	V_{CC} = 0 V; V_{PD} = 4.5 ... 5.5 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_C = 1 MHz

AC Characteristics for SAB 8052B/8032B/80513, 12 MHz

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to 70 °C for SAB 8052B/8032B/80513
T_A = – 40 to 85 °C for SAB 8052B/8032B/80513-T40/85
T_A = – 40 to 110 °C for SAB 8032B/80513-T40/110

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		Clock 12 MHz clock		Variable clock 1/tCLCL = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

tRLRH	$\overline{RD}$ pulse width	400	–	6tCLCL– 100	–	ns
tWLWH	$\overline{WR}$ pulse width	400	–	6tCLCL– 100	–	ns
tLLAX2	Address hold after ALE	132	–	2tCLCL– 35	–	ns
tRLDV	$\overline{RD}$ to valid data in	–	252	–	5tCLCL– 165	ns
tRHDX	Data hold after $\overline{RD}$	0	–	0	–	ns
tRHDZ	Data float after $\overline{RD}$	–	97	–	2tCLCL– 70	ns
tLLDV	ALE to valid data in	–	517	–	8tCLCL– 150	ns
tAVDV	Address to valid data in	–	585	–	9tCLCL– 165	ns
tLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3tCLCL– 50	3tCLCL + 50	ns
tAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4tCLCL– 130	–	ns
tWHLH	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	tCLCL– 40	tCLCL + 40	ns
tQVWX	Data valid to $\overline{WR}$ transition	33	–	tCLCL– 50	–	ns
tQVWH	Data setup before $\overline{WR}$	433	–	7tCLCL– 150	–	ns
tWHQX	Data hold after $\overline{WR}$	33	–	tCLCL– 50	–	ns
tRLAZ	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

tCLCL	Oscillator period	–	–	83.3	833.3	ns
tCHCX	High time	–	–	20	tCLCL– tCLCX	ns
tCLCX	Low time	–	–	20	tCLCL – tCHCX	ns
tCLCH	Rise time	–	–	–	20	ns
tCHCL	Fall time	–	–	–	20	ns

AC Characteristics for SAB 8052/8032B/80513, 12 MHz (cont'd)

Symbol	Parameter	Limit Values				Unit
		clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8052B/8032B/80513 to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8052B/8032B/80513, 16 MHz

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to 70 °C; for SAB 8052B/8032B/80513-16
T_A = – 40 to 85 °C for SAB 80513-16

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	33	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	28	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	153	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	88	–	$3t_{CLCL}$–100	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	48	–	t_{CLCL}–15	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	60	–	t_{CLCL}–3	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}$–90	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8052B-16/8032B/80513 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8052B/8032B/80513, 16 MHz(cont'd)

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	

External Data Memory Characteristics

t_{RLRH}	$\overline{RD}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	62.5	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

AC Characteristics for SAB 20 MHz/8032B-20, 20 MHz

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	
Program Memory Characteristics						
t_{LHLL}	ALE pulse width	60	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	20	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	20	–	$t_{CLCL}-30$	–	ns
t_{LLIV}	ALE to valid instruction in	–	100	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	25	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	115	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	75	–	$3t_{CLCL}-75$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	40	–	$t_{CLCL}-10$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	47	–	$t_{CLCL}-3$	–	ns
t_{AVIV}	Address to valid instruction in	–	190	–	$5t_{CLCL}-60$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8032B-20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8032B-20, 20 MHz (cont'd)

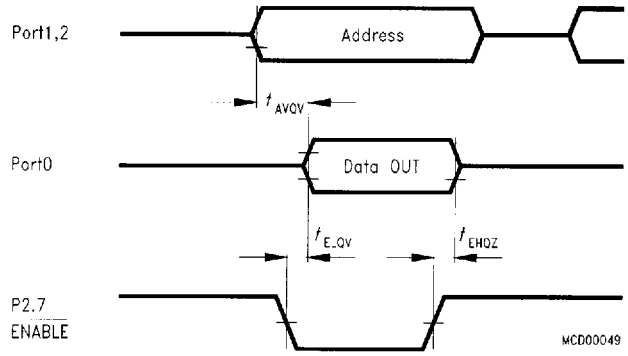
Symbol	Parameter	Limit Values				Unit
		Clock 20 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 20 MHz		
		min.	max.	min.	max.	
External Data Memory Characteristics						
t_{RLRH}	$\overline{RD}$ pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	70	–	$2t_{CLCL}-30$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	100	–	$5t_{CLCL}-150$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	40	–	$2t_{CLCL}-60$	ns
t_{LLDV}	ALE to valid data in	–	250	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	285	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	100	200	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	70	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	20	80	$t_{CLCL}-30$	$t_{CLCL}+30$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5	–	$t_{CLCL}-45$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	200	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	10	–	$t_{CLCL}-40$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns
External Clock Drive XTAL2						
t_{CLCL}	Oscillator period	–	–	50	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

ROM Verification Characteristics for SAB 8052B/8032B Family

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

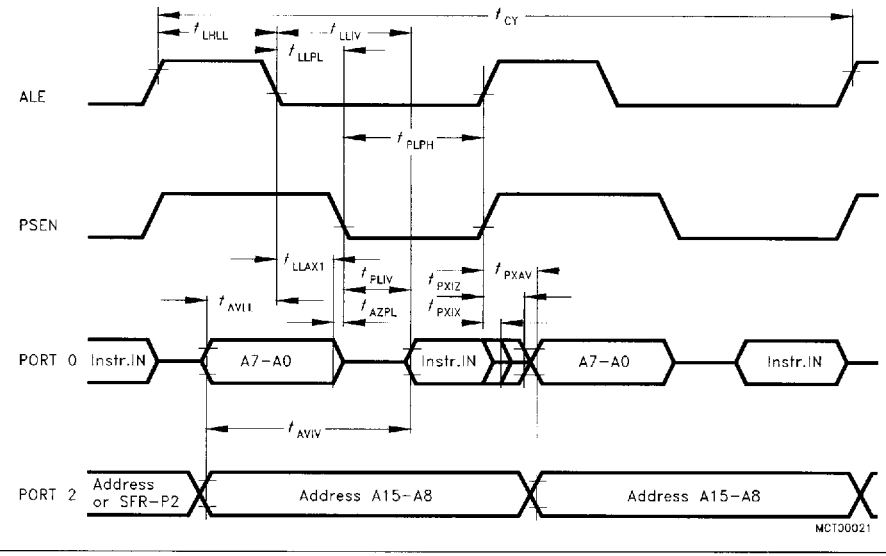
ROM Verification



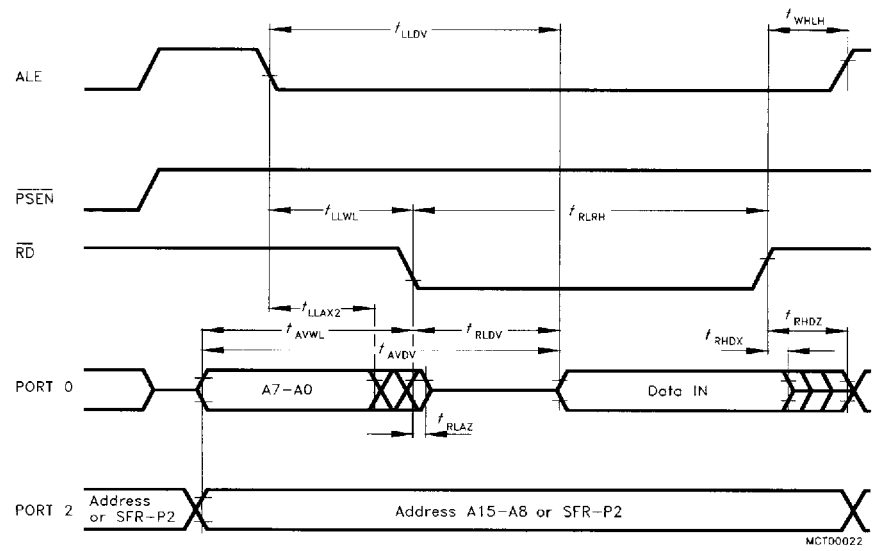
Microcontroller	Address	Data	Inputs	
SAB 8052B 8K × 8	P1.0 – P1.7 = A0 – A7 P2.0 – P2.4 = A8 – A12	Port 0 = D0 – D7	P2.5 – P2.6, $\overline{\text{PSEN}}$ ALE, $\overline{\text{EA}}$ RST/V_{PD}	= V_{SS} = V_{IH} = V_{IH1}
SAB 80513 16K × 8	P1.0 – P1.7 = A0 – A7 P2.0 – P2.5 = A8 – A13	Port 0 = D0 – D7	P2.6, $\overline{\text{PSEN}}$ ALE, $\overline{\text{EA}}$ RST/V_{PD}	= V_{SS} = V_{IH} = V_{IH1}

Waveforms

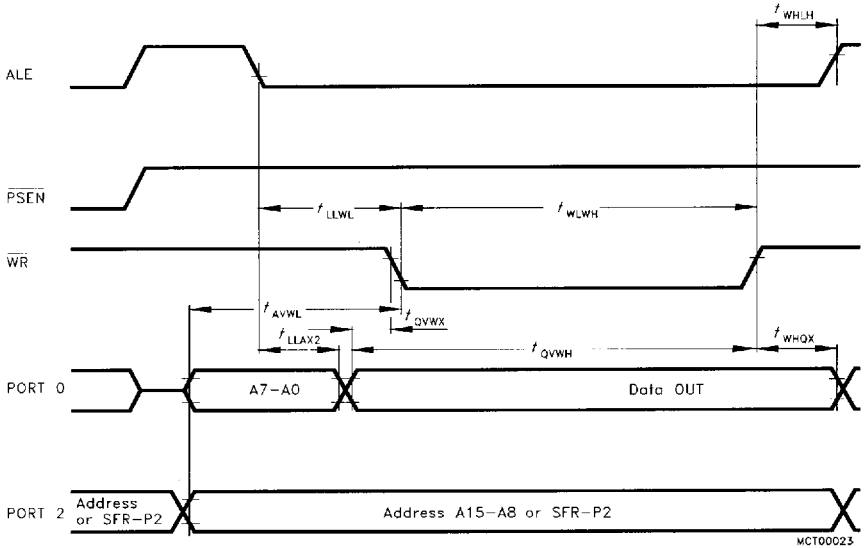
Program Memory Read Cycle



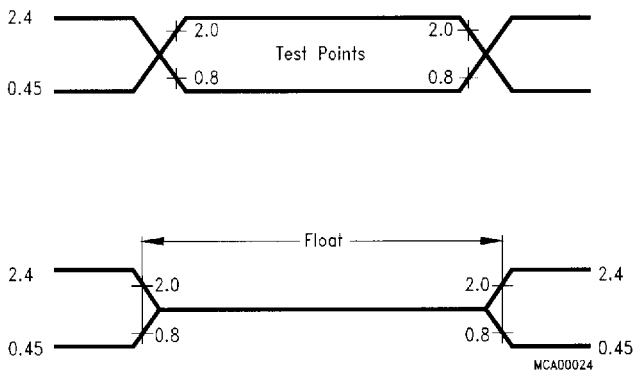
Data Memory Read Cycle



Data Memory Write Cycle

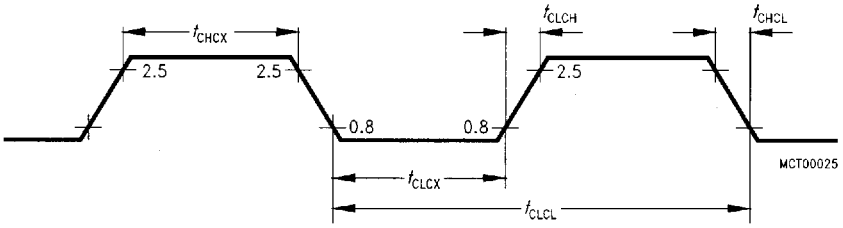


AC Testing Input, Output, Float Waveforms

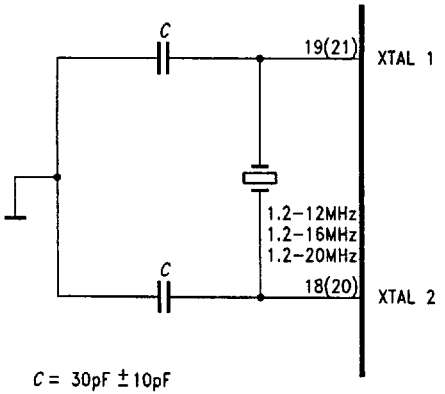


A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

External Clock Cycle

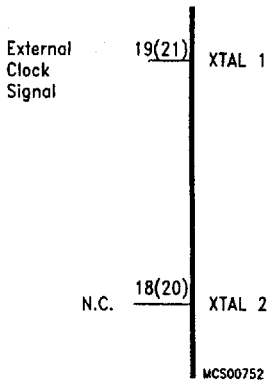


Recommended Oscillator Circuits



$C = 30pF \pm 10pF$

Crystal Oscillator Mode



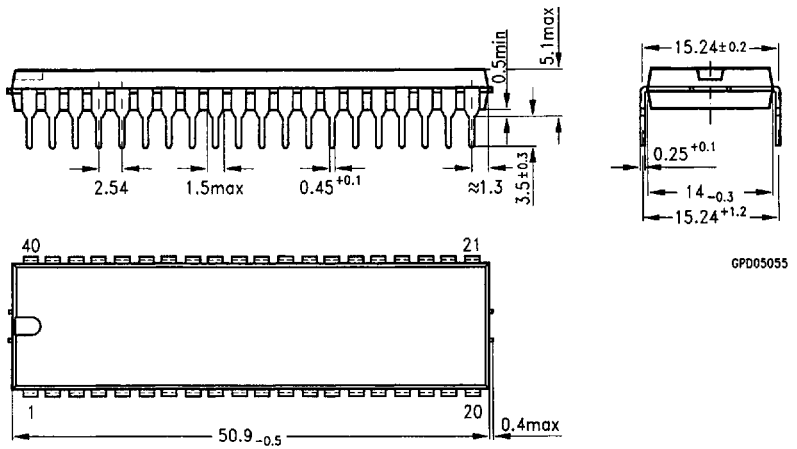
Driving from External Source

Pin numbers in (. . .) are specified for PL-CC-44 package.

Dimensions in mm

Package Outlines

Plastic Package, P-DIP-40
(Plastic Dual-in-Line Pack)



Plastic-Package, PL-CC-44
(Plastic Leaded Chip Carrier)