Product Specification

AHA4210 RSVP

Viterbi with Reed-Solomon Decoder

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Notes to Customers of AHA4210

1) Patent(s) pending. One or more patent(s) have been applied for this product.

2) Purchase of I^2C components of AHA conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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1.0 INTRODUCTION

The AHA4210, referred to as the RSVP, is a single-chip Forward Error Correction LSI device combining a Viterbi decoder, a Reed-Solomon decoder, a descrambler (energy dispersal) and a deinterleaver. The device conforms to the MPEG-II transport layer protocol specified by ISO/IEC standard and FEC requirements of Digital Video Broadcasting (DVB) DT/8622/DVB and DT/8610/III-B specification. These documents are referred to as the DVB specification.

The Viterbi decoder supports selectable code rates of 1/2, 2/3, 3/4, 5/6, 6/7 or 7/8 using industry standard puncturing algorithms. Viterbi decoded data rate is up to 62 Mbits/second at all code rates. The chip also performs byte alignment and block/packet synchronization detecting sync bytes used in transmission. The descrambling function is selectable with a programmable seed or performed externally. Each functional block may be bypassed giving more flexibility to a system designer.

Block size programmability, several code rate choices and programmable RS error correction capability allows flexibility to a digital communications system designer incorporating Forward Error Correction into a receiver. Intel 80C188 multiplexed parallel or serial I^2C protocol interface allows the system microprocessor to program internal registers and monitor channel performance.

This document contains key features, correction terms, functional description, signal functions, Related Technical Publications, DC and AC characteristics, pinout, package dimension and ordering information.

1.1 APPLICATIONS

- Satellite communications/VSAT
- DBS
- Military Communications

1.2 FEATURES

GENERAL:

- Conforms to the ISO/IEC-CD 13818-1 MPEG-II transport layer protocol and Digital Video Broadcasting (DVB)FEC specification
- Viterbi decoded data rates up to 62 Mbits/sec at any code rate
- Programmable block size from 34 to 255 bytes
- Multiplexed parallel Intel 80C188 or serial I^2C protocol microprocessor interface
- Byte or serial data output
- On-Chip error rate monitor
- Programmable bypass modes for each of the major blocks
- Configured to DVB mode of operation on power-up
- 68 pin PLCC

VITERBI DECODER:

- Selectable decoder rates 1/2, 2/3, 3/4, 5/6, 6/7 and 7/8 or automatic acquire mode
- 3-Bit soft-decision decoder inputs
- Constraint length k=7

SYNCHRONIZATION CONTROL:

- Automatic synchronization capability for QPSK based demodulator
- Up to one sync byte per block
- Responds to inverted sync byte

REED-SOLOMON:

- t=1 through 8 in increments of 0.5
- Correction capability of up to 8 bytes
- Internal FIFOs

DEINTERLEAVER:

- Programmable convolutional deinterleaving (Ramsey II, Ramsey II modified or Forney) to depth I=16
- No external RAM required

ENERGY DISPERSAL:

- Selectable on-chip DVB specification Energy Dispersal
- Optional bypass mode
- Programmable seed

1.3 CONVENTIONS AND NOTATIONS

- Certain signals are logically true at a voltage defined as “low” in the data sheet. All such signals have an “N” appended to the end of the signal name. For example, RSTN and RDYON.
- “Signal assertion” means the signal is logically true.
- Hex values are defined with a prefix of “0x”, such as “0x10”.
- A range of signal names is denoted by a set of colons between the numbers. Most significant bit is always shown first, followed by least significant bit. For example, ERRSTAT[6:0] represents number of bytes corrected by the Reed-Solomon decoder.
- A product of two variables is expressed with an “x”, for example, BLKLEN2 x JDEPTH represents Block Length multiplied by Interleave Depth.
- Megabytes per second is referred to as MBytes/sec or MB/sec. Megabits per second is referred as Mbits/sec or Mb/sec.
- Frequency of a clock signal is referred to as F(name). For example, F(VCLK) specifies frequency of VCLK.

1.4 DEFINITION OF TERMS AND PROGRAMMABILITY

VITERBI			
TERM	**NAME (other references)**	**DEFINITION**	**RANGE**
k	Constraint Length	Number of input bits over which convolutional code is computed.	7
	Traceback Depth	Length of path through the trellis over which the Viterbi decoder computes the likelihood of a decoded bit value.	minimum=115
	Puncturing	Process of deriving a higher rate code from a basic rate code.	N/A
	Puncture Pattern	Mapping between 1/2 rate encoded bits and new higher rate encoded bits.	N/A
	Convolutional Code Rate (Puncture Rate)	Ratio of input to output bits for convolutional code.	1/2, 2/3, 3/4, 5/6, 6/7, 7/8

DEINTERLEAVER			
TERM	**NAME (other references)**	**DEFINITION**	**RANGE**
	Ramsey or Forney	Convolutional interleave techniques.	N/A
J	Interleave Depth	Minimum separation in the interleaved stream.	1 through 16

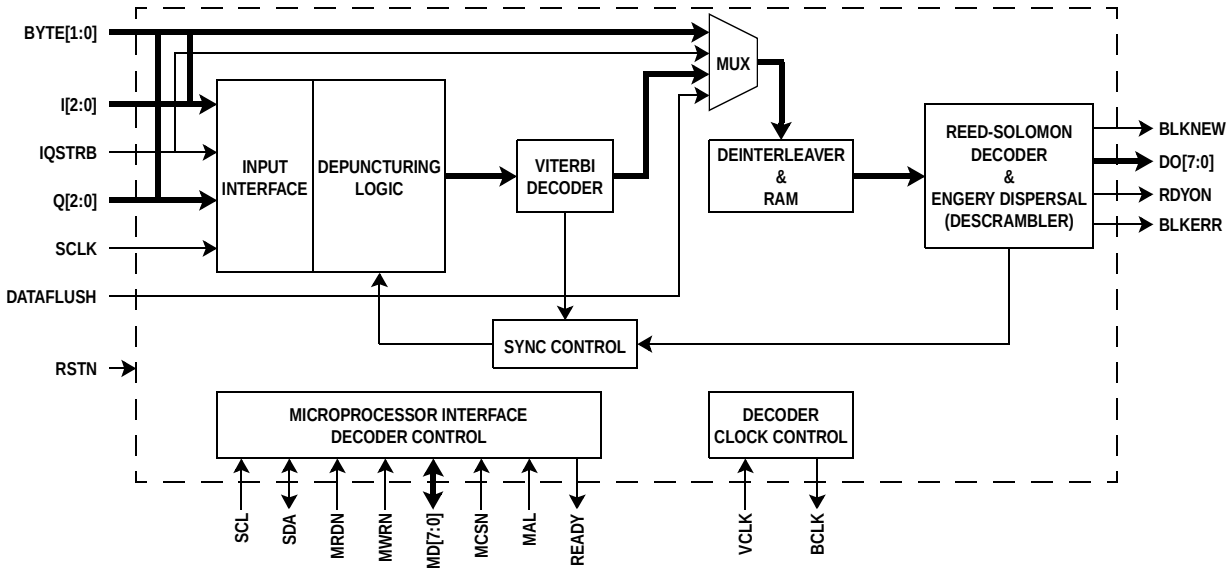
REED-SOLOMON			
TERM	**NAME (other references)**	**DEFINITION**	**RANGE**
K	Message Length (user data or message bytes)	Number of user data symbols in one message block. Size of a symbol in AHA4210 is 8-bits. Message length is $K = N - R$.	32 thru 253 bytes (32, 33, 34 . . . 253)
R	Check symbols (parity or redundancy)	Symbols appended to the user data to detect and correct errors. The number of check symbols required in a system is $R \geq 2e$. Every 2 check bytes correct 1 error byte.	2 thru 16 bytes in increments of 1 (2, 3, 4 . . . 16)
N	Codeword Length (block length)	Sum of message and check symbols. $N = K + R$.	34 thru 255 bytes (34, 35, 36 . . . 255)
t	Error Corrections	Maximum number of error corrections performed by the device. The value is t=Integer $\frac{N-K}{2}$.	1 thru 8 bytes in increments of 0.5 (1, 1.5, 2, 2.5 . . . 8)
e	Number of Errors	An error is defined as an erroneous byte whose correct value and position within the message block are both unknown.	minimum 0
	RS Code Rate	Ratio of message to block length, $\frac{K}{N}$.	0.67 through 0.99

GENERAL			
TERM	**NAME (other references)**	**DEFINITION**	**RANGE**
	Bypass	Processing data either through or around a functional block.	N/A
	Block	An entity of both message and Reed-Solomon check bytes. The number of message bytes is equal to the length of the MPEG-II packet for a DVB system.	(34, 35, . . . 255) bytes
	Packet	MPEG-II transport layer packet size.	188 including one sync mark byte

2.0 FUNCTIONAL DESCRIPTION

This section presents an architectural overview of the chip and its many functions, features and operating modes. Block diagram of the chip shows the Viterbi and Reed-Solomon decoder modules.

Figure 1: AHA4210 Block Diagram



2.1 SYNCHRONIZATION

This module synchronizes data received from Viterbi to byte and packet boundaries. The synchronization algorithm is summarized below.

Bit-to-byte mapping is performed while looking for sync marks specified in register VSYNCP. Every bit position is examined for a sync mark byte. If no sync mark is detected after looking for a minimum of two block lengths, then the phase is incremented and the process is repeated. Carrier and depuncture phases are cycled through searching for sync marks. This process terminates when sync is achieved.

After a sync mark is detected, additional sync marks as specified in SYNCON[2:0] are searched. Detection of additional sync completes the block sync process and data is output on the next inverted sync (or regular sync if VCON[7] = 0). Once the output data flow starts, consecutive sync marks are required if enabled by the VCON[6] to remain in sync. In this case if SYNCOFF[2:0] consecutive sync marks are missed, then the block goes out of the sync condition.

The block may also go out of sync if the Reed-Solomon uncorrectable blocks threshold is exceeded over a programmable number of blocks. This feature is enabled by VCON [5]. Total Block Count and Threshold are programmed by VRSSIZE and VRSTH registers.

2.1.1 EXPLANATION OF CLOCKING SCHEMES

The Viterbi block has two clock inputs: SCLK and VCLK. VCLK runs the actual Viterbi decoder block while SCLK simply drives the input stage for Viterbi. The data inputs I[2:0], Q[2:0] and IQSTRB are synchronous to SCLK.

There are two approaches to using this interface. Approach one involves tying IQSTRB to VDD (active) and assuring that:

$$\text{Frequency}(\text{SCLK}) \le \text{Frequency}\left(\frac{\text{VCLK}}{2 \times CR}\right)$$

Where *CR* is defined as the code rate. Note that this is a strict requirement and the chip will enter a state requiring a hard reset if this is not met.

One advantage to this approach is that in some designs SCLK is already available and I and Q are already synchronous to this signal.

The other method is to tie SCLK and VCLK together and throttle the data with IQSTRB. For any given code rate $\frac{X}{Y}$, where Y is even, IQSTRB would be held high (clocking in I[2:0] and Q[2:0] on that cycle) for no more than $\frac{Y}{2}$ out of every X clocks. If Y is odd then IQSTRB would be held high for no more than Y out of every $2X$ clocks and no more than $\frac{Y+1}{2}$ in every X clock cycles.

In the final approach it is not necessary to supply a separate clock (SCLK), however, the customer must supply the circuitry to drive IQSTRB appropriately.

The Viterbi decoder can be set up to cycle through all convolutional code rates. In this case, use convolutional code rate ≥ 7/8 in the equation:

$$F(SCLK) \le \frac{F(VCLK)}{2 \times CR}$$

2.2 VITERBI DECODER

The Viterbi decoder takes the data from an I and a Q channel and decodes these using a 3 bit soft decision. The Viterbi decoder is based on a 1/2 rate code, but also supports punctured codes with rates: 2/3, 3/4, 5/6, 6/7 and 7/8.

The generator polynomials are:

$g1$ = 171(octal) and $g2$ = 133(octal)

The minimum trace back depth is 115.

The output of the Viterbi decoder is converted to 8 bit bytes, sync bytes are detected and after which the data is run through the deinterleaver to restore the ECC blocks.

The Viterbi decoder can be bypassed by bit 2 of the IOCNTRL and disabled by bit 4 of the VCON register.

The latency of the Viterbi block is measured in two ways. First, there is a latency associated with "synching" to the incoming signal. Assuming that there is no valid sync byte patterns in the data the worst case sync time is given by:

$$(8 \times \text{block length} + 384) \times 4 \times (\text{\# of puncture phases}) + 512$$

This assumes that SCLK runs fast enough to keep the data pipeline full. Once the Viterbi block is synched up, the maximum latency from input to output is 258 VCLK cycles.

2.2.1 DEPUNCTURE

The Viterbi module can be programmed to depuncture according to a specified code rate or automatically find the code rate used in the channel. Following is a list of puncture patterns and number of phases that are cycled through in an attempt to align the puncture phase.

RATE	*PATTERN: X:Y*		*# OF PHASES*
1/2	X Y	1 1	1
2/3	X Y	10 11	3
3/4	X Y	101 110	2
5/6	X Y	10101 11010	3
6/7	X Y	100101 111010	7
7/8	X Y	1000101 1111010	4

During the encoding process, *X* and *Y* are mapped into I and Q by taking the nondeleted terms in order of *X*1, *Y*1, *X*2, *Y*2, etc. Deleted terms are simply skipped. The decoding process is simply the reverse of this procedure. Erasures are inserted on the pattern locations with zeroes. For example, the rate 5/6 I and Q have values:

I = *X*1, *Y*2, *Y*4, *X*1, *Y*2, *Y*4, . . .

Q = *Y*1, *X*3, *X*5, *Y*1, *X*3, *X*5, . . .

The chip is capable of supporting a limited number of depuncture codes not included in this specification. The procedure for supporting these codes are beyond the scope of this specification. Please contact AHA Applications Engineering for these codes.

The Viterbi core can be configured to self synchronize to the appropriate depuncture pattern phase and correct for $\frac{pi}{2}$ phase ambiguity. If VRSSIZE[6] is set, Viterbi sync does not cycle through carrier phases. If the code rate is not known, the core can also be configured to cycle through 1/2, 2/3, 3/4, 5/6, 6/7 and 7/8 code rates looking for a valid pattern.

2.3 DEINTERLEAVER

The deinterleaver supports a variety of programmed options:

TECHNIQUE	*TYPE*	*WITH VITERBI*	*WITHOUT VITERBI*
Ramsey	II	No	Yes
Forney/Ramsey	III	Yes	Yes
Modified Ramsey	II	Yes	Yes

A Ramsey type II interleaver is specified in J.L. Ramsey, "Realization of Optimal Interleavers," *IEEE Transaction on Information Theory,* May 1970, pp. 338-345. A Forney/Ramsey type III interleaver is specified in DVB DT/8622/DVB specification. The interleave depth is programmable up to 16 packets and the block size is programmable up to 255 bytes. However, the product of the interleave depth and block length cannot be larger than 2688 bytes. In addition to this, the following conditions must be satisfied for various applications.

APP	*INTERLEAVE*	*CONSTRAINT*
DVB	Forney/ Ramsey III	BLKLEN2/JDEPTH[3:0] must be an integer
	Ramsey II	BLKLEN and JDEPTH[3:0] must be relatively prime
	Ramsey II modified	Same as Ramsey II

Maximum processing latency =

$$8 \times (\text{NJM[3:0] \& NJL[7:0]}) \text{VCLKS}$$

Note that the "&" is a concatenation symbol.

2.4 RS DECODER

The RS block performs the outer decoding. The Reed-Solomon decoder conforms to the DVB specification. The RS block can be programmed to decode t=1, 1.5, 2, . . . 7.5, 8.

$$p(x) = x^8 + x^4 + x^3 + x^2 + 1$$

$$g(x) = (x + \alpha^0)(x + \alpha^1)\ldots(x + \alpha^{(2t-1)})$$

$$\alpha^1 = \text{primitive element}$$

The block length of the code is programmable up to 255 bytes. Block length is 204 with 16 check bytes and a correction power of 8 bytes per block for the DVB specification. Maximum latency through the RS Decoder Block is:

$$(N-1)\times 8 + 120 + 2R + N \times 2.67$$

2.5 DERANDOMIZE/ENERGY DISPERSAL

The derandomizer is specified in the DVB specification. It is built as a 15 stage pseudo-random binary sequence generator with initialization sequence specified by RSEED0 and RSEED1 registers. The randomization occurs over 8 blocks of MGSBYTES2 (188 bytes for DVB specification). Randomization does not occur over Reed-Solomon parity bytes nor sync bytes. However, the pseudo-random binary sequence generator continues to run during non-inverted sync bytes. Maximum latency = 10 VCLKs.

2.6 MODES OF OPERATION

The FEC decoder has been designed with a modular approach so that each of the four major functions: Viterbi decoding, deinterleaving, RS decoding and derandomization can be individually enabled or disabled. Five operating modes are supported by the device. These are:

1) Normal mode. All functions enabled. Inputs clocked with SCLK.
2) Byte Input mode. All functions except Viterbi enabled. Inputs clocked with VCLK. Tie SCLK to VCLK. Use Byte [1:0], I[2:0] and Q[2:0] as byte wide data path. Bytes must arrive on packet boundaries.
3) Viterbi decode mode. Inputs clocked with SCLK.
4) Reed-Solomon decode mode. Same input constraints as byte input mode.
5) Deinterleave mode. Same input constraints as byte input mode.

These modes may be operated with or without the derandomizer enabled.

Table 1: Various Modes Supported by the AHA4210 Device

MODE	*FUNCTIONAL BLOCK*			
	VITERBI	*DEINTERLEAVER*	*RS DECODER*	*DERANDOMIZER*
1) Normal	Enabled	Enabled	Enabled	Either
2) Byte Input	Disabled	Enabled	Enabled	Either
3) Viterbi Decode	Enabled	Disabled	Disabled	Either
4) RS Decode	Disabled	Disabled	Enabled	Either
5) Deinterleaver	Disabled	Enabled	Disabled	Either

Table 2: Register Settings for Functional Block Bypass

FUNCTIONAL BLOCK	*ENABLED*	*DISABLED*
Viterbi	VCON[4]=1 IOCNTRL[2]=0	VCON[4]=0 IOCNTRL[2]=1
Deinterleaver	JDEPTH[4]=1	JDEPTH[4]=0
Reed-Solomon	RSCONTROL=0C	RSCONTROL=1C
Derandomizer	IOCNTRL[7]=1; VCON[7]=1	IOCNTRL[7]=0; VCON[7]=0

2.7 MICROPROCESSOR INTERFACE

The device is capable of interfacing to a multiplexed eight bit bus or the I^2C serial interface. The system microprocessor is referred to as the host and behaves as a “master” and the AHA device is a “slave.”

2.7.1 PARALLEL 80C188 MICROPROCESSOR INTERFACE

The parallel interface supports an Intel 80C188 microprocessor with a multiplexed address and data bus. For a register read operation the chip select (MCSN) is asserted. The device asserts the READY signal low. This is followed by the host outputting the register address on the MD[7:0] bus along with the address latch enable (MAL). The host then asserts the read strobe (MRDN). The device responds by outputting the data on the MD[7:0] bus and tristating the READY signal. Valid data is available when READY is tristated by the device. Bus cycle is terminated by the host deasserting the MRDN signal.

A register write operation is similar to the register read except the host asserts the MWRN strobe along with the data. The device then loads the data into the appropriate register and tristates the READY signal. The bus cycle terminates when the MWRN strobe gets deasserted.

When using the parallel interface tie the SCL and the SDA signals high. ***MCSN must not glitch***.

2.7.2 SERIAL I^2C PROTOCOL INTERFACE

The I^2C interface is a serial microprocessor interface using two signals named SCL and SDA. Any drivers connected to these signals must be open drain or open collector to facilitate the wired-AND operation of this bus. There is one SCL pulse per data bit and the SDA line must be stable during the high period of the SCL pulse, changing only when SCL is low for data transfers.

In a target design using the I^2C serial interface, the following connections need to be made. Connect MRDN and MWRN to Ground. Tie MCSN high and connect MAL to Ground. The lower five bits of the MD[7:0] bus need to be hardwired to the correct Slave ID address. For example, if a Slave ID address of 5 is needed, connect bits 0 and 2 to VDD, and bits 1, 3 and 4 to Ground.

The following paragraphs describe briefly the serial communication over this bus. For more detailed information please refer to the I^2C Bus Specification listed in the Related Technical Publications section. This device works in either high speed mode or standard low speed mode.

In high speed mode, the first two bytes between a host and a slave device determine the device selected. These two bytes are the first two bytes following the Start condition as shown in Figure 5.

The bytes contain: 1, 1, 1, 1, 0, AD4, AD3, R/W, and AD2, AD1, AD0, A4, A3, A2, A1, A0.

AD[4:0] = Slave ID address
A[4:0] = Register address
R/W = Direction of data transfer where:
1 = Read; 0 = Write

When programming the registers in I^2C mode, the device performs auto increment of internal addresses. All 16 addresses may be accessed by writing 21 values to Address 0x00 as shown in Figure 2. Alternatively a register may be randomly accessed by specifying its address, such as 0x04.

Figure 2 is an example of writing to one or more registers. Figure 3 is an example of reading a register.

The serial I^2C interface protocol conforms to the I^2C Bus Specification. For electrical performance of this interface, please refer to the Timing section.

Notes:

1) *This document contains a very brief description of the I^2C Bus functions. For a detailed description, please refer to Specification documents available from Philips.*
2) *I^2C Bus protocol supported by AHA4210 requires a 10-bit addressing.*
3) *See Note 2 on back of cover page.*

Figure 2: I²C Internal Register Increment Example, Writing the Registers

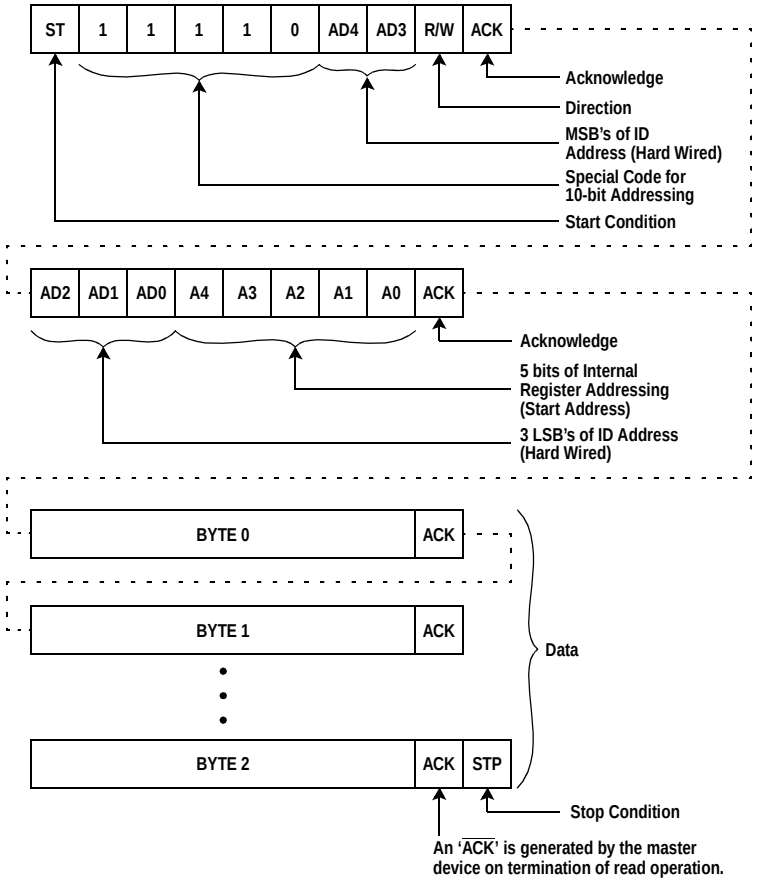


Figure 3: I²C Reading Internal Registers

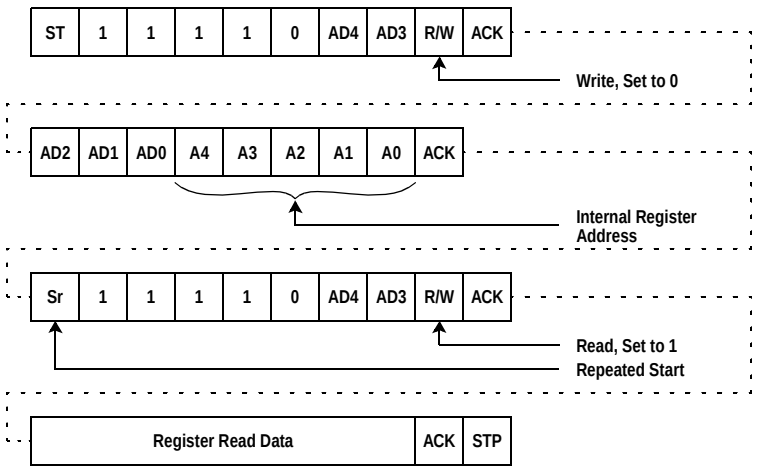


Figure 4: Bit Transfer

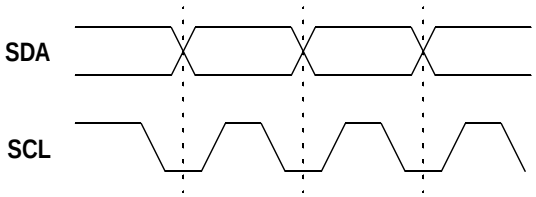
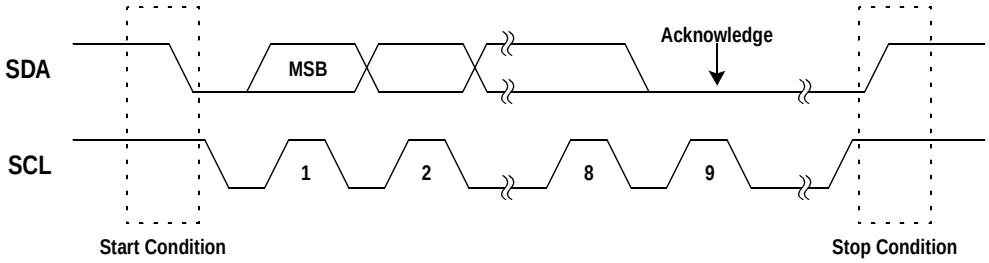


Figure 5: Start and Stop Conditions



2.8 LATENCY

Maximum latency measured in VCLK cycles through the various blocks is summarized in Table 3.

Table 3: Maximum Latency in VCLK Cycles

FUNCTIONAL BLOCK	*LATENCY*
Viterbi	258 (after sync has been acquired)
Deinterleaver	8 x (NJM[3:0] & NJL[7:0])
RS Decoder	(N-1)x8+120+2R+Nx2.67
Derandomizer	10

3.0 REGISTER DESCRIPTION

This section contains a summary and a description of registers. Unless otherwise specified, all registers are Read/Write. The following registers can be changed during operation: ERRSIZE, VRSSIZE[5:0], VSYNCP, VRSTH, VERTH, VCON[3:0], RSEED0 and RSEED1. The other registers must be programmed before the first data is input to the AHA4210 after a reset.

3.1 REGISTER SUMMARY

FUNCTIONAL BLOCK	*ADDRESS*	*MNEMONIC*	*REGISTER NAME*	*RESET VALUE*
Error Monitor	0x00	ERRSTAT	Error Count	0x00
	0x01	ERRSIZE	Total Block Count for ERRSTAT	0x20
Viterbi and Synchronizer	0x02	VRSSIZE	Total Block Count for VRSTH	0x18
	0x03	VSYNCP	Sync Decoder Pattern	0x47
	0x04	VRSTH	Reed-Solomon Uncorrectable Blocks Threshold	0x08
	0x05	VERTH	Sync Control	0x27
	0x06	VCON	Viterbi Control	0xB3
Derandomizer	0x07	MSGBYTES2	Message bytes, k	0xBC
	0x08	RSEED0	Derandomizer seed, LSB	0xA9
	0x09	RSEED1	Derandomizer seed, MSB	0x00
	0x0A	IOCNTRL	Input/Output Control	0x90
Deinterleaver	0x0B	NJL	Block Length times Interleave Depth, LSB	0x90
	0x0C	NJM	Block Length times Interleave Depth, MSB	0x09
	0x0D	BLKLEN2	Reed-Solomon Block Length, N	0xCC
	0x0E	JDEPTH	Interleave Depth	0x1C
Reed-Solomon	0x0F	RES RES CHKBYTES MSGBYTES BLKLEN RSCONTROL	Reserved Reserved Check bytes Message bytes Block Length Reed-Solomon Control	0xFF 0xFF 0x90 0xBC 0xCC 0x0C

Notes:

1) *Reed-Solomon registers, address 0x0F, are Write only. All other registers are Read/Write.*
2) *All six registers of the Reed-Solomon block must be programmed consecutively. Write to address 0x0F accesses these registers.*
3) *On Reset, the AHA4210 device is configured for DVB specification operation.*

3.2 ERRSTAT: ERROR COUNT STATUS

Address: 0x00; Reset Value = 0x00

BIT	*DESCRIPTION*
7	1 = One or more blocks within ERRSIZE is flagged uncorrectable. Bits [6:0] values do not represent total corrected locations. 0 = Errors have been corrected. Bits [6:0] represent total corrected locations.
6:0	Number of bytes corrected by RS in ERRSIZE blocks. These bits should be ignored when bit [7] is set to '1' or when RS is bypassed. If the number of errors exceeds 126, then the value in this register saturates at 127.

3.3 ERRSIZE: ERROR BLOCK COUNT

Address: 0x01; Reset Value = 0x20

BIT	DESCRIPTION
7:0	Total number of blocks over which ERRSTAT counts corrected bytes by Reed-Solomon.

3.4 VRSSIZE: TOTAL BLOCK COUNT FOR VRSTH

Address: 0x02; Reset Value = 0x18

BIT	DESCRIPTION
7	Reserved. Set to '0'.
6	If set, then Viterbi sync does not cycle through carrier phases.
5:0	The number of total blocks over which the number of uncorrectable blocks is counted and compared to the VRSTH value.

3.5 VSYNCP: SYNC DECODER PATTERN

Address: 0x03; Reset Value = 0x47

BIT	DESCRIPTION
7:0	The value of the sync byte. The inverted sync value is derived from VSYNCP.

3.6 VRSTH: RS UNCORRECTABLE BLOCKS THRESHOLD

Address: 0x04; Reset Value = 0x08

BIT	DESCRIPTION
7:4	Reserved. Set to '0'.
3:0	RSOFF is Reed-Solomon uncorrectable blocks threshold.

3.7 VERTH: SYNC CONTROL

Address: 0x05; Reset Value = 0x27

BIT	DESCRIPTION
7	Reserved. Set to '0'.
6:4	SYNCON is the number of sync bytes that must be detected before the synchronization block claims synchronization has been achieved. Minimum value is 2. Values of 0 and 1 are illegal and result in unknown operation. See *Inverted Sync Note*.
3	Specify mapping number on the input signal. 0 = mapping #1 0 = strongest zero, 3 = weakest zero 4 = weakest one, 7 = strongest one 1 = mapping #2 3 = strongest zero, 0 = weakest zero 4 = weakest one, 7 = strongest one
2:0	SYNCOFF is the number of sync bytes that must be missed before the synchronization block claims synchronization has been lost. 0 is illegal. See *Inverted Sync Note*.

Inverted Sync Note:

When the SYNCON value is set to '010' and VCON[7]=1, the AHA4210 can sync onto an inverted data stream, such as can occur if the demod is 180 degrees out of phase. When SYNCOFF value is set to '111' and VCON[7:5] is set to '110' or '100', the AHA4210 does not go out of sync when an inverted data stream occurs. In either case, enabling the Reed-Solomon error rate control over resynchronization VCON[5] causes the AHA4210 to recover from these conditions.

3.8 VCON: VITERBI CONTROL

Address: 0x06; Reset Value = 0xB3

BIT	DESCRIPTION
7	1 = enable, 0 = disable inverted sync detection.
6	1 = enable, 0 = disable resynchronization if the missed sync byte threshold (SYNCOFF) is exceeded. See *Burst Error Note*.
5	1 = enable, 0 = disable Reed-Solomon error rate control over resynchronization (VRSTH, VRSSIZE).
4	1 = enable, 0 = disable Viterbi decoder. This does not provide a bypass mode. It turns off the Viterbi for power savings.
3	1 = hard, 0 = soft decision input.
2:0	Puncture rate: 0 = automatic puncture detection 1 = 1/2 rate 2 = 2/3 rate 3 = 3/4 rate 4 = reserved 5 = 5/6 rate 6 = 6/7 rate 7 = 7/8 rate

Burst Error Note:

When the resynchronization of the AHA4210 is controlled only by the Reed-Solomon error rate control and a burst of all input values are zero of any strength, then the Reed-Solomon receives a valid codeword (of all 0s). In this case, the AHA4210 does not go out of sync during the burst and does not flag the output as uncorrectable. If this condition is unacceptable, enable the missed sync byte resynchronization mechanism, VCON[6].

3.9 MSGBYTES2: MESSAGE BYTES K

Address: 0x07; Reset Value = 0xBC

BIT	DESCRIPTION
7:0	Set equal to MSGBYTES. This value is used by the derandomizer module.

3.10 RSEED0: DERANDOMIZER SEED LSB

Address: 0x08; Reset Value = 0xA9

BIT	DESCRIPTION
7:0	Least significant byte of derandomizer seed.

3.11 RSEED1: DERANDOMIZER SEED MSB

Address: 0x09; Reset Value = 0x00

BIT	DESCRIPTION
7	Reserved. Set to ‘0’
6:0	Most significant byte of derandomizer seed.

3.12 IOCNTRL: INPUT/OUTPUT CONTROL

Address: 0x0A; Reset Value = 0x90

BIT	DESCRIPTION
7	1 = Enable derandomization. 0 = Bypass derandomization.
6	1 = Output check bytes. 0 = Do not output check bytes.
5	1 = Set error flag in packet header according to ISO/IEC CD 13818-1 (MPEG-II). (Bit seven of second byte of the block is set if the block is uncorrectable.) 0 = Do not set error flag in packet header.
4	1 = Bytes output. 0 = Serial output.
3	1 = 4 VCLK active RDYON. 0 = 1 VCLK active RDYON. See timing diagrams for these output modes for further details.
2:1	11 = Data is taken from BYTE[1:0]; I[2:0]; Q[2:0] directly into the deinterleaver on BCLK. Output is available on BCLK. When this mode is selected, set IOCNTRL[4:3]=10. 10 = Data is taken from BYTE[1:0]; I[2:0]; Q[2:0] directly into the deinterleaver on VCLK. Output is available on VCLK. 0x = Data taken from I[2:0] and Q[2:0] into the Viterbi decoder on SCLK. Output is available on VCLK.
0	Set to ‘1’ if deinterleaver is programmed to remove sync bytes.

3.13 NJL: BLOCK LENGTH TIMES INTERLEAVE DEPTH LSB

Address: 0x0B; Reset Value = 0x90

BIT	DESCRIPTION
7:0	LSByte of BLKLEN x JDEPTH product.

3.14 NJM: BLOCK LENGTH TIMES INTERLEAVE DEPTH MSB

Address: 0x0C; Reset Value = 0x09

BIT	DESCRIPTION
7:5	Reserved. Set to ‘0’.
4	Set for deinterleaver to remove the first byte of each block specified by BLKLEN2 register and perform a modified Ramsey II.
3:0	Most significant nibble of BLKLEN x JDEPTH product. This product must be less than or equal to 2688 decimal.

3.15 BLKLEN2: RS BLOCK LENGTH N

Address: 0x0D; Reset Value = 0xCC

BIT	DESCRIPTION
7:0	Set equal to BLKLEN except when NJM[4] is set. Then use BLKLEN2 = BLKLEN +1. Writing to this register loads the same value into a register in the synchronization (in Viterbi), derandomization and deinterleave modules.

3.16 JDEPTH: INTERLEAVE DEPTH

Address: 0x0E; Reset Value = 0x1C

BIT	DESCRIPTION
7	Reserved. Set to ‘0’.
6	A status bit indicating that deinterleaved data is being sent to the Reed-Solomon decoder. This bit is only valid if the deinterleaver is enabled (JDEPTH[4] is a ‘1’). When a ‘0’ is written to this bit then the current value is not changed. 0 = deinterleaver is not passing data. 1 = deinterleaver is passing data.
5	0 = Forney, 1 = Ramsey II
4	1 = Enable, 0 = Bypass
3:0	Interleave depth. 0 sets depth to 16. 1 is illegal. For more constraints on depth see Functional Description Section.

3.17 RSCONTROL: REED-SOLOMON CONTROL

The RS block must be programmed sequentially since there is only one address allocated for it.

Address: 0x0F; Reset Value = 0xFF, 0xFF, 0x90, 0xBC, 0xCC, 0x0C

BIT	DESCRIPTION
RES	
7:0	Reserved. Set to FF.
RES	
7:0	Reserved. Set to FF.
CHKBYTES	
7	Reserved. Set to ‘1’.
6:5	Reserved. Set to ‘0’.
4:0	Number of check bytes, R. Between 0x02 and 0x10.
MSGBYTES	
7:0	Number of message bytes in the code, K. Between 0x20 and 0xFD.
BLKLEN	
7:0	Number of bytes in a block, N. Between 0x22 and 0xFF.
RSCONTROL	
7:0	0C = Output corrected data. 1C = Pass uncorrected raw data through.

4.0 SIGNAL DESCRIPTIONS AND SPECIFICATIONS

This section describes the signals and each of their characteristics including setup and hold times relative to their synchronization clocks where applicable, reset conditions and load capacitances.

4.1 INPUT SIGNALS

SIGNAL	*NAME AND DESCRIPTION*	*ACTIVE STATE OR EDGE*
RSTN	Reset. When active, forces all internal control circuitry into a known state and initializes all data path elements. Must remain active and remain high as specified in AC Timing before the device can be used.	Low
SCLK	Symbol clock for I and Q.	Rising edge
VCLK	Clock input for Viterbi decoder and for outputs.	Rising edge
BYTE[1:0]	Byte input. Top two bits of input byte for Byte Input mode bypassing the Viterbi block. When this mode is not used, ground these pins.	N/A
I[2:0]	3-bit in-phase soft decision input. Soft decision component from demod to the Viterbi decoder. For hard decision input use I[2], I[1:0] are grounded. Used as middle three bits for byte input mode. Synchronized to VCLK in byte input mode, to SCLK for Viterbi.	N/A
Q[2:0]	3-bit quadrature-phase soft decision input. Soft decision component from demod to the Viterbi decoder. For hard decision input use I[2], I[1:0] are grounded. Used as lowest three bits for byte input mode. Synchronized to VCLK in byte input mode; to SCLK for Viterbi.	N/A
IQSTRB	Clock in I, Q and Byte data. When active, inputs Byte, I and Q are strobed into the device. For byte input mode, synchronize to VCLK; to SCLK for Viterbi. For byte input mode, max rate of IQSTRB is 1/8 VCLK or 1 BCLK. Active for one VCLK period.	High
MRDN	Microprocessor Read Enable. For I^2C operation, this must be tied to ground.	Low
MWRN	Microprocessor Write Enable. For I^2C operation, this must be tied to ground.	Low
MCSN	Microprocessor Chip Select. For I^2C operation, this must be tied high. For parallel 80C188 interface, this signal is low true and ***Must not Glitch***.	Low
MAL	Microprocessor Address Latch. For I^2C operation, this must be tied to ground.	High
SCL	I^2C Clock. Synchronous clock for I^2C interface. For 80C188 interface, this must be tied high.	See timing diagram
DATAFLUSH	Data Flush. A high signal for a minimum of one VCLK period resets the deinterleaver and initiates a data pipeline flush in Byte Input mode. New data must not be input for at least 16 x BLKLEN2 x VCLK periods after the signal goes low. This period is required to flush the data completely through the pipeline. For Viterbi input mode tie to VSS.	High

4.2 OUTPUT SIGNALS

SIGNAL	*NAME AND DESCRIPTION*	*ACTIVE STATE OR EDGE*
DO[7:0]	Data Output Bus. The output byte is driven from the rising edge of VCLK or BCLK. For serial output mode, DO[7] contains the data and DO[6:0] is '0'.	N/A
BLKNEW	Start of block signal. MPEG-II transport stream packet start flag. Valid with RDYON low during the first byte of each block.	High
RDYON	Output Ready strobe. Indicates that output data on DO[7:0] is valid. There is no external signal to throttle output data transfer. The max rate of RDYON is 1/8 VCLK or BCLK.	Low
BLKERR	Block uncorrectable. Active during first output byte of packet (with RDYON low and BLKNEW high) if the block to be output cannot be corrected. Should be ignored if Reed-Solomon block is bypassed.	High
READY	Microprocessor Access Ready. Indicates that the chip has completed a microprocessor read or write cycle. At the beginning of processor cycles, this output is driven to a low voltage, indicating that the chip is not ready. This signal is tristated when processor cycles are inactive. The reset state of this pin is high impedance.	Low when busy, Otherwise, tristated.
BCLK	Output Clock. This clock is derived from VCLK and is 1/8 frequency of VCLK.	

4.3 BIDIRECTIONAL SIGNALS

SIGNAL	*NAME AND DESCRIPTION*	*ACTIVE STATE OR EDGE*
MD[7:0]	Multiplexed Address/Data Bus. Mux bus supporting 80C188. For I^2C interface, MD[4:0] specify the top five bits of address for the device while MD[7:5] are don't cares and must be terminated high or low.	N/A
SDA	I^2C Data Bus. Serial data for I^2C interface. For 80C188, this must be tied high.	N/A

4.4 INPUT SPECIFICATIONS

PIN NUMBER	SIGNAL NAME	SELF LOAD (MAX IN pF)	STROBE
31	I[2]	10	VCLK/SCLK
30	I[1]	10	VCLK/SCLK
28	I[0]	10	VCLK/SCLK
25	Q[2]	10	VCLK/SCLK
24	Q[1]	10	VCLK/SCLK
23	Q[0]	10	VCLK/SCLK
37	BYTE[1]	10	VCLK
38	BYTE[0]	10	VCLK
48	RSTN	10	VCLK
26	IQSTRB	10	VCLK/SCLK
45	MRDN	10	See timing diagram
46	MWRN	10	
41	MCSN	10	
43	MAL	10	
21	SCLK	10	N/A
34	VCLK	10	N/A
39	SCL	10	VCLK
19	*Reserved, connect to VSS*	10	N/A
18	DATAFLUSH	10	VCLK

4.5 OUTPUT SPECIFICATIONS

PIN NUMBER	SIGNAL NAME	LOAD CAP (MAX IN pF)	STROBE REF
9	DO[7]	20	VCLK
8	DO[6]	20	VCLK
6	DO[5]	20	VCLK
4	DO[4]	20	VCLK
3	DO[3]	20	VCLK
1	DO[2]	20	VCLK
67	DO[1]	20	VCLK
66	DO[0]	20	VCLK
12	RDYON	20	VCLK
11	BLKNEW	20	VCLK
13	BLKERR	20	VCLK
51	READY	20	VCLK
16	BCLK	20	VCLK
14	*Reserved*	N/A	N/A

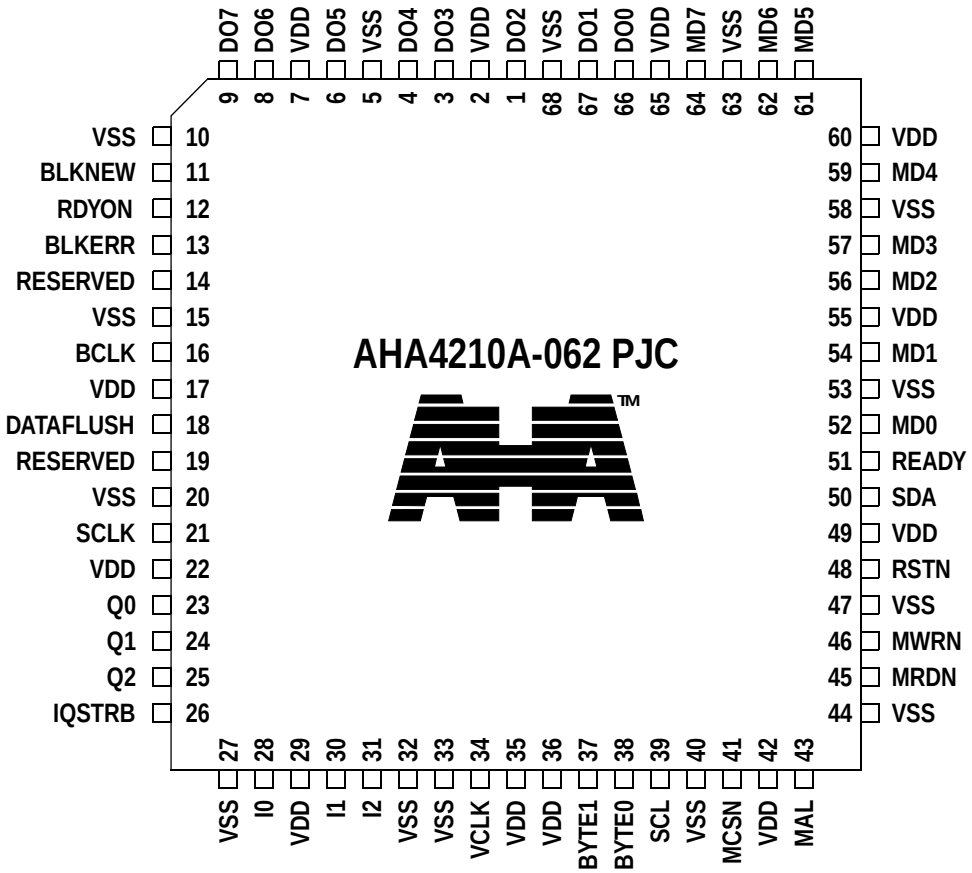
4.6 BIDIRECTIONAL PIN SPECIFICATIONS

PIN NUMBER	*SIGNAL NAME*	*SELF LOAD (MAX IN pF)*	*LOAD CAP (MAX IN pF)*	*STROBE REF*
50	SDA	10	20	VCLK
52	MD[0]	10	20	See timing diagrams
54	MD[1]	10	20	
56	MD[2]	10	20	
57	MD[3]	10	20	
59	MD[4]	10	20	
61	MD[5]	10	20	
62	MD[6]	10	20	
64	MD[7]	10	20	

4.7 POWER & GROUND PINS

PIN NUMBER	*SIGNAL NAME*
2, 7, 17, 22, 29, 35, 36, 42, 49, 55, 60, 65	VDD
5, 10, 15, 20, 27, 32, 33, 40, 44, 47, 53, 58, 63, 68	VSS

4.8 PINOUT

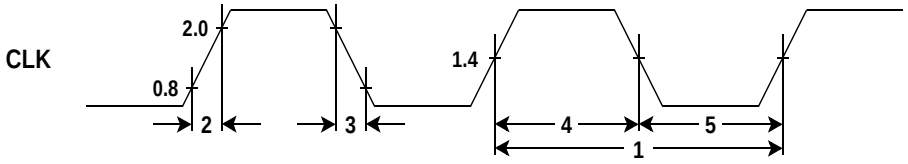


Reserved Pins: Leave pin 14 No Connect
Tie pin 19 to VSS

5.0 TIMING

Unless otherwise specified, all timing references from clock edges are referred to the crossover-to-crossover point of SCLK and VCLK at 1.4 Volts.

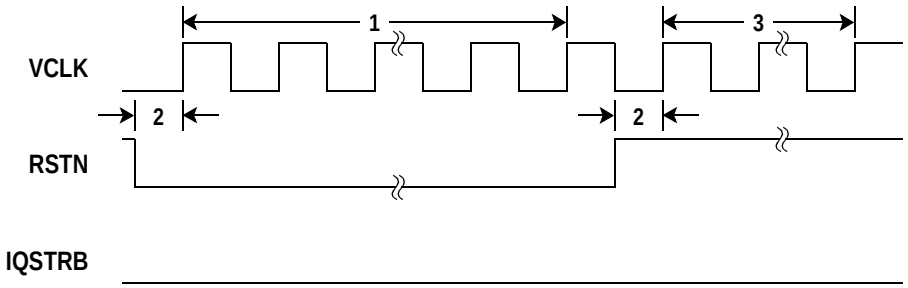
Figure 6: Clock Timing - SCLK and VCLK



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	VCLK period	16.13		nsec	1
1	VCLK period	16.13	100	nsec	2
1	VCLK period	16.13	400	nsec	3
1	SCLK period	16.13		nsec	
2	CLK rise time		2	nsec	4
3	CLK fall time		2	nsec	4
4	CLK high pulsewidth	6.4		nsec	
5	CLK low pulsewidth	7.7		nsec	

Notes:
1) In 80C188 mode.
2) In fast I^2C mode.
3) In standard I^2C mode.
4) Based on design goals.

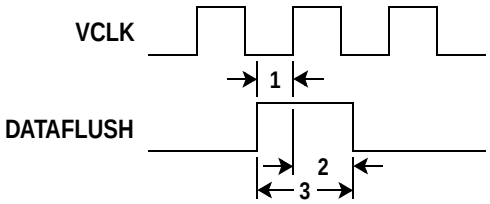
Figure 7: Reset Timing



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	RSTN low pulsewidth	20		VCLK clocks	
2	RSTN setup to VCLK	5		nsec	1
3	Internal initialization time	28		VCLK clocks	2

Notes:
1) The RSTN signal can be asynchronous to the VCLK signal. It is internally synchronized to the rising edge of VCLK.
2) Interaction with the chip can occur after this period.
3) Hold IQSTRB low until all registers are programmed.

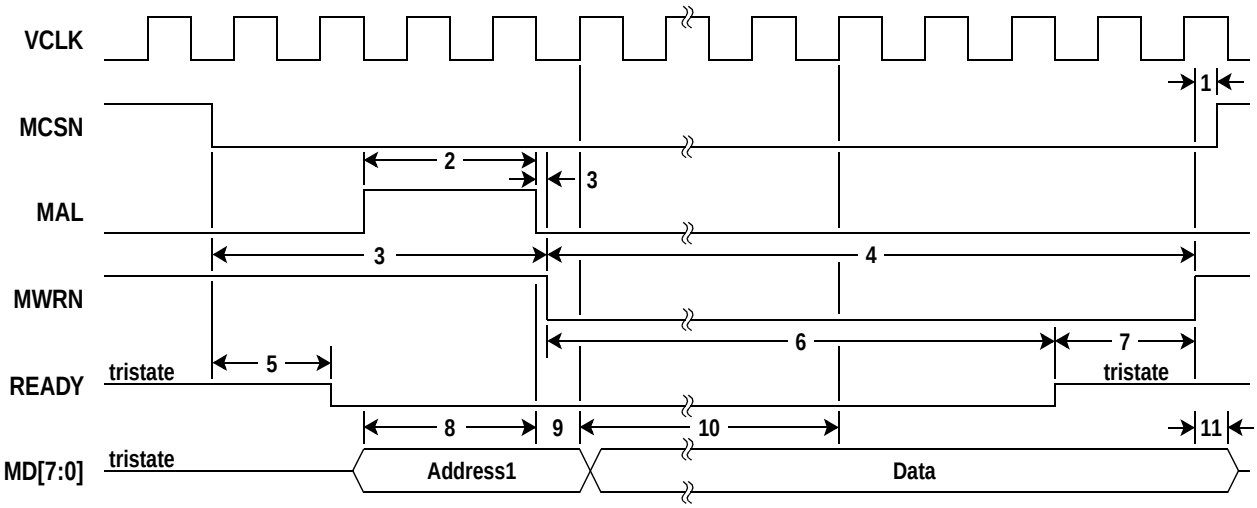
Figure 8: DATAFLUSH Timing - Byte Input Mode



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	DATAFLUSH setup	5		nsec	
2	DATAFLUSH hold	5		nsec	
3	DATAFLUSH pulsewidth	1		VCLK	

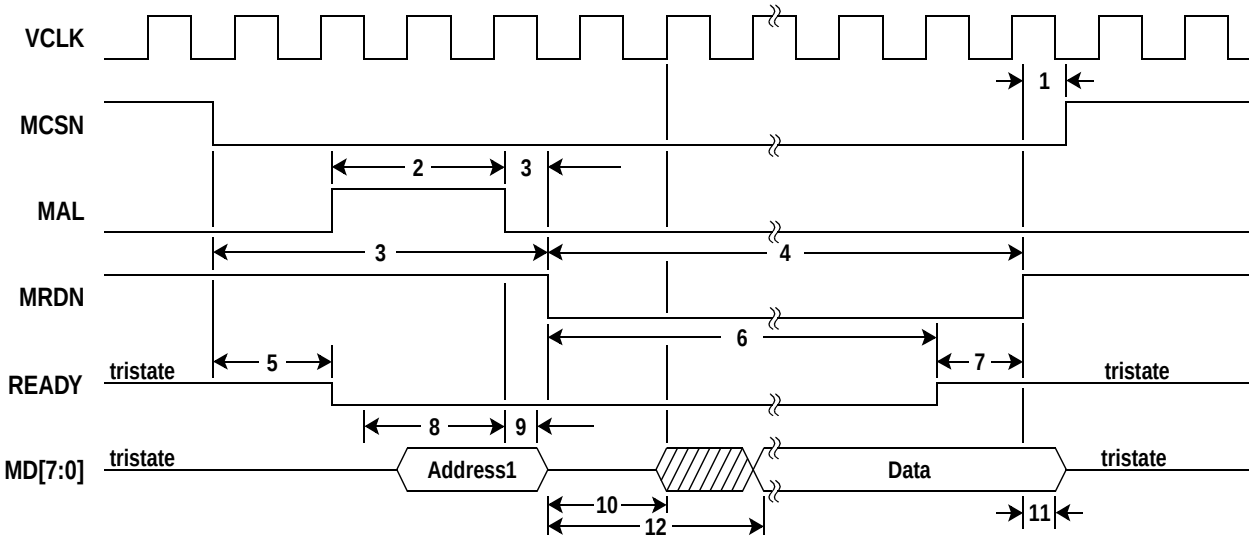
Notes:
1) DATAFLUSH function requires (16×BLKLEN2) VCLKs after the DATAFLUSH pulse.

Figure 9: Microprocessor Write Timing



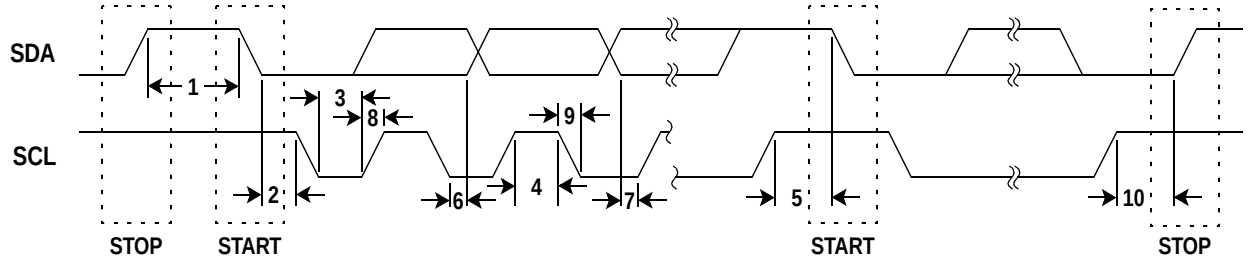
NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	MCSN hold from MWRN deasserted	0		nsec	
2	MAL pulsewidth	16		nsec	
3	MCSN low and MAL low to MWRN low	0		nsec	
4	MWRN pulsewidth	14		VCLK clocks	
5	MCSN low to READY low		22	nsec	
6	MWRN low to READY deasserted	12	14	VCLK clocks	
7	READY deasserted to MWRN high	0		nsec	
8	Address setup to MAL	10		nsec	
9	Address hold from MAL	5		nsec	
10	MWRN low to data valid		6	VCLK clocks	
11	DATA hold	0		nsec	

Figure 10: Microprocessor Read Timing



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	MCSN hold from MRDN deasserted	0		nsec	
2	MAL pulsewidth	16		nsec	
3	MCSN low and MAL low to MRDN low	0		nsec	
4	MRDN pulsewidth	12		VCLK clocks	
5	MCSN low to READY low		22	nsec	
6	MRDN low to READY deasserted		12	VCLK clocks	
7	READY deasserted to MRDN high	0		nsec	
8	Address setup to MAL fall	10		nsec	
9	Address hold from MAL fall	5		nsec	
10	MRDN low to data driven	0		nsec	
11	MRDN deassert to data released	0		nsec	
12	MRDN low to data valid		7	VCLK clocks	

Figure 11: I²C Interface Timing



NUMBER	PARAMETER	STANDARD MODE(1)		HIGH SPEED(1)		UNIT
		MIN	MAX	MIN	MAX	
	SCL Clock frequency		100		400	KHz
1	Bus free time between a STOP and START condition	4.7		1.3		µsec
2	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4		0.6		µsec
3	Low period of the SCL clock	4.7		1.3		µsec
4	High period of the SCL clock	4.0		0.6		µsec
5	Setup time for a repeated START	4.7		0.6		µsec
6	Data hold time	0(2)		0(2)	0.9(3)	µsec
7	Data setup time	250		100(4)		nsec
8	Rise time of both SDA and SCL		250		250	nsec
9	Fall time of both SDA and SCL		250		250	nsec
10	Setup time for STOP condition	4.0		0.6		µsec

Notes:

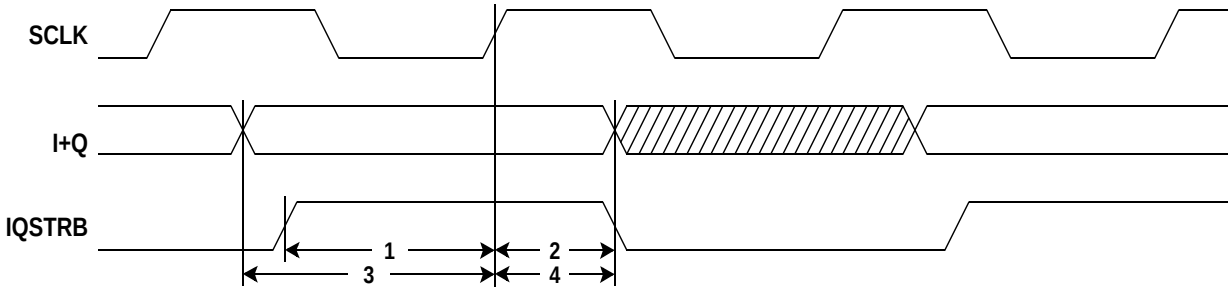
(1) All I²C Interface timings are based on design goals.

(2) A device must internally provide a hold time of at least 300 nsec for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

(3) The maximum data hold time, 6, has only to be met if the device does not stretch the low period, 7, of the SCL signal.

(4) A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement for data setup time ≥ 250 nsec must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the signal, it must output the next data bit to the SDA line $t_{R\ max} + t_{SU:DAT}$ = 1000 + 250 +1250 nsec (according to the standard mode I²C bus specification) before the SCL line is released.

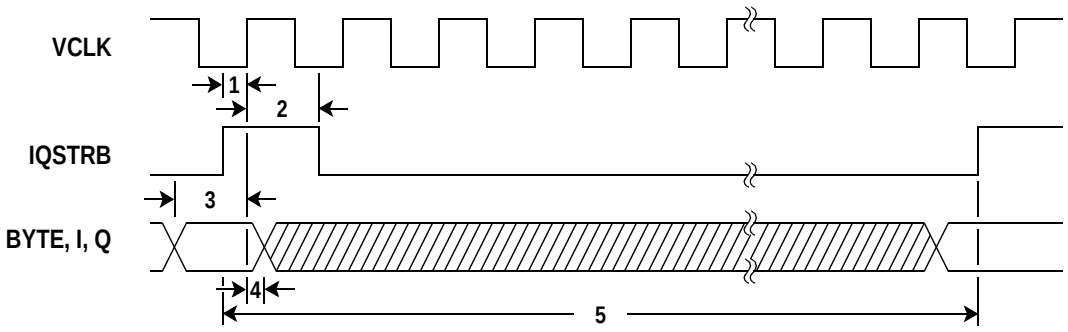
Figure 12: Input - Serial Mode: IOCNTRL[2:1] = 0x Mode



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	IQSTRB setup to SCLK	5		nsec	
2	IQSTRB hold from SCLK	1		nsec	
3	IQ setup to SCLK	5		nsec	
4	IQ hold from SCLK	1		nsec	

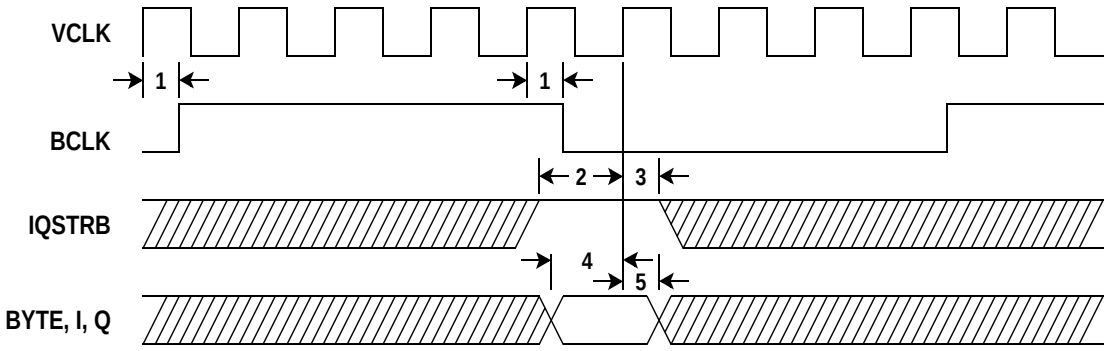
Note:I and Q signals may be strobed once per SCLK and IQSTRB may be held high. The timing diagram above illustrates I and Q data on every other SCLK.

Figure 13: Input - Byte Mode: IOCNTRL[2:1] = 10 Mode



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	IQSTRB setup to VCLK	5		nsec	
2	IQSTRB hold from VCLK	3		nsec	
3	Byte, I and Q setup to VCLK	5		nsec	
4	Byte, I and Q hold from VCLK	3		nsec	
5	IQSTRB period	8		VCLK clocks	

Figure 14: Input - Byte Mode IOCNTRL[2:1] = 11



NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	BCLK delay from VCLK		11	nsec	
2	IQSTRB setup to VCLK	5		nsec	1
3	IQSTRB hold to VCLK	3		nsec	1
4	Byte, I and Q setup to VCLK	5		nsec	1
5	Byte, I and Q hold to VCLK	3		nsec	1

Note:

1) Data and IQSTRB are latched on the rising edge of VCLK when BCLK is low and IQSTRB is high.

Figure 15: Output - BCLK Mode: IOCNTRL[4:3] = 10, [2:1] = 11

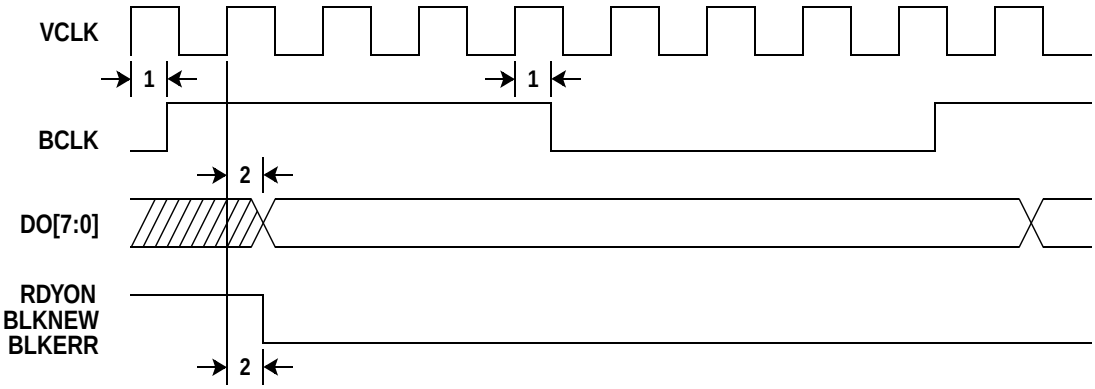
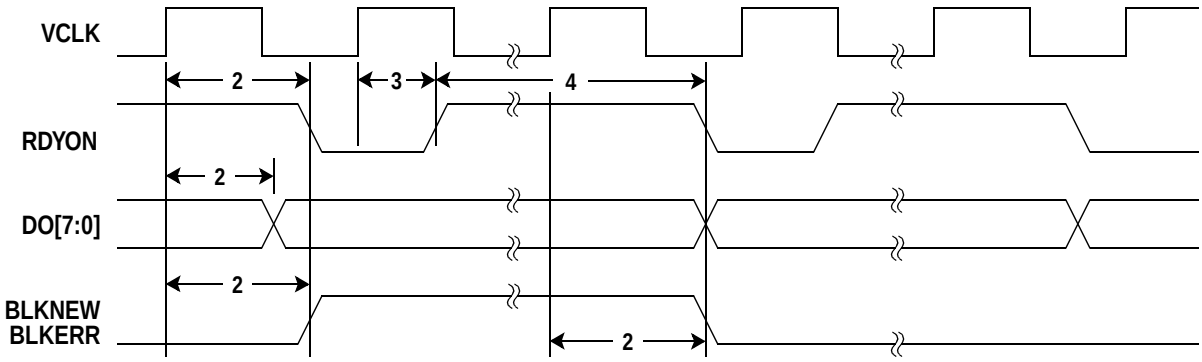


Figure 16: Output - Byte Mode: IOCNTRL[4:3] = 10, IOCNTRL[2:1] ≠11



Note: RDYON remains asserted for one clock period. Output data stays asserted for eight clocks minimum.

NUMBER	PARAMETER	MIN	MAX	UNITS	NOTES
1	BCLK delay from VCLK		11	nsec	
2	DO [7:0], RDYON, BLKNEW and BLKERR from VCLK		11	nsec	
3	RDYON output hold	1		nsec	
4	RDYON deassert time	7		VCLK clocks	

Timing diagrams 15 through 18 show first two bytes of a block with uncorrectable errors for various RDYON modes.

Figure 17: IOCNTRL[4:3] = 00, Serial Output

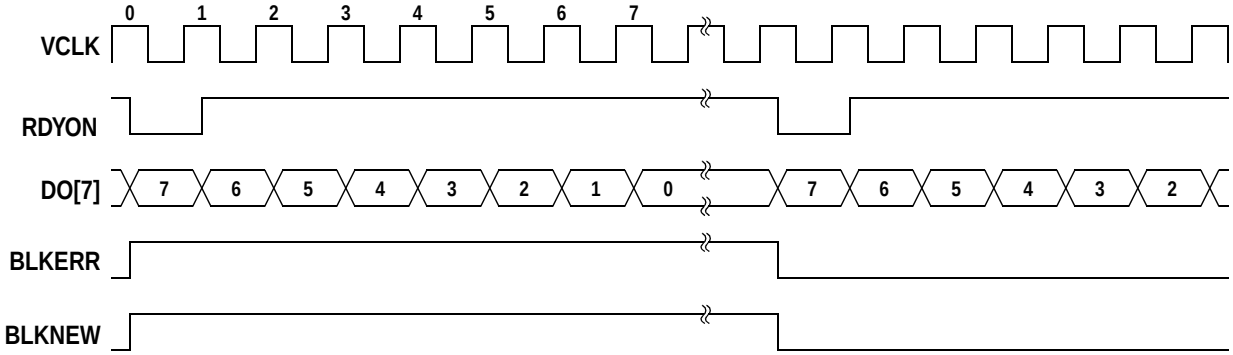


Figure 18: IOCNTRL[4:3] = 01, Serial Output

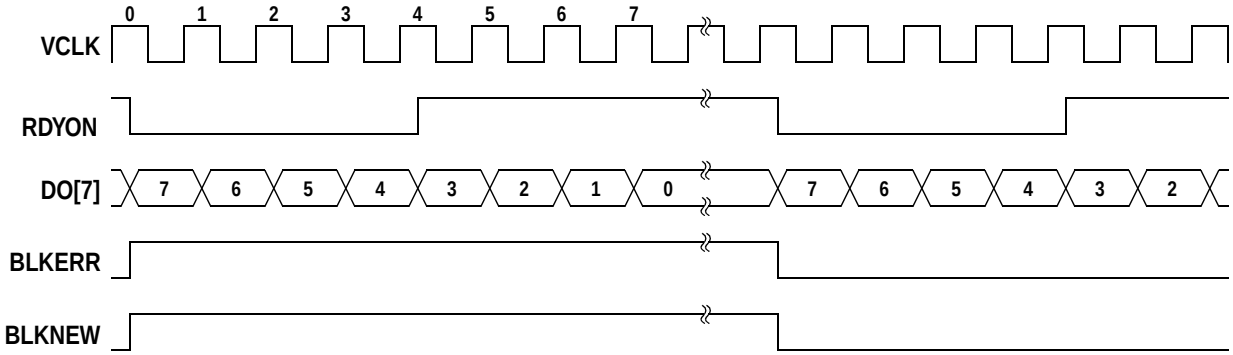


Figure 19: IOCNTRL[4:3] = 10, Byte Output

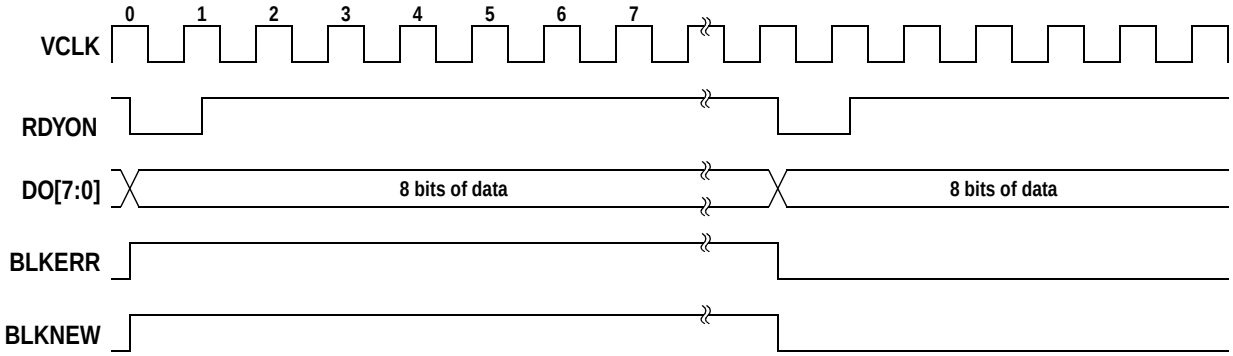
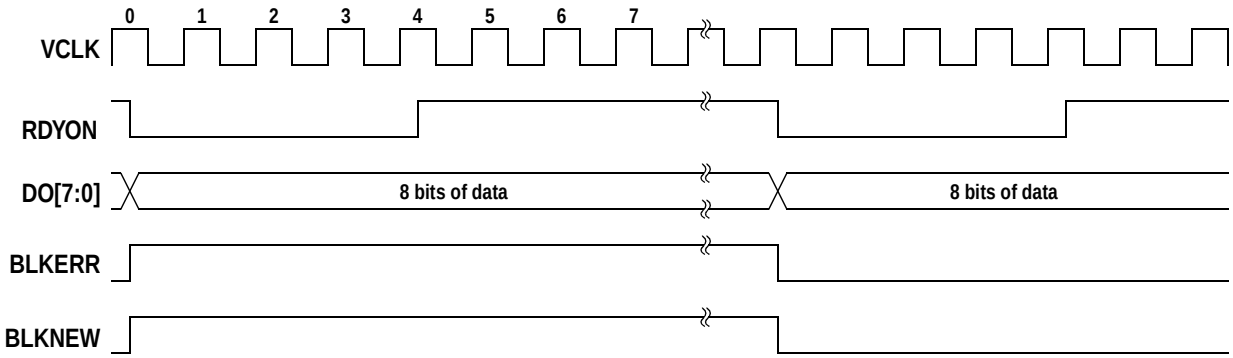


Figure 20: IOCNTRL[4:3] = 11, Byte Output



6.0 DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM STRESS RATINGS					
SYMBOL	**CHARACTERISTICS**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Tstg	Storage temperature	-55	150	°C	
Vdd	Supply voltage	-0.5	6.0	V	
Vin	Input voltage	Vss-0.5	Vdd+0.5	V	
Package: 68 pin PLCC					

OPERATING CONDITIONS					
SYMBOL	**CHARACTERISTICS**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Vdd	Supply voltage	4.75	5.25	V	
Idd	Supply current		1	mA	Static - clocks stopped
Idd	Supply current		360	mA	@43 MHz; Dynamic; modes 1 and 3 at 5.25V; Figure 21
Idd	Supply current		240	mA	@62 MHz; Dynamic; modes 2, 4 and 5 at 5.25V. *Note 1*
Ta	Ambient temperature	0	70	°C	Figure 22

Note 1: Modes 2, 4 and 5 data are based on design goals and charaterization of sample devices, not production tested.

INPUTS					
SYMBOL	**CHARACTERISTICS**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Vih	Input high voltage	2.0	Vdd	V	
Vil	Input low voltage	Vss	0.8	V	All signals except VCLK
Vil	Input low voltage for VCLK	Vss	0.6	V	
Iil	Input leakage	-10	10	µA	0<Vin<Vdd
Cin	Self load capacitance		10	pF	

OUTPUTS					
SYMBOL	**CHARACTERISTICS**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Voh	Output high voltage	2.4	Vdd	V	Ioh=4mA
Vol	Output low voltage	Vss	0.4	V	Iol=4mA
Ioh	Output high current	-4		mA	Voh=2.4V
Iol	Output low current		4	mA	Vol=0.4
Ioz	High Impedance leakage		10	µA	0<Vout<Vdd bidirectionals only
Cout	Self load capacitance		10	pF	
Cl	Load capacitance		20	pF	

Figure 21: Power vs. VCLK Rate, Estimated for Modes 1 and 3

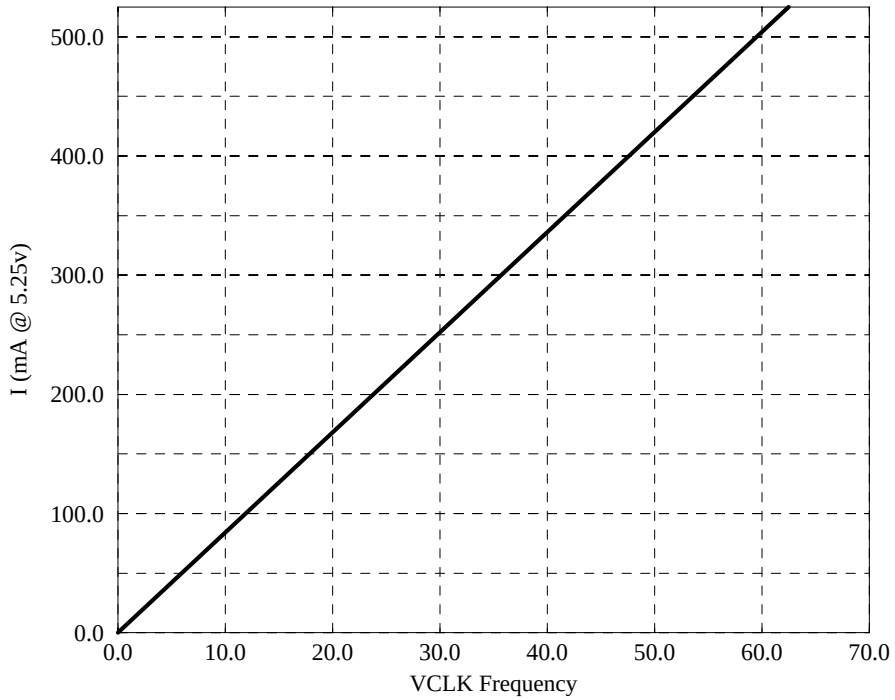
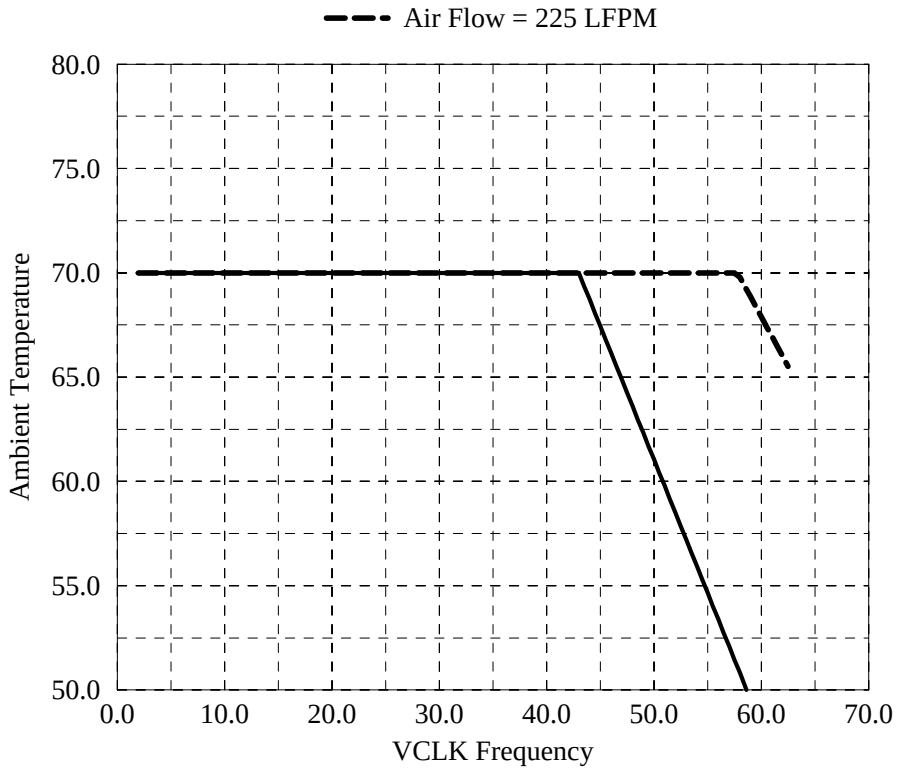


Figure 22: Max Ambient Temperature (Ta) vs. VCLK Rate, Estimated for Modes 1 and 3



Note: Curves represent 68 pin PLCC. For other packaging options, please contact AHA.

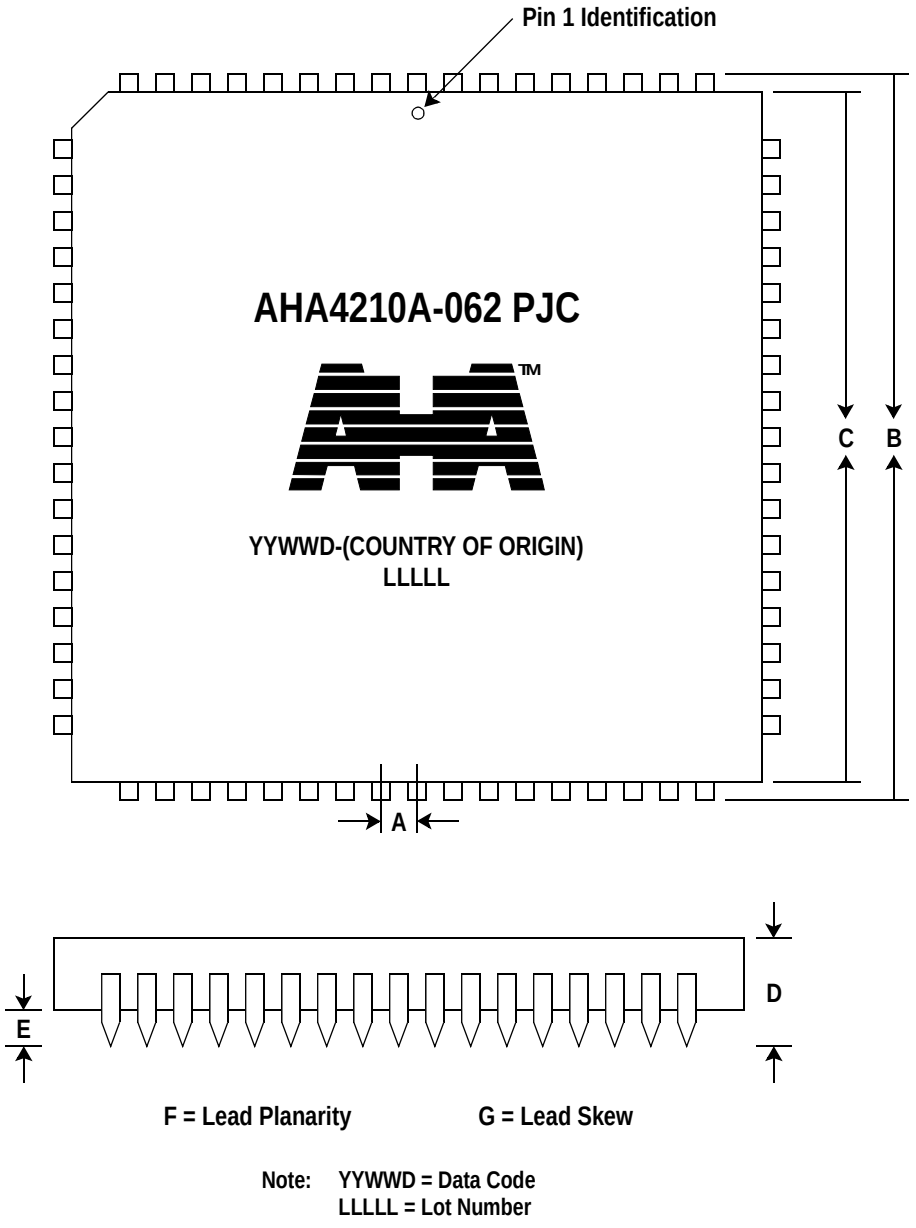
7.0 PACKAGING

PLCC Dimensions

Inches
(Millimeters)

A	*B* *min/max*	*C* *min/max*	*D* *min/max*	*E* *min*	*F* ±	*G* ±
.050 (1.27)	.985/.995 (25.02/25.27)	.950/.956 (24.13/24.28)	.165/.200 (4.19/5.08)	.020 (0.51)	.002 (0.051)	.0035 (0.089)

Packaging



Note: YYWWD = Data Code
LLLLL = Lot Number

Complete Package Drawing Available Upon Request

8.0 ORDERING INFORMATION

8.1 AVAILABLE PARTS

PART NUMBER	*DESCRIPTION*
AHA4210A-062 PJC	Viterbi with Reed-Solomon Decoder

8.2 PART NUMBERING

AHA	*4210*	*A-*	*062*	*P*	*J*	*C*
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:

4210

Revision Letter:

A

Package Material Codes:

P Plastic

Package Type Codes:

J J - Leaded Chip Carrier

Test Specifications:

C Commercial 0°C to +70°C

9.0 AHA RELATED TECHNICAL PUBLICATIONS

DOCUMENT #	*DESCRIPTION*
ABRS05	AHA Application Brief - Programming the AHA4210 for Non-DVB/DAVIC Applications
ABSTD1	AHA Application Brief - Data Compression and Forward Error Correction Standards
ANRS01	AHA Application Note - Primer: Reed-Solomon Error Correction Codes (ECC)
ANRS02	AHA Application Note - Reed-Solomon Interleaving for Burst Error Correction
ANRS06	AHA Application Note - Code Performance, Error Rate Monitoring and Processing Delays Through the AHA4210
ANRS07	AHA Application Note - Soft Decision Thresholds and Effects on Viterbi Performance
ANRS08	AHA Application Note - AHA4210 RSVP Synchronization Performance
ANRS09	AHA Application Note - Frequently Asked Questions and Answers about the AHA4210 RSVP
ANRS10	AHA Application Note - AHA4210 Viterbi Decoder Low Code Rate Noise Floor
FECESW	Concatenated FEC Encoder Software (RSVP)
GLGEN1	General Glossary of Terms
IEEEART	Greg Zweigle, TJ Berge, Paul Winterrowd and Aziz Makhani, "*A Viterbi, Convolutional Interleave, and Reed-Solomon Decoder IC*," IEEE 1995 International Conference on Consumer Electronics

10.0 OTHER TECHNICAL PUBLICATIONS

DOCUMENT
J.L. Ramsey, "Realization of Optimal Interleavers," *IEEE Transaction on Information Theory*, May 1970, pp. 338-345
Philips/Signetics, "The I^2C Bus and How to Use It," January 1992
Philips, "Specification IIC bus." *TVE 80134*
Digital Video Broadcasting, DT/8622/DVB, "Implementation Guidelines for the use of MPEG-II Systems, Video and Audio in Satellite and Cable Broadcasting Applications in Europe," May 26, 1994
Digital Video Broadcasting, DT/8610/III-B, "User Requirements for Digital Broadcasting Systems by Satellite and Cable," May 2, 1994