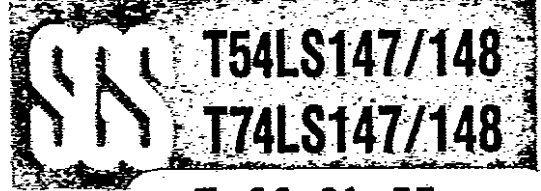


# LOW POWER SCHOTTKY INTEGRATED CIRCUITS



67C 16208

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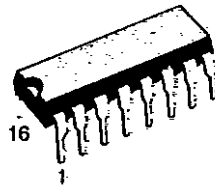
T-66-21-57

## PRELIMINARY DATA

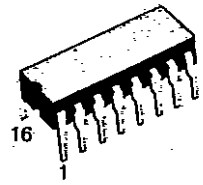
### 10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

#### DESCRIPTION

These priority Encoders decode the inputs to ensure that only the highest order data line is encoded. All inputs and outputs data of both devices are active at the low logic level. The LS147 encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition because zero is enclosed when all nine data lines are at a high logic level. The LS148 encodes eight data lines to three line (4-2-1) binary (octal). Cascading circuitry (Enable input EI and Enable Output EO) has been provided to allow octal expansion without needing external circuitry.



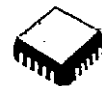
**B1**  
Plastic Package



**D1/D2**  
Ceramic Package



**M1**  
Micro Package



**C1**  
Plastic Chip Carrier

#### ORDERING NUMBERS:

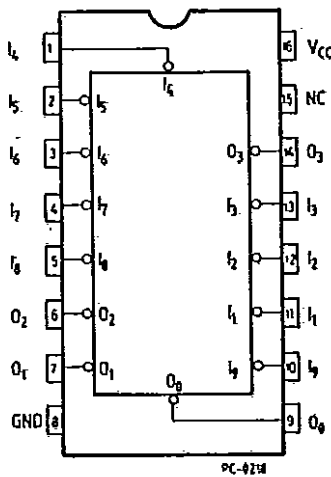
T54LSXXX D2  
T74LSXXX D1  
T74LSXXX B1

T74LSXXX C1  
T74LSXXX M1

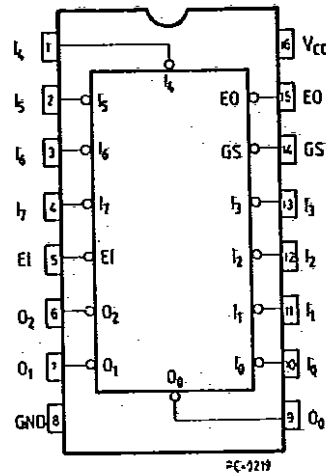
### PIN CONNECTION (top view)

#### DUAL IN LINE

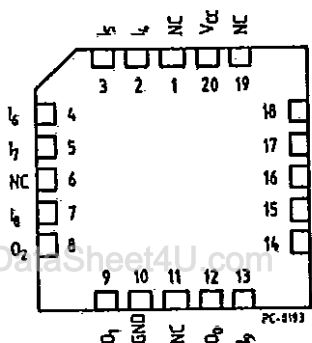
**LS147**



**LS148**

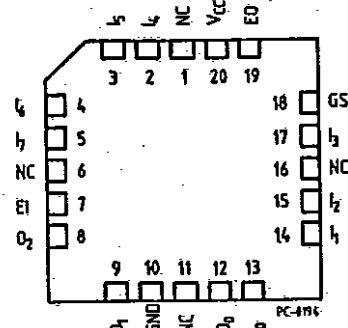


**LS147**

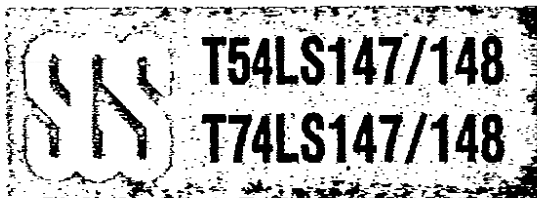


#### CHIP CARRIER

**LS148**



NC = No Internal Connection



T54LS147/148

T74LS147/148

**TRUTH TABLE**

LS147										LS148																		
INPUTS									OUTPUTS				INPUTS							OUTPUTS								
1	2	3	4	5	6	7	8	9	D	C	B	A	EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO		
H	H	H	H	H	H	H	H	H	H	H	H	H	H	X	X	X	X	X	X	X	X	X	X	H	H	H	H	H
X	X	X	X	X	X	X	X	X	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
X	X	X	X	X	X	X	L	H	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	X	X	X	X	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H	L	L	L	L	L	L	H	
X	X	X	X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	L	L	H	
X	X	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	
X	L	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	

L = LOW Voltage Level - H = HIGH Voltage Level - X = Don't Care

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to 7	V
V <sub>I</sub>	Input Voltage, Applied to Input	-0.5 to 15	V
V <sub>O</sub>	Output Voltage, Applied to Output	0 to 10	V
I <sub>I</sub>	Input Current, Into Inputs	-30 to 5	mA
I <sub>O</sub>	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

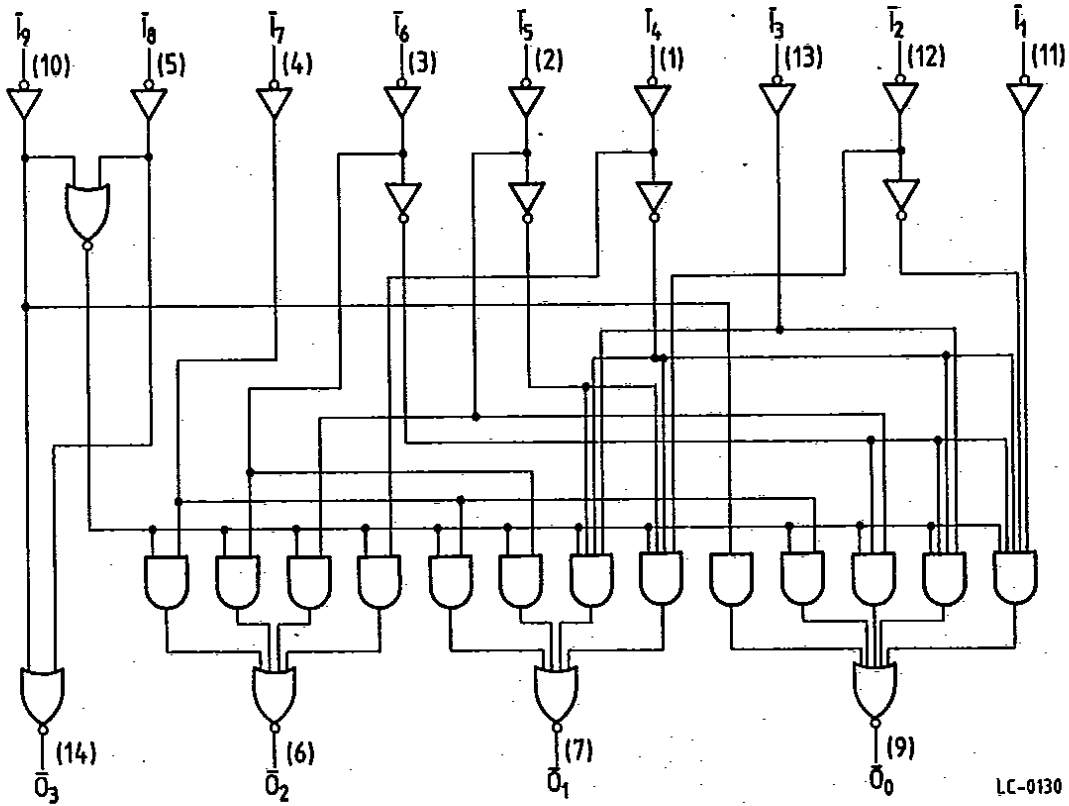
**GUARANTEED OPERATING RANGES**

Part Numbers	Supply Voltage			Temperature
	Min	Typ	Max	
T54LS147/148D2	4.5 V	5.0 V	5.5 V	-55°C to +125°C
T74LS147/148XX	4.75 V	5.0 V	5.25 V	0°C to +70°C

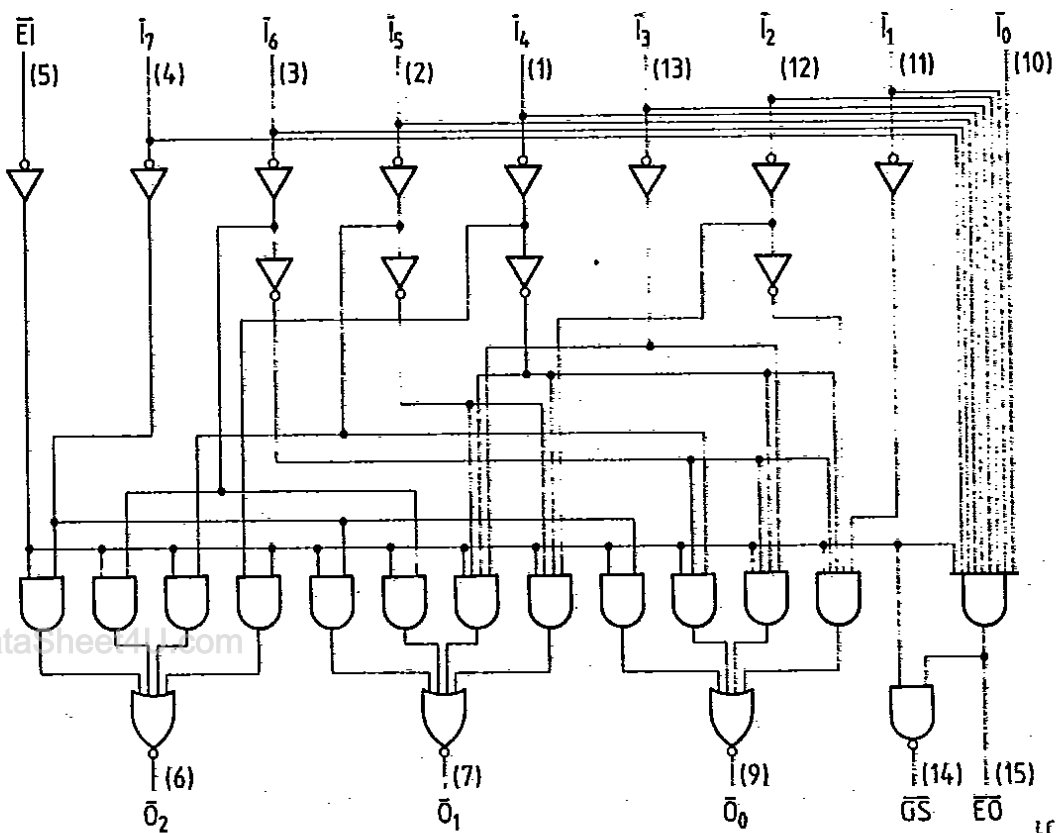
XX = package type.

**FUNCTIONAL BLOCK DIAGRAMS**

**LS147**



**LS148**



**VCC = Pin 16**  
**GND = Pin 8**  
**( ) = Pin number**

### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter		Limits			Test Conditions (Note 1)	Units
			Min.	Typ.	Max.		
$V_{IH}$	Input HIGH Voltage		2.0			Guaranteed input HIGH Voltage for all Inputs	V
$V_{IL}$	Input LOW Voltage	54			0.7	Guaranteed Input LOW Voltage for all Inputs	V
		74			0.8		
$V_{CD}$	Input Clamp Diode Voltage			-0.65	-1.5	$V_{CC} = \text{MIN}, I_{IN} = -18\text{mA}$	V
$V_{OH}$	Output HIGH Voltage	54	2.5	3.5		$V_{CC} = \text{MIN}, I_{OH} = -400\mu\text{A}, V_{IN} = V_{IH}$ or $V_{IL}$ per Truth Table	V
		74	2.7	3.5			
$V_{OL}$	Output LOW Voltage	54,74		0.25	0.4	$I_{OL} = 4.0\text{mA}$	V
		74		0.35	0.5	$I_{OL} = 8.0\text{mA}$	
$I_{IH}$	Input HIGH Current All Others Inputs 1-7 (LS148)				20 40	$V_{CC} = \text{MAX}, V_{IN} = 2.7\text{V}$	$\mu\text{A}$
	All Others Inputs 1-7 (LS148)				0.1 0.2	$V_{CC} = \text{MAX}, V_{IN} = 7.0\text{V}$	mA
$I_{IL}$	Input LOW Current All Others Inputs 1-7 (LS148)				-0.4 -0.8	$V_{CC} = \text{MAX}, V_{IN} = 0.4\text{V}$	mA
$I_{OS}$	Output Short Circuit Current (Note 2)		-20		-120	$V_{CC} = \text{MAX}, V_{OUT} = 0\text{V}$	mA
$I_{CC}$	Power Supply Current				20	$V_{CC} = \text{MAX}, \text{Inputs 7, EI, GND, Others Open}$	mA
					17	$V_{CC} = \text{MAX}, \text{A Inputs}$	

### AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$ (T54/74LS147)

Symbol	From (Input)	To (Output)	Waveforms	Limits			Test Conditions	Units
				Min.	Typ.	Max.		
$t_{PLH}$ $t_{PHL}$	Any	Any	In-phase output		12 12	18 18	$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	ns
$t_{PLH}$ $t_{PHL}$	Any	Any	Out-of-phase output		21 15	33 23		

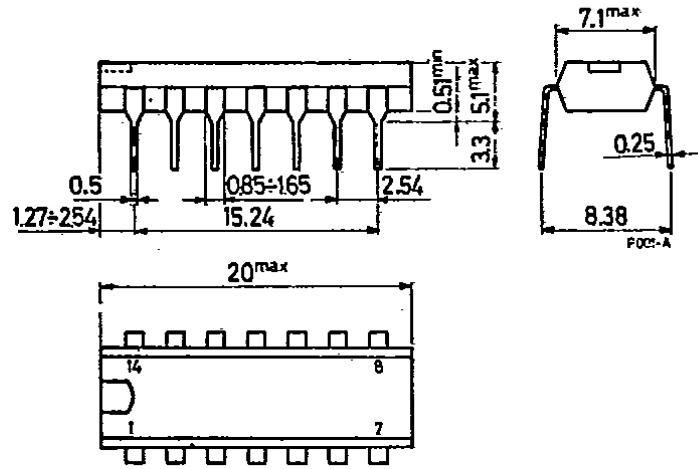
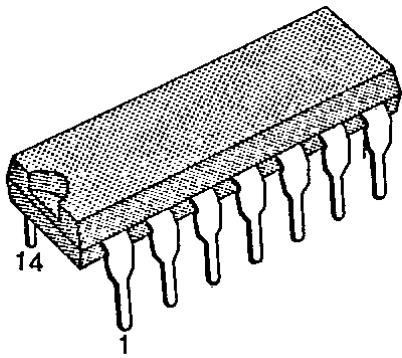
Notes: [www.DataSheet4U.com](http://www.DataSheet4U.com)

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at  $V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}$

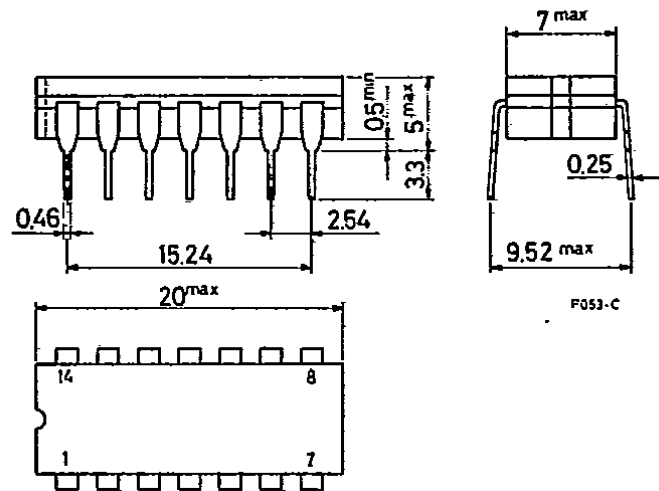
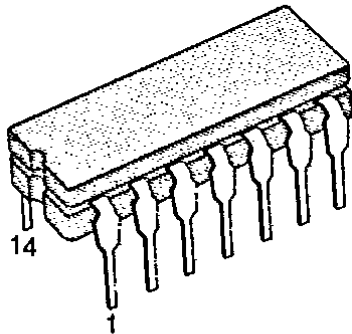
**AC CHARACTERISTICS: T<sub>A</sub> = 25°C (T54/74LS148)**

Symbol	From (Input)	To (Output)	Waveforms	Limits			Test Conditions	Units
				Min.	Typ.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	1 thru 7	A0, A1 or A2	In-Phase output		14 15	18 25	C <sub>L</sub> = 15pF R <sub>L</sub> = 2kΩ	ns
t <sub>PLH</sub> t <sub>PHL</sub>	1 thru 7	A0, A1 or A2	Out-of-Phase output		20 16	36 29		ns
t <sub>PLH</sub> t <sub>PHL</sub>	0 thru 7	EO	Out-of-Phase output		7.0 25	18 40		ns
t <sub>PLH</sub> t <sub>PHL</sub>	0 thru 7	GS	In-Phase output		35 9.0	55 21		ns
t <sub>PLH</sub> t <sub>PHL</sub>	E1	A0, A1 or A2	In-Phase output		16 12	25 25		ns
t <sub>PLH</sub> t <sub>PHL</sub>	E1	GS	In-Phase output		12 14	17 36		ns
t <sub>PLH</sub> t <sub>PHL</sub>	E1	E0	In-Phase output		12 23	21 35		ns

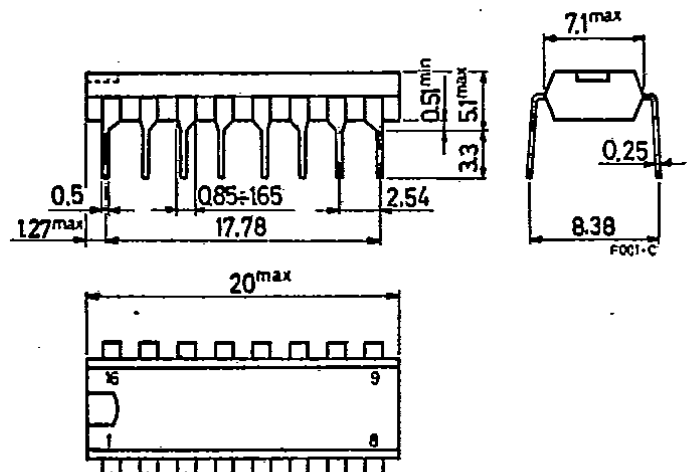
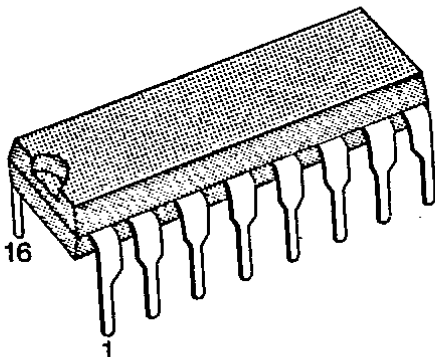
# 14-LEAD PLASTIC DIP



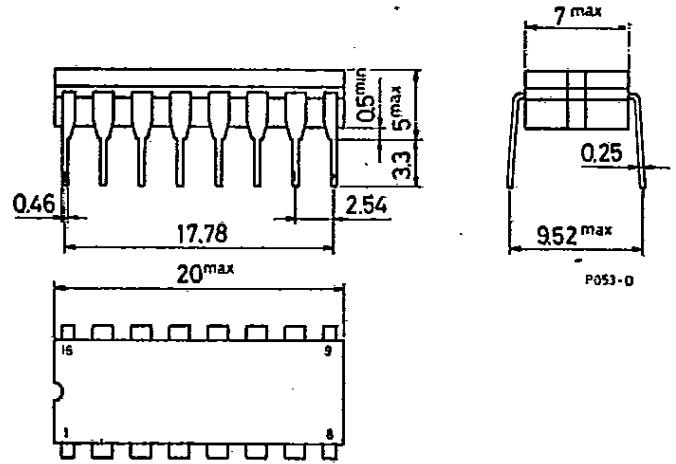
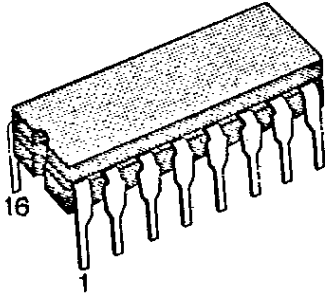
# 14-LEAD CERAMIC DIP



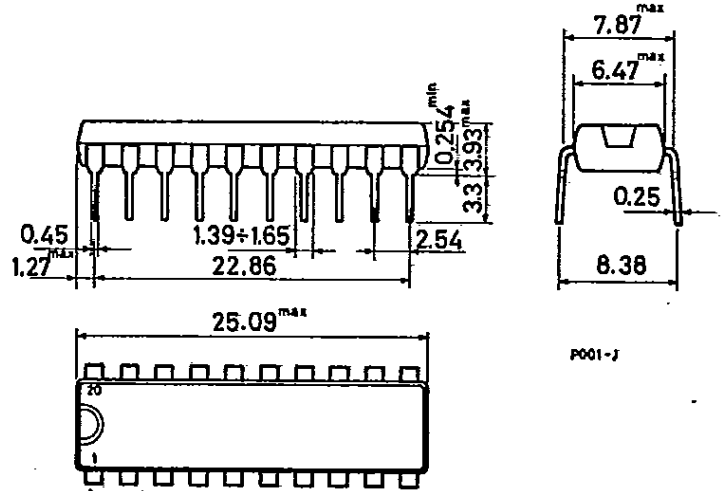
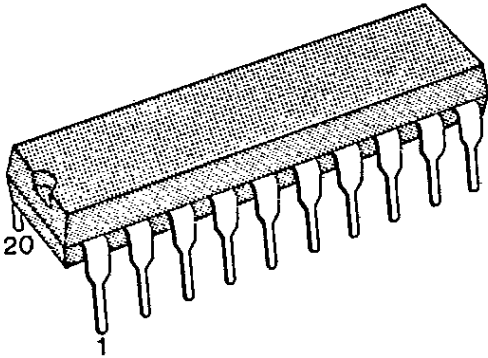
# 16-LEAD PLASTIC DIP



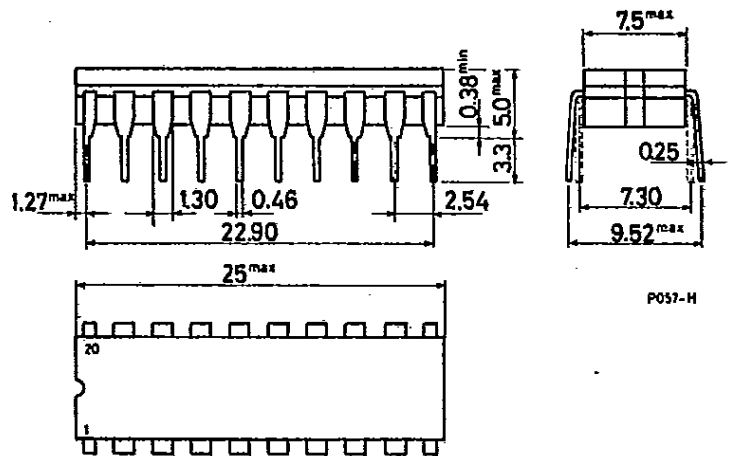
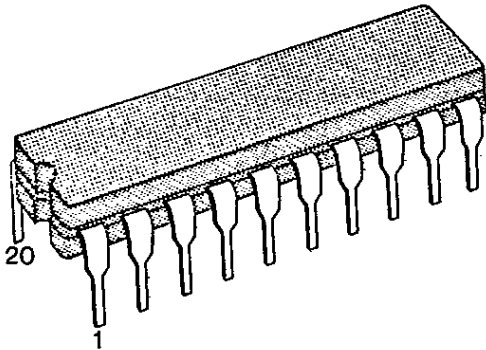
## 16-LEAD CERAMIC DIP



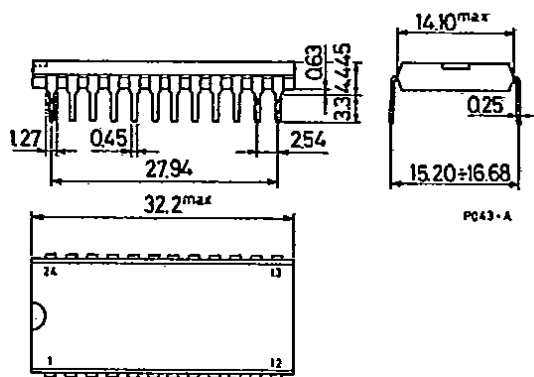
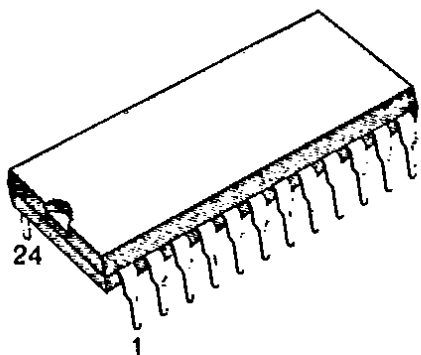
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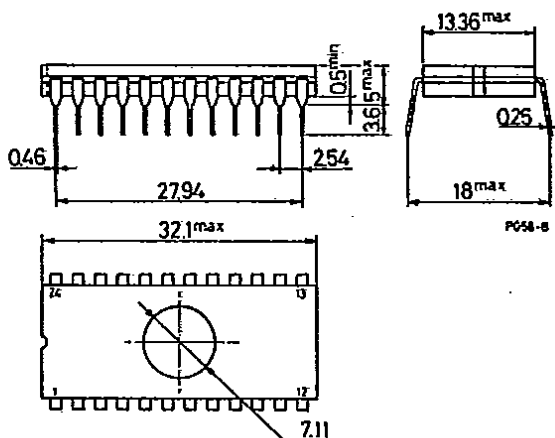
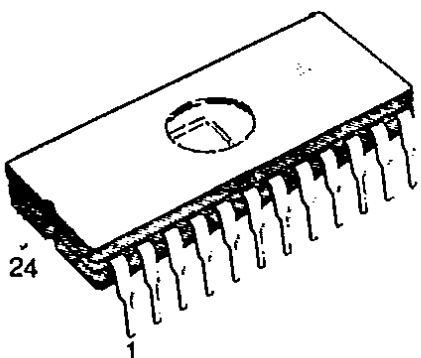
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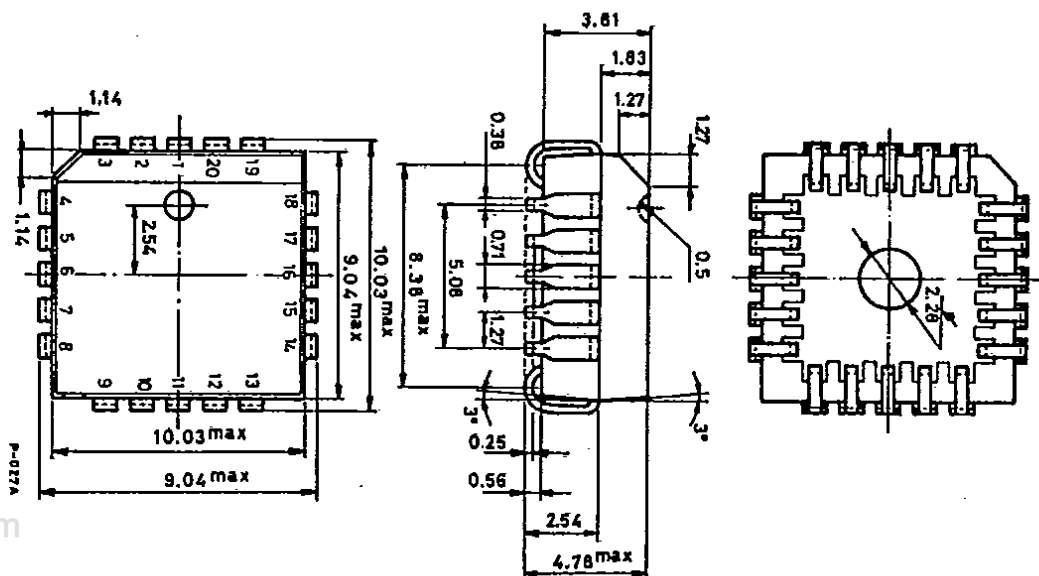
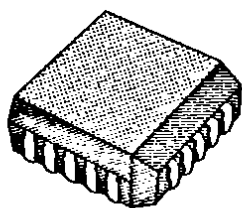
## 24-LEAD PLASTIC DIP



## 24-LEAD CERAMIC DIP

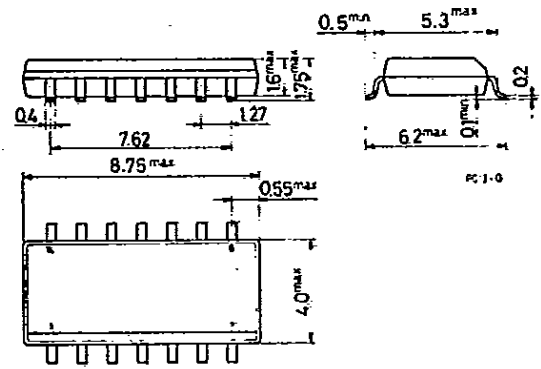
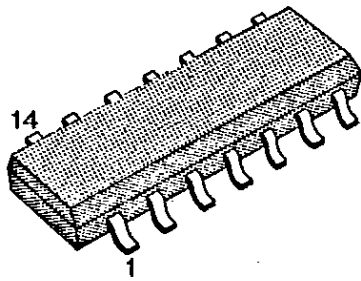


## CHIP CARRIER 20 LEAD PLASTIC

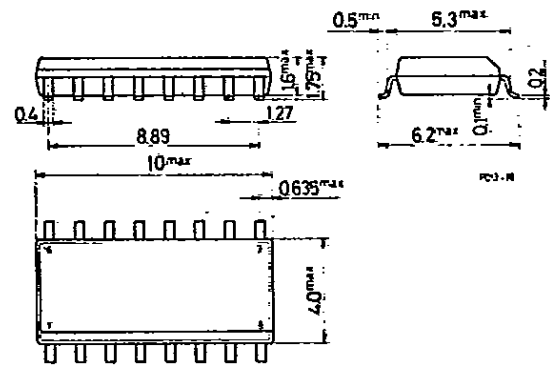
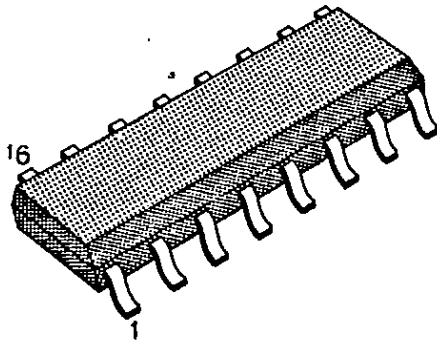




## 14-LEAD PLASTIC DIP MICROPACKAGE



## 16-LEAD PLASTIC DIP MICROPACKAGE



NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

# Surface Mounted

67C 16548

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T-90-20

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages. The advantages given by using these devices are:

## PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

## Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

## Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

## Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propagation delay between the external pins, with respect to the standard type.

## Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.

