

# GI3403

## P-CHANNEL ENHANCEMENT MODE POWER MOSFET

BVDSS	-30V
RDS(ON)	200mΩ
ID	-10A

### Description

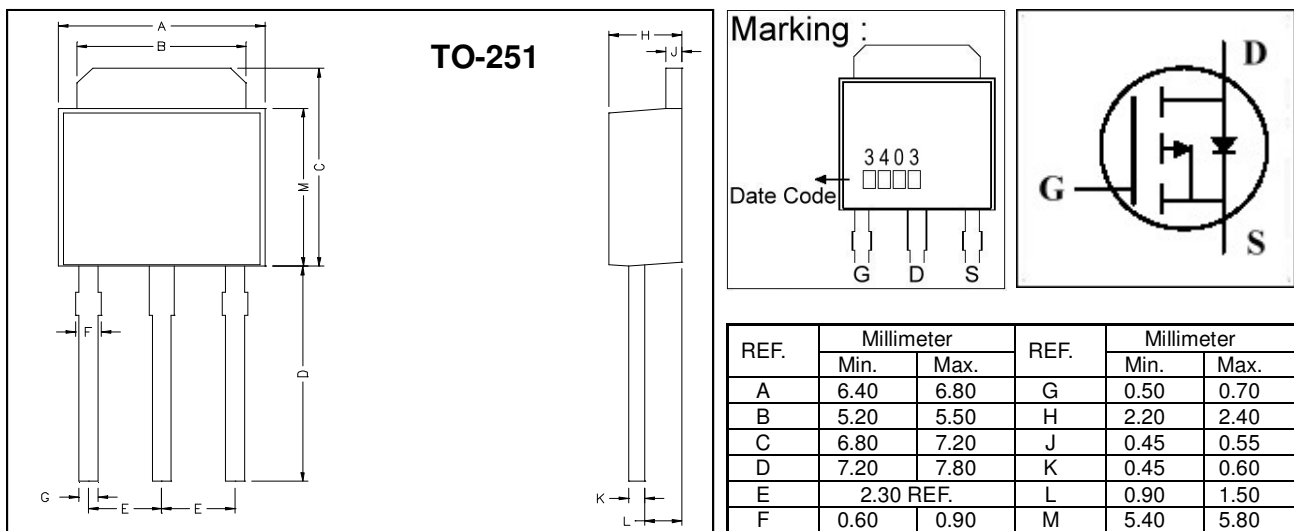
The GI3403 utilized advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device.

The TO-251 package is universally used for commercial-industrial applications.

### Features

- \*Simple Drive Requirement
- \*Lower Gate Charge
- \*Fast Switching

### Package Dimensions



### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D @ T_C=25^\circ C$	-10	A
Continuous Drain Current	$I_D @ T_C=70^\circ C$	-8.6	A
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	-48	A
Total Power Dissipation	$P_D @ T_C=25^\circ C$	36.7	W
Linear Derating Factor		0.29	W/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	-55 ~ +150	$^\circ C$

### Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-case Max.	Rthj-case	3.4	$^\circ C/W$
Thermal Resistance Junction-ambient Max.	Rthj-amb	110	$^\circ C/W$

**Electrical Characteristics (T<sub>j</sub> = 25°C unless otherwise specified)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	-30	-	-	V	V <sub>GS</sub> =0, I <sub>D</sub> =-250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	-0.1	-	V/°C	Reference to 25°C, I <sub>D</sub> =-1mA
Gate Threshold Voltage	V <sub>GS(th)</sub>	-1.0	-	-3.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA
Forward Transconductance	g <sub>fs</sub>	-	2	-	S	V <sub>DS</sub> =-10V, I <sub>D</sub> =-6A
Gate-Source Leakage Current	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±20V
Drain-Source Leakage Current(T <sub>j</sub> =25°C)	I <sub>DSS</sub>	-	-	-1	uA	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0
Drain-Source Leakage Current(T <sub>j</sub> =150°C)		-	-	-25	uA	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	-	-	200	mΩ	V <sub>GS</sub> =-10V, I <sub>D</sub> =-6A
		-	-	400		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	-	3.8	-	nC	I <sub>D</sub> =-6A V <sub>DS</sub> =-24V V <sub>GS</sub> =-4.5V
Gate-Source Charge	Q <sub>gs</sub>	-	1.7	-		
Gate-Drain ("Miller") Charge	Q <sub>gd</sub>	-	1.6	-		
Turn-on Delay Time <sup>2</sup>	T <sub>d(on)</sub>	-	6.7	-	ns	V <sub>DS</sub> =-15V I <sub>D</sub> =-6A V <sub>GS</sub> =-10V R <sub>G</sub> =2Ω R <sub>D</sub> =2.5Ω
Rise Time	T <sub>r</sub>	-	20.8	-		
Turn-off Delay Time	T <sub>d(off)</sub>	-	14.9	-		
Fall Time	T <sub>f</sub>	-	4.4	-		
Input Capacitance	C <sub>iss</sub>	-	217	-	pF	V <sub>GS</sub> =0V V <sub>DS</sub> =-25V f=1.0MHz
Output Capacitance	C <sub>oss</sub>	-	103	-		
Reverse Transfer Capacitance	C <sub>rss</sub>	-	31	-		

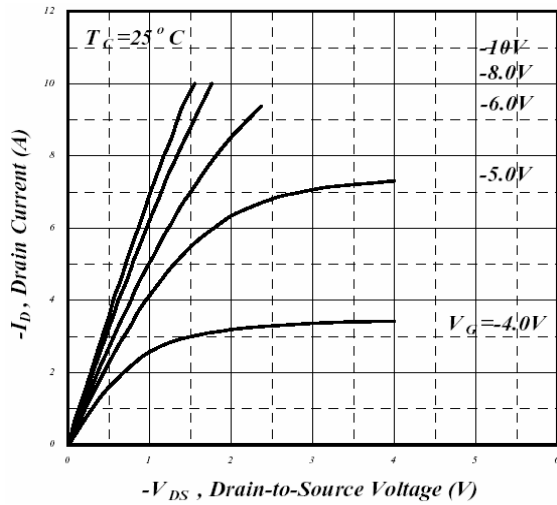
**Source-Drain Diode**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage <sup>2</sup>	V <sub>SD</sub>	-	-	-1.2	V	I <sub>S</sub> =-1.25A, V <sub>GS</sub> =0V
Reverse Recovery Time	T <sub>rr</sub>	-	35	-	ns	I <sub>S</sub> =-6A, V <sub>GS</sub> =0V dI/dt=100A/μs
Reverse Recovery Charge	Q <sub>rr</sub>	-	63	-	nC	

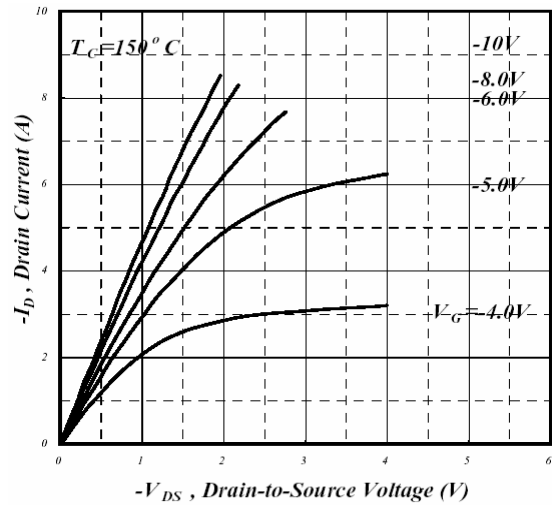
Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

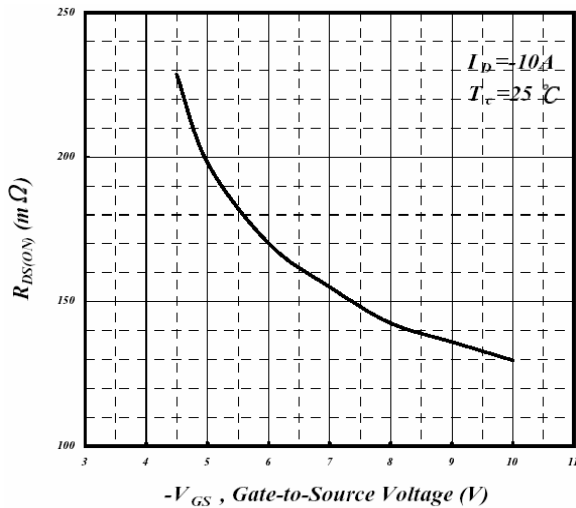
## Characteristics Curve



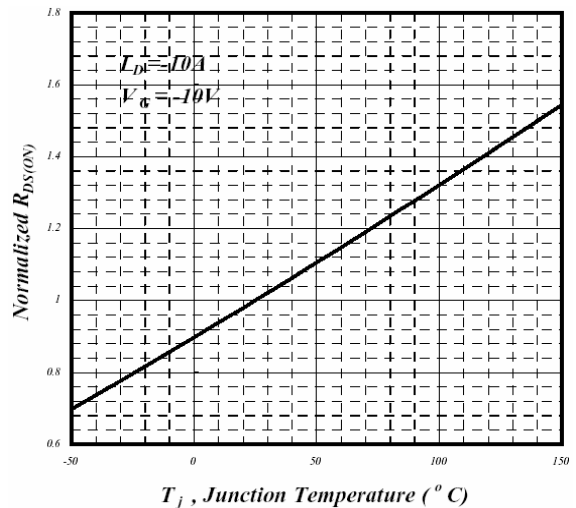
**Fig 1. Typical Output Characteristics**



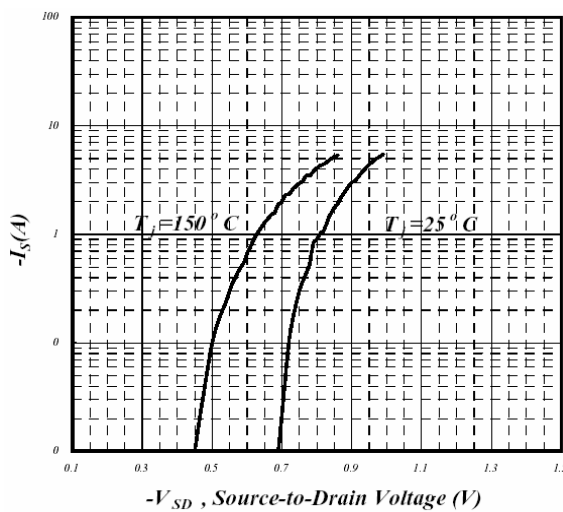
**Fig 2. Typical Output Characteristics**



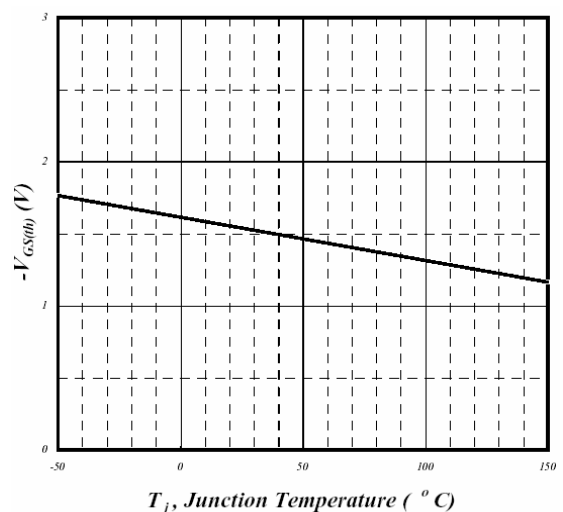
**Fig 3. On-Resistance v.s. Gate Voltage**



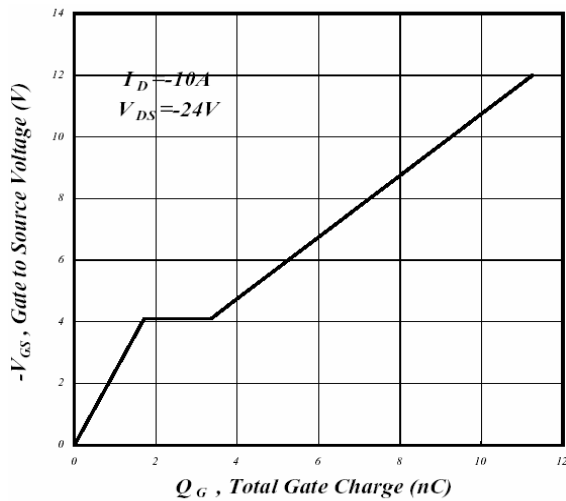
**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



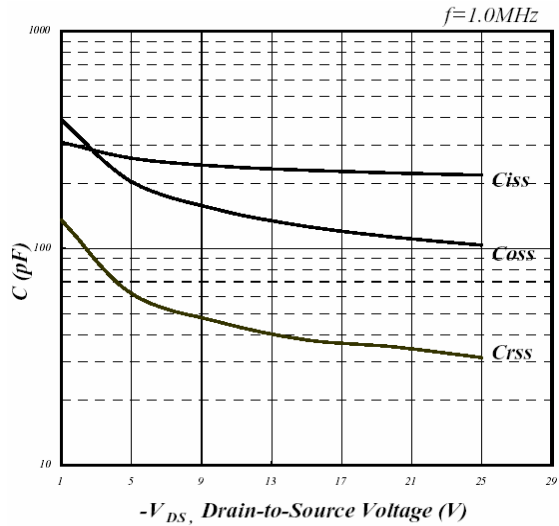
**Fig 5. Forward Characteristics of Reverse Diode**



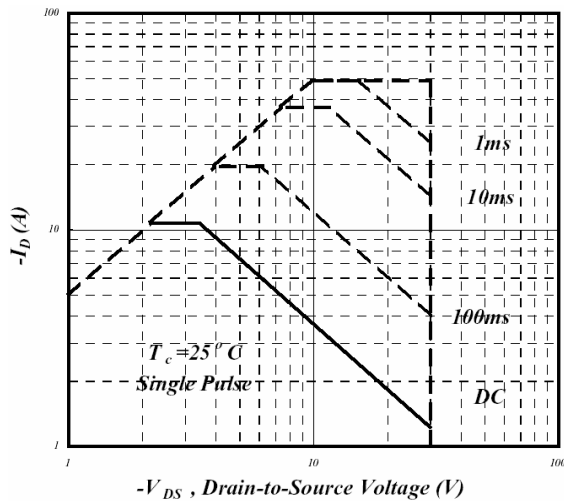
**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



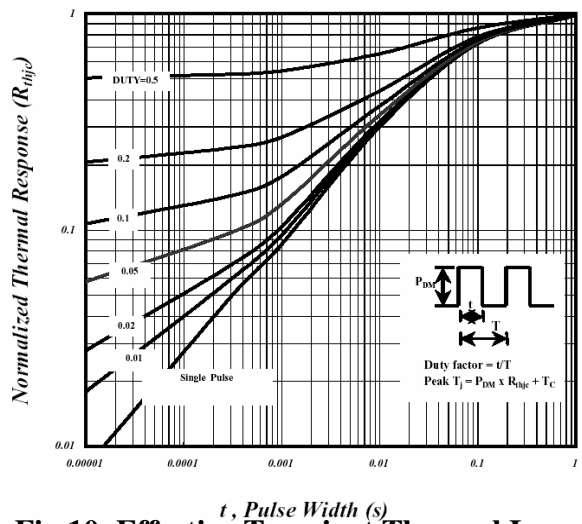
**Fig 7. Gate Charge Characteristics**



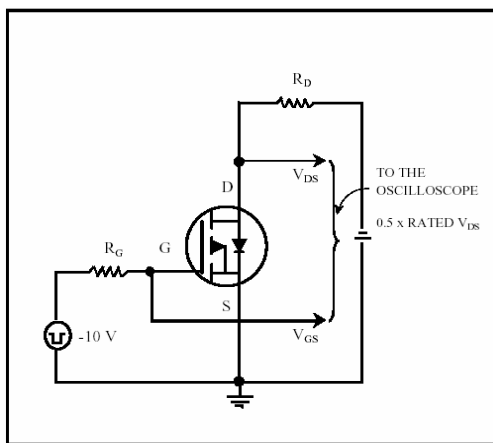
**Fig 8. Typical Capacitance Characteristics**



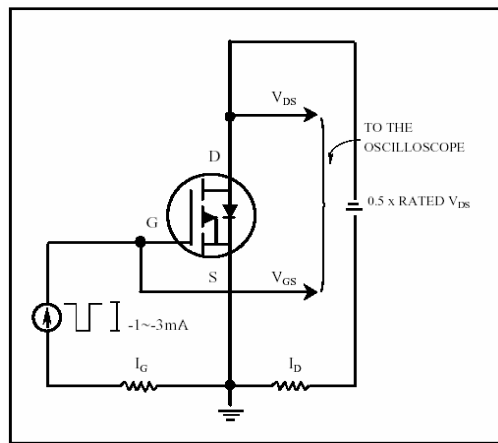
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Switching Time Circuit**



**Fig 12. Gate Charge Circuit**

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