



Features

- 4A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10 μ A Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver



Description

The IXDD604/IXDF604/IXDI604/IXDN604 dual high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. Each of the two outputs can source and sink 4A of peak current while producing voltage rise and fall times of less than 10ns. The input of each driver is virtually immune to latch up, and proprietary circuitry eliminates cross conduction and current “shoot-through.” Low propagation delay and fast, matched rise and fall times make the IXDD604/IXDF604/IXDI604/IXDN604 ideal for high-frequency and high-power applications.

The IXDD604 is a dual non-inverting driver with an enable. The IXDN604 is a dual non-inverting driver, the IXDI604 is a dual inverting driver, and the IXDF604 has one inverting driver and one non-inverting driver.

The IXDD604/IXDF604/IXDI604/IXDN604 family is available in a standard 8-lead DIP (PI), 8-lead SOIC (SIA), 8-lead SOIC with an exposed grounded metal back (SI), and an 8-lead DFN (D2) package.

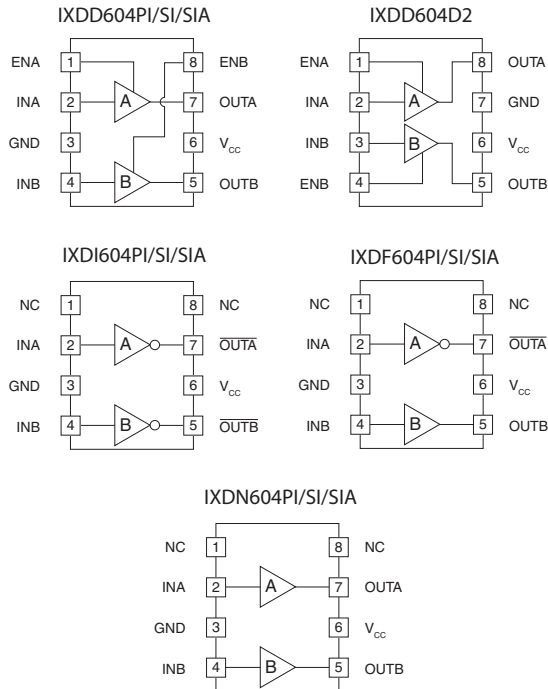
Ordering Information

Part Number	Logic Configuration	Package Type	Packing Method	Quantity
IXDD604D2TR		8-Lead DFN	Tape & Reel	2000
IXDD604PI	ENA	8-Lead DIP	Tube	50
IXDD604SI	INA	8-Lead SOIC with Exposed, Grounded Metal Back	Tube	100
IXDD604SITR	ENB	8-Lead SOIC with Exposed, Grounded Metal Back	Tape & Reel	2000
IXDD604SIA	INB	8-Lead SOIC	Tube	100
IXDD604SIATR		8-Lead SOIC	Tape & Reel	2000
IXDF604PI		8-Lead DIP	Tube	50
IXDF604SI	INA	8-Lead SOIC with Exposed, Grounded Metal Back	Tube	100
IXDF604SITR		8-Lead SOIC with Exposed, Grounded Metal Back	Tape & Reel	2000
IXDF604SIA	INB	8-Lead SOIC	Tube	100
IXDF604SIATR		8-Lead SOIC	Tape & Reel	2000
IXDI604PI		8-Lead DIP	Tube	50
IXDI604SI	INA	8-Lead SOIC with Exposed, Grounded Metal Back	Tube	100
IXDI604SITR		8-Lead SOIC with Exposed, Grounded Metal Back	Tape & Reel	2000
IXDI604SIA	INB	8-Lead SOIC	Tube	100
IXDI604SIATR		8-Lead SOIC	Tape & Reel	2000
IXDN604PI		8-Lead DIP	Tube	50
IXDN604SI	INA	8-Lead SOIC with Exposed, Grounded Metal Back	Tube	100
IXDN604SITR		8-Lead SOIC with Exposed, Grounded Metal Back	Tape & Reel	2000
IXDN604SIA	INB	8-Lead SOIC	Tube	100
IXDN604SIATR		8-Lead SOIC	Tape & Reel	2000

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1 Specifications

1.1 Lead Configurations



1.2 Lead Definitions

Lead Name	Description
INA	Channel A Logic Input
INB	Channel B Logic Input
ENA	Channel A Enable Input - Drive lead low to disable Channel A and force Channel A Output to a high impedance state
ENB	Channel B Enable Input - Drive lead low to disable Channel A and force Channel A Output to a high impedance state
<u>OUTA</u> OUTA	Channel A Output -Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
<u>OUTB</u> OUTB	Channel B Output -Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT
V _{CC}	Supply Voltage - Provides power to the device
GND	Ground - Common ground reference for the device

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V _{CC}	-	40	V
All Other Leads	-	-0.3	V _{CC} +0.3	V
Output Current		-	±4	A
Junction Temperature	T _J	-55	+150	°C
Storage Temperature	T _{STG}	-65	+150	°C

Absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage	V _{CC}	4.5	35	V
Operating Temperature Range	T _A	-40	+125	°C

1.5 Electrical Characteristics

Test Conditions: $T_A=25^\circ\text{C}$, $4.5\text{V} \leq V_{CC} \leq 35\text{V}$, one channel (unless otherwise noted).

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IH}	3	-	-	V
Input Voltage, Low	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IL}	-	-	0.8	
Input Voltage Range	-	V_{IN}	-5	-	$V_{CC}+0.3$	
Input Current	$0\text{V} \leq V_{IN} \leq V_{CC}$	I_{IN}	-10	-	10	μA
High EN Input Voltage	IXDD604 only	V_{ENH}	$2/3V_{CC}$	-	-	V
Low EN Input Voltage	IXDD604 only	V_{ENL}	-	-	$1/3V_{CC}$	
Output Voltage, High	-	V_{OH}	$V_{CC}-0.025$	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	$V_{CC}=18\text{V}$, $I_{OUT}=-10\text{mA}$	R_{OH}	-	1.3	2.5	Ω
Output Resistance, Low State	$V_{CC}=18\text{V}$, $I_{OUT}=10\text{mA}$	R_{OL}	-	1.1	2	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	± 1	A
Rise Time	$C_{LOAD}=1000\text{pF}$, $V_{CC}=18\text{V}$	t_R	-	9	16	ns
Fall Time	$C_{LOAD}=1000\text{pF}$, $V_{CC}=18\text{V}$	t_F	-	8	14	
On-Time Propagation Delay	$C_{LOAD}=1000\text{pF}$, $V_{CC}=18\text{V}$	t_{ONDLY}	-	29	50	
Off-Time Propagation Delay	$C_{LOAD}=1000\text{pF}$, $V_{CC}=18\text{V}$	t_{OFFDLY}	-	35	50	
Enable to Output-High Delay Time	IXDD604 only	t_{ENOH}	-	35	55	
Disable to High Impedance State Delay Time	IXDD604 only	t_{DOLD}	-	40	55	
Enable Pull-Up Resistor	-	R_{EN}	-	200	-	$\text{k}\Omega$
Power Supply Current	$V_{CC}=18\text{V}$, $V_{IN}=3.5\text{V}$	I_{CC}	-	1	3	mA
	$V_{CC}=18\text{V}$, $V_{IN}=0\text{V}$		-	-	10	μA
	$V_{CC}=18\text{V}$, $V_{IN}=V_{CC}$		-	-	10	

1.6 Electrical Characteristics

Test Conditions: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 35\text{V}$, $T_J < 150^{\circ}\text{C}$, one channel (unless otherwise noted).

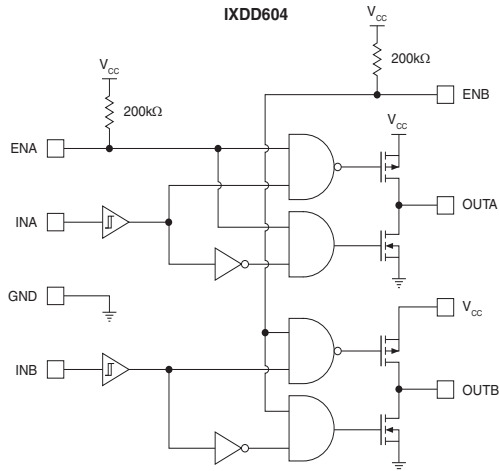
Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Input Voltage, High	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IH}	3.1	-	-	V
Input Voltage, Low	$4.5\text{V} \leq V_{CC} \leq 18\text{V}$	V_{IL}	-	-	0.65	
Input Voltage Range	-	V_{IN}	-5	-	$V_{CC} + 0.3$	
Input Current	$0\text{V} \leq V_{IN} \leq V_{CC}$	I_{IN}	-10	-	10	μA
Output Voltage, High	-	V_{OH}	$V_{CC} - 0.025$	-	-	V
Output Voltage, Low	-	V_{OL}	-	-	0.025	
Output Resistance, High State	$V_{CC} = 18\text{V}$, $I_{OUT} = -10\text{mA}$	R_{OH}	-	-	3	Ω
Output Resistance, Low State	$V_{CC} = 18\text{V}$, $I_{OUT} = 10\text{mA}$	R_{OL}	-	-	2.5	
Output Current, Continuous	Limited by package power dissipation	I_{DC}	-	-	± 1	A
Rise Time	$C_{LOAD} = 1000\text{pF}$, $V_{CC} = 18\text{V}$	t_R	-	-	16	ns
Fall Time	$C_{LOAD} = 1000\text{pF}$, $V_{CC} = 18\text{V}$	t_F	-	-	14	
On-Time Propagation Delay	$C_{LOAD} = 1000\text{pF}$, $V_{CC} = 18\text{V}$	t_{ONDLY}	-	-	65	
Off-Time Propagation Delay	$C_{LOAD} = 1000\text{pF}$, $V_{CC} = 18\text{V}$	t_{OFFDLY}	-	-	65	
Enable to Output-High Delay Time	IXDD604 only	t_{ENOH}	-	-	65	
Disable to High Impedance State Delay Time	IXDD604 only	t_{DOLD}	-	-	65	
Power Supply Current	$V_{CC} = 18\text{V}$, $V_{IN} = 3.5\text{V}$	I_{CC}	-	1	3.5	mA
	$V_{CC} = 18\text{V}$, $V_{IN} = 0\text{V}$		-	-	150	μA
	$V_{CC} = 18\text{V}$, $V_{IN} = V_{CC}$		-	-	150	

1.7 Thermal Characteristics

Package	Parameter	Rating	Units
IXDD604D2 (8-Lead DFN)	θ_{JA}	35	$^{\circ}\text{C/W}$
IXD_604PI (8-Lead DIP)		125	
IXD_604SI (8-Lead SOIC with Exposed, Grounded Metal Back)		85	
IXD_604SIA (8-Lead SOIC)		120	

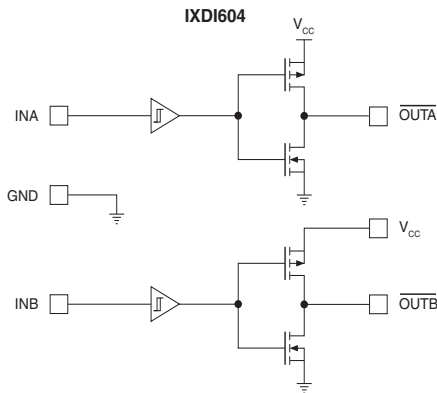
2 Functional Description

2.1 IXDD604 Functional Block Diagram



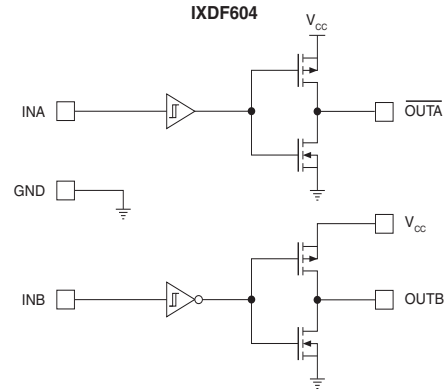
IN _x	EN _x	OUT _x
0	1 or open	0
1	1 or open	1
0	0	Z
1	0	Z

2.2 IXDI604 Functional Block Diagram



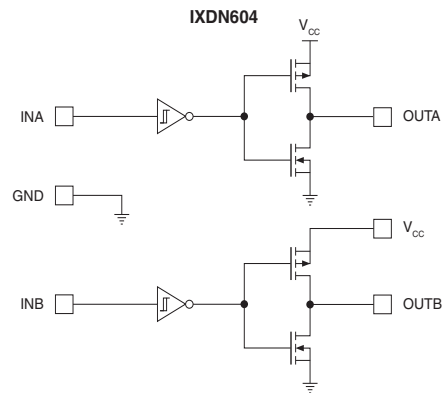
IN _x	OUT _x
0	1
1	0

2.3 IXDF604 Functional Block Diagram



INA	OUTA
0	1
1	0
INB	OUTB
0	0
1	1

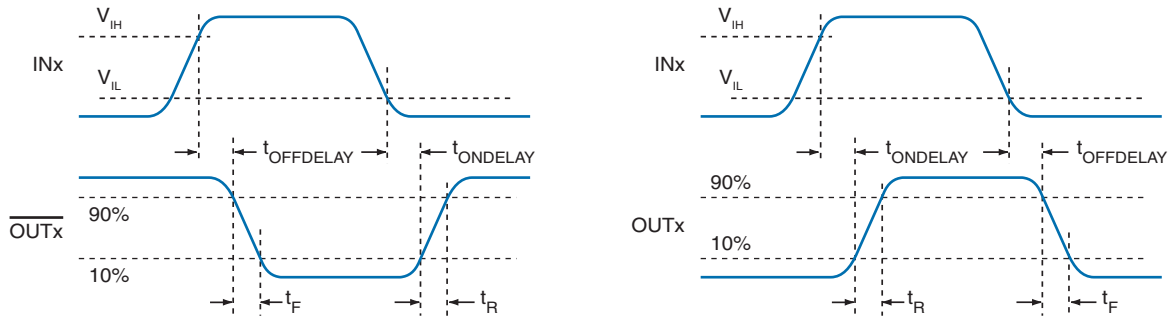
2.4 IXDN604 Functional Block Diagram



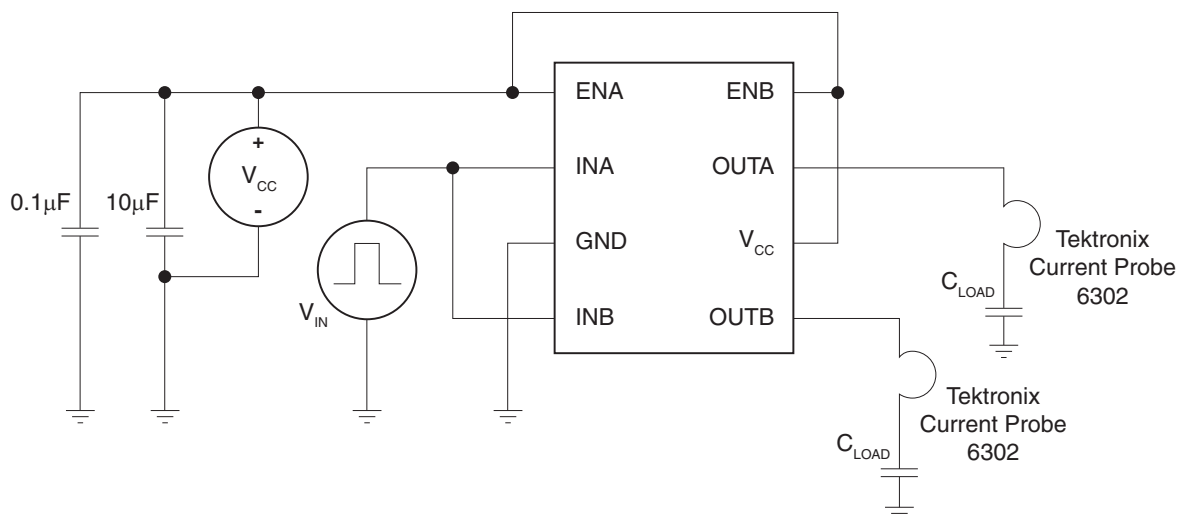
IN _x	OUT _x
0	0
1	1

3 IXD_604 Performance

3.1 Timing Diagrams

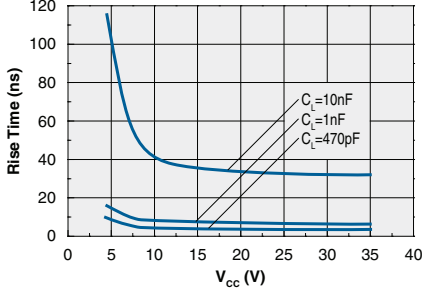


3.2 Characteristics Test Diagram

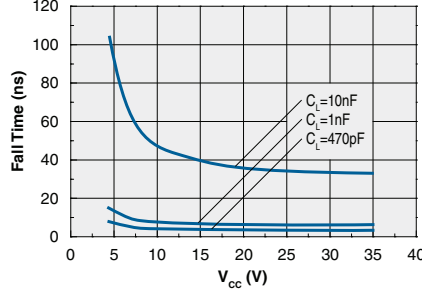


3.3 Typical Performance Characteristics

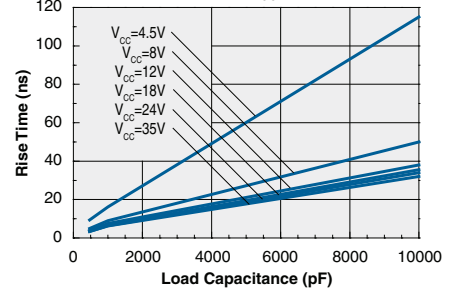
A&B Rise Times vs. V_{CC}
for Various Load Capacitances
(Input=0-5V, $f=10\text{kHz}$, $T_A=25^\circ\text{C}$)



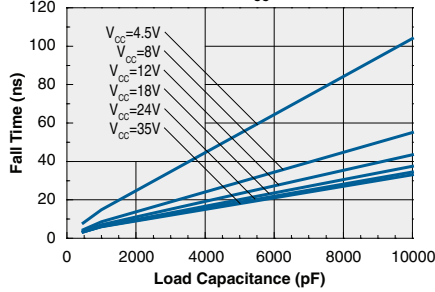
A&B Fall Times vs. V_{CC}
for Various Load Capacitances
(Input=0-5V, $f=10\text{kHz}$, $T_A=25^\circ\text{C}$)



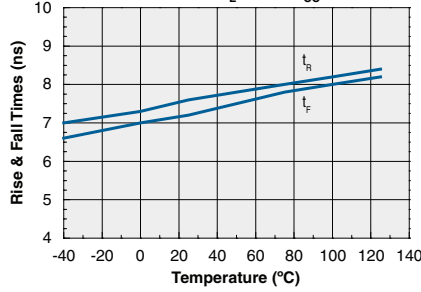
A&B Rise Time vs. Load Capacitance
at Various V_{CC} Levels



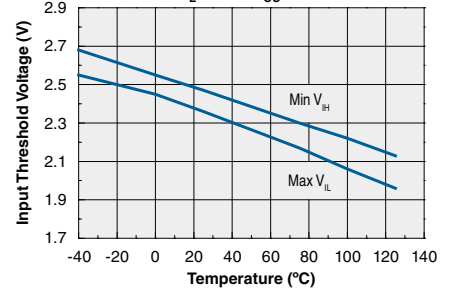
A&B Fall Time vs. Load Capacitance
at Various V_{CC} Levels



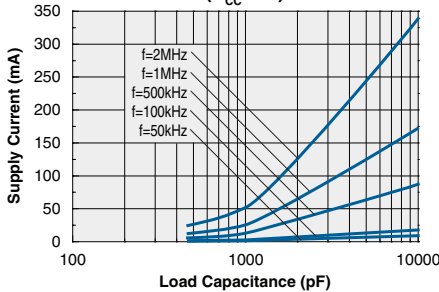
A&B Rise and Fall Times
vs. Temperature
(Input=0-5V, $C_L=1\text{nF}$, $V_{CC}=18\text{V}$)



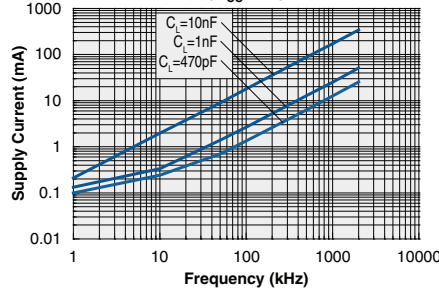
Input Threshold Voltage
vs. Temperature
($C_L=1\text{nF}$, $V_{CC}=18\text{V}$)



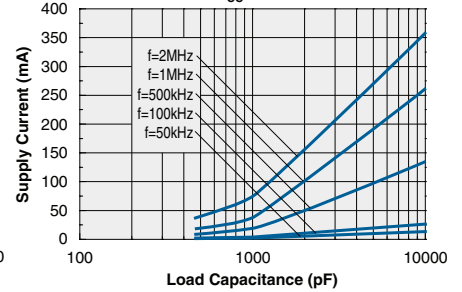
Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=8\text{V}$)



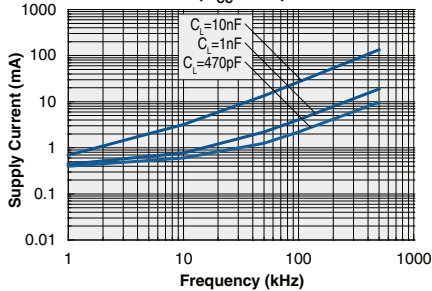
Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=8\text{V}$)



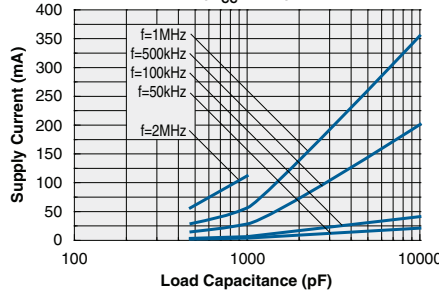
Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=12\text{V}$)



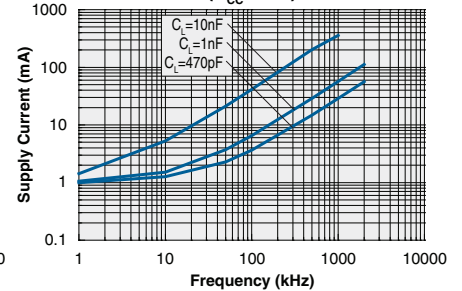
Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=12\text{V}$)



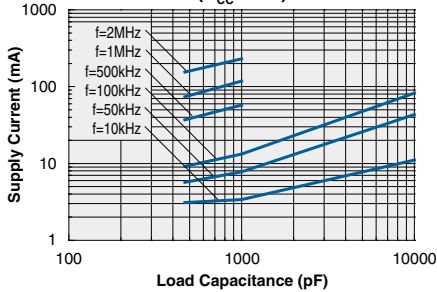
Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=18\text{V}$)



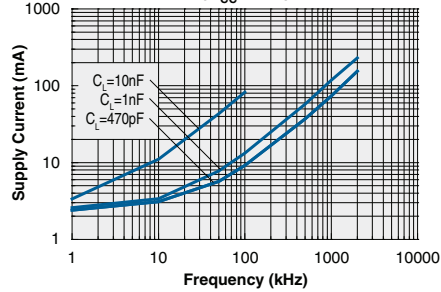
Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=18\text{V}$)



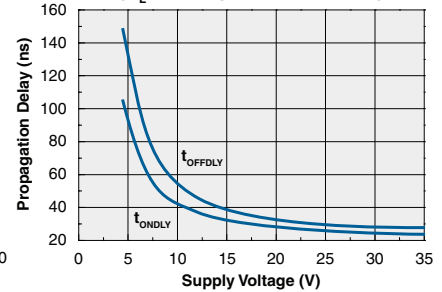
**Supply Current vs. Load Capacitance
Both Outputs Active
($V_{CC}=35V$)**



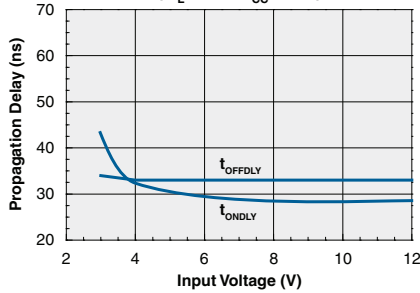
**Supply Current vs. Frequency
Both Outputs Active
($V_{CC}=35V$)**



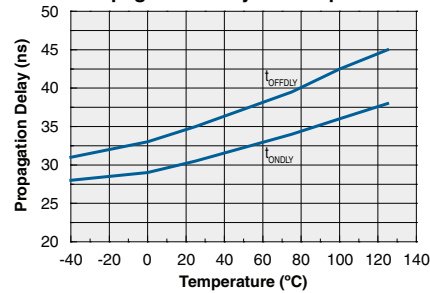
**Propagation Delay vs. Supply Voltage
($C_L=1nF$, Input=0-5V, f=1kHz)**



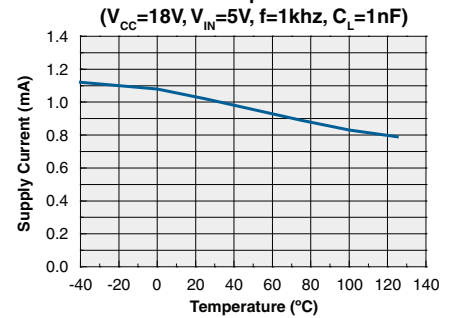
**Propagation Delay vs. Input Voltage
($C_L=1nF$, $V_{CC}=15V$)**



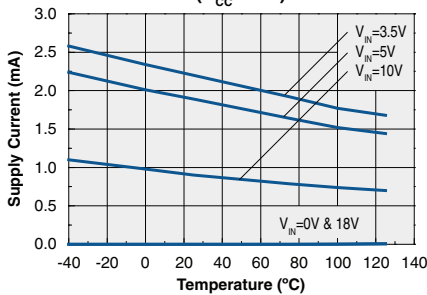
Propagation Delay vs. Temperature



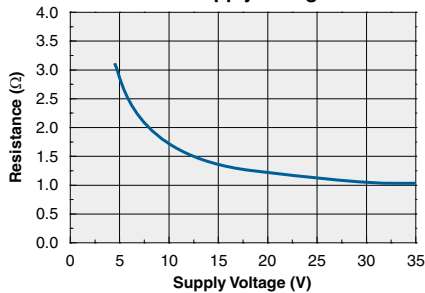
**Dynamic Supply Current
vs. Temperature**



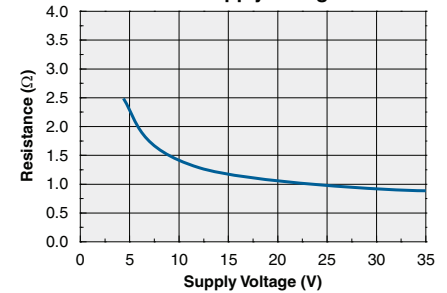
**Quiescent Supply Current
vs. Temperature
($V_{CC}=18V$)**



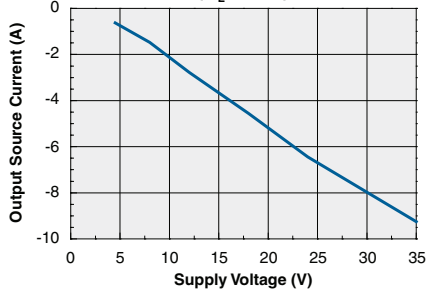
**High State Output Resistance @ -10mA
vs. Supply Voltage**



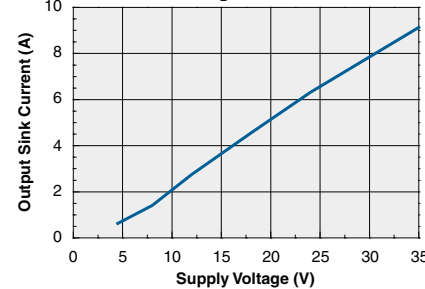
**Low State Output Resistance @ +10mA
vs. Supply Voltage**



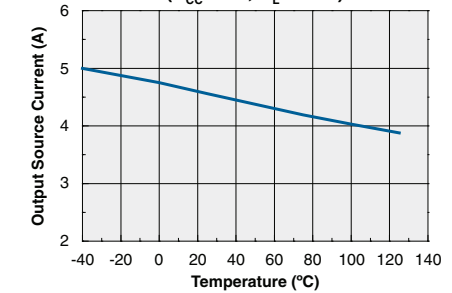
**Output Source Current
vs. Supply Voltage
($C_L=10nF$)**

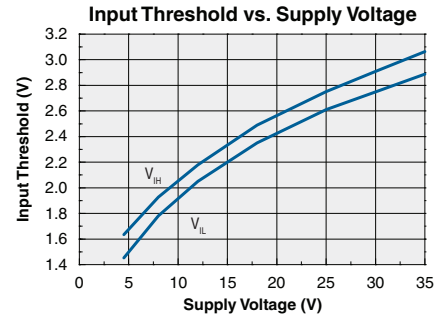
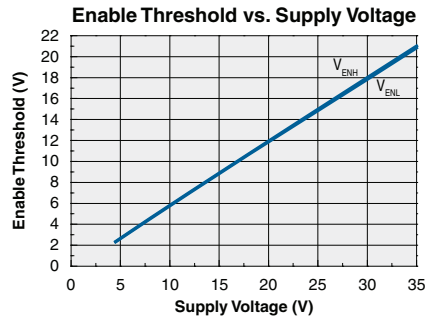
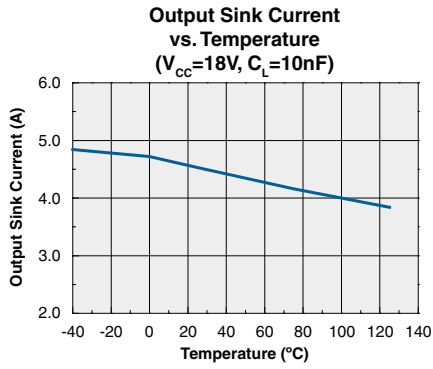


**Output Sink Current
vs. Supply Voltage
($C_L=10nF$)**



**Output Source Current
vs. Temperature
($V_{CC}=18V$, $C_L=10nF$)**





4 Manufacturing Information

4.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
IXDD604D2	MSL 3
IXD_604PI/SI/SIA	MSL 1

4.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
IXD_604SI/SIA/D2	260°C for 30 seconds
IXD_604PI	250°C for 30 seconds

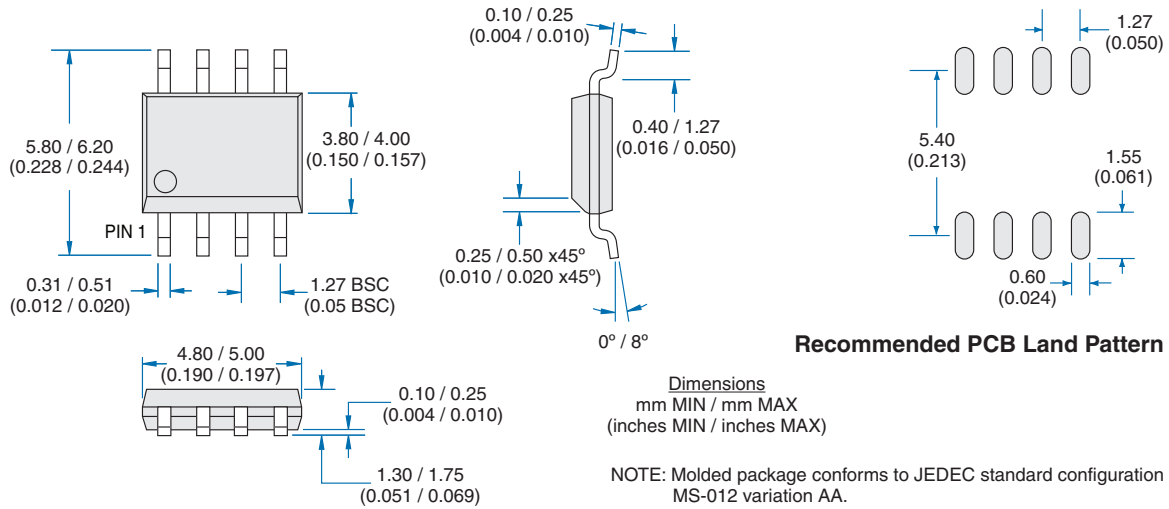
4.4 Board Wash

Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable. Since Clare employs the use of silicone coating as an optical waveguide in many of its optically isolated products, the use of a short drying bake could be necessary if a wash is used after solder reflow processes. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

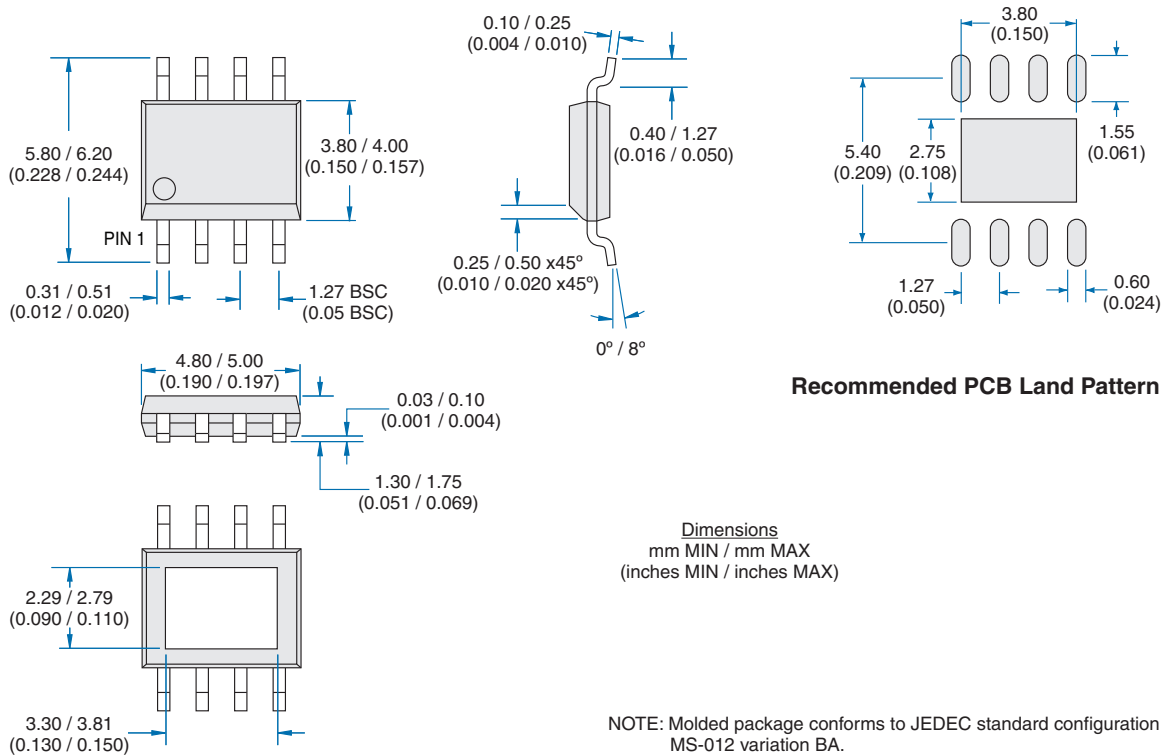


4.5 Mechanical Dimensions

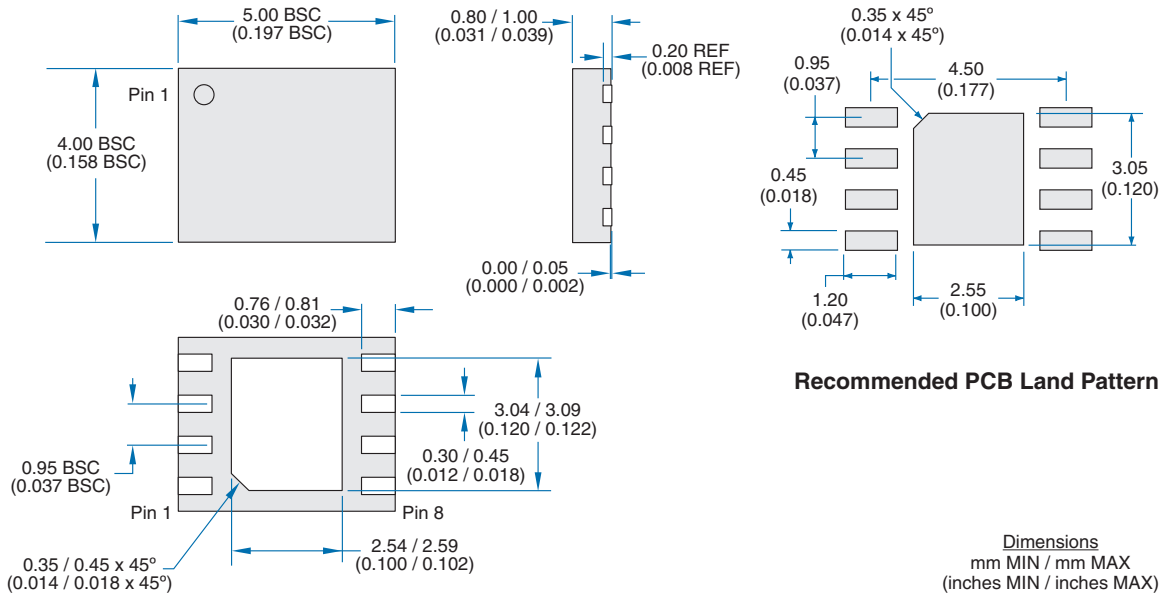
4.5.1 IXD_604SIA (8-Lead SOIC)



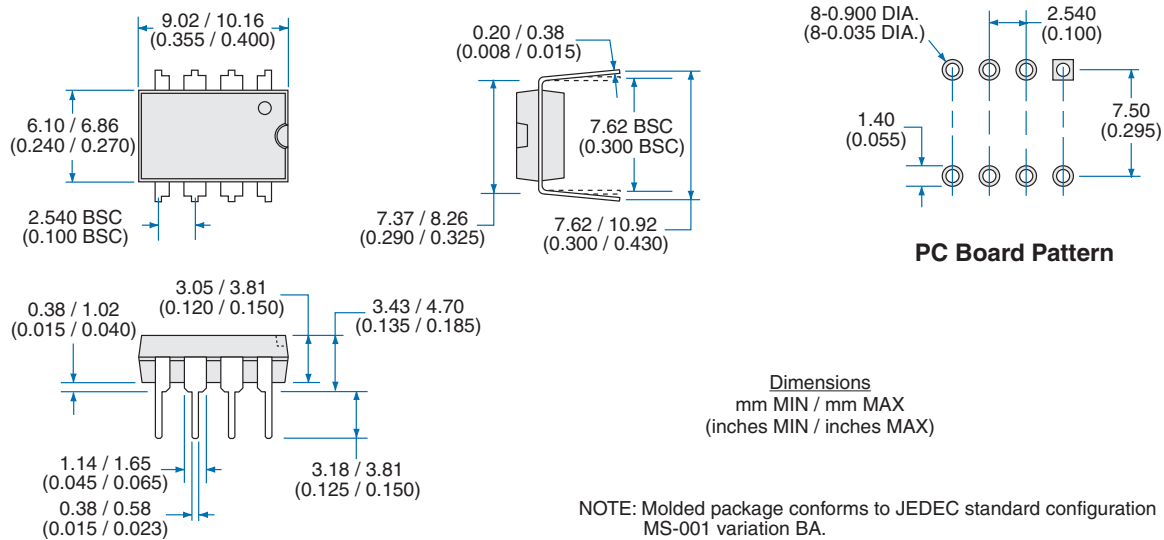
4.5.2 IXD_604SI (8-Lead SOIC with Exposed, Grounded Metal Back)



4.5.3 IXDD604D2 (8-Lead DFN)



4.5.4 IXD_604PI (8-Lead DIP)



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