DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM	TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
	A	2004.12.10	First Release.	ZHU LING JUN	LI HUA MING
A	B	2006.03.10	Items 1 to 2 were updated. 1)(Page 5, Figure 1) The module specification was updated. 2)(Page 16, Point 6) The Quality Units was updated.	ZHU LING JUN	LI HUA MING

CONTENTS

Specification of LCD Module Type
Item No.: TM0027-Z-LED

1. General Description

- 128 x 64 Dots FSTN Positive Transflective Dot Matrix LCD Module.
- Viewing Angle: 6 O'clock direction.
- Driving duty: 1/65 Duty, 1/9 bias.
- 'SITRONIX' ST7565V-G LCD Controller &Driver or equivalent.
- Chip-On-Glass (COG).
- High-speed 8-bit MPU interface or Serial interface.
- Power Supply: +3.0V.
- FPC.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	39.1(W) x 33.0(H) x 2.0(D)(Exclude FPC, Include LCD end seal) 39.1(W) x 53.0(H) x 2.0(D)(Include FPC, Include LCD end seal)	mm
Viewing area	33.8(W) x 22.2(H)	mm
Display format	128 x 64 dots	-
Dot size	0.225(W) x 0.285(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.240 (W) x 0.300(H)	mm
Weight:	TBD	grams

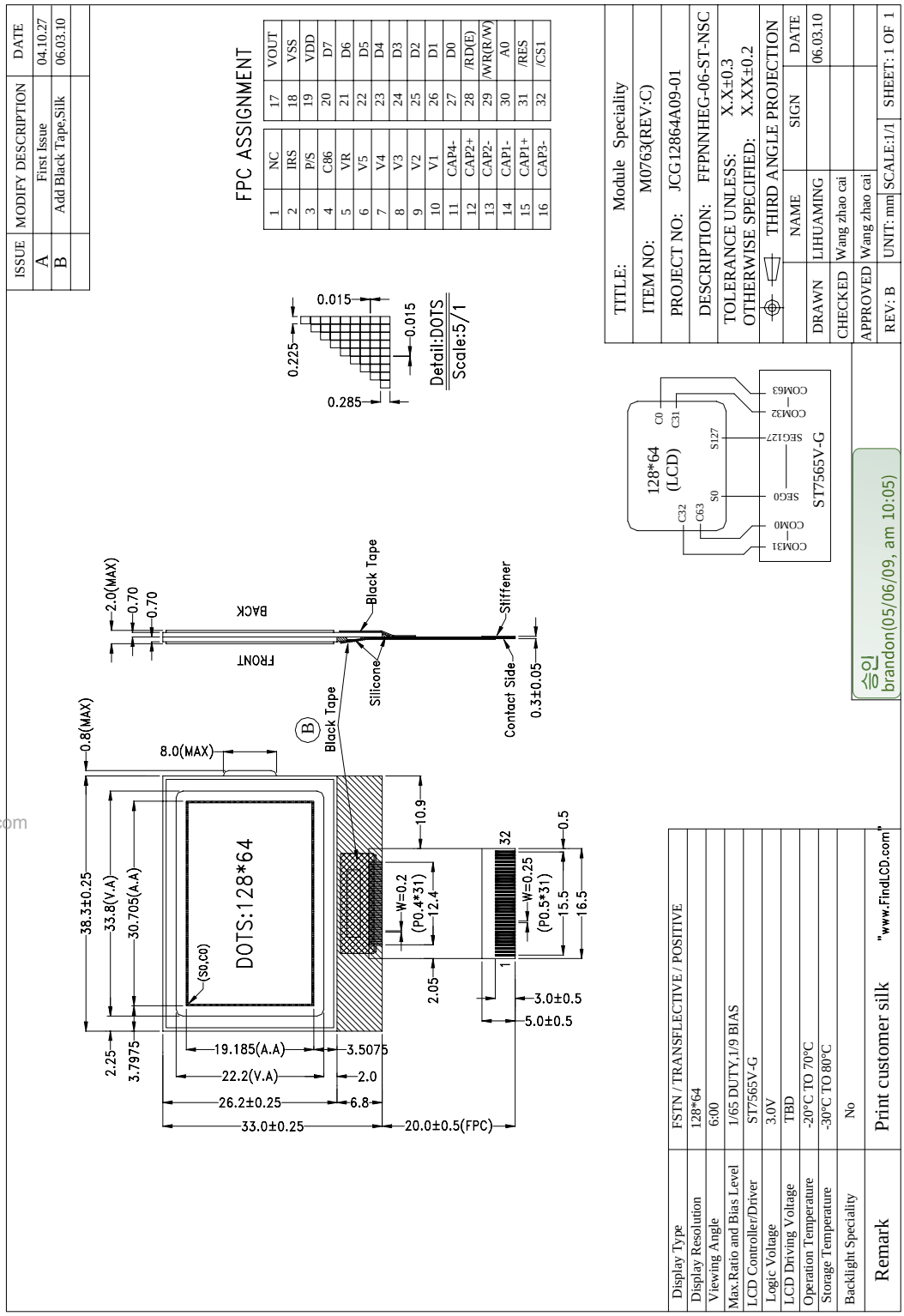
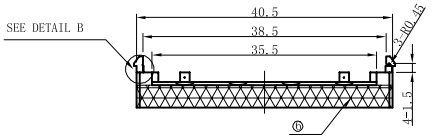
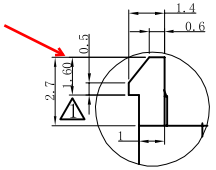


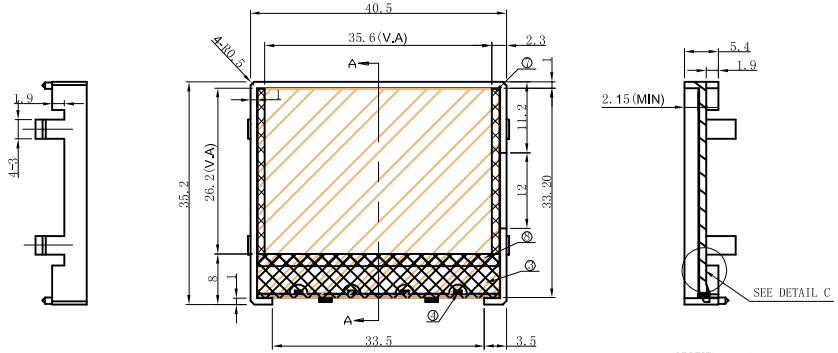
Figure 1: Module Specification

GEMINI TECHNOLOGY CO., LTD.				SPECIFICATION FOR BACKLIGHT 规 格			
				CUSTOMER'S CODE: (客户料号)	TM0027	EDITION: (版本号)	A
Date:(日期)	04/12/02	Page:(页数)	1/1 第三角法	P.N MODEL NO.: (普耐料号)	PBE523	EDITION: (版本号)	A
						Revies by: (承认)	
						Confirm by: (审查)	
						Measured by: (设计)	李绍华

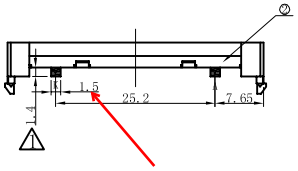




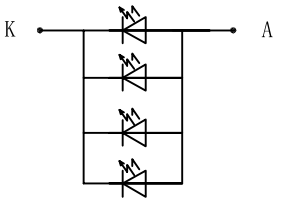
DETAIL B
SCALE, 4.000

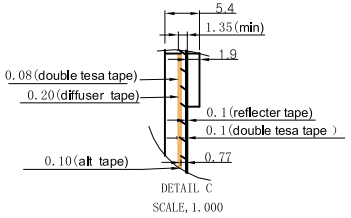


SECTION A-A



电路图





DETAIL C
SCALE, 1.000

Notes:
备注
1. Unit:mm.
单位: mm
2. Do not scale drawing.
未按比例出图
3. ⚠Modification rev.number.
⚠为修改标记
4. Without tolorance is ±0.2
未注公差为±0.2
5. BLUE WAVELENGTH:465-475nm
蓝光波长为465-475纳米
6. Vf=3.2±0.2V.
电压为3.2±0.2伏特
7. RATE≥70%; Lv≥40cd/m2
??????70%;????40cd/m2

REV(标记)	DATE (日期)	DESCRIPTION (描述)
⚠	04.12.02	更改A, K高度和钩子结构

NO.(序号)	TITLE (项目)	QUANTITY (数量)
8	DOUBLE SIDE TAPE(双面胶)	1
7	DOUBLE SIDE TAPE(双面胶)	2
6	SHADE TAPE (侧遮光片)	3
5	REFLECTOR TAPE (反射片)	1
4	BLUE LED(兰灯4个)	4
3	DIFFUSER AND SHIELDING (扩散遮光片)	1
2	PCB(基板)	1
1	LIHGT GUIDE (导光板)	1

Customer Name: 客户名称	集美电子	Approval Date: 承认日期		Approved by: 承认		Please Confirm This Drawing On/Before 请 签 回 此 图	

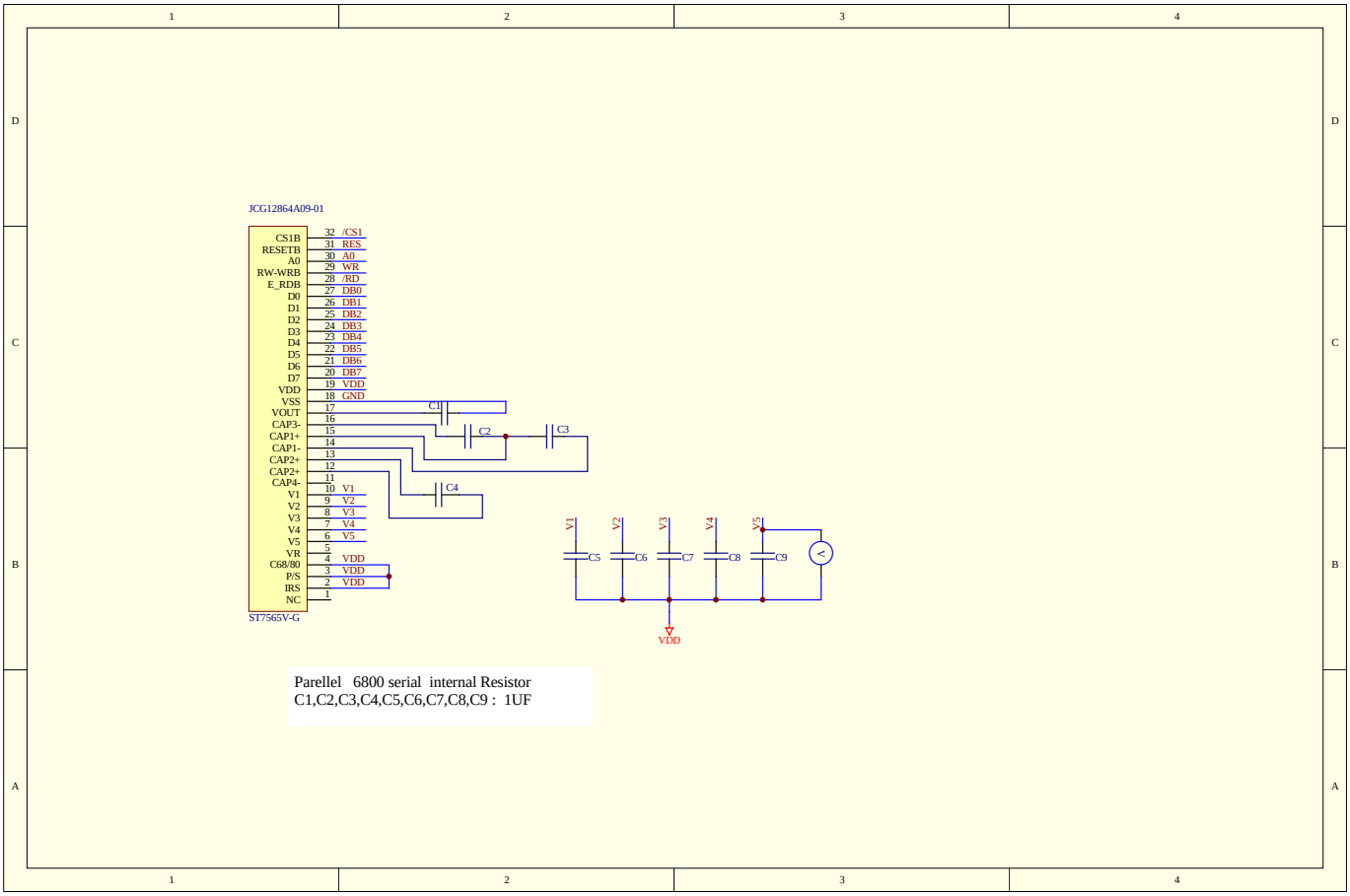


Figure 2: Recommend Outer circuit

3. Interface signals

Table 2(a)

Pin No.	Symbol	Description
1	NC	No connection.
2	IRS	This terminal selects the resistors for the V5 voltage level adjustment. IRS = "H": Use the internal resistors IRS = "L": Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
3	P/S	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input.
4	C86	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 MPU interface.
5	VR	Output voltage regulator terminal. Provides the voltage between VDD and V5 through a resistive voltage divider. IRS = "L": the V5 voltage regulator internal resistors are not used . IRS = "H": the V5 voltage regulator internal resistors are used .
6	V5	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op.amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. VDD (= V0) ≧V1 ≧V2 ≧V3 ≧V4 ≧V5 When the power supply turns ON, the internal power supply circuits produce theV1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.
7	V4	
8	V3	
9	V2	
10	V1	
11	CAP4-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
12	CAP2+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.
13	CAP2-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.
14	CAP1-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.
15	CAP1+	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.
16	CAP3-	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.

LCD bias	V1	V2	V3	V4
1/9 bias	(1/9) x V5	(2/9) x V5	(7/9) x V5	(8/9) x V5

Table 2(b)

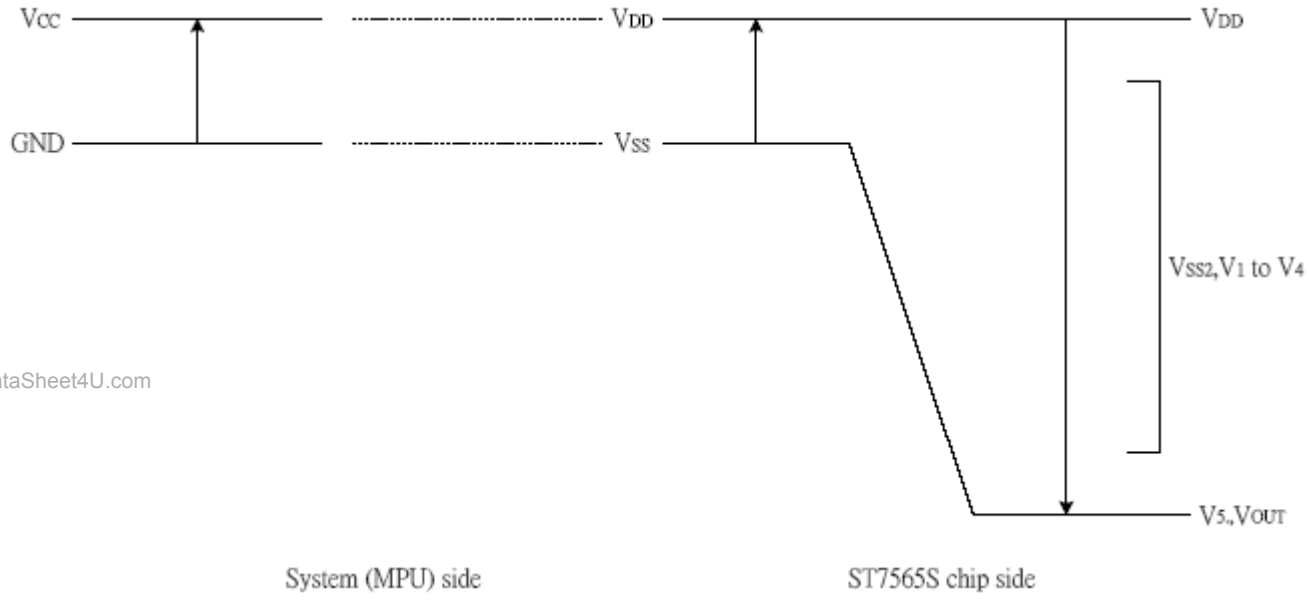
Pin No.	Symbol	Description
17	VOUT	Voltage converter input / output pin.
18	VSS	Ground (0V).
19	VDD	Power supply for logic.
20	D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L") : D7: serial data input (SI); D6 : the serial clock input (SCL). D0 to D5 are set to high impedance. When the chip select is not active, D0 to D7 are set to high impedance.
21	D6	
22	D5	
23	D4	
24	D3	
25	D2	
26	D1	
27	D0	
28	/RD(E)	When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565V series data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.
29	/WR(R/W)	When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write.
30	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
31	/RES	When /RES is set to "L," the settings are initialized. The reset operation is performed by the /RES signal level.
32	/CS1	This is the chip select signal.

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD -VSS	-0.3	+5.0	V
Power Supply voltage	VSS2	-4.0	-1.8	V
Power Supply voltage	V5, VOUT	-18.0	+0.3	V
Power Supply voltage	V1, V2, V3, V4	V5	+0.3	
Input voltage range	VIN	-0.3	VDD+0.3	V
Output voltage	VO	-0.3	VDD+0.3	V



Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

1. All voltage values are referenced to VSS = 0V.
2. Insure that the voltage levels of V1, V2, V3, and V4 are always such that
   VDD ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ V5.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3.0V±0.1V, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		2.9	3.0	3.1	V
Supply voltage (LCD)	VLCD = VDD-V5	VDD =+3.0V, Note 1	8.8	9.0	9.2	V
Input signal voltage For A0, D0 to D5, D6 (SCL), D7 (SI), /RD (E), /WR (R/W), /CS1, C86, /RES, IRS, P/Spins.	V_{IH}	"H" level	0.8VDD	-	VDD	V
	V_{IL}	"L" level	VSS	-	0.2VDD	V
Supply Current (Logic & LCD)	IDD	Note 1	-	0.3	0.45	mA

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At Ta = -20 °C To +70 °C, VDD = +3.0V±0.1V, VSS = 0V.
Refer to Fig. 3, the bus timing diagram for Read / write timing chart (8080-series MPU).

Table 6

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		100	—	
Enable H pulse width (WRITE)		t_{CCHW}		100	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		100		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		10	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

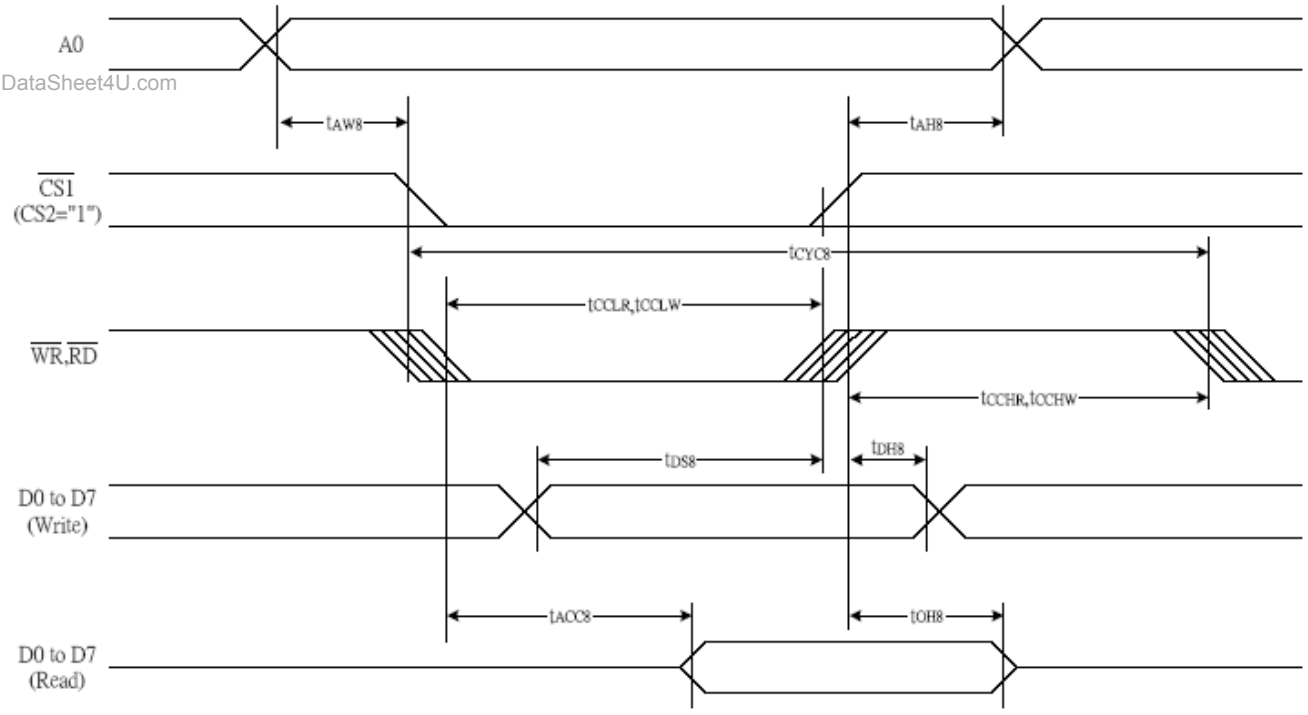


Figure 3: Read / write timing chart (8080-series MPU)

At Ta = -20 °C To +70 °C, VDD = +3.0V±0.1V, VSS = 0V.

Refer to Fig. 4, the bus timing diagram for Read / write timing chart (6800-series MPU).

Table 7

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		100	—	
Enable H pulse width (WRITE)		t_{EWHW}		100	—	
Enable L pulse width (READ)	RD	t_{EWLR}		100	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		10	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

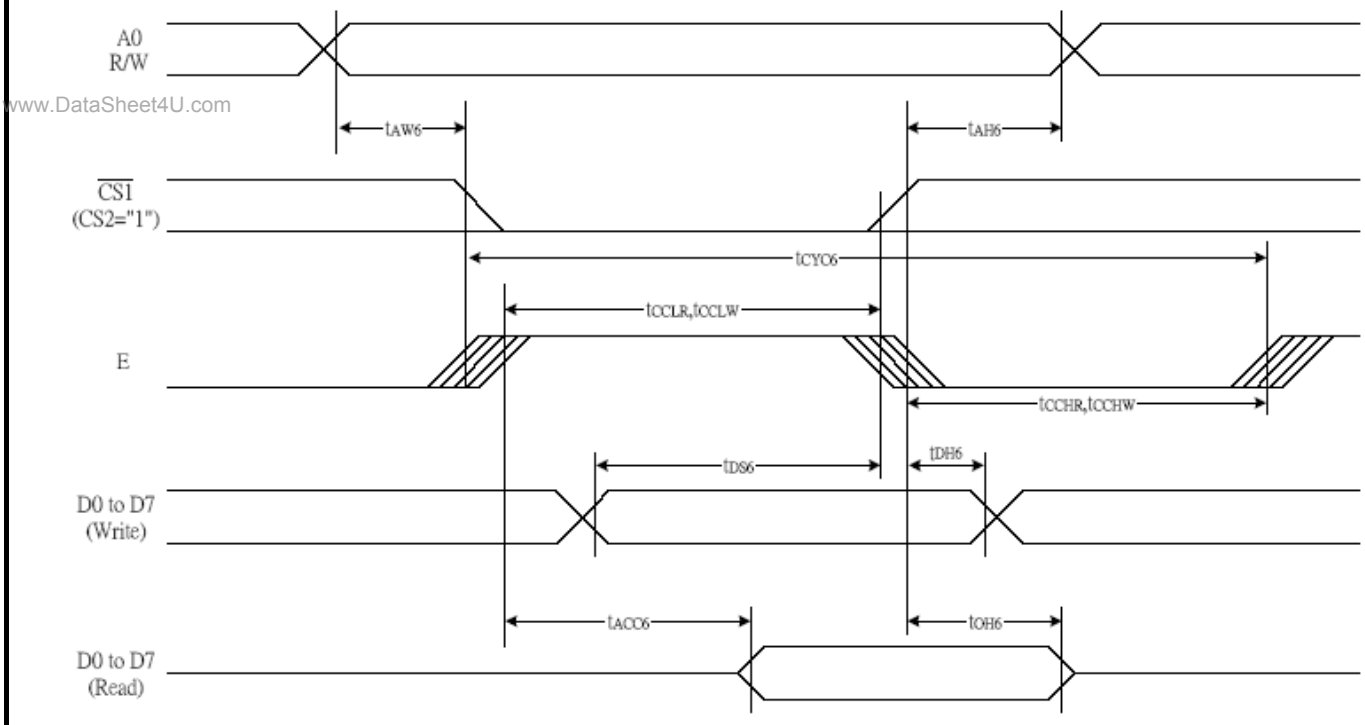


Figure 4: Read / write timing chart (6800-series MPU)

At Ta = -20 °C To +70 °C, VDD = +3.0V±0.1V, VSS = 0V.

Refer to Fig. 5, the bus timing diagram for Serial Interface.

Table 8

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		100	—	ns
SCL "H" pulse width		T_{shw}		50	—	
SCL "L" pulse width		T_{SLW}		50	—	
Address setup time	A0	T_{SAS}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{SDH}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

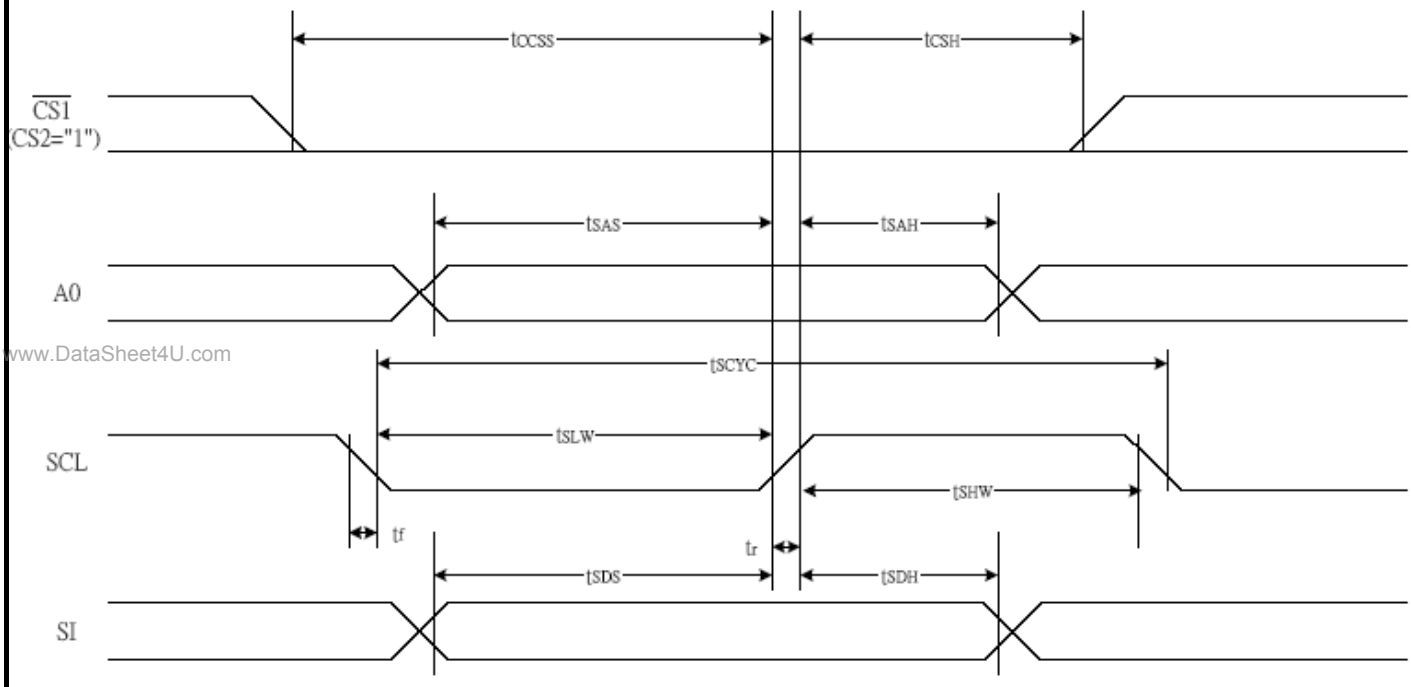


Figure 5: Read/Write timing for Serial Interface

At Ta = -20 °C To +70 °C, VDD = +3.0V±0.1V, VSS = 0V.
Refer to Fig. 6, the bus timing diagram for reset timing.

Table 9

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.0	us
Reset "L" pulse width	/RES	t_{RW}		1.0	—	—	us

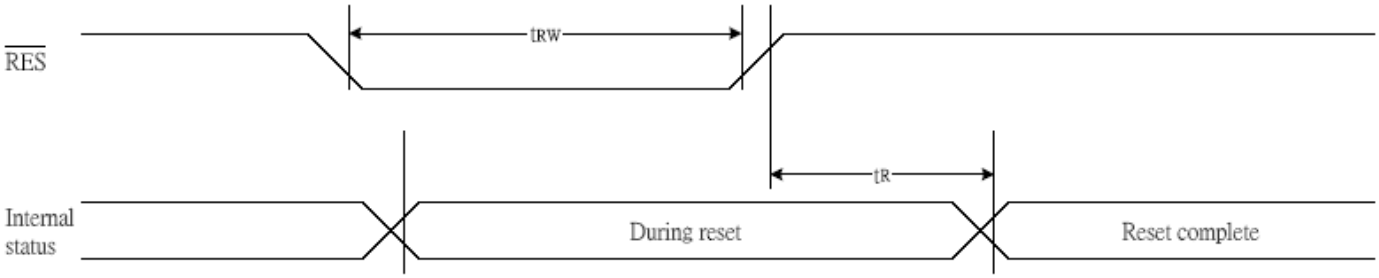


Figure 6: Reset Timing

5.3 Instruction Table

Table 10

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565V)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Set the V_5 output voltage electronic volume register
Electronic volume register set				0	0	Electronic volume value						
(19) Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
Static indicator register set				0	0	0	0	0	0	0	Mode	Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 0	0 0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
										step-up value		
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command