TRULY® LCD MODULE MSC-G12864DYSY-5N Version : 1.1 Aug 3, 1998

LLOYD'S REGISTER QUALITY COMPANY ISO9002

NATIONAL ACCREDITATION OF CERTIFICATION BODIES

CERT. No. 946535

PRODUCT SPECIFICATIONS

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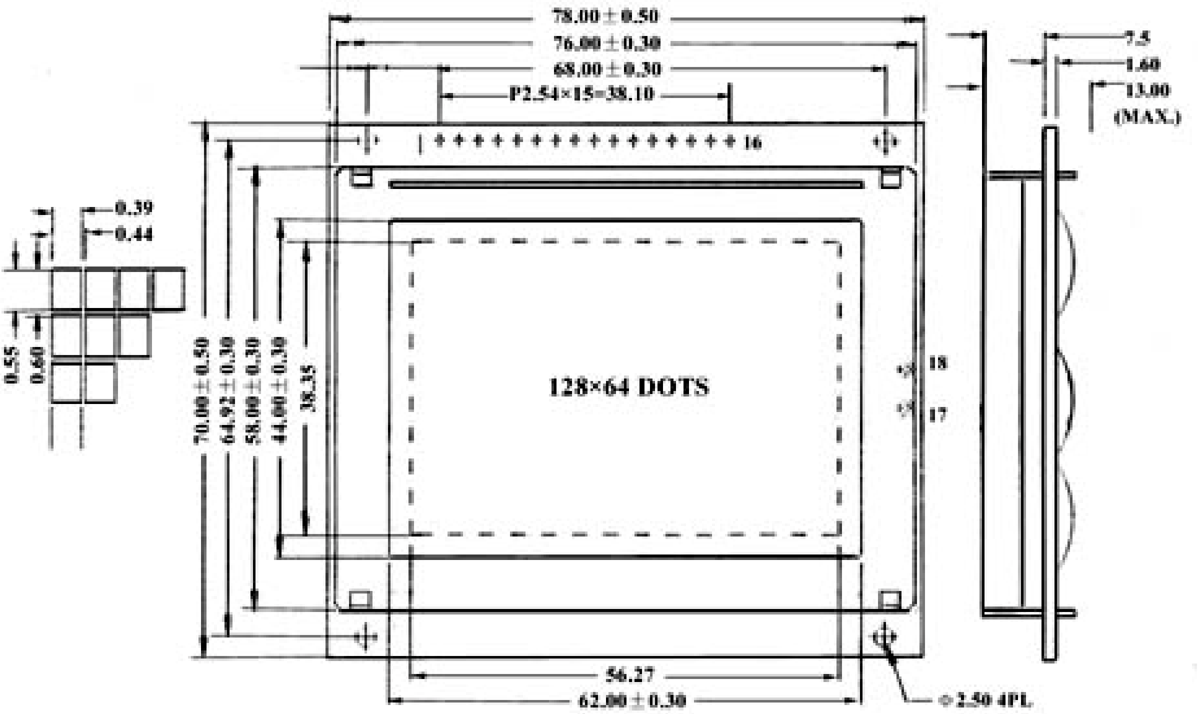
- USING LCD MODULES

■ PHYSICAL DATA

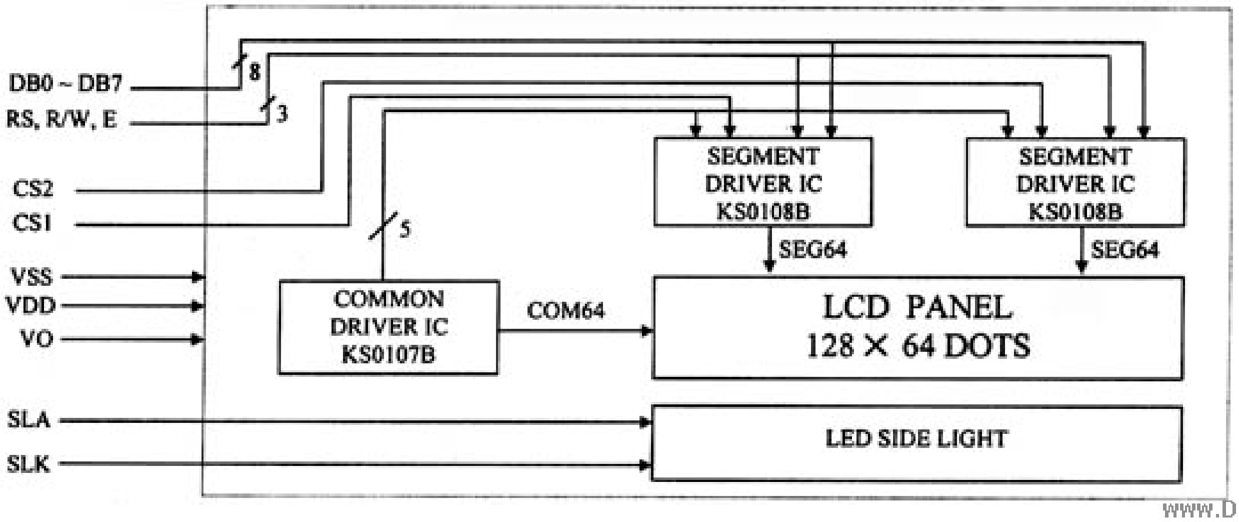
Item	Contents	Unit
LCD type	STN	---
LCD duty	1/64	---
LCD bias	1/9	---
Viewing direction	6	o'clock
Module size (W×H×T)	78 × 70 × 13MAX (3.07″ × 2.76″ × 0.51″MAX)	mm
Viewing area (W×H)	62 × 44 (2.44″ × 1.73″)	mm
Number of dots	128 × 64	dots
Dot size (W×H)	0.39 × 0.55 (0.015″ × 0.022″)	mm
Dot pitch (W×H)	0.44 × 0.60 (0.017″ × 0.024″)	mm

■ EXTERNAL DIMENSIONS


78.00±0.50
76.00±0.30
68.00±0.30
P2.54×15=38.10
7.5
1.60
13.00
(MAX.)
16
0.39
0.44
0.55
0.60
70.00±0.50
64.92±0.30
58.00±0.30
44.00±0.30
38.35
128×64 DOTS
18
17
56.27
62.00±0.30
φ2.50 4PL

■ BLOCK DIAGRAM

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CS1	CS2	VSS	VDD	VO	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	SLA	SLK


DB0 ~ DB7
8
RS, R/W, E
3
CS2
CS1
5
VSS
VDD
VO
SEGMENT DRIVER IC KS0108B
SEGMENT DRIVER IC KS0108B
SEG64
SEG64
COMMON DRIVER IC KS0107B
COM64
LCD PANEL 128 × 64 DOTS
SLA
SLK
LED SIDE LIGHT

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■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Min	Max	Unit
Supply voltage for logic	VDD	-0.3	7.0	V
Supply voltage for LCD	VDD - VO	-0.3	VDD+0.3	V
Input voltage	VI	-0.3	VDD+0.3	V
Operating temperature	TOP	0	50	℃
Storage temperature	TST	-10	60	℃

■ ELECTRICAL CHARACTERISTICS (VDD = +5V±5% , VSS = 0V, Ta = 25℃)

◆ DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for logic	VDD	---	4.5	5.0	5.5	V
Supply current for logic	IDD	---	---	2.62	4	mA
Operating voltage for LCD	VDD - VO	0℃	10.4	10.9	11.4	V
		25℃	9.8	10.3	10.7	V
		50℃	9.1	9.6	10.1	V
Supply voltage for side light	VF	---	---	4.2	4.6	V
Supply current for side light	IF	VF=4.2V	---	140	240	mA
Input voltage ' H ' level	VIH	---	0.7VDD	---	VDD	V
Input voltage ' L ' level	VIL	---	0	---	0.3VDD	V

◆ AC Characteristics

- MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E cycle	tcyc	1000	---	---	ns
E high level width	twhE	450	---	---	ns
E low level width	twlE	450	---	---	ns
E rise time	t_r	---	---	25	ns
E fall time	tf	---	---	25	ns
Address set-up time	tas	140	---	---	ns
Address hold time	tah	10	---	---	ns
Data set-up time	tdsw	200	---	---	ns
Data delay time	tddr	---	---	320	ns
Data hold time(write)	tdhw	10	---	---	ns
Data hold time(read)	tdhr	20	---	---	ns

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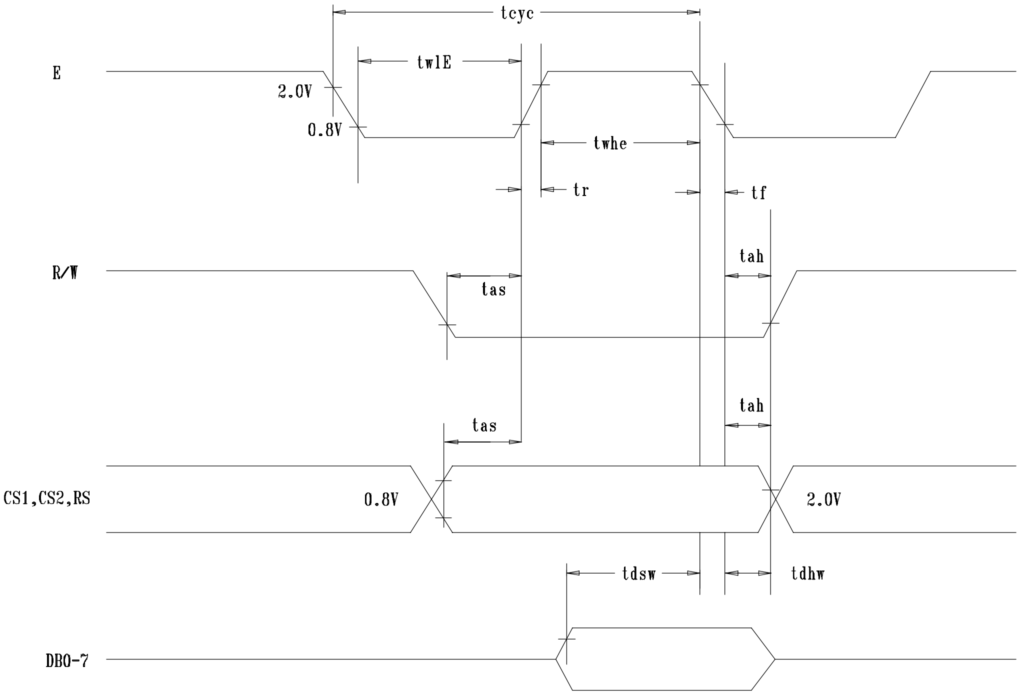
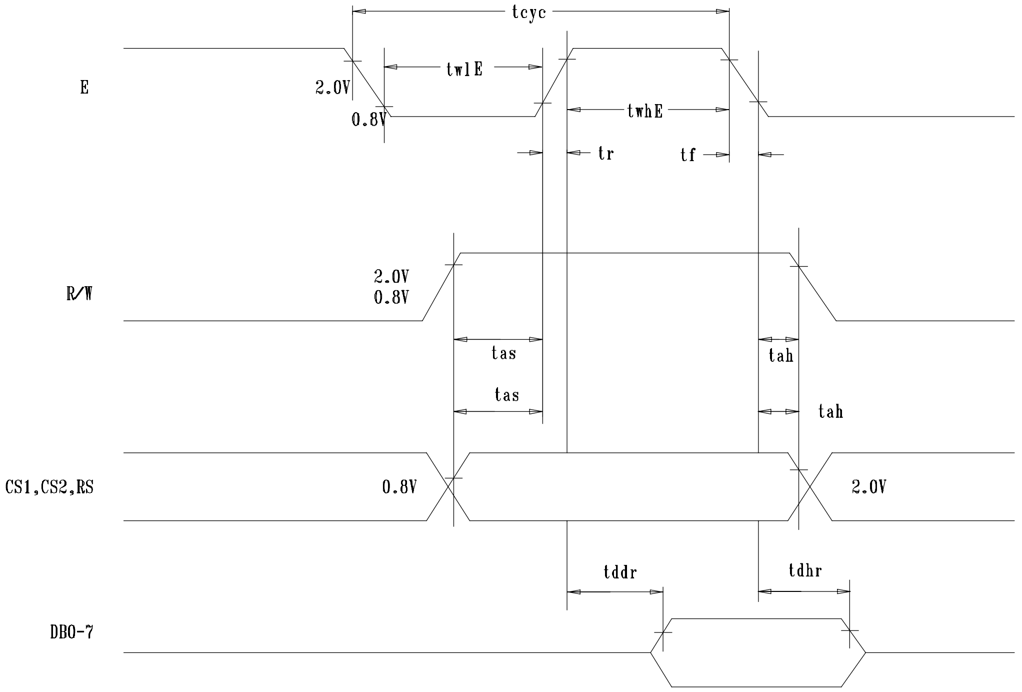

tcyc
E
twlE
2.0V
0.8V
twhe
tr
tf
R/W
tah
tas
tah
tas
CS1,CS2,RS
0.8V
2.0V
tdsw
tdhw
DB0-7

MPU Write Timing


tcyc
E
twlE
2.0V
0.8V
twhE
tr
tf
R/W
2.0V
0.8V
tas
tah
tas
tah
CS1,CS2,RS
0.8V
2.0V
tddr
tdhr
DB0-7

MPU Read Timing

■ OPERATING PRINCIPLES & METHODS

◆ I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1 or CS2 is in active mode, input or output of data and instruction do not execute. Therefore internal state is not changed. But RSTB can operate regardless of CS1 and CS2.

◆ Input Register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display data RAM.

When CS1 or CS2 is in the active mode, R/W and RS select the input register. The data from MPU is written into input register and then write it into display data RAM. Data is latched when falling of the E signal and written automatically into the display data RAM by internal operation.

◆ Output Register

Output register stores the data temporarily from display data RAM when CS1 or CS2 is in active mode and R/W and RS=H. Stored data in display data RAM is latched in output register. When CS1 or CS2 is in active mode and R/W=H, RS=L, status data (busy check)can be read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read does not need dummy read.

RS	R/W	Function
0	0	Instruction
	1	Status read(busy cheek)
1	0	Data write(from input register to display data RAM
	1	Data read(from display data RAM to output register)

◆ Reset

System reset can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register becone set by 0.(Z-address 0)

While RSTB is low level, no instruction except status read can be accepted. Reset status appears at DB4. After DB4 is low, any instruction can be accepted.

The Conditions of power supply at initial power up are shown in table 1.

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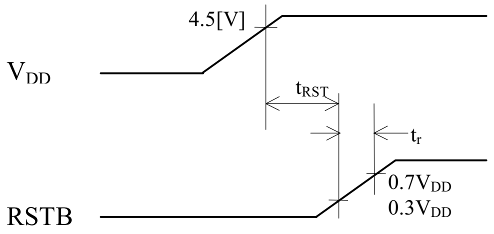
Table 1. Power Supply Initial Conditions

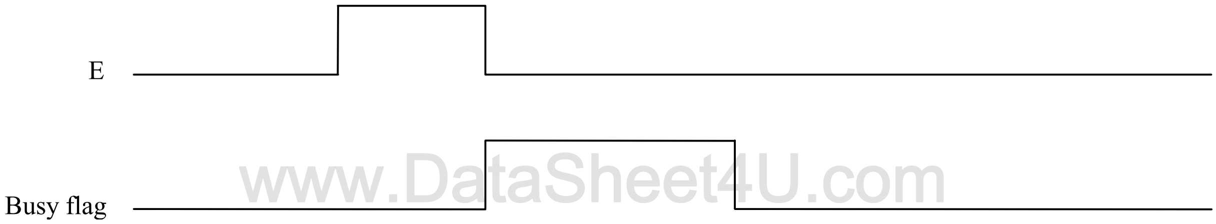
Item	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	---	---	us
Rise time	t_r	---	---	200	ns



◆ Busy Flag

Busy flag indicates that KS0108B is operating or not operating. When busy flag is high, KS0108B is in internal operating. When busy flag is low, KS0108B can accept the data or instruction.

DB7 indicates busy flag of the KS0108B.



◆ Display ON/OFF Flip-Flop

The display on/off flip-flop makes on/off of the liquid crystal display. When flip-flop is reset (logical low). selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logical high).non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can change status by instruction. The display data at all segment disappear while RSTB is low. The status of the flip-flop is output to DB5 by read instruction.

◆ X page Register

X page register designates page of the internal display data RAM. It has not count function. An address is set by instruction.

◆ Y Address Counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

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◆ Display Data RAM

Display data RAM stores a display data for liquid crystal display. To express on state of dot matrix of liquid crystal display. write data 1. The other way. off state writes 0.

◆ Display Start Line Register

The display start line register indicates address of display data RAM to display top line of liquid crystal display. Bit data (DB<0:5>) of the display start line set instruction is latched in display start line register. It is used for scrolling of the liquid crystal display screen.

◆ Display Control Instruction

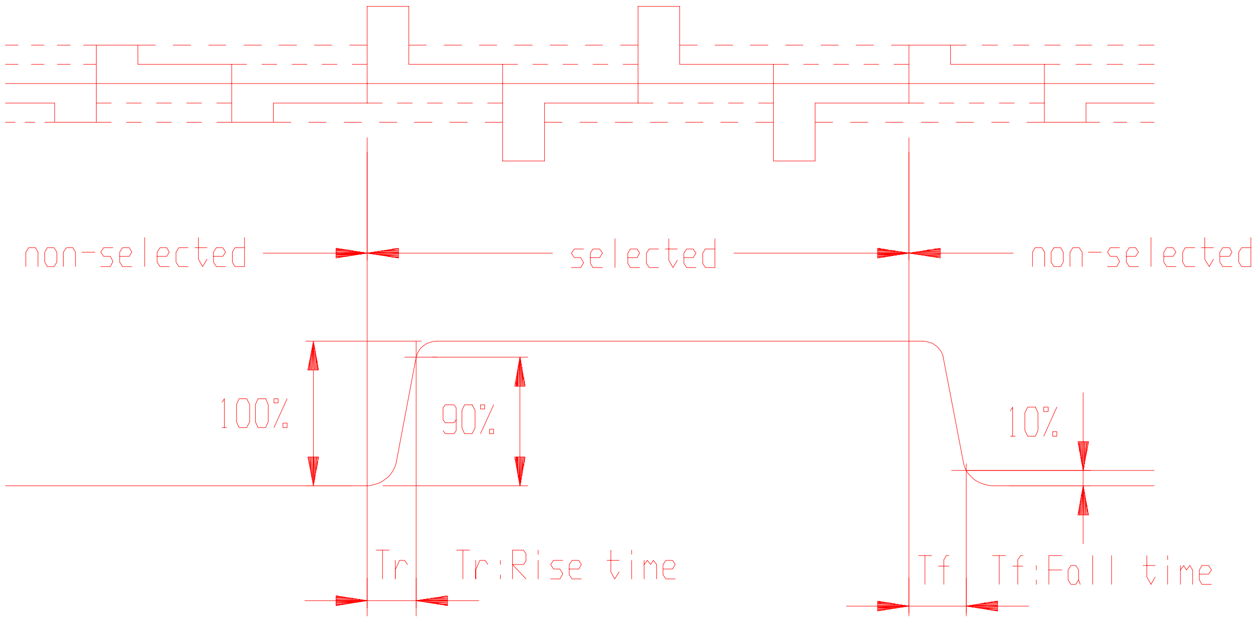
The display control instructions control the internal state of the KS0108B. Instruction is received fom MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Display ON/OFF	0	0	0	0	1	1	1	1	1	0/1	Controls the display on or off. Internal status and display RAM data are not affected. 0:OFF, 1:ON
Set Address	0	0	0	1	Y address (0~63)						Sets the Y address in the Y address counter.
Set Page (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the display data RAM displayed at the top of the screen.
Status Read	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0	Read status. BUSY 0 : Ready 1 : In operation ON/OFF 0 : Display ON 1 : Display OFF RESET 0 : Normal 1 : Reset
Write Display Data	1	0	Write Data								Writes data (DB0:7) into display data RAM. After writing instruction, Y address is increased by 1 automatically.
Read Display Data	1	1	Read Data								Reads data (DB0:7) from display data RAM to the data bus.

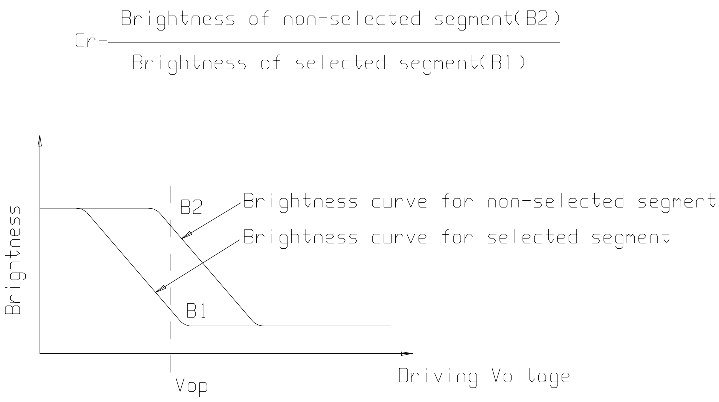
■ ELECTRO-OPTICAL CHARACTERISTICS (Vop = 10.0V, Ta = 25℃)

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response time	Tr	---	---	186	---	ms	---	1
	Tf	---	---	91	---	ms	---	1
Contrast ratio	Cr	---	---	12.7	---	---	---	2
Viewing angle range	θ	Cr ≥ 2	25	---	---	deg	∅ = 90°	3
			23	---	---	deg	∅ = 270°	3
			30	---	---	deg	∅ = 0°	3
			54	---	---	deg	∅ = 180°	3

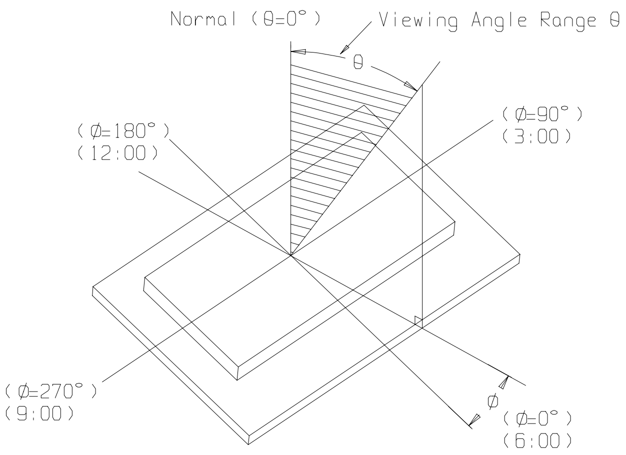
Note1: Definition of response time.


non-selected
selected
non-selected
100%
90%
10%
Tr
Tr:Rise time
Tf
Tf:Fall time

Note2: Definition of contrast ratio 'cr' .



Note3: Definition of viewing angle range 'θ'.


Normal (θ=0°)
Viewing Angle Range θ
θ
(∅=180°)
(12:00)
(∅=90°)
(3:00)
(∅=270°)
(9:00)
∅
(∅=0°)
(6:00)

■ INTERFACE PIN CONNECTIONS

Pin No.	Symbol	Level	Description
1	CS1	H	Chip select signal for KS0108B(1)
2	CS2	H	Chip select signal for KS0108B(2)
3	VSS	0V	Ground
4	VDD	5.0V	Supply voltage for logic
5	VO	---	Input voltage for LCD
6	RS	H/L	H : Data signal, L : Instruction signal
7	R/W	H/L	H : Read mode, L : Write mode
8	E	H, H → L	Chip enable signal
9	DB0	H/L	Data bit 0
10	DB1	H/L	Data bit 1
11	DB2	H/L	Data bit 2
12	DB3	H/L	Data bit 3
13	DB4	H/L	Data bit 4
14	DB5	H/L	Data bit 5
15	DB6	H/L	Data bit 6
16	DB7	H/L	Data bit 7
17	SLA	4.2V	Side light anode
18	SLK	0V	Side light cathode

■ PART LIST

Part Name	Description	Quantity
IC	KS0107B.PCC	1
IC	KS0108B.PCC	2
LCD	TSD0063-DYFDCN	1
PCB	MCG12864A8-3	1
Frame	MG12864-5B	1
Rubber connector	67×6.4×2.6mm YS	2
Heatal connector	6405	1
Resistor	3KΩ	4
Resistor	15KΩ	1
Resistor	10KΩ	1
Resistor	47KΩ	1
Capacitor	27pF±5%	1
Capacitor	0.1μF	1
LED PCB	LB12864A5-2	2
LED light	ED-011YGU	24