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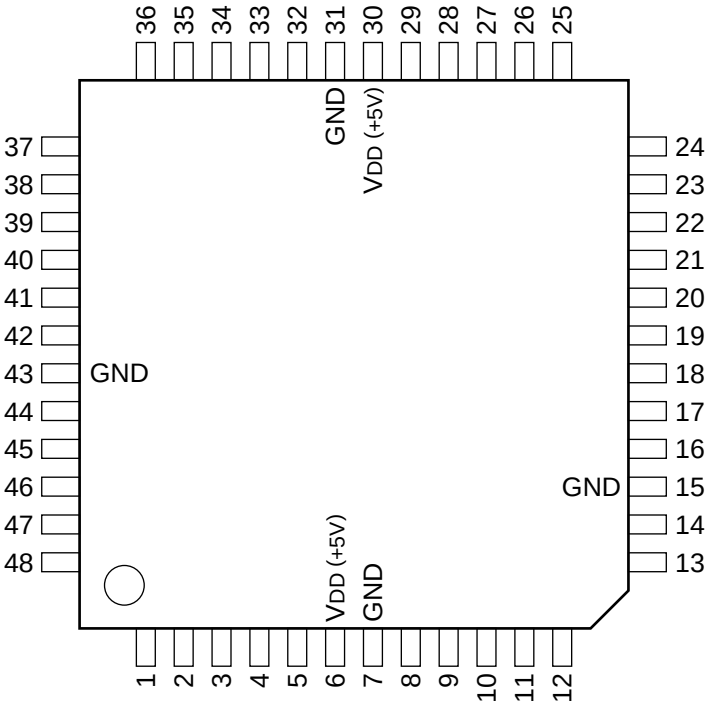
IL22

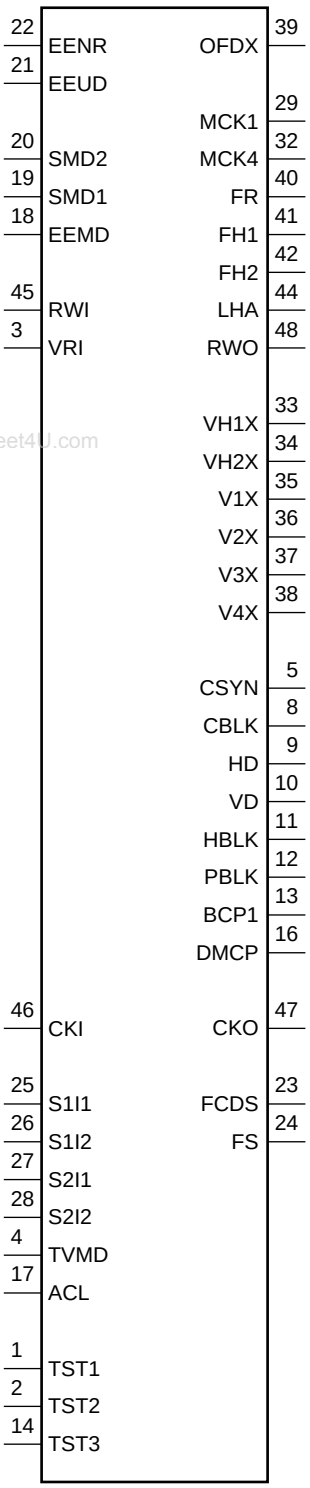
C-MOS GATE ARRAY LSI

-TOP VIEW-



(V_{DD} = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	TST1	13	O	BCP1	25	I	S1I1	37	O	V3X
2	I	TST2	14	I	TST3	26	I	S1I2	38	O	V4X
3	I	VRI	15	—	GND	27	I	S2I1	39	O	OFDX
4	I	TVMD	16	O	DMCP	28	I	S2I2	40	O	FR
5	O	CSYN	17	I	ACL	29	O	MCK1	41	O	FH1
6	—	V_{DD}	18	I	EEMD	30	—	V_{DD}	42	O	FH2
7	—	GND	19	I	SMD1	31	—	GND	43	—	GND
8	O	CBLK	20	I	SMD2	32	O	MCK4	44	O	LHA
9	O	HD	21	I	EEUD	33	O	VH1X	45	I	RWI
10	O	VD	22	I	EENR	34	O	VH2X	46	I	CKI
11	O	HBLK	23	O	FCDS	35	O	V1X	47	O	CKO
12	O	PBLK	24	O	FS	36	O	V2X	48	O	RWO



INPUT

ACL	;	AC ON INITIAL STATE SETTING
CKI	;	REFERENCE CLOCK
EEMD	;	ELECTRONIC SHUTTER CONTROL
EENR	;	SHUTTER SPEED SETTING
EEUD	;	SHUTTER SPEED SETTING
RWI	;	PHASE ADJUST (FR OUTPUT)
S1I1, S1I2	;	PHASE ADJUST (FCDS OUTPUT)
S2I1, S2I2	;	PHASE ADJUST (FS OUTPUT)
SMD1, SMD2	;	SHUTTER SPEED SETTING
TST1-TST3	;	TEST
TVMD	;	TELEVISION MODE SELECT
VRI	;	EXTERNAL V RESET

OUTPUT

BCP1	;	REF. BLACK LEVEL CLAMP COMPOSITE SIGNAL (AREA SENSOR OUTPUT)
CBLK	;	COMPOSITE BLANKING
CKO	;	REFERENCE CLOCK
CSYN	;	EIA, CCIR REFERENCE COMPOSITE SYNC
DMCP	;	DUMMY CLAMP CONTINUOUS HORIZONTAL PERIOD (AREA SENSOR OUTPUT)
FCDS	;	FEED SLEW CLAMP (AREA SENSOR OUTPUT)
FH1, FH2	;	AREA SENSOR HORIZONTAL TRANSLATE
FR	;	AREA SENSOR RESET
FS	;	SIGNAL SAMPLING (AREA SENSOR OUTPUT)
HBLK	;	AREA SENSOR HORIZONTAL TRANSLATE STOP = LOW
HD	;	HORIZONTAL SYNC
LHA	;	AREA SENSOR HORIZONTAL LAST GATE
MCK1, MCK4	;	PHASE ADJUST (FCDS, FS OUTPUT)
OFDX	;	AREA SENSOR ELECTRIC SWEEPING AND DUMPING
PBLK	;	PRE-BLANKING
RWO	;	FR PHASE ADJUST
V1X-V4X	;	VERTICAL TRANSLATE
VD	;	VERTICAL SYNC
VH1X, VH2X	;	PHOTO DIODE ELECTRIC VERTICAL SHIFT REGISTER TRANSLATE