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GENERAL INSTRUMENT | 28C64 | PRELIMINARY INFORMATION

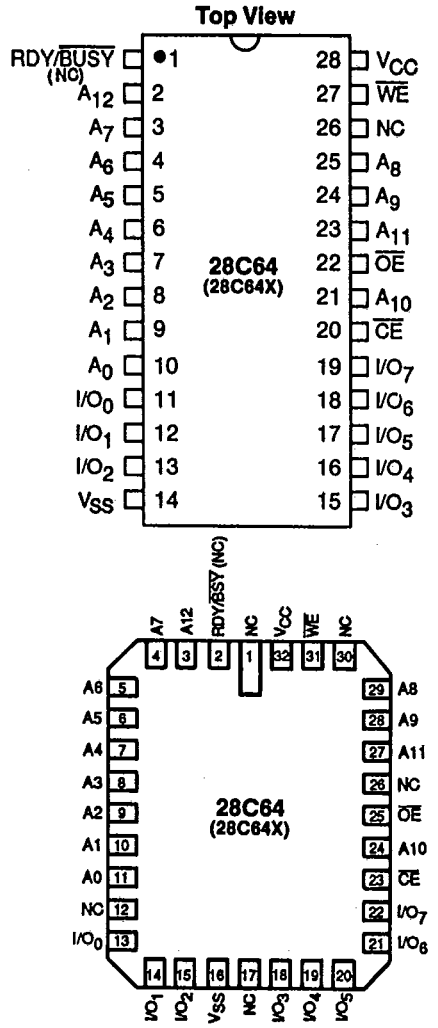
64K (8K x 8) CMOS Electrically Erasable PROM

FEATURES

- Fast Read Access Time — 150 ns
- High Performance CMOS Technology for Low Power Dissipation
  - — 100 μA Standby
  - — 30 mA Active
- Fast Byte Write Time — 200 μs or 1 ms
- High Endurance 10^5 Erase/Write Cycles
- Automatic Write Operation
  - — Internal Control Timer
  - — Auto-Clear Before Write Operation
  - — On-Chip Address and Data Latches
- $\overline{\text{DATA}}$ Polling
- Ready/$\overline{\text{BUSY}}$ (Open Drain)
- Chip Clear Function
- Enhanced Data Protection
  - — V_{CC} Detector
  - — Power-Up Timer
- Electronic Signature
  - — Device Identification
  - — Tracking
- Data Retention > 10 years
- 5-Volt Only Operation
- JEDEC-Approved Byte-Wide Pinout
  - — 28-Pin DIP
  - — 32-Pin LCC/PLCC
- Full Commercial and Industrial Temperature Ranges
  - — 0° to +70°C Commercial (28C64)
  - — -40° to +85°C Industrial (28C64I)
- Also available in military temperature range
  - — -55° to +125°C Military (28C64MR)

PIN CONFIGURATION

Top View



PIN NAMES

A_0 - A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_0 - I/O_7	DATA INPUTS/OUTPUTS
RDY/$\overline{BUSY}$	READY/BUSY
NC	NO CONNECT

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DESCRIPTION

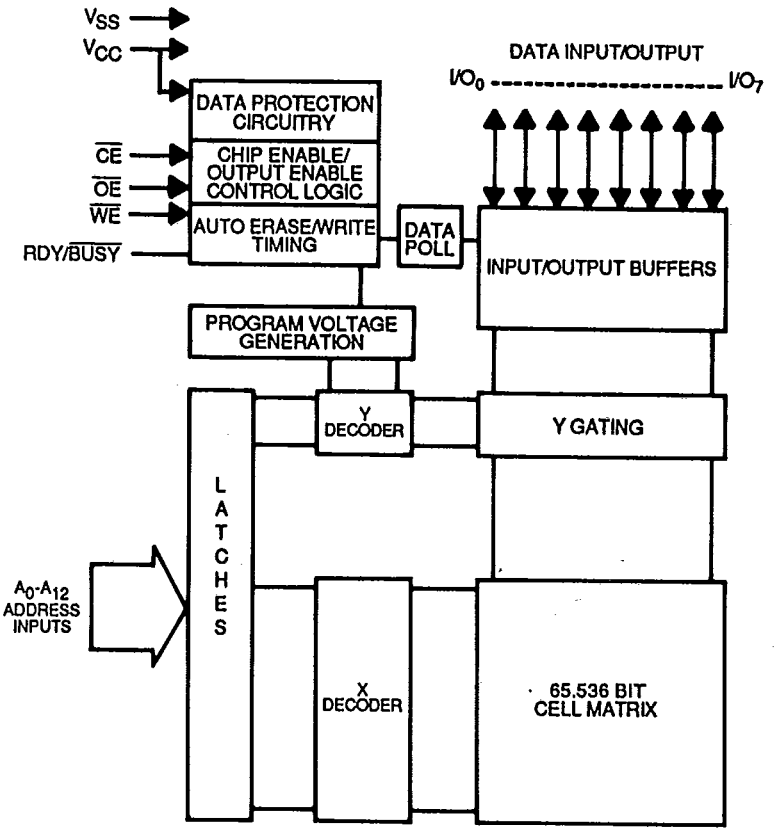
The General Instrument 28C64 is a low-power, high-performance 8,192 x 8 bit non-volatile Electrically Erasable and Programmable Read Only Memory with popular, easy to use features. The device is manufactured with General Instrument's advanced and reliable non-volatile CMOS technology.

The 28C64 is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer.

To determine when the write cycle is complete, the user has a choice of monitoring the Ready/$\overline{\text{Busy}}$ output or using $\overline{\text{DATA}}$ polling. The Ready/$\overline{\text{Busy}}$ pin is an open drain output, which allows easy configuration in wired-or systems. Alternatively, $\overline{\text{DATA}}$ polling allows the user to read the location last written to when the write operation is complete.

The 28C64 operates from a single 5V supply and is packaged in standard JEDEC-approved packages. All necessary programming voltages are internally generated and timed.

The CMOS technology offers fast access times of 150 ns (28C64-15) at low power dissipation of 30 mA. When the chip is deselected, the standby current is less than 100 μA. The 28C64's fast memory access time allows for direct polling with microprocessors without waiting.



FUNCTIONAL BLOCK DIAGRAM
28C64

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DEVICE OPERATION

The General Instrument 28C64 has four basic modes of operation — read, standby, write inhibit, and byte write — as outlined in the following table.

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Rdy/$\overline{Busy}$(1)
READ	L	L	H	D_{OUT}	H
STANDBY	H	X	X	High Z	H
WRITE INHIBIT	H	X	X	High Z	H
WRITE INHIBIT	X	L	X	—	H
WRITE INHIBIT	X	X	H	—	H
BYTE WRITE	L	H	L	D_{IN}	L
BYTE CLEAR	Automatic Before Each "Write"				

Note 1: Open Drain Output

READ MODE

The 28C64 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The 28C64 is placed in the standby mode by applying a high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

DATA PROTECTION

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (3.8 volts typical) will inhibit the initiation of a non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip. In addition, on power-up an internal timer (5 ms typical) will inhibit the recognition of any program operation. During this period, all normal read functions will be operational. After both the V_{CC} detection and the internal timer have elapsed, normal programming operation can be performed.

Second, there is a $\overline{WE}$ filtering circuit that prevents $\overline{WE}$ pulses of less than 20 ns duration from initiating a write cycle.

Third, holding $\overline{WE}$ or $\overline{CE}$ high, or $\overline{OE}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

WRITE MODE

The 28C64 has a write cycle similar to that of a Static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/$\overline{Busy}$ pin goes to a logic low level indicating that the 28C64 is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/$\overline{Busy}$ goes back to a high, the 28C64 has completed writing and is ready to accept another cycle.

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DATA POLLING

The 28C64 features DATA Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O_7 (I/O_0 to I/O_6 are indeterminable). After completion of the write cycle, true data is available. DATA polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DEVICE IDENTIFICATION

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 1FEO to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP CLEAR

All data may be cleared to 1s in a chip clear cycle by raising $\overline{OE}$ to 12 volts and bringing the $\overline{WE}$ and $\overline{CE}$ low. This procedure clears all data.

RETENTION ENDURANCE

Read retention for data written into the 28C64 is greater than 10 years, with up to 10^5 write cycles. There is no limit to the number of times data may be read.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Temperature under Bias ..... -10°C to +85°C (Industrial: -50°C to +95°C)
Storage Temperature ..... -65°C to +125°C
All Input Voltages with Respect to Ground ..... +6.25V to -0.6V
All Output Voltages with Respect to Ground ..... V_{CC} +0.6V to -0.6V
Voltage on OE with Respect to Ground ..... +13.5V to -0.6V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

28C64 T_A = 0°C to +70°C, V_{CC} = 5V ±10% unless otherwise specified.
28C64I T_A = -40°C to +85°C, V_{CC} = 5V ±10% unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage Current		10	µA	-0.1 to V_{CC}+1
I_{LO}	Output Leakage Current		10	µA	-0.1 to V_{CC}+0.1
I_{CC}	V_{CC} Current Standby		100 2 3	µA mA mA	$\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1 $\overline{CE}$ = V_{IH} (0°C to +70°C) $\overline{CE}$ = V_{IH} (-40°C to +85°C)
I_{CC}	V_{CC} Current Active		30	mA	f = 1 MHz
V_{IL}	Input Low Voltage	-0.1	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+1	V	
V_{OL}	Output Low Voltage		.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 µA

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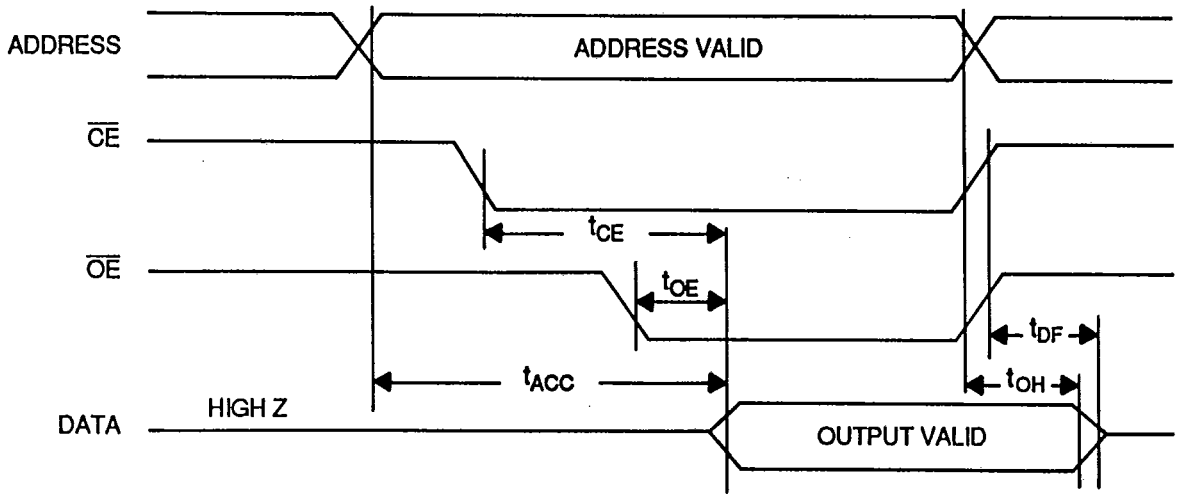
AC CHARACTERISTICS — READ CYCLE

SYMBOL	PARAMETER	28C64-15 MIN	28C64-15 MAX	28C64-20 MIN	28C64-20 MAX	28C64-25 MIN	28C64-25 MAX	UNITS	TEST CONDITIONS
t_{ACC}(1)	Address to Output Delay		150		200		250	ns	$\overline{OE} = \overline{CE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250	ns	$\overline{OE} = V_{IL}$
t_{OE}	$\overline{OE}$ to Output Delay		70		80		120	ns	$\overline{CE} = V_{IL}$
t_{DF}(2,3)	$\overline{OE}$ High to Output Float	0	50	0	55	0	70	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first.		10		10		10	ns	$\overline{CE} = \overline{OE} = V_{IL}$



Notes:

1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. This parameter is only sampled and is not 100% tested.
3. t_{DF} is specified from $\overline{OE}$ to $\overline{CE}$, whichever occurs first.

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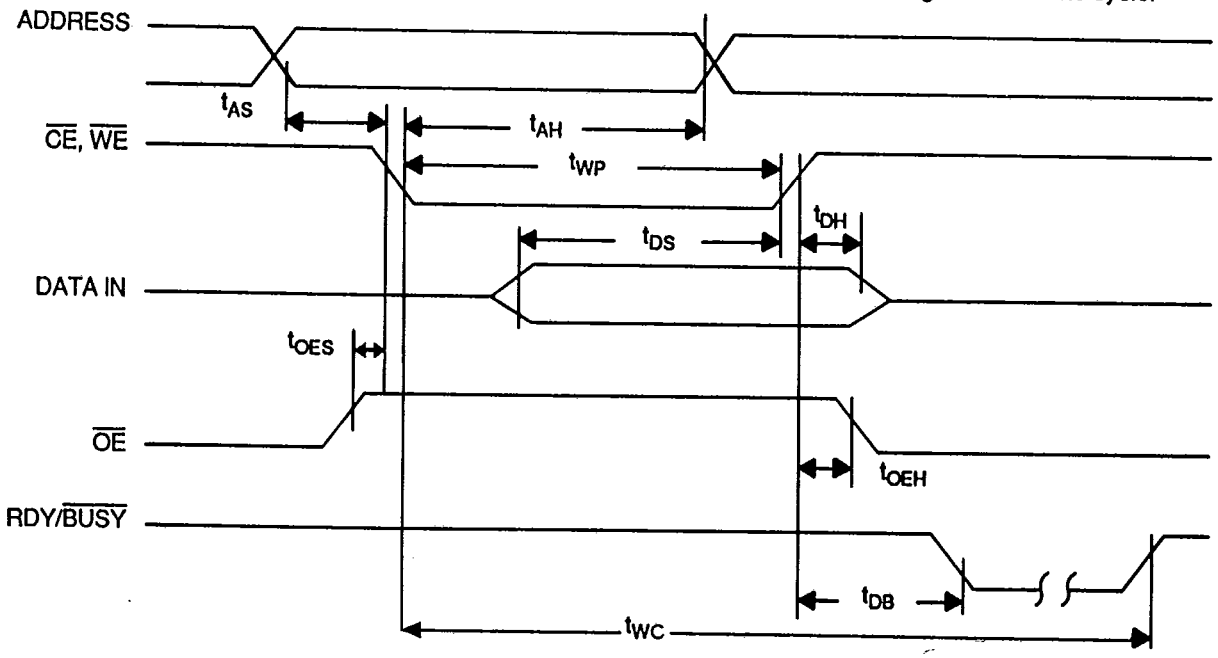
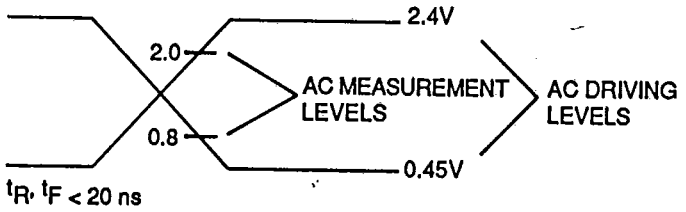
AC CHARACTERISTICS — BYTE WRITE

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
t_{AS}	Address, Setup Time	10		ns	
t_{AH}	Address, Hold Time	50		ns	
t_{WP}	Write Pulse Width	100	1000	ns	(1)
t_{DS}	Data Setup Time	50		ns	
t_{DH}	Data Hold Time	10		ns	
t_{DB}	Time to Device Busy		50	ns	
t_{OEH}	$\overline{OE}$ Hold Time	10		ns	
t_{OES}	$\overline{OE}$ Setup Time	10		ns	
t_{WC}	Write Cycle Time 28C64		1	ms	Typically 0.5 ms
	28C64F		200	μs	Typically 100 μs

Note 1: If t_{WP} is extended more than the maximum limit, data must be held valid throughout the write cycle.



AC TESTING, INPUT AND OUTPUT WAVEFORMS



AC testing inputs are driven at 2.4V AC for a Logic 1 and 0.45V for a Logic 0. Timing measurements are made at 2.0V for a Logic 1 and 0.8V for a Logic 0.

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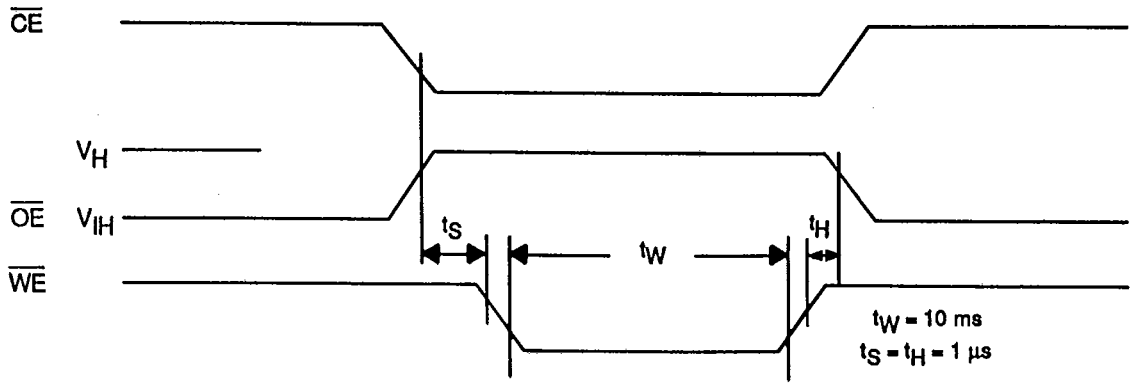
CHIP CLEAR



SUPPLEMENTARY CONTROL

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_I	V_{CC}	I/O_I
Chip Clear	V_{IL}	V_H		X	V_{CC}	
Extra Row Read	V_{IL}	V_{IL}	V_{IH}	A9 = V_H	V_{CC}	Data Out
Extra Row Write		V_{IH}		A9 = V_H	V_{CC}	Data In

$V_H = 12.0 \pm 0.5$ volts.

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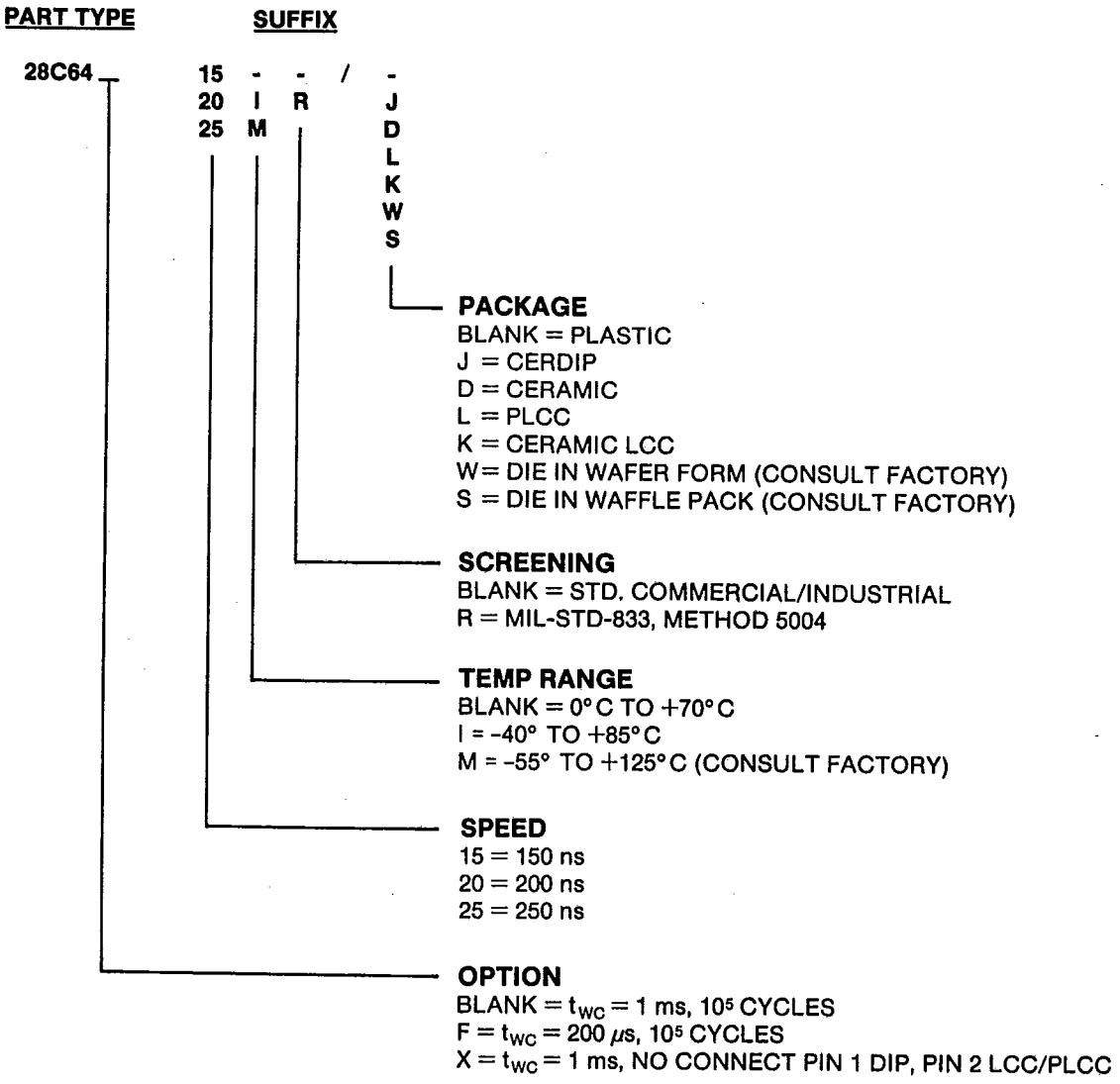
ORDERING INFORMATION



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