DATA SHEET

SPMC75F2413A

16-bit MCU with
Two Channels Motor Controller

Feb. 16, 2006

Version 1.1

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16-BIT MCU WITH TWO CHANNELS MOTOR CONTROLLER

1. GENERAL DESCRIPTION

The SPMC75F2413A, a 16-bit architecture product, carries the newest 16-bit microprocessor, *μ'nSP*™ (pronounced as *micro-n*-SP), developed by Sunplus Innovation Technology. The high processing speed assures the *μ'nSP*™ is capable of handling complex digital signal processes easily and rapidly. The memory capacity includes 32K-word flash memory plus a 2K-word working SRAM. Also, a 2-channel motor driver is incorporated which can drive two BLDC (Brushless DC) or AC induction motors simultaneously. Other features include PLL, 64 programmable multi-functional I/Os, UART, SPI, five 16-bit general-purpose timers, two compare match timers, low voltage reset, 8-ch 10-bit ADC input and many others. The device is suitable for home appliances with motors, such as air conditioners, washing machines, or refrigerators.

2. FEATURES

- SunplusIT 16-bit *μ'nSP* processor (ISA 1.2)
- Operating voltage:
  - 4.5V ~ 5.5V
- Operating speed: 12~24MHz
- Operating temperature: -40℃~85℃
- On-chip Memory
  - 32KW (32K*16) Flash
  - 2KW (2K*16) SRAM
- Clock for system operation
  - Crystal oscillator, On-chip PLL and external clock for clock generation
  - Monitoring for clock failed
- Power management
  - 2 power-down modes: Wait/Standby
  - Each peripheral can be powered down independently
- Up to 38 interrupt sources
- Up to 6 reset status flag
- Up to 64 GPIO pins
- Twelve 16-bit motor drive PWM outputs (MCP)
  - 2-channel motor drive PWM outputs (3-phase 6-pin complementary PWM outputs)
  - Center- or Edge-aligned PWM outputs
  - PWM overload protection with external OL1/OL2 input pins
  - Emergency PWM outputs shutdown with external fault protection pins
  - Programmable dead-time control
  - PWM service and fault interrupt generation
  - Capable of driving AC induction and BLDC motors
- Five 16-bit general-purpose timers (TPM)
  - Timer 0/1 each supports 3-channel Capture/Compare/PWM function
  - Timer 2 supports 2-channel Capture/Compare/PWM function
  - Timer 3/4 supports motor drive PWM function
- Two Compare Match Timers
- One Timebase timer
- 10-bit analog-to-digital converter
  - 8 multiplexed input channels
  - 10μs (100kHz) conversion time
  - Support top reference voltage input
- Serial communication interface
  - UART
  - SPI
- Watchdog timer
- Embedded In-Circuit-Emulation Circuit

3. BLOCK DIAGRAM

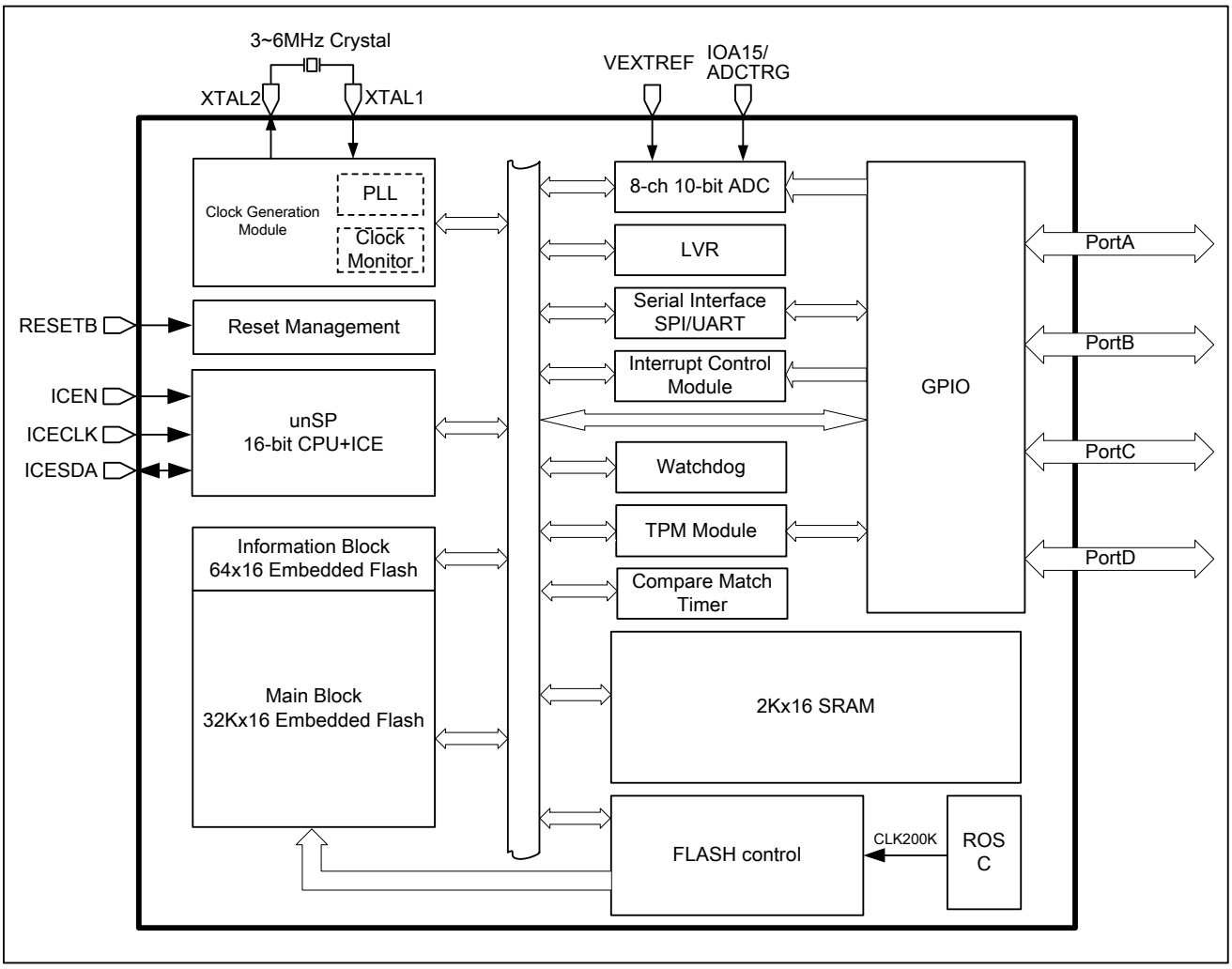


Figure 3-1 SPMC75F2413A function block diagram

4. SIGNAL DESCRIPTIONS

4.1. Pin Descriptions

4.1.1. 80-Pin QFP/ 64-Pin QFP package signals description

Mnemonic	PIN No		Type	Description
	QFP80	QFP64		
ICEN	1	1	I (PL)	ICE/Program or Normal mode control
ICECLK	2	-	I/O	ICE serial clock input (3V IO)
ICESDA	3	-	I/O	ICE serial address/data input/output (3V IO)
IOD0/ICECLK	4	2	I/O	IOD0 or ICE serial clock input (for QFP64 package)
IOD1/ICESDA	5	3	I/O	IOD1 or ICE serial address/data input/output (for QFP64 package)
IOD2	6	4	I/O	IOD2
RESETB	7	5	I (PH)	External reset
IOD3	8	6	I/O	IOD3
NC	9	-	-	No Connection
NC	10	-	-	No Connection
IOB0/TIO3F/W1N	11	7	I/O	IOB0 or TPM channel 3 input/output F or motor drive W1N phase output
IOB1/TIO3E/V1N	12	8	I/O	IOB1 or TPM channel 3 input/output E or motor drive V1N phase output
IOB2/TIO3D/U1N	13	9	I/O	IOB2 or TPM channel 3 input/output D or motor drive U1N phase output
IOB3/TIO3C/W1	14	10	I/O	IOB3 or TPM channel 3 input/output C or motor drive W1 phase output
IOB4/TIO3B/V1	15	11	I/O	IOB4 or TPM channel 3 input/output B or motor drive V1 phase output
IOB5/TIO3A/U1	16	12	I/O	IOB5 or TPM channel 3 input/output A or motor drive U1 phase output
IOB6/FTIN1	17	13	I/O	IOB6 or external fault protection input 1
IOB7/OL1	18	14	I/O	IOB7 or overload protection input 1
IOB8/TIO0C	19	15	I/O	IOB8 or TPM channel 0 input/output C
IOB9/TIO0B	20	16	I/O	IOB9 or TPM channel 0 input/output B
IOB10/TIO0A	21	17	I/O	IOB10 or TPM channel 0 input/output A
IOB11/SCK	22	18	I/O	IOB11 or SPI clock input/output
IOB12/SDI/RXD1	23	19	I/O	IOB12 or SPI data input or UART receive data input 1
IOB13/SDO/TXD1	24	20	I/O	IOB13 or SPI data output or UART transmit data output 1
IOB14	25	21	I/O	IOB14
IOB15	26	22	I/O	IOB15
IOD12	27	-	I/O	IOD12
IOD13	28	-	I/O	IOD13
IOD14	29	-	I/O	IOD14
IOD15	30	-	I/O	IOD15
IOA8	31	23	I/O	IOA8
IOA9/TIO2A	32	24	I/O	IOA9 or TPM channel 2 input/output A
IOA10/TIO2B	33	25	I/O	IOA10 or TPM channel 2 input/output B
IOA11/TCLKA	34	26	I/O	IOA11 or external clock A input
IOA12/TCLKB	35	27	I/O	IOA12 or external clock B input
IOA13/TCLKC	36	28	I/O	IOA13 or external clock C input
IOA14/TCLKD	37	29	I/O	IOA14 or external clock D input
IOA15/ADCTRG	38	30	I/O	IOA15 or A/D converter external trigger to start a conversion
VDD	39	31	P	5V power input for IO and built-in regulator
VSS	40	32	P	Ground for IO

Mnemonic	PIN No		Type	Description
	QFP80	QFP64		
IOA0/AN0	41	33	I/O	IOA0 or analog input channel 0 of ADC
IOA1/AN1	42	34	I/O	IOA1 or analog input channel 1 of ADC
IOA2/AN2	43	35	I/O	IOA2 or analog input channel 2 of ADC
IOA3/AN3	44	36	I/O	IOA3 or analog input channel 3 of ADC
IOA4/AN4	45	37	I/O	IOA4 or analog input channel 4 of ADC
IOA5/AN5	46	38	I/O	IOA5 or analog input channel 5 of ADC
IOA6/AN6	47	39	I/O	IOA6 or analog input channel 6 of ADC
IOA7/AN7	48	40	I/O	IOA7 or analog input channel 7 of ADC
VEXTREF	49	41	I	ADC top voltage reference
AVSS	50	42	P	Analog ground for ADC
AVDD	51	43	P	Analog power for ADC
VDDL	52	44	P	External capacitance pin for internal step-down regulator/Digital power
XTAL1	53	45	I	External 3-6MHz crystal input for crystal oscillator
XTAL2	54	46	O	External 3-6MHz crystal output / External clock input
VSSL	55	47	P	Digital ground
IOD4	56	48	I/O	IOD4
IOD5	57	-	I/O	IOD5
IOD6	58	-	I/O	IOD6
IOD7	59	-	I/O	IOD7
IOD8	60	-	I/O	IOD8
IOD9	61	-	I/O	IOD9
IOD10	62	-	I/O	IOD10
IOD11	63	-	I/O	IOD11
NC	64	-	-	No connection
IOC0/RXD2	65	49	I/O	IOC0 or UART receive data input 2
IOC1/TXD2	66	50	I/O	IOC1 or UART transmit data output 2
IOC2/EXINT0	67	51	I/O	IOC2 or external interrupt input 0
IOC3/EXINT1	68	52	I/O	IOC3 or external interrupt input 1
IOC4/BZO	69	53	I/O	IOC4 or buzzer output
IOC5/TIO1A	70	54	I/O	IOC5 or TPM channel 1 input/output A
IOC6/TIO1B	71	55	I/O	IOC6 or TPM channel 1 input/output B
IOC7/TIO1C	72	56	I/O	IOC7 or TPM channel 1 input/output C
IOC8/OL2	73	57	I/O	IOC8 or overload protection input 2
IOC9/FTIN2	74	58	I/O	IOC9 or external fault input 2
IOC10/TIO4A/U2	75	59	I/O	IOC10 or TPM channel 4 input/output A or motor drive U2 phase output
IOC11/TIO4B/V2	76	60	I/O	IOC11 or TPM channel 4 input/output B or motor drive V2 phase output
IOC12/TIO4C/W2	77	61	I/O	IOC12 or TPM channel 4 input/output C or motor drive W2 phase output
IOC13/TIO4D/U2N	78	62	I/O	IOC13 or TPM channel 4 input/output E or motor drive U2N phase output
IOC14/TIO4E/V2N	79	63	I/O	IOC14 or TPM channel 4 input/output E or motor drive V2N phase output
IOC15/TIO4F/W2N	80	64	I/O	IOC15 or TPM channel 4 input/output F or motor drive W2N phase output

Legend: I = Input, O = Output, P = Power, PL = Pull-low, PH = Pull-high

4.2. Pin Assignment

4.2.1. 80-Pin QFP Package

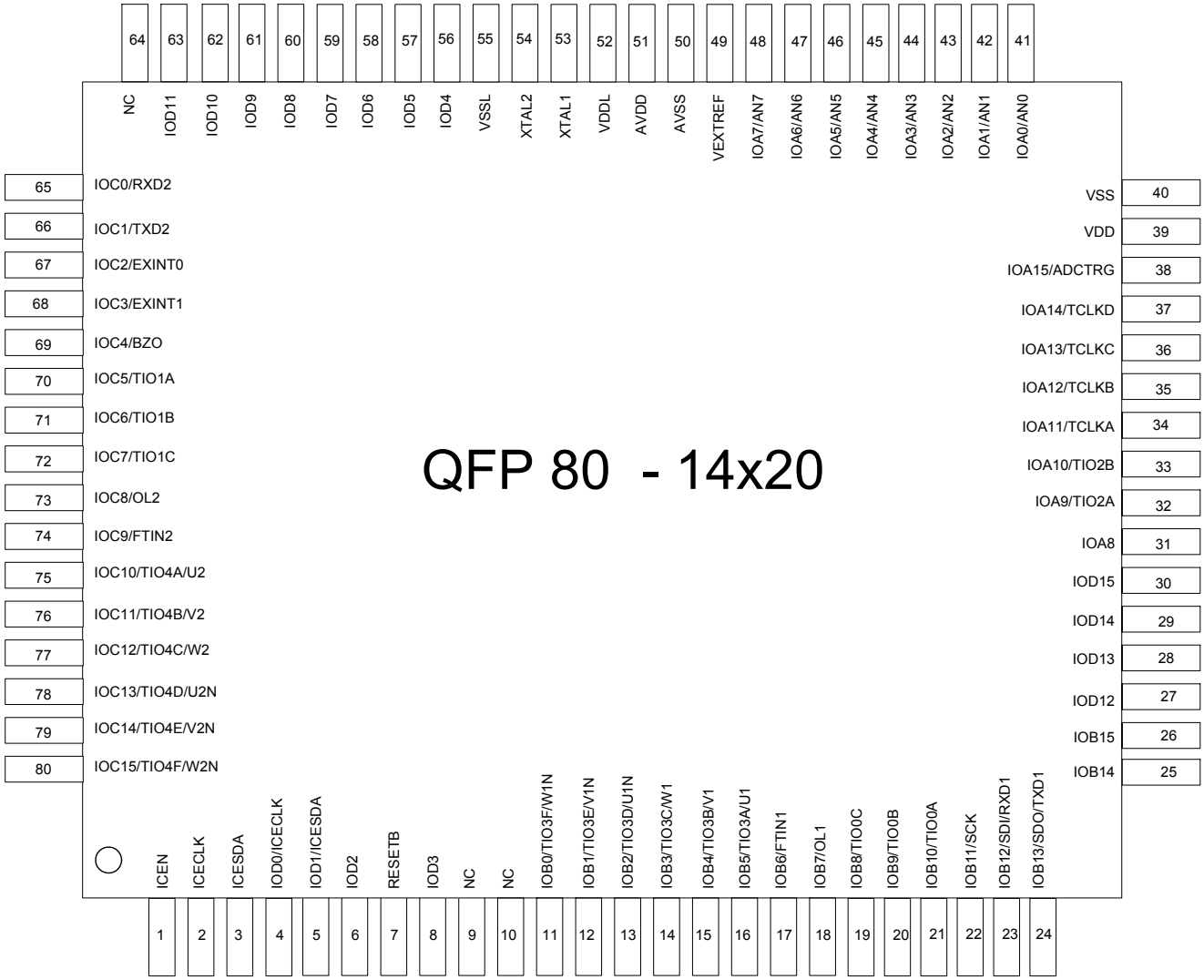


Figure 4-1 SPMC75F2413A QFP80 package

4.2.2. 64-Pin QFP Package

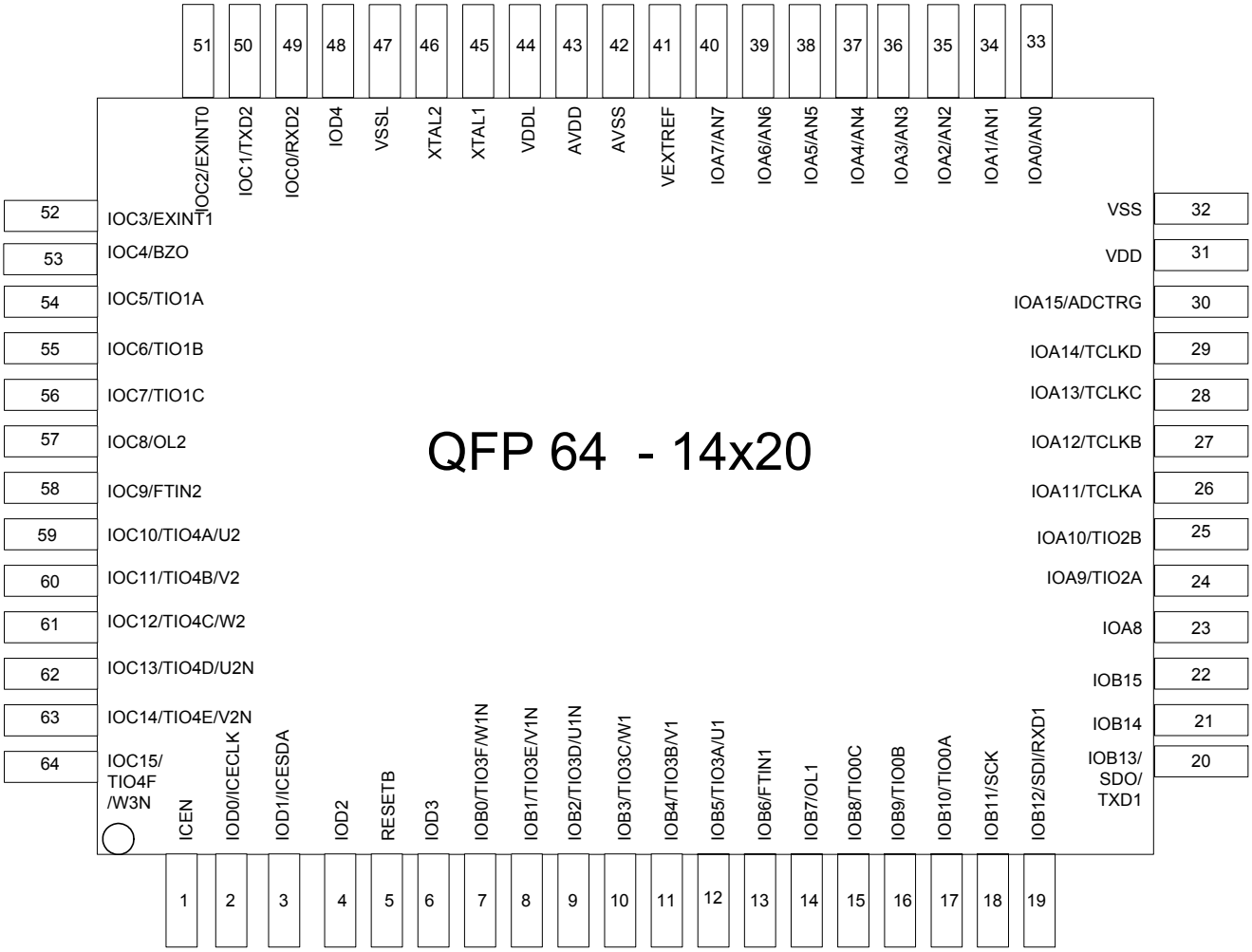


Figure 4-2 SPMC75F2413A QFP64 package

5. FUNCTIONAL DESCRIPTIONS

5.1. CPU Core

The SPMC75F2413A consists the newest 16-bit microprocessor, *μ'nSP*™ (pronounced as *micro-n*-SP), developed by Sunplus Innovation Technology. The CPU features include:

- 16-bit data bus / 22-bit address bus
  - 4M words (8M bytes) memory space
  - 64 banks / 64k words per bank
- Thirteen 16-bit registers
  - 5 general registers (R1-R5)
  - 4 secondary registers (SR1-SR4)
  - 3 system registers (SP, SR, PC)
  - Inner registers (FR)
- Ten interrupts
  - 1 fast interrupt (FIQ)
  - 8 normal interrupts (IRQ0-IRQ7)
  - 1 software interrupt (BRK)
  - Support IRQ nested mode
- Six addressing modes
  - Immediate (I6/I16)
  - Direct (A6/A16)
  - Indirect+ auto indexing address (DS indirect)
  - Relative (BP+IM6)
  - Multiple indirect (PUSH/POP)
  - Register
- 16x16 multiplication & up to 16-level inner product operation
  - Three multiplication mode: signed x signed, signed x unsigned, unsigned x unsigned
  - 4 bits guard bit of inner product operation to avoid overflow
  - Integer/Fraction mode
- 1-bit division
  - DIVS: divide the sign bit; DIVQ: divide the quotient
  - Divide 32-bit numerator and a 16-bit denominator
- Effective-exponent detect operation (EXP)
- Bit operation
  - Bit test / set / clr / inv operation to full memory space or registers
- Multi-cycles 16-bit shift operation
  - Support 32-bit shift with combining 2 shift instructions
- Far Indirect JMP by MR register
- Far Indirect Call by MR register
- NOP operation
- DS segment access instructions
- CPU inner flags access instructions

5.2. Memory Organization

5.2.1. Memory Map

The device contains 32KW flash and 2KW SRAM. The memory space can be separated into three blocks: SRAM, I/O port registers, and flash. The SRAM is used for stack, variable or data storage. The I/O port register is used to control the peripheral modules. The embedded flash is designed for programming code. The block diagram of memory is shown as Figure 5-1. Table 5-1 shows the detailed memory allocation.

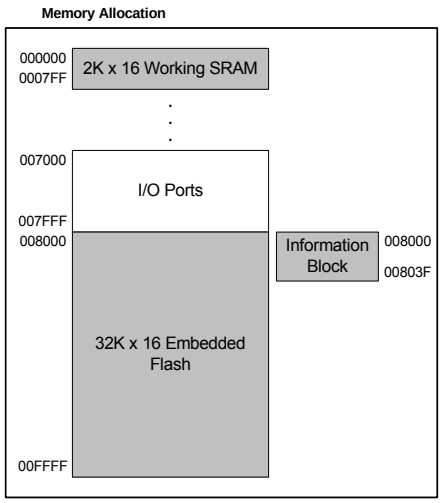


Figure 5-1 Memory allocation

Note: The address of 000800 – 006FFF and 010000 – 3FFFFF is reserved and cannot be accessed. An IAR (Illegal Address Reset) will be generated if CPU reads or writes these addresses.

Table 5-1 Detailed Address Mapping

I/O Address (Hex)	Mapping
0000~07FF	2KW SRAM
0800~6FFF	Illegal
7000~701F	System Control
7020~704F	Memory Control
7050~705F	Reserved
7060~709F	I/O Port Control
70A0~70AF	Interrupt Control
70B0~70BF	Time Base Control
70C0~70DF	Timer Control
70E0~70FF	Reserved
7100~711F	UART Control
7120~713F	Reserved
7140~715F	SPI Control
7160~73FF	Reserved
7400~747F	Timer/PWM Module Control (for motor control)
7500~751F	Compare Match Timer Control
7600~7FFF	Illegal
8000~FFFF	32KW Program ROM
10000~ 3FFFFF	Illegal

5.2.2. Flash Organization and Control

5.2.2.1. Introduction

The SPMC75F2413A has two flash blocks: information block and normal block. Only one of the two blocks can be addressed at the same time. The information block contains 64 words. The address of information block is mapped from 0x8000 ~ 0x803F. The 0x8000 is a system option register P_System_Option. The other addresses are used for storing important information such version control, date, vender name, project name etc. The information block's structure is in Figure 5-2 and they only can be written in ICE mode or by writer. The 32K words of normal block are partitioned into 16 banks, 2K words each. Except the bank between 0xF000 and 0xF7FF can be programmed to be read-only or read-write in free run mode independently, the others are read-only bank. Moreover, each 2K-word bank can also be separated by eight frames so that the 32K embedded flash can be divided to 128 frames. The user can erase each frame separately. The relation of page and frame of flash is shown in Figure 5-3.

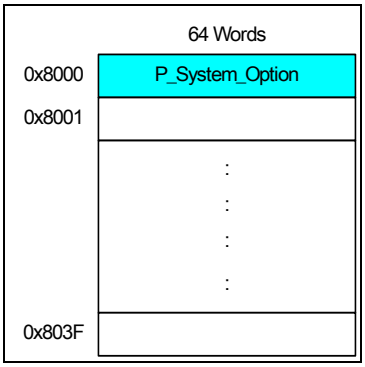


Figure 5-2 Structure of Information block

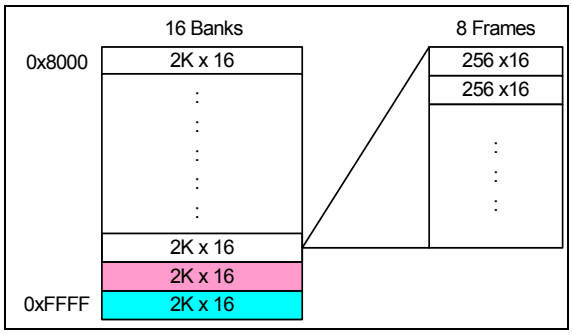


Figure 5-3 Page0 and frame of flash

5.2.2.2. Flash Operation

There are two registers for flash control: P_Flash_RW (0x704D) and P_Flash_Cmd (0x7555). The flash access control, P_Flash_RW (0x704D), can be configured by two consecutive write cycles, keeping away from inadvertent writing. First, write 0x5a5a to P_Flash_RW, and then write the configuration data to P_Flash_RW within 16 clock cycles.

The flash command register, P_Flash_Cmd, is a write only register that is for accepting/performing flash command. Before performing any commands, users should write 0xAAAA to P_Flash_Cmd for entering flash command mode at first. Table 5-2 shows the command and access flow.

Remarkably, the characteristic of flash is that the data bit can only be programmed from 1 to 0, but it is not allowed to be from 0 to 1. Therefore, if users intend to program flash, the frame erase instruction must be executed first, which erase data bit from 0 to 1.

【**Example 6-1**】: Set bank14 as read-only mode

```
#define   CW_FlashRW_CMD              0x5A5A          //Flash RW Command
#define   CB_BK14WDIS                 (0x4000 >> 14)
P_Flash_RW->W = CW_FlashRW_CMD;                       /* Flash Read Write Command */
P_Flash_RW->B.BK14WENB = CB_BK14WDIS;                 /* Set Bank 14 as Read Only */
```

Listing 6-1 read-only mode for bank 14 of flash memory

Table 5-2 Command function and access flow

	Frame Erase	**Program Mode**	**Sequential Program Mode**
1 cycle	P_Flash_Cmd = **0xAAAA**		
2 cycle	[P_Flash_Cmd] = **0x5511**	[P_Flash_Cmd] = **0x5533**	[P_Flash_Cmd] = **0x5544**
3 cycle	Set Frame Address	Write Data	Write Data
4 cycle	Write any data and wait 20ms End ─ Auto	Wait 40us End ─ Auto	Wait 40us ─ Auto
			Go to 2 cycle
			[P_Flash_Cmd]= **0xFFFF** → Go to End

【**Example 6-2**】: Example for frame erasing:

```
#define  CW_FlashCMD                0xAAAA          //Flash Command FLash   Block
#define  CW_PageErase               0x5511          //Flash Page Erase Command
unsigned int *P_WordAdr;
P_Flash_Cmd->W = CW_FlashCMD;
P_Flash_Cmd->W = CW_PageErase;
P_WordAdr   = (unsigned int *)0xF000;              /* P_WordAdr = start address of bank 14 */
*P_WordAdr = 0;                                    /* Write any data to erase the first frame of bank 14 */
```

Listing 6-2 frame erasing of flash memory

【**Example 6-3**】: Example for program mode: Write 0x1234 to the address of 0xF000

```
#define CW_FlashCMD                0xAAAA          //Flash Command FLash   Block
#define CW_Program                 0x5533          //Flash Program Command
unsigned int *P_WordAdr;
P_Flash_Cmd->W = CW_FlashCMD;
P_Flash_Cmd->W = CW_Program;
P_WordAdr = (unsigned int *)0xF000;                /* P_WordAdr = start address of bank 14 */
*(unsigned int *)P_WordAdr = 0x1234;               /* program one word = 0x1234 */
```

Listing 6-3 program mode of flash memory

【**Example 6-4**】 Example for sequential program mode: Write data to flash with sequential program mode, address is from 0xF000 to 0xF020.

```
#define CW_FlashCMD                0xAAAA          //Flash Command FLash   Block
#define CW_Sequential              0x5544          //Flash Sequential Program Command
#define CW_SequentialEnd           0xFFFF          //Flash Sequential Program End Command
unsigned int *P_WordAdr;
unsigned int i,uiData=1;
P_Flash_Cmd->W = CW_FlashCMD;

for(i=0xF000;i<=0xF020;i++)
{
    P_Flash_Cmd->W = CW_Sequential;
    P_WordAdr = (unsigned int *)i;                 // program address is the content of i
    *(unsigned int *)P_WordAdr = uiData;           // program uiData to P_WordAdr
     uiData ++;
}/* End For Loop */

P_Flash_Cmd->W = CW_SequentialEnd;
```

Listing 6-4 sequential program mode of flash memory

- **P_Flash_RW (0x704D): Embedded Flash Access Control Register**

The flash access control, P_Flash_RW, exclusively sets up banks14 with read only or full access in free run mode. This port can be configured by two consecutive write cycle to keep away from inadvertent writing. First, write 0x5A5A to P_Flash_RW, and then write configuration data to P_Flash_RW in duration of less than 16 clock cycles.

B15	B14	B13	B12	B11	B10	B9	B8
R	R/W	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved	BK14WENB	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
1	1	1	1	1	1	1	1
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

B15	Reserved			
B14	BK14WENB	F000h-F7FFh access control	0= Read/write	1= Read-only
B13-0	Reserved			

- **P_Flash_Cmd (0x7555): Embedded flash command register**

This port is used to issue flash command. Before performing any commands, users should write 0xAAAA to P_Flash_Cmd for entering flash command mode at first. Please see the Table 5-2.

B15	B14	B13	B12	B11	B10	B9	B8
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
FlashCmd							

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
FlashCmd							

- **P_System_Option (0x8000): System Option Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	1	0	1	0	1
Verification Pattern							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	0	1	0	1	1	1
Verification Pattern			SCB	Reserved	LVR	WDG	CLKS

B15-5	Verification Pattern	ICE or Writer will write 01010101010 to this area		
B4	SCB	Security enable, active low	0: Security enabled, the normal block in the flash cannot be accessed	1: Security disabled, can be readable or write-able
B3	Reserved			
B2	LVR	Enable low voltage reset function	0: Disable	1: Enable
B1	WDG	Enable watchdog function	0: Disable	1: Enable

B0	CLKS	Clock Source Selection	0: external clock input, connect an oscillator or clock source to XTAL2.	1: crystal oscillator, connect a crystal device between XTAL1 and XTAL2.

The “mass erase” command execute on main block is to erase main block only, but erase main block and information block if the command execute on information block. In case of security option in information block is enabled, SPMC75F2413A are protected from reading data through ICE or Writer function. If the security is enabled on under ICE enable mode, the flash main block does not allow to be read/write but information block can be read by ICE and the only command that user can perform is “mass erase”. In addition, SRAM cannot be accessed (read/write) in ICE enable mode. Please refer to Table 5-3 for detail.

In normal operation (ICEN = 0), CPU can access the flash data and the working SRAM. The ICE cannot program the flash memory when the ICE mode is activated and security is enabled. This hardware protection prevents hackers from downloading a program to flash or SRAM then write source code out to GPIOs. Table 5-3 shows Flash and SRAM access table.

Table 5-3 Flash/SRAM access table in normal and ICE mode

Normal mode(ICEN=0)				
	SCB =0		SCB =1	
	Read	**Write**	**Read**	**Write**
SRAM	Yes	Yes	Yes	Yes
FLASH main block	Yes	Yes	Yes	Yes
FLASH information block	Yes	No	Yes	No
ICE mode(ICEN=1)				
SRAM	No	No	Yes	Yes
FLASH main block	No	No (but mass erase)	Yes	Yes
FLASH information block	No	No (but mass erase)	Yes	Yes

5.2.2.3. Power-up procedure

When power is turned on, option bits are read by the system. The option bits are stored in the first word of embedded flash information block (address = 0x8000). When power is turned on, the system reset is activated until the power-on-timer counts 16384 cycles of 200KHz clock then, reset signal is released. Remarkably, all GPIO is on the high impedance state initially and can be configured after power-on procedure.

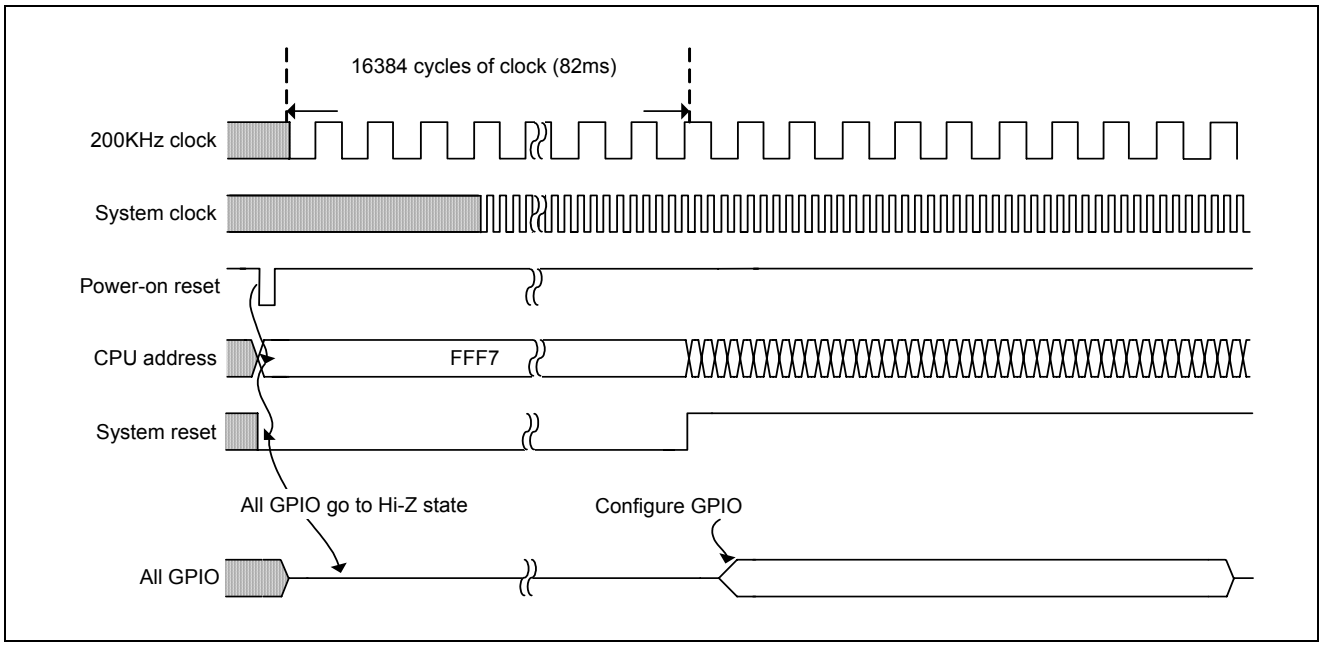


Figure 5-4 Power-up procedure

5.2.3. SRAM

The SRAM can be used for stack, variable and data storage. Stack is used for storing the return address of function call and pushing instruction data. The direction of stack goes from bottom to up. This stack is a FILO (first in last out) structure, and the stack address is indicated by stack pointer (SP).

The variable and data storage is configured by the user. Users can use direct access, indirect access or base pointer (BP) to load or save SRAM data. Note that the stack and variable or storage data must not overlap each other; otherwise, CPU will run into an unknown state. The SPMC75F2413A addresses maximum 2K-word SRAM. The address range is from 0x0000 to 0x07FF. In addition, the stack pointer (SP) is allocated at the end of maximum address initially, i.e. 0x07FF.

5.2.4. Reset and Interrupt Vectors

Addresses 0xFFF5 to 0xFFFF are reserved for reset and interrupt vectors. A reset forces the program counter (PC) points to address 0xFFF7. When a device reset occurs, the program execution will branch to 0xFFF7, named “Reset Vector Address”. The SPMC75F2413A has 10 interrupts. The address and function name list are given in the following table.

Table 5-4 Interrupts vectors list

Reset or IRQ vector	Address
BRK	0xFFF5
FIQ	0xFFF6
Reset	0xFFF7
IRQ0	0xFFF8
IRQ1	0xFFF9
IRQ2	0xFFFA
IRQ3	0xFFFB
IRQ4	0xFFFC
IRQ5	0xFFFD
IRQ6	0xFFFE
IRQ7	0xFFFF

CPU and Peripherals Control Registers List

- **CPU control/status registers**

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7006-7555: CPU control/status registers											
0x7006	P_Reset_Status	0x0000	R	–							
				–	IIRF	IARF	–	LVRF	WDRF	PORF	EXTRF
				The flag of reset status for firmware checking.							
			W								
				–	IIRF	IARF	–	LVRF	WDRF	PORF	EXTRF
				To properly clear reset flags, FCHK must be written to 0x55 with specified reset flag is se to 1.							
0x7007	P_Clk_Ctrl	0x0000	R	OSCSF	OSCIE	–					
				–							
				This register is used for monitoring CPU clock status							
			W	OSCSF	OSCIE	–					
				–							
				Write ‘1’ to OSCSF will clear this flag.							
0x700A	P_WatchDog_Ctrl	0x0000	R	WDEN	WDRS	–					
				WDCHK						WDPS	
				This register provides the watchdog clear timer and on/off function for firmware setting							
			W	WDEN	WDRS	–					
				WDCHK						WDPS	
				To change the settings of this register, WDCHK must be written with “10101”.							
0x700B	P_WatchDog_Clr	0x0000	R	Watchdog Clear Register							
				Watchdog Clear Register							
				This register is used to clear watchdog timer, Write 0xA005 to clear watchdog timer							
0x700C	P_Wait_Enter	0x0000	R	Wait-Mode Entrance Register							
				Wait-Mode Entrance Register							
				Read 0x0001 indicates that it is wake-up from wait mode.							
			W	Wait-Mode Entrance Register							
				Wait-Mode Entrance Register							
				Write 0x5005 to enter wait mode (CPU off, PLL on) and write 0x0001 will clear wait flag.							
0x700E	P_Stdby_Enter	0x0000	R	Standby-Enter Entrance Register							
				Standby-Enter Entrance Register							
				Read 0x0001 indicates that it is wake-up from Standby mode.							
			W	Standby-Enter Entrance Register							
				Standby-Enter Entrance Register							
				Write 0xA00A to enter standby mode (CPU off, PLL off) and write 0x0001 will clear standby flag.							
0x700F	P_Wakeup_Ctrl	0x0000	R/W	KEYWE	UARTWE	SPIWE	EXT1WE	EXT0WE	–		
				TPM2WE	PDC1WE	PDC0WE	CMTWE	–			
				This register determines the wakeup source when the chip is in power-saving mode.							
0x704D	P_Flash_RW	0x0000	R/W	–	BK14WNB	–					
				–							

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				First, write 0x5A5A to P_Flash_RW, and then write configuration data to P_Flash_RW in duration of less than 16 clock cycles.							
0x7555	P_Flash_Cmd	0x0000	R/W	Embedded Flash Access Control Register							
				Embedded Flash Access Control Register							
				This port is used to issue flash command.							

- **IO Port registers**

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7060-0x7084: CPU control/status registers											
0x7060	P_IOA_Data	0x0000	R	IO Port A Data Register							
				IO Port A Data Register							
				Read data from the I/O pad							
			W	IO Port A Data Register							
				IO Port A Data Register							
				Write data into the data register and read data from the I/O pad							
0x7061	P_IOA_Buffer	0x0000	R	IO Port A Buffer Register							
				IO Port A Buffer Register							
				Read data from the I/O buffer							
			W	IO Port A Buffer Register							
				IO Port A Buffer Register							
				Write data into the data register and read data from the I/O pad							
0x7062	P_IOA_Dir	0x0000	R/W	IO Port A Direction Register							
				IO Port A Direction Register							
				Direction-vector from/into the direction register							
0x7063	P_IOA_Attrib	0xFFFF	R/W	IO Port A Attrib Register							
				IO Port A Attrib Register							
				The attribute setting gives a feature to the pin, float / pull for input, not inverted/ inverted for output							
0x7064	P_IOA_Latch	0x0000	R	IO Port A Latch Register							
				IO Port A Latch Register							
				Read this port to latch data on the I/O PortA for key change wakeup before getting into sleep mode							
0x7068	P_IOB_Data	0x0000	R	IO Port B Data Register							
				IO Port B Data Register							
				Read data from the I/O pad							
			W	IO Port B Data Register							
				IO Port B Data Register							
				Write data into the data register and read data from the I/O pad							
0x7069	P_IOB_Buffer	0x000	R	IO Port B Buffer Register							
				IO Port B Buffer Register							
				Read data from the I/O buffer							

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
			W	IO Port B Buffer Register							
				IO Port B Buffer Register							
				Write data into the data register and read data from the I/O pad							
0x706A	P_IOB_Dir	0x0000	R/W	IO Port B Direction Register							
				IO Port B Direction Register							
				Direction-vector from/into the direction register							
0x706B	P_IOB_Attrib	0xFFFF	R/W	IO Port B Attrib Register							
				IO Port B Attrib Register							
				The attribute setting gives a feature to the pin, float / pull for input, not inverted/ inverted for output							
0x7070	P_IOC_Data	0x000	R	IO Port C Data Register							
				IO Port C Data Register							
				Read data from the I/O pad							
			W	IO Port C Data Register							
				IO Port C Data Register							
				Write data into the data register and read data from the I/O pad							
0x7071	P_IOC_Buffer	0x000	R	IO Port C Buffer Register							
				IO Port C Buffer Register							
				Read data from the I/O buffer							
			W	IO Port C Buffer Register							
				IO Port C Buffer Register							
				Write data into the data register and read data from the I/O pad							
0x7072	P_IOC_Dir	0x000	R/W	IO Port C Direction Register							
				IO Port C Direction Register							
				Direction-vector from/into the direction register							
0x7073	P_IOC_Attrib	0xFFFF	R/W	IO Port C Attrib Register							
				IO Port C Attrib Register							
				The attribute setting gives a feature to the pin, float / pull for input, not inverted/ inverted for output							
0x7078	P_IOD_Data	0x000	R	IO Port D Data Register							
				IO Port D Data Register							
				Read data from the I/O pad							
			W	IO Port D Data Register							
				IO Port D Data Register							
				Write data into the data register and read data from the I/O pad							
0x7079	P_IOD_Buffer	0x000	R	IO Port D Buffer Register							
				IO Port D Buffer Register							
				Read data from the I/O buffer							
			W	IO Port D Buffer Register							
				IO Port D Buffer Register							
				Write data into the data register and read data from the I/O pad							
0x707A	P_IOD_Dir	0x000	R/W	IO Port D Direction Register							
				IO Port D Direction Register							

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				Direction-vector from/into the direction register							
0x707B	P_IOD_Attrib	0xFFFF	R/W	IO Port D Attrib Register							
				IO Port D Attrib Register							
				The attribute setting gives a feature to the pin, float / pull for input, not inverted/ inverted for output							
0x7080	P_IOA_SPE	0x0000	R/W	–	TCLKDEN	TCLKCEN	TCLKBEN	TCLKAEN	TIO2BEN	TIO2AEN	–
				–							
				PortA special function enable register							
0x7081	P_IOB_SPE	0x003F	R/W	–					TIO0AEN	TIO0BEN	TIO0AEN
				OL1EN	FTIN1EN	U1EN	V1EN	W1EN	U1NEN	V1NEN	W1NEN
				PortB special function enable register							
0x7082	P_IOC_SPE	0xFC00	R/W	W2NEN	V2NEN	U2NEN	W2EN	V2EN	U2EN	FTIN2EN	OL2EN
				TIO1CEN	TIO1BEN	TIO1AEN	–	EXINT1EN	EXINT0EN	–	
				PortC special function enable register							
0x7084	P_IOA_KCER	0x000	R/W	KC15EN	KC14EN	KC13EN	KC12EN	KC11EN	KC10EN	KC9EN	KC8EN
				–							
				PortA key-change pin enable register							

Address	Function	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x70A0	P_INT_Status	0x0000	R/W	KEYIF	UARTIF	SPIIF	EXT1IF	EXT0IF	ADCIF	MCP4IF	MCP3IF
				TPM2IF	PDC1IF	PDC0IF	CMTIF	–	OLIF	OSCSF	FTIF
				Only the KEYIF, EXT0IF and EXT1IF can write '1' to clear these flags. Other status flags are and read only.							
0x70A4	P_INT_Priority	0x0000	R/W	KEYIP	UARTIP	SPIIP	–	EXTIP	ADCIP	MCP4IP	MCP3IP
				TPM2IP	PDC1IP	PDC0IP	CMTIP	–	OLIP	OSCIP	FTIP
				Set interrupt source as IRQ or FIQ. Only one of interrupt source can be set as FIQ							
0x70A8	P_MisINT_Ctrl	0x0000	R/W	KEYIE	EXT1MS	EXT0MS	EXT1IE	EXT0IE	–		
				–							
				Miscellaneous setting for key-change and external input interrupt enable							
0x70B8	P_TMB_Reset	0x0000	W	Time Base Reset Register							
				Time Base Reset Register							
				Write 0x5555h to this register to reset the time base counter register to initial the clock sources of all peripherals on the chip							
0x70B9	P_BZO_Ctrl	0x000	R/W	BZOEN	–						
				–							BZOCK
				Buzzer output frequency selection and output enable							

- **ADC control/status registers**

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7160	P_ADC_Setup	0x0000	R/W	ADCCS	ADCEN	–			ADCFS		ADC EXTRG
				ASPEN	–						
				Control the ADC block power on or off, ADC conversion clock and event selection to trigger the start operation of ADC							
0x7161	P_ADC_Ctrl	0x0000	R/W	ADCIF	ADCIE	–					
				ADCRDY	ADCSTR	–			ADCCHS		
				ADC interrupt enable on/off, manually start ADC conversion and ADC convert channels selection							
0x70A2	P_ADC_Channel	0x0000	R/W	–							
				ADCCH7	ADCCH6	ADCCH5	ADCCH4	ADCCH3	ADCCH2	ADCCH1	ADCCH0
				Configures the IOA[7:2] is either GPIO port or analog input port							
0x7162	P_ADC_Data	0xFFC0	R	ADCDATA							
				ADCDATA	–						
				10-bits ADC conversion result register							

- **UART and SPI control/status registers**

Address	Function	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7100	P_UART_Data	0x0000	R	–				OE	–	PE	FE
				UARTDATA							
				Data register for UART reception. This register also indicates the error flags during reception.							
			W	–							
				UARTDATA							
				Data register for UART transmission							
0x7101	P_UART_RXStatus	0x0000	R	–							
				–				OE	–	PE	FE
				This register indicates the error flags during reception							
0x7102	P_UART_Ctrl	0x000	R/W	RXIE	TXIE	RXEN	TXEN	Reset	TXCHSEL	RXCHSEL	–
				–				SBSEL	PSEL	PEN	–
				Control the setting for UART receive/transmit pin enable, stop bit, and parity selection							
0x7103	P_UART_BaudRate	0x000	R/W	UART Baud Rate Setup Register							
				UART Baud Rate Setup Register							
				This register determines the baud-rate of UART							
0x7104	P_UART_Status	0x000	R	RXIF	TXIF	–					
				–	RXBF	–		BY	–		
				UART reception and transmission status flags							
0x7140	P_SPI_Ctrl	0x0000	R/W	SPIE	–			SPIRST	SPISPCLK		SPIMS
				–		SPIPHA	SPIPOL	SPISMPS	SPIFS		
				The configuration register for SPI module							

Address	Function	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7141	P_SPI_TxStatus	0x000	R	SPITXIF	SPITXIE	SPITXBF	–				
				–							
				SPI transmission interrupt enable and status flags							
0x7142	P_SPI_TxBuf	0x0000	R/W	–							
				SPITXBUF							
				SPI transmission buffer register							
0x7143	P_SPI_RxStatus	0x0000	R/W	SPIRXIF	SPIRXIE	–			FERR	–	
				–							
				SPI reception interrupt enable and status flags							
0x7144	P_SPI_RxBuf	0x000	R/W	–							
				SPIRXBUF							
				SPI reception buffer register							

- **PDC0/1 Timers control/status registers**

Address	Function	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7405	P_TMR_Start	0x0000	R/W	–							
				–			TMR4ST	TMR3ST	TMR2ST	TMR1ST	TMR0ST
				PDC0/1, TPM2, and MCP3/4 timers start or stop control register							
0x7400	P_TMR0_Ctrl	0x0000	R/W	SPCK		MODE				CLEGS	
				CCLS		CKEGS		TMRPS			
				Configures the selection of timer clock source, counter clock edge, counter clear source, counter clear edge, capture input sample clock and timer operating modes							
0x7401	P_TMR1_Ctrl	0x0000	R/W	SPCK		MODE				CLEGS	
				CCLS		CKEGS		TMRPS			
				Configures the selection of timer clock source, counter clock edge, counter clear source, counter clear edge, capture input sample clock and timer operating modes							
0x7410	P_TMR0_IOCtrl	0x0000	R/W	–				IOCMODE			
				IOBMODE				IOAMODE			
				Controls the PWM output, input capture, and position detection change action type of TIO0A, TIO0B, and TIO0C pins							
0x7411	P_TMR1_IOCtrl	0x0000	R	–				IOCMODE			
				IOBMODE				IOAMODE			
				Controls the PWM output, input capture, and position detection change action type of TIO1A, TIO1B, and TIO1C pins							
0x7420	P_TMR0_INT	0x0000	R/W	–							PDCIE
				TADSE	TCUIE	TCVIE	TPRIE	–	TGCIE	TGBIE	TGAIE
				Enable or disable A/D conversion start request by TGRA compare match, interrupt requests for position detection changes, overflow/underflow of TCNT, period register compare match and input capture/compare match of TGRA, TGRB, TGRC							
0x7421	P_TMR1_INT	0x000	R/W	–							PDCIE
				TADSE	TCUIE	TCVIE	TPRIE	–	TGCIE	TGBIE	TGAIE

Address	Function	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				Enable or disable A/D conversion start request by TGRA compare match, interrupt requests for position detection changes, overflow/underflow of TCNT, period register compare match and input capture/compare match of TGRA, TGRB, TGRC							
0x7425	P_TMR0_Status	0x000	R/W	–							PDCIF
				TCDF	TCUIF	TCVIF	TPRIF	–	TGCIF	TGBIF	TGAIF
				Indicates the event generation of position detection changes, an underflow/overflow of TCNT, period register compare match and input capture/compare match of TGRA, TGRB, TGRC							
0x7426	P_TMR1_Status	0x000	R/W	–							PDCIF
				TCDF	TCUIF	TCVIF	TPRIF	–	TGCIF	TGBIF	TGAIF
				Indicates the event generation of position detection changes, an underflow/overflow of TCNT, period register compare match and input capture/compare match of TGRA, TGRB, TGRC							
0x7462	P_POS0_DectCtrl	0x0000	R/W	SPLCK		SPLMOD		SPLCNT			
				PDEN	SPDLY						
				Control the sampling settings of position detection signals from TIO0A, TIO0B and TIO0C input pins.							
0x7463	P_POS1_DectCtrl	0x0000	R/W	SPLCK		SPLMOD		SPLCNT			
				PDEN	SPDLY						
				Control the sampling settings of position detection signals from TIO1A, TIO1B and TIO1C input pins.							
0x7464	P_POS0_DectData	0x0000	R	–							
				–					PDR		
				The current filtered position data will be latched to this register							
0x7465	P_POS1_DectData	0x000	R	–							
				–					PDR		
				The current filtered position data will be latched to this register							
0x7430	P_TMR0_TCNT	0x000	R	Timer 0 Counter Register							
				Timer 0 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7431	P_TMR1_TCNT	0x000	R	Timer 1 Counter Register							
				Timer 1 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7440	P_TMR0_TGRA	0x0000	R/W	Timer 0 General Register A							
				Timer 0 General Register A							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7441	P_TMR0_TGRB	0x0000	R/W	Timer 0 General Register B							
				Timer 0 General Register B							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7442	P_TMR0_TGRC	0x0000	R	Timer 0 General Register C							
				Timer 0 General Register C							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7433	P_TMR1_TGRA	0x0000	R/W	Timer 1 General Register A							

Address	Function	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				Timer 1 General Register A							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7444	P_TMR1_TGRB	0x0000	R/W	Timer 1 General Register B							
				Timer 1 General Register B							
0x7445	P_TMR1_TGRC	0x0000	R/W	Timer 1 General Register C							
				Timer 1 General Register C							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7450	P_TMR0_TBRA	0x0000	R	Timer 0 Buffer Register A							
				Timer 0 Buffer Register A							
				The timer buffer register is the double buffer for TGRA. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7451	P_TMR0_TBRB	0x000	R	Timer 0 Buffer Register B							
				Timer 0 Buffer Register B							
				The timer buffer register is the double buffer for TGRB. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7452	P_TMR0_TBRC	0x000	R	Timer 0 Buffer Register C							
				Timer 0 Buffer Register C							
				The timer buffer register is the double buffer for TGRC. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7453	P_TMR1_TBRA	0x0000	R	Timer 1 Buffer Register A							
				Timer 1 Buffer Register A							
				The timer buffer register is the double buffer for TGRA. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7454	P_TMR1_TBRB	0x000	R	Timer 1 Buffer Register B							
				Timer 1 Buffer Register B							
				The timer buffer register is the double buffer for TGRB. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7455	P_TMR1_TBRC	0x000	R	Timer 1 Buffer Register C							
				Timer 1 Buffer Register C							
				The timer buffer register is the double buffer for TGRC. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7435	P_TMR0_TPR	0xFFFF	R/W	Timer 0 Period Register							
				Timer 0 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							
0x7436	P_TMR1_TPR	0xFFFF	R/W	Timer 1 Period Register							
				Timer 1 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							

- **TPM2 Timers control/status registers**

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7402	P_TMR2_Ctrl	0x0000	R/W	SPCK		MODE				CLEGS	
				CCLS			CKEGS		TMRPS		
				Configures the selection of timer clock source, counter clock edge, counter clear source, counter clear edge, capture input sample clock and timer operating modes							
0x7412	P_TMR2_IOCtrl	0x0000	R/W	–							
				IOBMODE				IOAMODE			
				Controls the PWM output and input capture action type of TIO2A, and TIO2B pins							
0x7422	P_TMR2_INT	0x0000	R/W	–							
				TADSE	–		TPRIE	–		TGBIE	TGAIE
				Enable or disable A/D conversion start request by TGRA compare match, interrupt requests for period register compare match and input capture/compare match of TGRA or TGRB.							
0x7427	P_TMR2_Status	0x0000	R/W	–							
				TCDF	–		TPRIF	–		TGBIF	TGAIF
				Indicates the event generation of a period registers compare match and input capture/compare match of TGRA or TGRB							
0x7432	P_TMR2_TCNT	0x0000	R	Timer 2 Counter Register							
				Timer 2 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7446	P_TMR2_TGRA	0x0000	R/W	Timer 2 General Register A							
				Timer 2 General Register A							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7447	P_TMR2_TGRB	0x0000	R/W	Timer 2 General Register B							
				Timer 2 General Register B							
				The 16-bit register, functioning as either PWM output or input capture register							
0x7456	P_TMR2_TBRA	0x0000	R	Timer 2 Buffer Register A							
				Timer 2 Buffer Register A							
				The timer buffer register is the double buffer for TGRA. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7457	P_TMR2_TBRB	0x0000	R	Timer 2 Buffer Register B							
				Timer 2 Buffer Register B							
				The timer buffer register is the double buffer for TGRB. When used as input capture function, the TCNT value is stored at the falling edge of input capture port.							
0x7437	P_TMR2_TPR	0xFFFF	R/W	Timer 2 Period Register							
				Timer 2 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							

- **MCP 3/4 Timers control/status registers**

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7409	P_TPWM_Write	0x000	R/W	-							
				-						TMR4WE	TMR3WE
				Write 0x5A01 and 0x5A03 to this register to enable timer 3 or 4 for timer PWM generation.							
0x740A	P_TMR_LDOK	0x000	R/W	-							
				TLDCHK						LDOK1	LDOK0
				To correctly set the LDOK bits, the pattern '101010' must be written to.							
0x7403	P_TMR3_Ctrl	0x0000	R/W	PRDINT	MODE					–	
				CCLS			CKEGS		TMRPS		
				Configures the selection of timer clock source, counter clock edge, counter clear source, TPR interrupt frequency and timer operating modes.							
0x7404	P_TMR4_Ctrl	0x000	R/W	PRDINT	MODE					–	
				CCLS			CKEGS		TMRPS		
				Configures the selection of timer clock source, counter clock edge, counter clear source, TPR interrupt frequency and timer operating modes.							
0x7413	P_TMR3_IOCtrl	0x0000	R/W	–				IOCMODE			
				IOBMODE				IOAMODE			
				Controls the PWM compare match output action type of TIO3A, TIO3B, and TIO3C pins.							
0x7414	P_TMR4_IOCtrl	0x0000	R/W	–				IOCMODE			
				IOBMODE				IOAMODE			
				Controls the PWM compare match output action type of TIO4A, TIO4B, and TIO4C pins.							
0x7423	P_TMR3_INT	0x000	R/W	–							
				TADSE	–		TPRIE	TGDIE	–		
				Enable or disable A/D conversion start request by TGRD compare match, interrupt requests for period register compare match and compare match of TGRD.							
0x7424	P_TMR4_INT	0x0000	R/W	–							
				TADSE	–		TPRIE	TGDIE	–		
				Enable or disable A/D conversion start request by TGRD compare match, interrupt requests for period register compare match and compare match of TGRD.							
0x7428	P_TMR3_Status	0x000	R/W	–							
				TCDF	–		TPRIF	TGDIF	–		
				Indicates the event generation of period register compare match and compare match of TGRD. These flags show the interrupt sources.							
0x7429	P_TMR4_Status	0x000	R/W	–							
				TCDF	–		TPRIF	TGDIF	–		
				Indicates the event generation of period register compare match and compare match of TGRD. These flags show the interrupt sources.							
0x7428	P_TMR_Output	0x0000	R/W	–		TMR4FOE	TMR4EOE	TMR4DOE	TMR4COE	TMR4BOE	TMR4AOE
				–		TMR3FOE	TMR3EOE	TMR3DOE	TMR3COE	TMR3BOE	TMR3AOE
				Enables/disables the PWM outputs of MCP3/4 timer module. The PWM output will be high-impedance if disabled.							
0x7407	P_TMR3_OutputCtrl	0x000	R/W	DUTY MODE	POLP					WPWM	VPWM

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				UPWM	SYNC	WOC		VOC		UOC	
				Setting for the PWM waveform output type of MCP3 timer.							
0x7408	P_TMR4_OutputCtrl	0x0000	R/W	DUTY MODE	POLP	–				WPWM	VPWM
				UPWM	SYNC	WOC		VOC		UOC	
				Setting for the PWM waveform output type of MCP4 timer.							
0x7460	P_TMR3_DeadTime	0x0000	R/W	–	DTWE	DTVE	DTUE	–			
				–	DTP						
				Dead time setting for MCP3 timer outputs.							
0x7461	P_TMR4_DeadTime	0x000	R/W	–	DTWE	DTVE	DTUE	–			
				–	DTP						
				Dead time setting for MCP4 timer outputs.							
0x7466	P_Fault1_Ctrl	0x0000	R/W	OCE	OCIE	OCLS	OSF	–			
				FTPINE	FTPINIE	FTPINIF	–	FTCNT			
				Fault control configuration settings for FTIN1.							
0x7467	P_Fault2_Ctrl	0x000	R/W	OCE	OCIE	OCLS	OSF	–			
				FTPINE	FTPINIE	FTPINIF	–	FTCNT			
				Fault control configuration settings for FTIN2.							
0x746A	P_Fault1_Release	0x000	R/W	Fault 1 Flag Release Register							
				Fault 1 Flag Release Register							
				1. Write 0x55AA then 0xAA55 sequentially to clear FTPINIF flag in P_Fault1_Ctrl register. 2. Write 0xAA55 then 0x55AA sequentially to clear OSCSF flag in P_Fault1_Ctrl register.							
0x746B	P_Fault2_Release	0x0000	R/W	Fault 2 Flag Release Register							
				Fault 2 Flag Release Register							
				1. Write 0x55AA then 0xAA55 sequentially to clear FTPINIF flag in P_Fault2_Ctrl register. 2. Write 0xAA55 then 0x55AA sequentially to clear OSCSF flag in P_Fault2_Ctrl register.							
0x7468	P_OL1_Ctrl	0x000	R/W	OLEN	CNTSP	OLMD		OLST	RTTMB	RTPWM	RTOL
				OLIE	OLIF	–		OLCNT			
				Overload control configuration settings for OL1.							
0x7469	P_OL2_Ctrl	0x000	R/W	OLEN	CNTSP	OLMD		OLST	RTTMB	RTPWM	RTOL
				OLIE	OLIF	–		OLCNT			
				Overload control configuration settings for OL2.							
0x7433	P_TMR3_TCNT	0x0000	R	Timer 3 Counter Register							
				Timer 3 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7434	P_TMR4_TCNT	0x000	R	Timer 4 Counter Register							
				Timer 4 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7448	P_TMR3_TGRA	0x0000	R/W	Timer 3 General Register A							
				Timer 3 General Register A							
				The 16-bit readable/writable registers, functioning as PWM duty for TIO3A/TIO3D.							
0x7449	P_TMR3_TGRB	0x0000	R/W	Timer 3 General Register B							
				Timer 3 General Register B							

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				The 16-bit readable/writable registers, functioning as PWM duty for TIO3B/TIO3E.							
0x744A	P_TMR3_TGRC	0x000	R/W	Timer 3 General Register C							
				Timer 3 General Register C							
				The 16-bit readable/writable registers, functioning as PWM duty for TIO4C/TIO4F.							
0x744B	P_TMR3_TGRD	0x000	R/W	Timer 3 General Register D							
				Timer 3 General Register D							
				Used as the ADC conversion start signal when TCNT counter value match this register content or general compare match register.							
0x744C	P_TMR4_TGRA	0x000	R/W	Timer 4 General Register A							
				Timer 4 General Register A							
				The 16-bit readable/writable registers, functioning as PWM duty for TIO4A/TIO4D.							
0x744D	P_TMR4_TGRB	0x000	R/W	Timer 4 General Register B							
				Timer 4 General Register B							
				The 16-bit readable/writable registers, functioning as PWM duty for TIO4B/TIO4E.							
0x744E	P_TMR4_TGRC	0x000	R/W	Timer 4 General Register C							
				Timer 4 General Register C							
				The 16-bit readable/writable registers, functioning as PWM duty for TIO4C/TIO4F.							
0x744F	P_TMR4_TGRD	0x000	R/W	Timer 4 General Register D							
				Timer 4 General Register D							
				Used as the ADC conversion start signal when TCNT counter value match this register content or general compare match register.							
0x7458	P_TMR3_TBRA	0x000	R	Timer 3 Buffer Register A							
				Timer 3 Buffer Register A							
				The timer buffer register is the double buffer for TGRA.							
0x7459	P_TMR3_TBRB	0x0000	R	Timer 3 Buffer Register B							
				Timer 3 Buffer Register B							
				The timer buffer register is the double buffer for TGRB.							
0x745A	P_TMR3_TBRC	0x000	R	Timer 3 Buffer Register C							
				Timer 3 Buffer Register C							
				The timer buffer register is the double buffer for TGRC.							
0x745C	P_TMR4_TBRA	0x000	R	Timer 4 Buffer Register A							
				Timer 4 Buffer Register A							
				The timer buffer register is the double buffer for TGRA.							
0x745D	P_TMR4_TBRB	0x000	R	Timer 4 Buffer Register B							
				Timer 4 Buffer Register B							
				The timer buffer register is the double buffer for TGRB.							
0x745E	P_TMR4_TBRC	0x000	R	Timer 4 Buffer Register C							
				Timer 4 Buffer Register C							
				The timer buffer register is the double buffer for TGRC.							
0x7438	P_TMR3_TPR	0xFFFF	R/W	Timer 3 Period Register							
				Timer 3 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							
0x7439	P_TMR4_TPR	0xFFFF	R/W	Timer 4 Period Register							

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
				Timer 4 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							

- **CMT timer control/status registers**

Address	Register Name	Reset value	R/W	Bit Field							
				B15	B14	B13	B12	B11	B10	B9	B8
				B7	B6	B5	B4	B3	B2	B1	B0
0x7500	P_CMT_Start	0x0000	R/W	—							
				—						ST1	ST0
				CMT01 and CMT1 timers start or stop control register							
0x7501	P_CMT_Ctrl	0x000	R/W	CM1IF	CM1IE	—			CKB		
				CM0IF	CM0IE	—			CKA		
				CMT0 and CMT1 timers interrupt enable and clock selection register.							
0x7508	P_CMT0_TCNT	0x000	R	Compare Match Timer 0 Counter Register							
				Compare Match Timer 0 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7509	P_CMT1_TCNT	0x000	R	Compare Match Timer 1 Counter Register							
				Compare Match Timer 1 Counter Register							
				The 16-bit readable registers that increment/decrement according to input clocks							
0x7510	P_CMT0_TPR	0xFFFF	R/W	Compare Match Timer 0 Period Register							
				Compare Match Timer 0 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							
0x7511	P_CMT1_TPR	0xFFFF	R/W	Compare Match Timer 1 Period Register							
				Compare Match Timer 1 Period Register							
				The 16-bit readable/writable register. It is used to setup the period interrupt of timer.							

5.3. Clock Generation Module (CGM)

The Clock Generation Module generates all the clock sources needed for system operation. It contains a crystal oscillator, PLL (Phase-Lock-Loop) circuit, external clock and clock monitoring circuit. Additionally, the built-in RC oscillator is dedicated to Power-on timer and flash control for writing operation.

5.3.1. Crystal Oscillator

The crystal oscillator uses crystal device for clock generation. The range is between 3M ~ 6MHz. The oscillator output will be used as PLL clock source and the PLL circuit pumps the input clock to four times. Thus, if the 6MHz crystal is connected, the PLL output clock will be pumped to 24MHz.

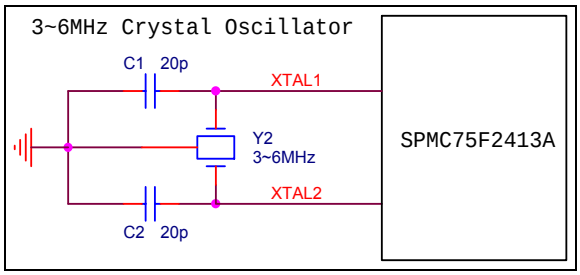


Figure 5-5 The crystal circuit connection

5.3.2. Phase-lock Loop (PLL)

There is an on-chip PLL circuit available. The PLL takes a reference clock for generating system clock. The on-chip crystal clock is used as the reference clock of PLL circuit. The PLL output clock rate is four times of reference clock. During power-on or system reset or wake-up from standby, CPU will halt 16384 oscillator reference clocks (F_{IN}) for oscillator and PLL to be stable. The stable time is about 2.7ms when oscillator reference clock is 6MHz. The PLL will output about 1MHz clock when oscillator clock is not available. Following diagram shows the relationship between crystal oscillator and PLL circuit.

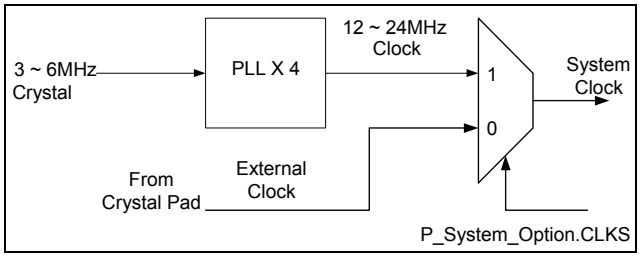


Figure 5-6 PLL and external clock block diagram

5.3.3. External clock

The CLKS in P_System_Option can configure an external clock between 12MHz and 24MHz as the clock source. Figure 5-7 shows the connection of external clock from oscillator.

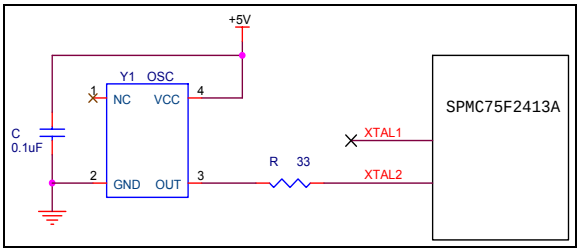


Figure 5-7 The external clock from oscillator connection

5.3.4. Clock Monitoring

A clock monitoring circuit is also available to detect whether the oscillator clock and system clock run normally. If a clock halt is detected, the twelve motor drive PWM pins (TIO3A~F and TIO4A~F) will be set to high-impedance state, regardless their pin function settings, and an interrupt will be issued to notify CPU. Remarkably, the state will be released only by power-on reset if the PWM pins are set to high-impedance state.

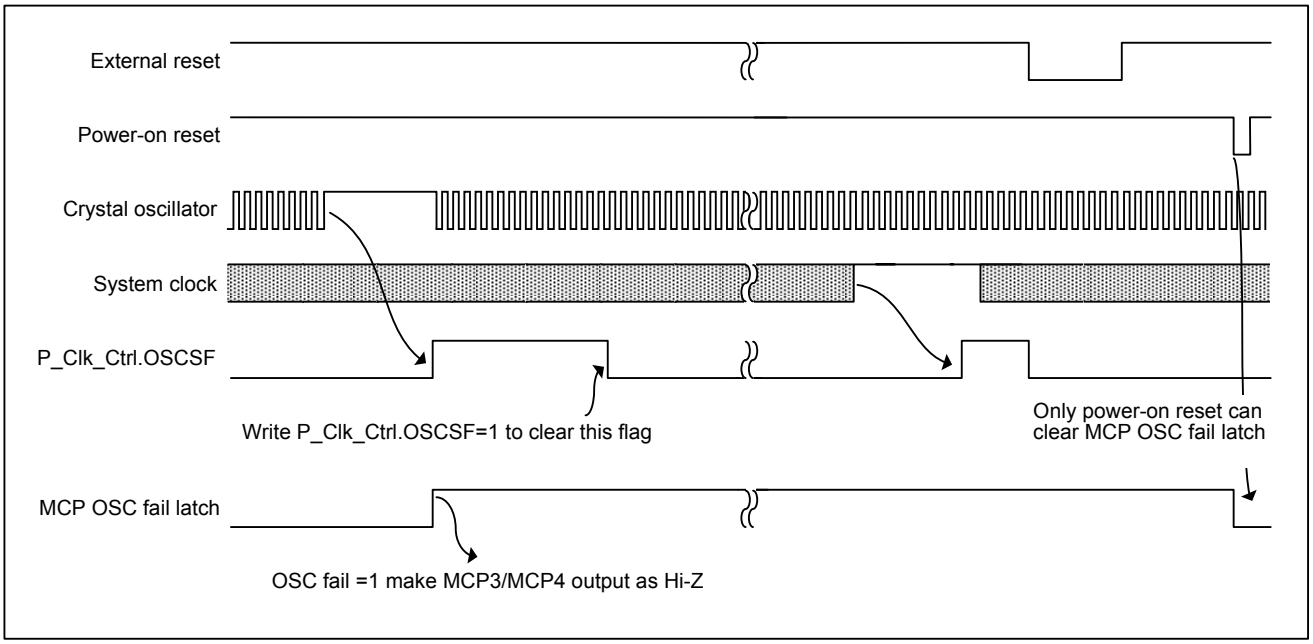


Figure 5-8 Clock Fail timing

- **P_Clk_Ctrl (0x7007): System Clock Control Register**

This register is used for monitoring CPU clock status.

B15	B14	B13	B2	B11	B10	b9	B8
R/W	R/W	R	R	R	R	R	R
0	0	0	0	0	0	0	0
OSCSF	OSCIE	Reserved					

B7	B6	B5	B4	B3	Bb2	b1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B15	OSCSF※	Oscillator status flag	Read 0: Oscillator operates normally Write 1: Clear this flag	Read 1: Oscillator failed
B14	OSCIE	Oscillator fail interrupt enable bit	0: Disable	1: Enable
B10-8	Reserved			

※: write “1” to clear this flag

5.3.5. RC Oscillator

The 200KHz clock that is derived from build-in oscillator is provided for power-on timer and flash controller to generate the necessary control signals meeting the timing specifications of flash erasing and programming. It can be disabled in either sleep mode or standby mode for power saving.

5.4. Power Saving Modes

There are three operating modes available in this device: Normal mode, Wait mode, and Standby mode.

Normal mode

When device operates in normal mode, it consumes the maximum power, and all peripherals can be used.

Wait mode

Both of CPU and watchdog are powered-down in wait mode to decrease CPU power consumption. Other peripherals keep their previous states and are operable. When waking up, CPU will resume and execute next instruction. Figure 5-9 shows the Wait mode timing. Table 5-5 shows the relationship between power saving mode and related operation.

Standby mode

All modules are disabled in this mode. Power consumption is minimized in this mode. When waking-up, CPU will reset and back to normal operation mode. Other peripherals can be turned off individually by software. Note that if TPM (Timer/PWM Module) channel 3 or channel 4 has been set to PWM output mode, the device will not enter Wait mode or Standby mode. Figure 5-10 shows the Standby mode timing.

Table 5-5 the relationship between mode and operation

	Wait	Standby
CPU	OFF	OFF
PLL	ON	OFF
Peripherals	ON	OFF
Wakeup from	Next instruction	Reset CPU

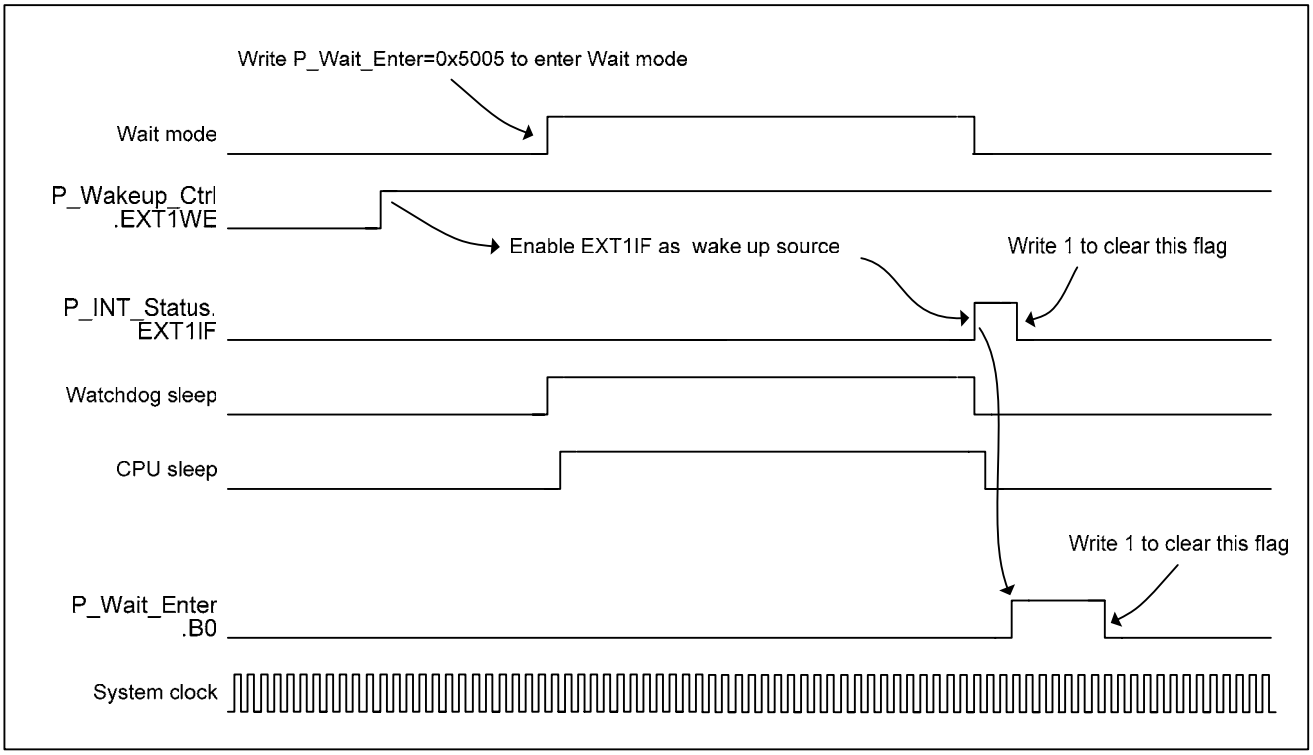


Figure 5-9 Wait mode timing

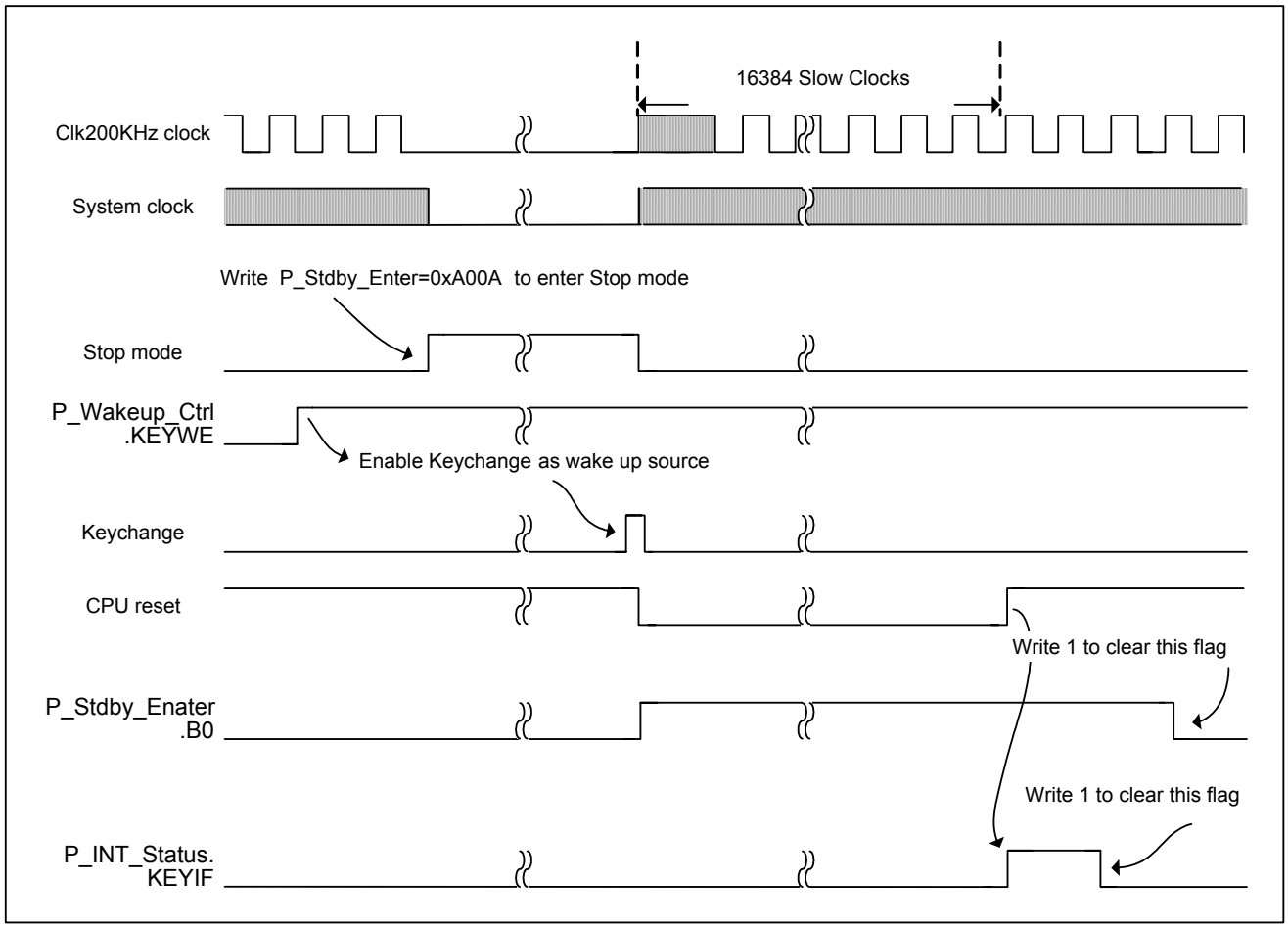


Figure 5-10 Standby mode timing

5.4.1. Wake-up Sources

The wake-up event may come from the following sources (total 28 sources):

Timer/PWM Module

- Channel 0: TPR_0, TGRA_0, TGRB_0, TGRC_0, Position detection change, overflow, underflow
- Channel 1: TPR_1, TGRA_1, TGRB_1, TGRC_1, Position detection change, overflow, underflow
- Channel 2: TPR_2, TGRA_2, TGRB_2
- Channel 3: TPR_3, TGRD_3
- Channel 4: TPR_4, TGRD_4

Compare Match Timer

- Channel 0: CMT_0 compare match
- Channel 1: CMT_1 compare match

IO

- Key change

External Interrupt

- EXINT0
- EXINT1

Serial Communication Interface

- UART
- SPI

- **P_Wakeup_Ctrl (0x700F)：Wake-up Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
KEYWE	UARTWE	SPIWE	EXT1WE	EXT0WE	Reserved		

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TPM2WE	PDC1WE	PDC0WE	CMTWE	Reserved			

B15	KEYWE	Key-change wake-up enable bit	0: Disable	1: Enable
B14	UARTWE	UART wake-up enable bit	0: Disable	1: Enable
B13	SPIWE	SPI wake-up enable bit	0: Disable	1: Enable
B12	EXT1WE	External interrupt 1 wake-up enable bit	0: Disable	1: Enable
B11	EXT0WE	External interrupt 0 wake-up enable bit	0: Disable	1: Enable
B10-8	Reserved			
B7	TPM2WE	TPM channel 2 wake-up enable bit	0: Disable	1: Enable
B6	PDC1WE	PDC channel 1 wake-up enable bit	0: Disable	1: Enable
B5	PDC0WE	PDC channel 0 wake-up enable bit	0: Disable	1: Enable
B4	CMTWE	Compare match timer wake-up enable bit	0: Disable	1: Enable
B3-0	Reserved			

- **P_Wait_Enter (0x700C)：Wait-mode Entrance Registe**

B15	B14	B13	B12	B11	B10	B9	B8
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
WaitCMD							

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	W	W	R/W
0	0	0	0	0	0	0	0
WaitCMD							

B15-0	WaitCMD	Wait-mode Entrance/Status flag	1. Write 0x5005 to enter wait mode (CPU off, PLL on). 2. Write 0x0001 will clear wait flag. 3. Read 0x0001 indicates that it is wake-up from wait mode. 4. Note that to enter Wait mode, MCP channel 3 or 4 must not be set to PWM output mode. In ICE mode, SPMC75F2413A cannot enter into wait mode.

- **P_Stdby_Enter (0x700E)：Standby-mode Entrance Register**

B15	B14	B13	B12	B11	B10	B9	B8
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
StdbyCMD							

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	W	W	R/W
0	0	0	0	0	0	0	0
StdbyCMD							

B15-0	StdbyCMD	Standby-mode Entrance/Status flag	1. Write 0xA00A to enter standby mode (CPU off, PLL off). 2. Write 0x0001 will clear standby flag. 3. Read 0x0001 indicates that it is wake-up from Standby mode. 4. Note that to enter Standby mode, MCP channel 3 or 4 must not be set to PWM output mode. In ICE mode, SPMC75F2413A cannot enter into standby mode.

5.5. Interrupt

The SPMC75F2413A has 38 interrupt sources. These 38 interrupt sources can be grouped into two types, FIQ (Fast Interrupt Request) and IRQ0~IRQ7 (Interrupt request). Besides, the SPMC75F2413A also implements a software interrupt, BREAK. The priority of BREAK, FIQ, and IRQ is as follows: BREAK > FIQ > IRQ 0 > IRQ 1 > IRQ 2 > IRQ 3 > IRQ 4 > IRQ 6 > IRQ 7. The BREAK and FIQ have higher priority than IRQ. An IRQ can be interrupted by a FIQ, BREAK, or another IRQ that has higher priority. An FIQ can only be interrupted by BREAK. If IRQNEST mode is off and more than two IRQ occurred, the priority of IRQ are IRQ0, IRQ1, and IRQ2 ……IRQ7. However, if a lower priority IRQ occurred first, even a higher priority IRQ cannot interrupt the existed IRQ. For example, if IRQ4 is occurred first, IRQ3 is unable to interrupt IRQ4. The priority takes over only when two IRQ occurred concurrently. If IRQNEST mode is on, a higher priority IRQ can interrupt the lower priority IRQ occurred first. For example, if IRQ4 is occurred first, IRQ3 is able to interrupt IRQ4. The current interrupts are listed in Table 5-6. In this table, it shows the interrupt sources, interrupt name, IRQ number and FIQ selection.

5.5.1. Interrupt Source

The interrupt may come from the following sources (total 38 sources):

Timer/PWM Module

- Channel 0: TPR_0, TGRA_0, TGRB_0, TGRC_0, Position detection change, overflow, underflow
- Channel 1: TPR_1, TGRA_1, TGRB_1, TGRC_1, Position detection change, overflow, underflow
- Channel 2: TPR_2, TGRA_2, TGRB_2
- Channel 3: TPR_3, TGRD_3
- Channel 4: TPR_4, TGRD_4

Compare Match Timer

- Channel 0: CMT_0 compare match
- Channel 1: CMT_1 compare match

IO

- Key change

A/D Converter

- Conversion finished

External Interrupt

- EXINT0
- EXINT1

Serial Communication Interface

- UART
- SPI

Fault Protection

- FTINT1
- FTINT2
- Output short

Clock Monitoring

- Oscillator fail

Table 5-6 Interrupt sources of each IRQ level

IRQ Level	Register Check Interrupt Flag		Name	Description
IRQ0 (highest)	P_INT_Status.FTIF	or P_Fault1_Ctrl.FTPINIF	FTIN1_INT	Fault input pin 1 interrupt
	P_INT_Status.FTIF	or P_Fault2_Ctrl.FTPINIF	FTIN2_INT	Fault input pin 2 interrupt
	P_INT_Status.FTIF	or P_Fault1_Ctrl.OSF	OS1_INT	Output short 1 interrupt
	P_INT_Status.FTIF	or P_Fault2_Ctrl.OSF	OS2_INT	Output short 2 interrupt
	P_INT_Status.OLIF	or P_OL1_Ctrl.OLIF	OL1_INT	Overload pin 1 interrupt
	P_INT_Status.OLIF	or P_OL2_Ctrl.OLIF	OL2_INT	Overload pin 2 interrupt
	P_INT_Status.OSCSF	or P_Clk_Ctrl. OSCSF	OSCF_INT	Oscillator failed interrupt
IRQ1	P_INT_Status.PDC0IF	or P_TMR0_Status.TPRIF	TPR0_INT	Timer 0 TPR interrupt
	P_INT_Status.PDC0IF	or P_TMR0_Status.TGAIF	TGRA0_INT	Timer 0 TGRA interrupt
	P_INT_Status.PDC0IF	or P_TMR0_Status.TGBIF	TGRB0_INT	Timer 0 TGRB interrupt
	P_INT_Status.PDC0IF	or P_TMR0_Status.TGCIF	TGRC0_INT	Timer 0 TGRC interrupt
	P_INT_Status.PDC0IF	or P_TMR0_Status.PDCIF	PDC0_INT	Timer 0 position detection change interrupt
	P_INT_Status.PDC0IF	or P_TMR0_Status.TCVIF	TCV0_INT	Timer 0 counter overflow interrupt
	P_INT_Status.PDC0IF	or P_TMR0_Status.TCUIF	TUV0_INT	Timer 0 counter underflow interrupt
IRQ2	P_INT_Status.PDC1IF	or P_TMR1_Status.TPRIF	TPR1_INT	Timer 1 TPR interrupt
	P_INT_Status.PDC1IF	or P_TMR1_Status.TGAIF	TGRA1_INT	Timer 1 TGRA interrupt
	P_INT_Status.PDC1IF	or P_TMR1_Status.TGBIF	TGRB1_INT	Timer 1 TGRB interrupt
	P_INT_Status.PDC1IF	or P_TMR1_Status.TGCIF	TGRC1_INT	Timer 1 TGRC interrupt
	P_INT_Status.PDC1IF	or P_TMR1_Status.PDCIF	PDC1_INT	Timer 1 position detection change interrupt
	P_INT_Status.PDC1IF	or P_TMR1_Status.TCVIF	TCV1_INT	Timer 1 counter overflow interrupt
	P_INT_Status.PDC0IF	or P_TMR1_Status.TCUIF	TUV1_INT	Timer 1 counter underflow interrupt
IRQ3	P_INT_Status.MCP3IF	or P_TMR3_Status.TPRIF	TPR3_INT	Timer 3 TPR interrupt
	P_INT_Status.MCP3IF	or P_TMR3_Status.TGDIF	TGRD3_INT	Timer 3 TGRD interrupt
	P_INT_Status.MCP4IF	or P_TMR4_Status.TPRIF	TPR4_INT	Timer 4 TPR interrupt
	P_INT_Status.MCP4IF	or P_TMR4_Status.TGDIF	TGRD4_INT	Timer 4 TGRD interrupt
IRQ4	P_INT_Status.TPM2IF	or P_TMR2_Status.TPRIF	TPR2_INT	Timer 2 TPR interrupt
	P_INT_Status.TPM2IF	or P_TMR2_Status.TGAIF	TGRA2_INT	Timer 2 TGRA interrupt
	P_INT_Status.TPM2IF	or P_TMR2_Status.TGBIF	TGRB2_INT	Timer 2 TGRB interrupt
IRQ5	P_INT_Status.EXT0IF		EXT0_INT	External 0 interrupt
	P_INT_Status.EXT1IF		EXT1_INT	External 1 interrupt
IRQ6	P_INT_Status.UARTIF	or P_UART_Status.RXIF	UART_RX_INT	UART receive complete interrupt
	P_INT_Status.UARTIF	or P_UART_Status.TXIF	UART_TX_INT	UART transmit ready interrupt
	P_INT_Status.SPIIF	or P_SPI_RxStatus.SPIRXIF	SPI_RX_INT	SPI receive interrupt
	P_INT_Status.SPIIF	or P_SPI_TxStatus.SPITXIF	SPI_TX_INT	SPI transmit interrupt
IRQ7 (Lowest)	P_INT_Status.KEYIF		IOKEY_INT	IO Key change interrupt
	P_INT_Status.ADCIF	or P_ADC_Ctrl.ADCIF	ADC_INT	ADC conversion complete interrupt
	P_INT_Status.CMTIF	or P_CMT_Ctrl.CM0IF	CMT0_INT	Compare match timer 0 interrupt
	P_INT_Status.CMTIF	or P_CMT_Ctrl.CM1IF	CMT1_INT	Compare match timer 1 interrupt

5.5.2. Interrupt procedure

When the interrupt event occurred, the status is recorded and cleared only by write “1” to clear.

If the event occurs and interrupt enable bit has been set, the CPU will entering interrupt request (IRQ) procedure as follows:

1. CPU jumps to interrupt vector to look up the address of corresponding interrupt service routine.
2. Push the data in SR (Status register) and the return address in PC (Program Counter register) to stack memory.
3. CPU jumps to the address of service routine to execute program and clear interrupt flag.
4. Pop the data in SR register to restore the system status. Pop the return address to PC.
5. CPU returns to the original address and keep executing the program.

The timing diagram of interrupt procedure and stack operation is as the following Figure 5-11 and Figure 5-12, respectively.

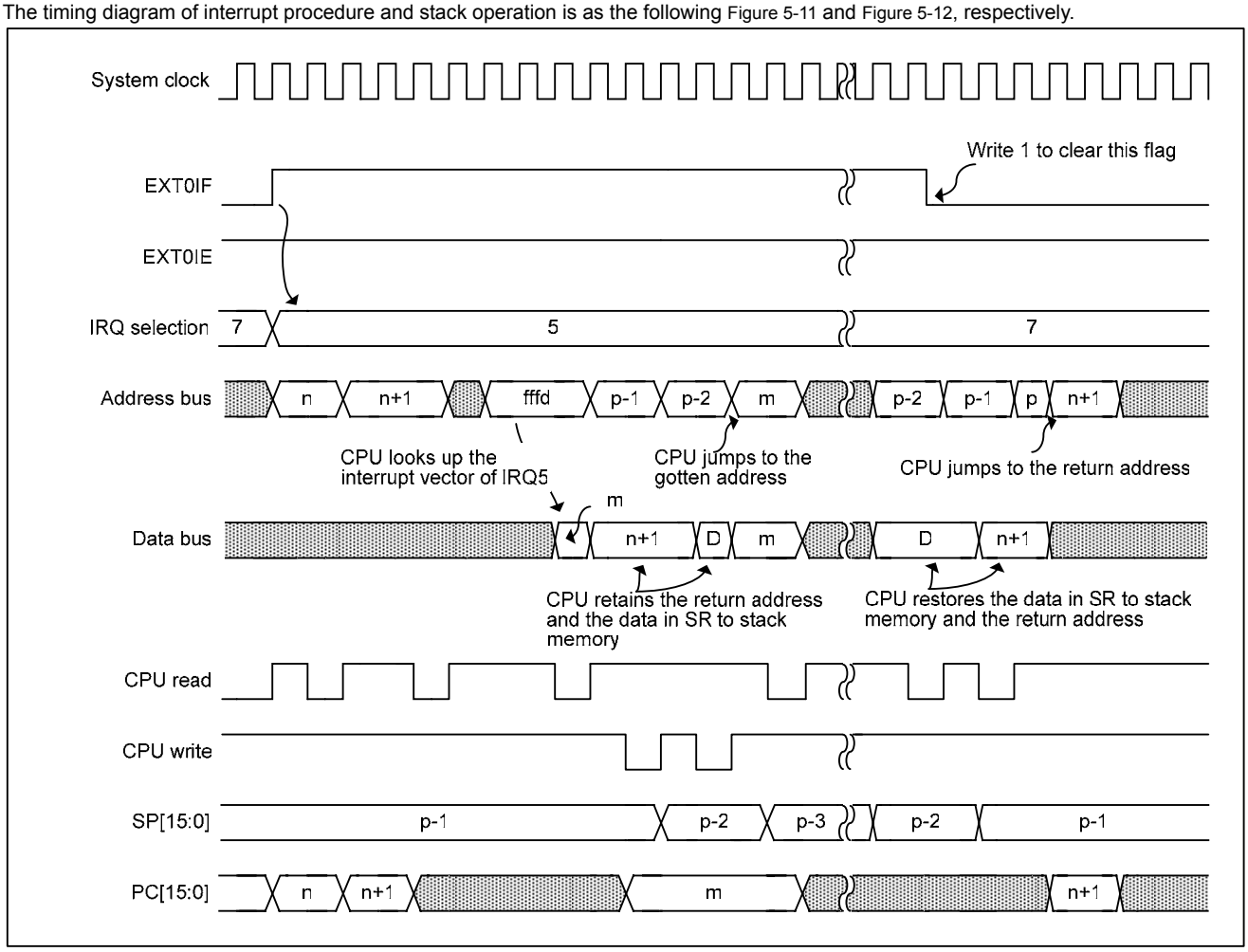


Figure 5-11 Interrupt procedure timing

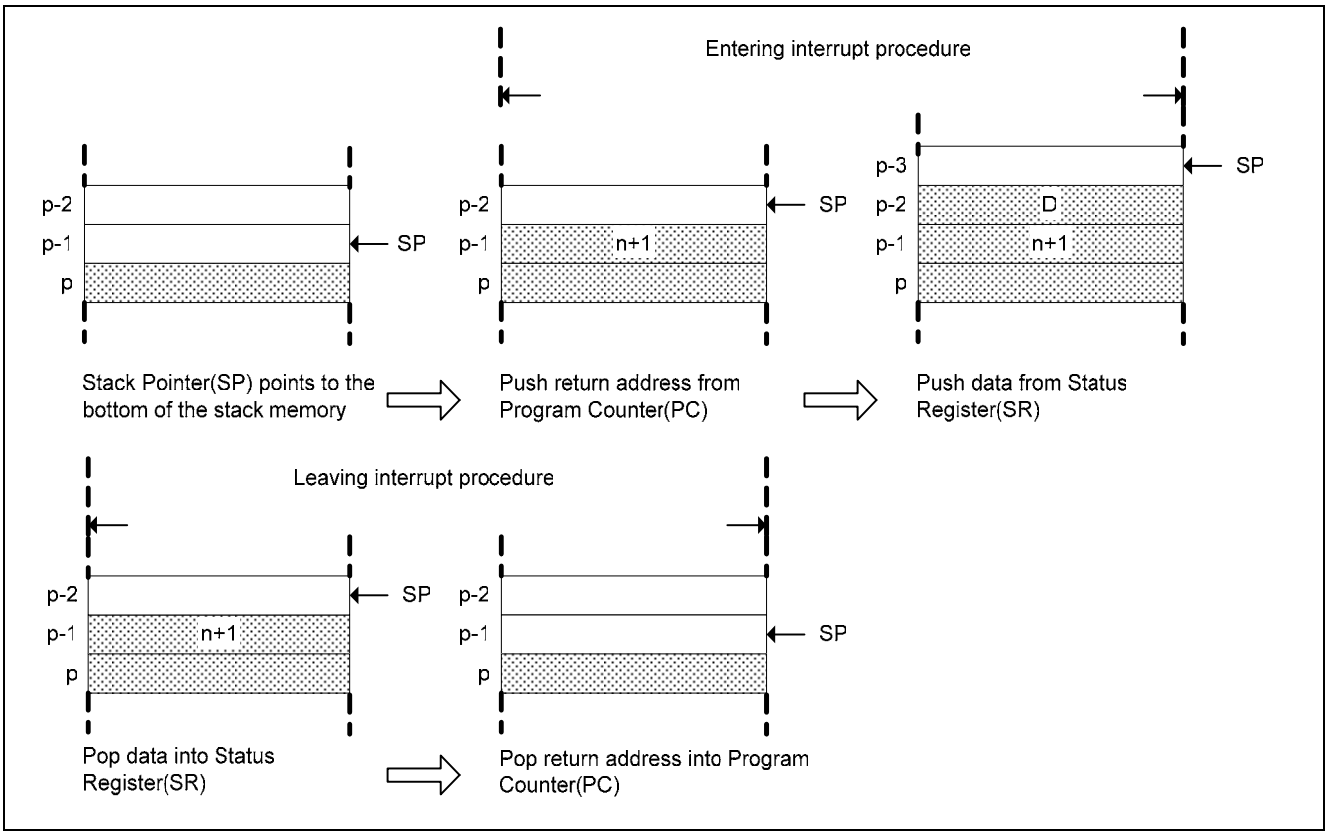


Figure 5-12 Stack memory operation with interrupt procedure

- **P_INT_Status (0x70A0): Interrupt Status Register**

This register is a look-up table for all interrupts status flags. Most status flags are composed of some flags. Please refer to Table 5-6 for detail. Only the KEYIF, EXT1IF and EXT0IF can write '1' to clear these flags. Others are the status flags from other registers and read only.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R	R	R/W	R/W	R	R	R
0	0	0	0	0	0	0	0
KEYIF	UARTIF	SPIIF	EXT1IF	EXT0IF	ADCIF	MCP4IF	MCP3IF

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TPM2IF	PDC1IF	PDC0IF	CMTIF	Reserved	OLIF	OSCSF	FTIF

B15	KEYIF※	Key-change interrupt status flag	0: Not occurred	1: Has occurred
B14	UARTIF	UART interrupt status flag	0: Not occurred	1: Has occurred
B13	SPIIF	SPI interrupt status flag	0: Not occurred	1: Has occurred
B12	EXT1IF※	External interrupt 1 status flag	0: Not occurred	1: Has occurred
B11	EXT0IF※	External interrupt 0 status flag	0: Not occurred	1: Has occurred
B10	ADCIF	A/D-converter interrupt status flag	0: Not occurred	1: Has occurred
B9	MCP4IF	MCP4 Timer 4 interrupt status flag	0: Not occurred	1: Has occurred
B8	MCP3IF	MCP3 Timer 3 interrupt status flag	0: Not occurred	1: Has occurred
B7	TPM2IF	TPM2 Timer 2 interrupt status flag	0: Not occurred	1: Has occurred
B6	PDC1IF	PDC Timer 1 interrupt status flag	0: Not occurred	1: Has occurred

B5	PDC0IF	PDC Timer 0 interrupt status flag	0: Not occurred	1: Has occurred
B4	CMTIF	Compare match timer interrupt status flag	0: Not occurred	1: Has occurred
B3	Reserved			
B2	OLIF	Overload interrupt status flag	0: Not occurred	1: Has occurred
B1	OSCSF	Oscillator status flag	0: Oscillator normal	1: Oscillator failed
B0	FTIF	Fault protection interrupt status flag	0: Not occurred	1: Has occurred

※: write '1' to clear this flag

- **P_INT_Priority (0x70A4): IRQ and FIQ Priority Selection Register**

This port can set interrupt source as IRQ or FIQ. The default set as FIQ at P_INT_Priority. interrupt source is IRQ. Note: Only one of interrupt source can be

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
KEYIP	UARTIP	SPIIP	Reserved	EXTIP	ADCIP	MCP4IP	MCP3IP

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R	R	R/W	R/W
0	0	0	0	0	0	0	0
TPM2IP	PDC1IP	PDC0IP	CMTIP	Reserved	OLIP	OSCIP	FTIP

B15	KEYIP	Key-change interrupt priority select bit	0: IRQ7	1: FIQ
B14	UARTIP	UART interrupt priority select bit	0: IRQ6	1: FIQ
B13	SPIIP	SPI interrupt priority select bit	0: IRQ6	1: FIQ
B12	Reserved			
B11	EXTIP	External interrupt priority select bit	0: IRQ5	1: FIQ
B10	ADCIP	ADC interrupt priority select bit	0: IRQ7	1: FIQ
B9	MCP4IP	MCP Timer 4 interrupt priority select bit	0: IRQ3	1: FIQ
B8	MCP3IP	MCP Timer 3 interrupt priority select bit	0: IRQ3	1: FIQ
B7	TPM2IP	TPM Timer 2 interrupt priority select bit	0: IRQ4	1: FIQ
B6	PDC1IP	PDC Timer 1 interrupt priority select bit	0: IRQ2	1: FIQ
B5	PDC0IP	PDC Timer 0 interrupt priority select bit	0: IRQ1	1: FIQ
B4	CMTIP	CMT interrupt priority select bit	0: IRQ7	1: FIQ
B3	Reserved			
B2	OLIP	Overload interrupt priority select bit	0: IRQ0	1: FIQ
B1	OSCIP	Oscillator fail interrupt priority select bit	0: IRQ0	1: FIQ
B0	FTIP	Fault protection interrupt priority select bit	0: IRQ0	1: FIQ

- **P_MisINT_Ctrl (0x70A8): Miscellaneous Interrupt Control Register**

This port can be set to enable interrupt. Write "1" to any bit to enable the interrupt.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R	R	R
0	0	0	0	0	0	0	0
KEYIE	EXT1MS	EXT0MS	EXT1IE	EXT0IE	Reserved		

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B15	KEYIE	Key-change interrupt enable bit	0: Disable	1: Enable
B14	EXT1MS	External interrupt 1 trigger edge select bit	0: Falling edge trigger	1: Rising edge trigger
B14	EXT0MS	External interrupt 0 trigger edge select bit	0: Falling edge trigger	1: Rising edge trigger
B12	EXT1IE	External interrupt 1 enable bit	0: Disable	1: Enable
B11	EXT0IE	External interrupt 0 enable bit	0: Disable	1: Enable
B10-B0	Reserved			

5.6. Reset Management

In SPMC75F2413A, the reset logic is used for leading MCU into a known state when device operates abnormally. The source of reset can be determined by using the reset status bits. The reset circuit can be used for increasing system reliability.

5.6.1. Power on reset (POR)

A power-on reset is generated when VDD rising is detected. When VDD is rising to acceptable level, the power-up timer starts counting. After finish counting 16384 crystal clock ticks, system reset will be released and CPU starts operating.

5.6.2. External reset

By pulling external reset pin RESETB to VSS, system reset will be generated and will be released after 16384 crystal clocks.

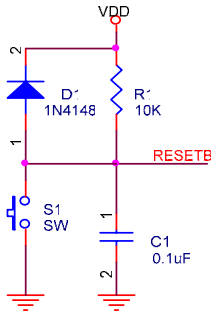


Figure 5-13 External reset circuit

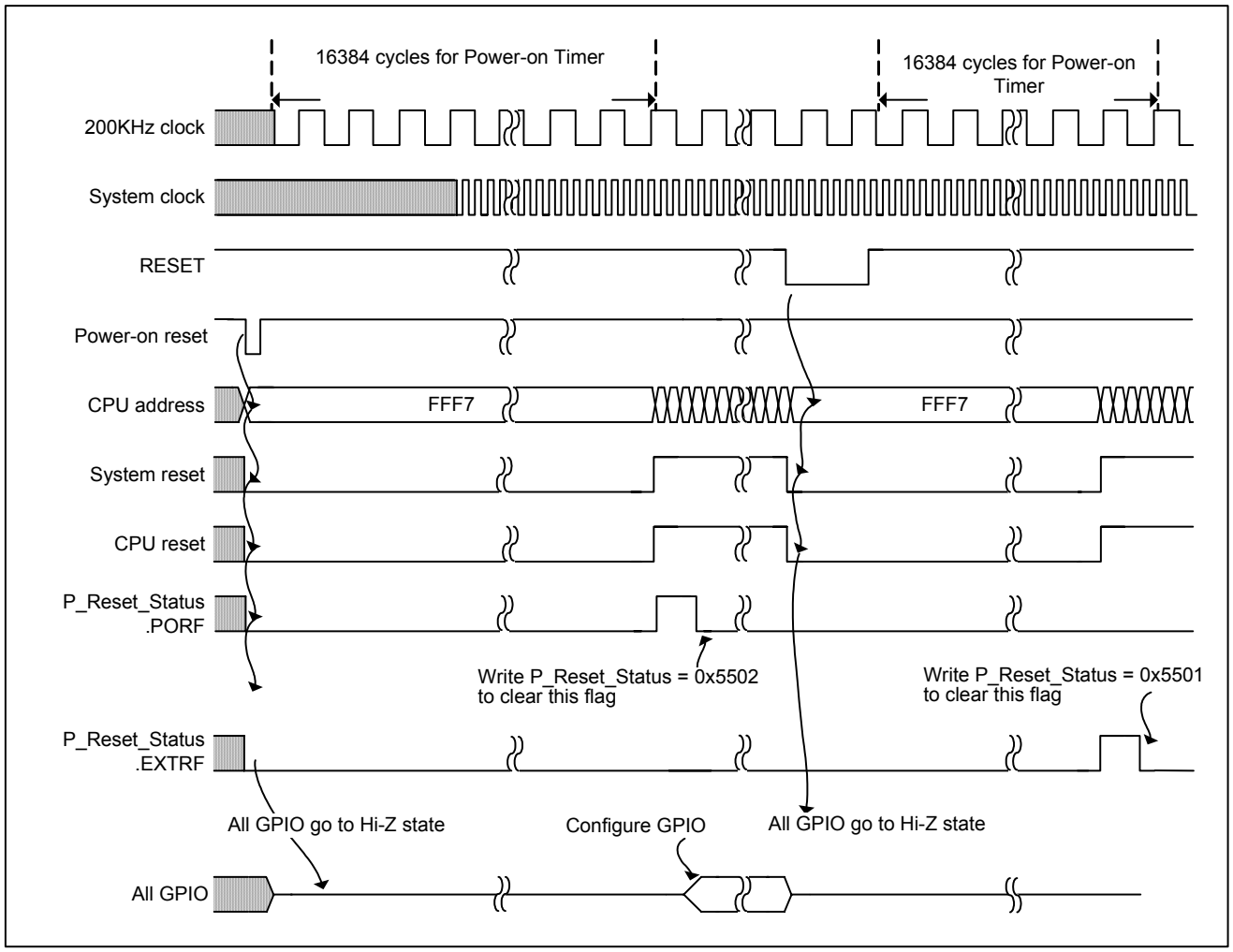


Figure 5-14 Power-on reset, external reset and power-up timer timing

5.6.3. Low voltage reset (LVR)

When power supply voltage drops below 4.09V, a low voltage reset will be issued. When LVR is asserted, a system reset will be generated. CPU and all peripherals will be reset. When supply voltage up to 4.19V, device will leave reset status. Figure 5-15 shows the low voltage reset timing.

5.6.4. Watchdog timer reset (WDTR)

On-chip watchdog circuitry makes the device entering into reset when the MCU goes into unknown state and without any watchdog clearance. This function ensures the MCU does not continue to work in abnormal condition. When "0xA005" is written into P_WatchDog_Clr(W) (0x700B), the watchdog timer will be cleared and continue to count. If P_WatchDog_Clr is not written between watchdog overflow intervals, the device will be forced into reset state.

Figure 5-16 shows the watchdog timer reset timing.

5.6.5. Illegal address reset (IAR)

The device offers an illegal address reset for preventing system from accessing illegal address. When an illegal address is being accessed, a CPU reset will be generated.

Figure 5-17 shows illegal address reset timing.

5.6.6. Illegal instruction reset (IIR)

When an invalid instruction is being decoded by CPU, an illegal instruction reset will be issued and reset CPU.

Figure 5-18 shows the illegal instruction reset timing.

Following table shows the effected modules of different reset sources.

Table 5-7 Reset source and effected modules

Reset Source	CPU	Peripheral
External Reset Pin	V	V
Power-on Reset	V	V
Watchdog Reset	V	Option※
Low Voltage Reset	V	V

Reset Source	CPU	Peripheral
Illegal Address Reset	V	-
Illegal Instruction Reset	V	-

※ Please refer to P_WatchDog_Ctrl for details

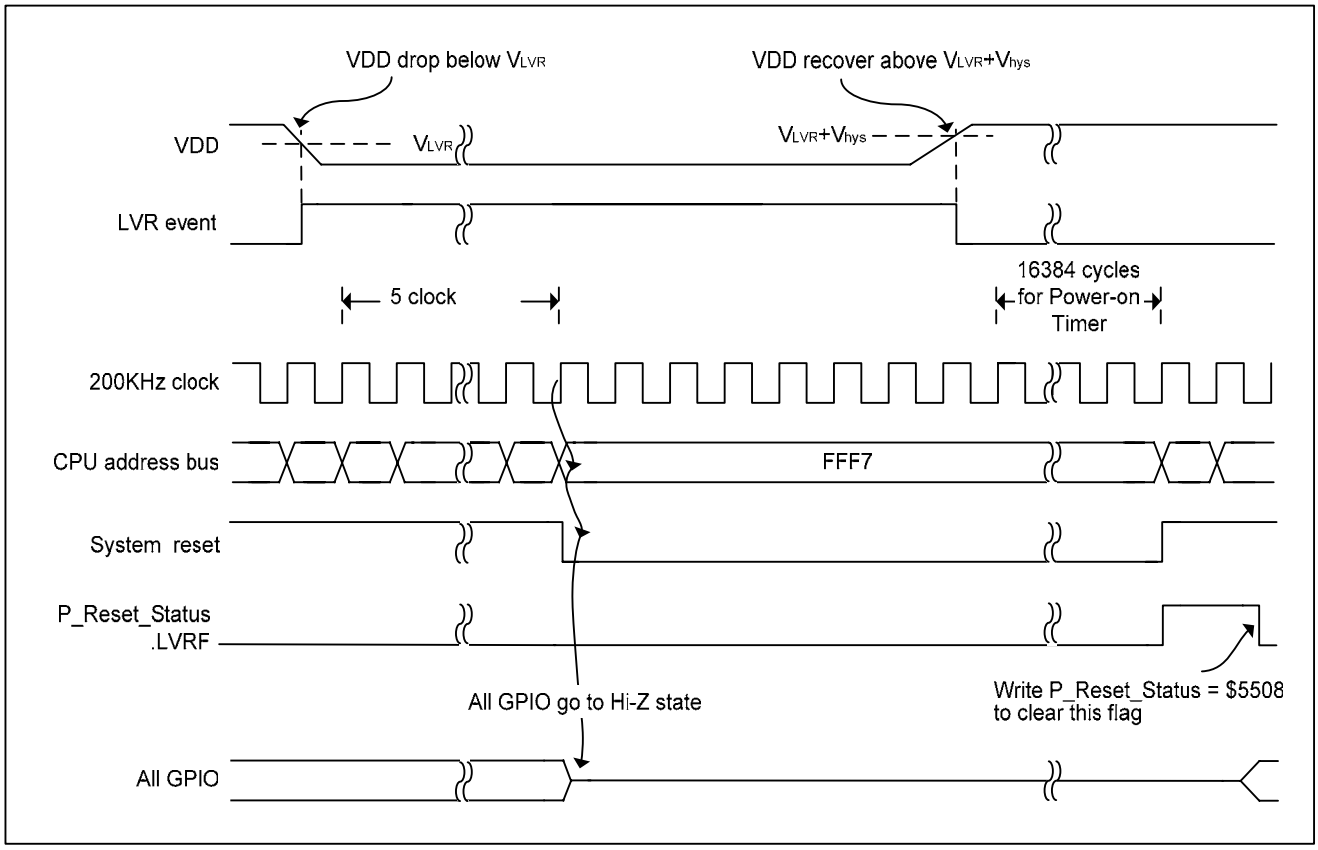


Figure 5-15 Low voltage reset timing

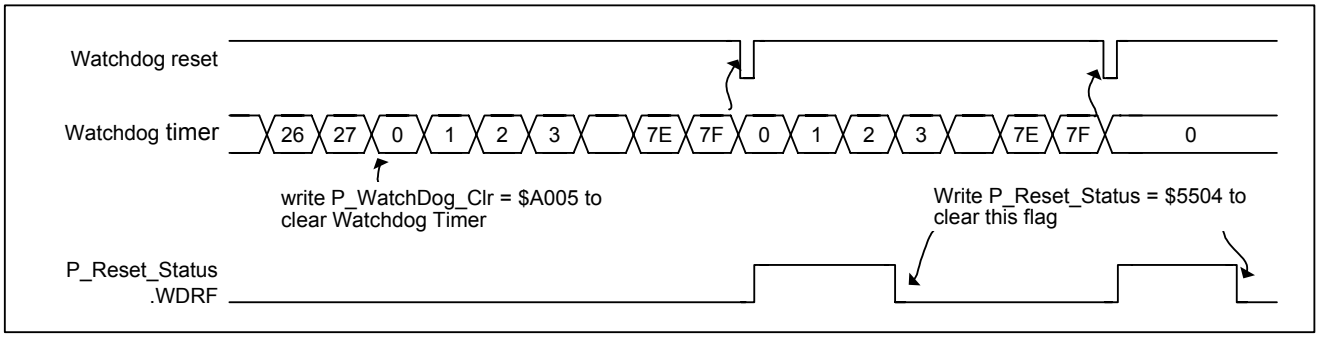


Figure 5-16 Watchdog timer reset timing

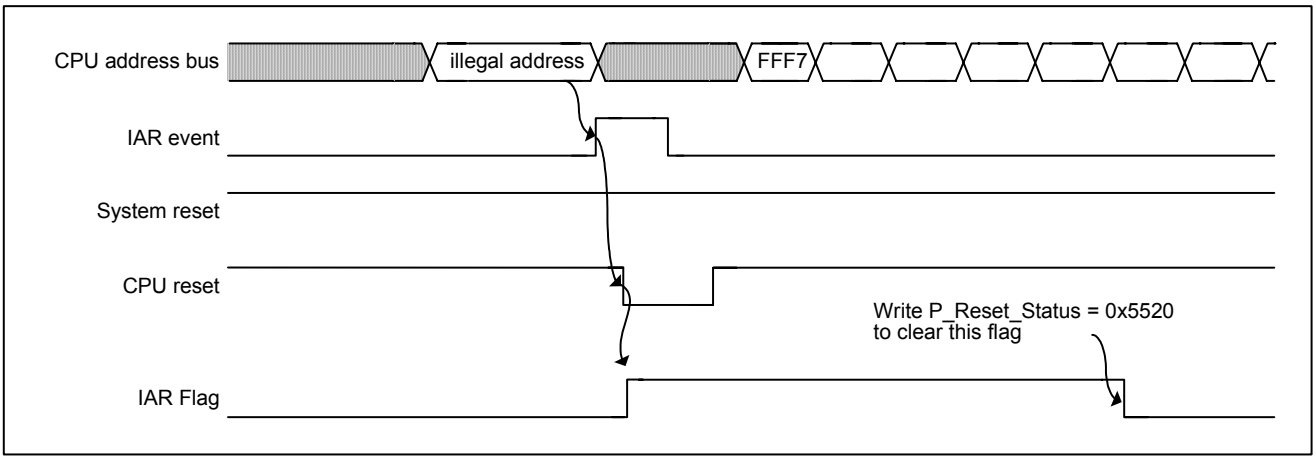


Figure 5-17 Illegal address reset timing

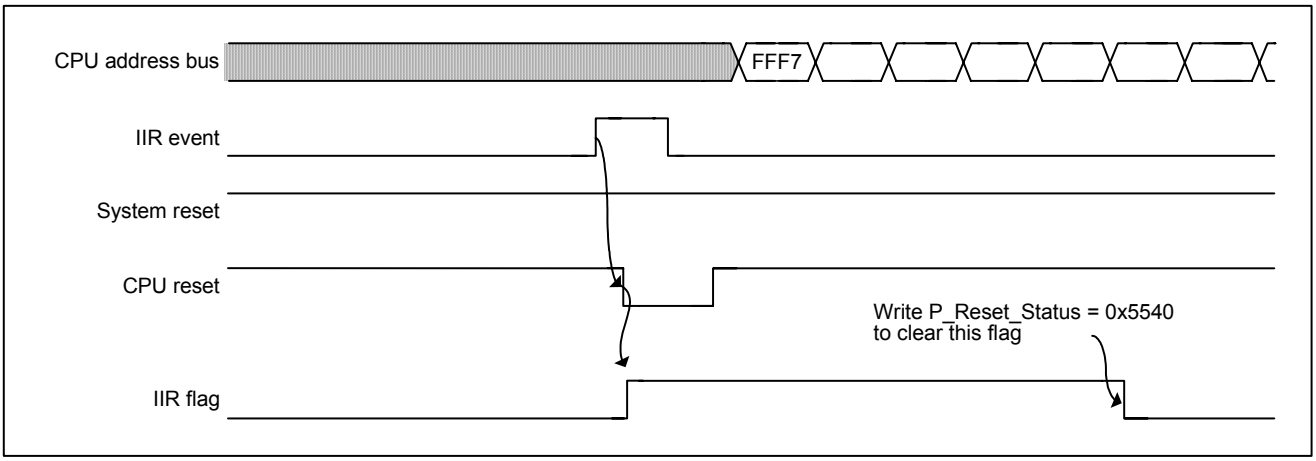


Figure 5-18 Illegal instruction reset timing

- **P_Reset_Status(0x7006): Reset Status Register**

This register shows the flag of reset status for firmware checking.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
FCHK							

B7	B6	B5	B4	B3	B2	B1	B0
R	R/W	R/W	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved	IIRF	IARF	Reserved	LVRF	WDRF	PORF	EXTRF

B15-8	FCHK	Flag clear check bits pattern. To properly clear reset flags, these bits must be written to '0x55'. Otherwise, the flags will not be cleared. These bits will be read as '0'.		
B7	Reserved			
B6	IIRF	Illegal instruction reset flag	0: Not occurred	1: Occurred
B5	IARF	Illegal address reset flag	0: Not occurred	1: Occurred
B4	Reserved			
B3	LVRF	Low voltage reset flag	0: Not occurred	1: Occurred
B2	WDRF	Watchdog reset flag	0: Not occurred	1: Occurred

B1	PORF	Power-on reset flag	0: Not occurred	1: Occurred
B0	EXTRF	External reset pin reset flag		

5.7. General Purpose I/O Ports (GPIO)

General purpose I/O ports allow the device to communicate with other devices. To add flexibility and functionality to a device, some parts of I/O pins are multiplexed with an alternative function. These functions can be switched through appropriate registers. For most general I/O ports, the I/O structure contains five parts: data, buffer, direction, attribution, latch and special function enable registers.

Four programmable I/O ports are available in the device: Port A, Port B, Port C, and Port D. Each I/O pin on these 4 ports can be bit-by-bit configured by software programming. Except Port D, almost every I/O pin on these 4 ports can be programmed as special function. In other words, many special function control signals share with I/O ports.

Table 5-9 shows the I/O configurations and

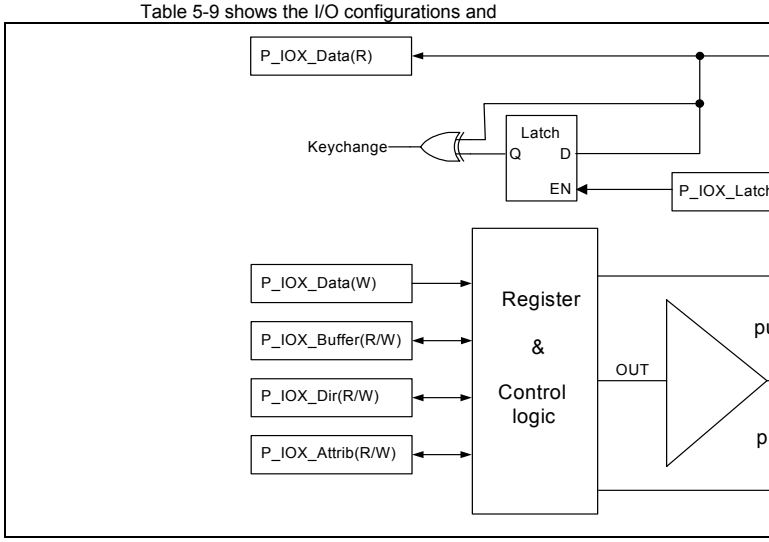


Figure 5-19 shows the structure of a typical I/O ports. The open-drain configuration can be achieved by setting the registers of direction, attribution and buffer as the following table.

Table 5-8 Open-drain Configuration

Direction	Attribution	Buffer	Open drain Function
0	1	0	Output high
1	1	0	Output low

Table 5-9 I/O Configuration

Direction	Attribution	Data	Function	Keychange	Description
0	0	0	Pull Low	Yes	Input with pull low
0	0	1	Pull High	Yes	Input with pull high
0	1	0	Float※	Yes	Input with float
0	1	1	Float	No	Input with float
1	0	0	Inverted	No	Output with data inverted (write “0” to the Data Port and will output “1” to the I/O pad)
1	0	1	Inverted	No	Output with data inverted (write “1” to the Data Port and will output “0” to the I/O pad)
1	1	0	Not Inverted	No	Output with buffer (data not inverted)
1	1	1	Not Inverted	No	Output with buffer (data not inverted)

※Default: Input with floating when power on

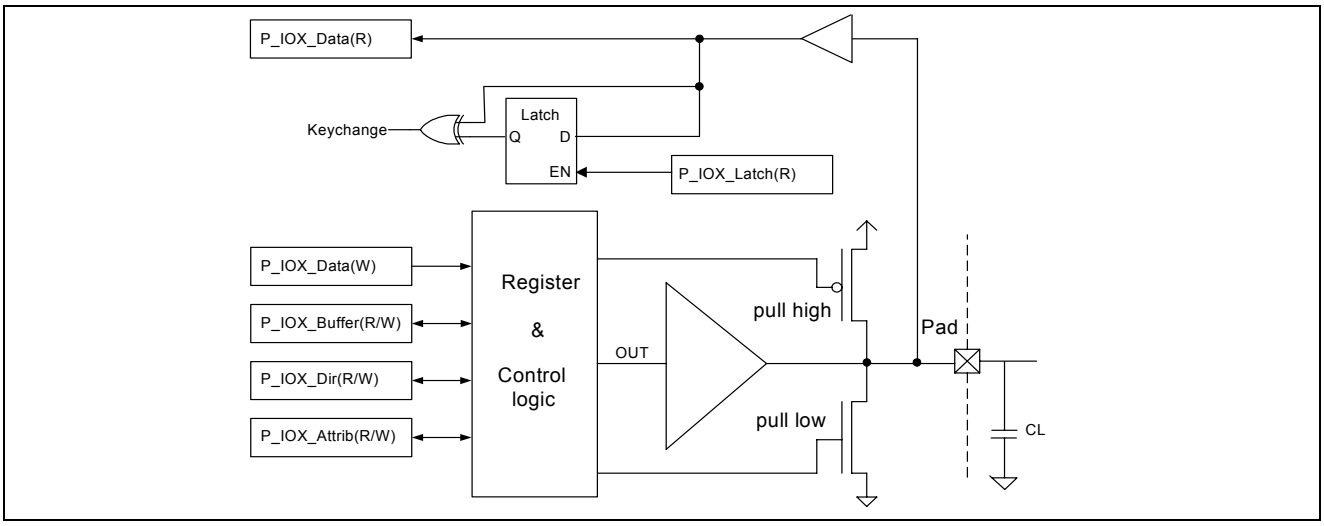


Figure 5-19 IO structure diagram

All output ports contain a register P_IOx_Buffer (x=A,B,C,D). Therefore, the output data are retained by the register. There are two methods to write data into P_IOx_Buffer. One is P_IOx_Buffer(W), the other is P_IOx_Data(W) (x=A,B,C,D). P_IOx_Data(W) and P_IOx_Buffer(W) have the same result exactly. However, P_IOx_Buffer(R) reads the data stored in P_IOx_Buffer. P_IOx_Data(R) reads the input port: Port A, Port B, PortC and PortD, respectively. As a result, user should pay more attention to the operations on P_IOx_Data. For example, the data in P_IOx_Buffer and data from P_IOx_Data(R) may be different. The P_IOx_Buffer will be altered incorrectly if the bit operations SETB, CLRB and INVB are performed on P_IOx_Data. Therefore, it is suggested that user should perform the bit operations on P_IOx_Buffer (x=A,B,C,D) exclusively.

Please refer to Figure 5-20. None of the input ports has a register. Therefore, the input data is desirable to be retained on the input port until it is read in, or read several times and acquire average data before being processed. The input/output timing of Port A is shown as follows.

Large Driving Pins

IOA[15:8], IOB[15:12], IOB[5:0], IOC[3:0], and IOC[15:10], total 28 I/O ports support large-current output capability that can direct drive LED.

Key-change Interrupt Pins

There are 8 I/O ports, IOA[15:8], support key-change function. Each I/O port can be enable/disable separately. The key-change function is enabled by setting the appropriate direction, attribution and buffer configuration as listed on Table 5-9 and setting P_IOA_KCER to enable the IO port used as key-change source. Next, P_IOA_Latch(R) should be performed to latch the value of Port A. The key-change event occurs if the Port A is different from the value that have stored into P_IOA_Latch. Additionally, the key-change event occurs once until P_IOA_Latch(R) is performed again, which is called one shot. The operation of key-change IOA15 is shown as Figure 5-21.

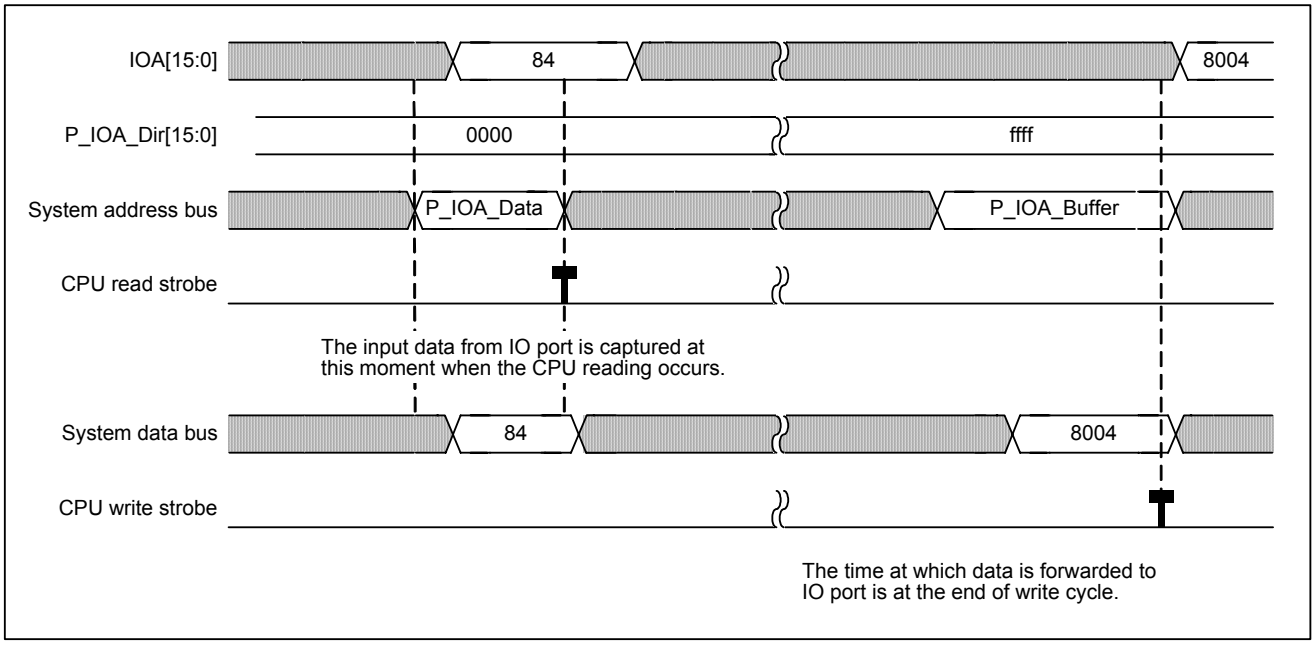


Figure 5-20 GPIO input/output timing

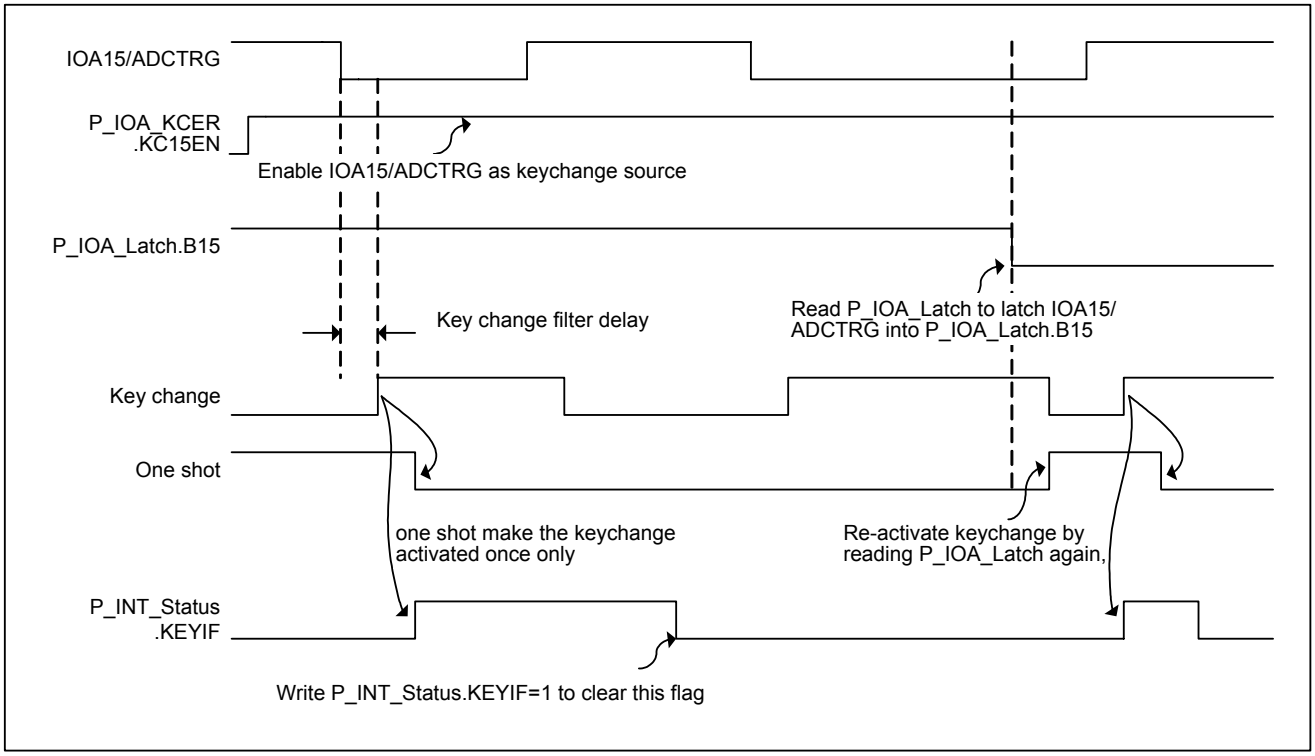


Figure 5-21 Keychange timing

- **P_IOA_Data (0x7060)：IO Port A Data Register**

Write data into the data register and read data from the I/O pad. Writing data into P_IOA_Data will be the same as writing into P_IOA_Buffer. To prevent unwanted operation at unmodified bit data, bit operation instruction should apply at P_IOA_Buffer instead of P_IOA_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOA_Data							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOA_Data							

- **P_IOA_Buffer (0x7061)：IO Port A Buffer Register**

Reading means to read data from data register. Write data into P_IOA_Buffer will be the same as writing into P_IOA_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOA_Buffer							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOA_Buffer							

Note: The reading of P_IOA_Data (R)(0x7060) and P_IOA_Buffer (R)(0x7061) is through different physical path. The data is from I/O pad by reading P_IOA_Data (R)(0x7060). The data is form I/O buffer by reading P_IOA_Buffer (R)(0x7061).

- **P_IOA_Dir (0x7062)：IO Port A Direction Register**

Read/Write direction vector from/into the Direction Register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOA_Dir							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOA_Dir							

- **P_IOA_Attrib (0x7063)：IO Port A Attribute Register**

Read/Write attribute vector from/into the Attribute Register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOA_Attrib							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOA_Attrib							

- **P_IOA_Latch (0x7064)：IO Port A Latch Register**

Read this port to latch data on the I/O PortA for key change wakeup before getting into sleep mode.

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
P_IOA_Latch							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

- **P_IOA_SPE (0x7080)：IO Port A Special Function Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R/W	R/W	R/W	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0
Reserved	TCLKDEN	TCLKCEN	TCLKBEN	TCLKAEN	TIO2BEN	TIO2AEN	Reserved

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B15	Reserved			
B14	TCLKDEN	External clock D input pin	0: Disable	1: Enable
B13	TCLKCEN	External clock C input pin	0: Disable	1: Enable
B12	TCLKBEN	External clock B input pin	0: Disable	1: Enable
B11	TCLKAEN	External clock A input pin	0: Disable	1: Enable
B10	TIO2BEN	P_TMR2_TGRB input capture input/PWM output enable	0: Disable	1: Enable
B9	TIO2AEN	P_TMR2_TGRA input capture input/PWM output enable	0: Disable	1: Enable
B8-0	Reserved			

- **P_IOA_KCER (0x7084)：IO Port A Key Change Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
KC15EN	KC14EN	KC13EN	KC12EN	KC11EN	KC10EN	KC9EN	KC8WE

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B15	KC15EN	PortA.15 Key change enable	0: Disable	1: Enable
B14	KC14EN	PortA.14 Key change enable	0: Disable	1: Enable
B13	KC13EN	PortA.13 Key change enable	0: Disable	1: Enable
B12	KC12EN	PortA.12 Key change enable	0: Disable	1: Enable
B11	KC11EN	PortA.11 Key change enable	0: Disable	1: Enable
B10	KC10EN	PortA.10 Key change enable	0: Disable	1: Enable
B9	KC9EN	PortA.9 Key change enable	0: Disable	1: Enable
B8	KC8EN	PortA.8 Key change enable	0: Disable	1: Enable
B7-0	Reserved			

- **P_IOB_Data (0x7068)：IO Port B Data Register**

Write data into data register and read from I/O pad. Writing data into P_IOB_Data will be the same as writing into P_IOB_Buffer. To prevent unwanted operation at unmodified bit data, bit operation instruction should apply at P_IOB_Buffer instead of P_IOB_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOB_Data							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOB_Data							

- **P_IOB_Buffer (0x7069)：IO Port B Buffer Register**

Write data into the data register and read data from the I/O buffer. Writing data into P_IOB_Buffer will be the same as writing into P_IOB_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOB_Buffer							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOB_Buffer							

Note: The reading of P_IOB_Data (R)(0x7068) and P_IOB_Buffer (R)(0x7069) is through different physical path. The data is from I/O pad by reading P_IOB_Data (R)(0x7068). The data is form I/O buffer by reading P_IOB_Buffer (R)(0x7069).

- **P_IOB_Dir (0x706A)：IO Port B Direction Register**

Read/Write direction vector from/into the Direction Register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOB_Dir							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOB_Dir							

- **P_IOB_Attrib (0x706B)：IO Port B Attribute Register**

Read/Write attribute vector from/into the Attribute Register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOB_Attrib							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOB_Attrib							

- **P_IOB_SPE (0x7081)：IO Port B Special Function Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved					TIO0AEN	TIO0BEN	TIO0CEN

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	1	1	1	1	1
OL1EN	FTIN1EN	U1EN	V1EN	W1EN	U1NEN	V1NEN	W1NEN

B15-11	Reserved			
B10	TIO0AEN	P_TMR0_TGRA input capture input/PWM output pin or position detection input enable	0: Disable	1: Enable
B9	TIO0BEN	P_TMR0_TGRB input capture input/PWM output pin or position detection input enable	0: Disable	1: Enable
B8	TIO0CEN	P_TMR0_TGRC input capture input/PWM output pin or position detection input enable	0: Disable	1: Enable
B7	OL1EN	Overload protection input 1 enable	0: Disable	1: Enable
B6	FTIN1EN	External fault protection input 1 enable	0: Disable	1: Enable
B5	U1EN	U1 pin mode selection	0: GPIO	1: U1 phase
B4	V1EN	V1 pin mode selection	0: GPIO	1: V1 phase
B3	W1EN	W1 pin mode selection	0: GPIO	1: W1 phase
B2	U1NEN	U1N pin mode selection	0: GPIO	1: U1N phase
B1	V1NEN	V1N pin mode selection	0: GPIO	1: V1N phase
B0	W1NEN	W1N pin mode selection	0: GPIO	1: W1N phase

- **P_IOC_Data (0x7070)：IO Port C Data Register**

Write data into data register and read from I/O pad. Writing data into P_IOC_Data will be the same as writing into P_IOC_Buffer. To prevent unwanted operation at unmodified bit data, bit operation instruction should apply at P_IOC_Buffer instead of P_IOC_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOC_Data							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOC_Data							

- **P_IOC_Buffer (0x7071)：IO Port C Buffer Register**

Write data into the data register and read data from the I/O buffer. P_IOC_Data.

Writing data into P_IOC_Buffer will be the same as writing into

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOC_Buffer							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOC_Buffer							

Note: The reading of P_IOC_Data (R)(0x7070) and P_IOC_Buffer (R)(0x7071) is through different physical path. The data is from I/O pad by reading P_IOC_Data (R)(0x7070). The data is form I/O buffer by reading P_IOB_Buffer (R)(0x7071)

- **P_IOC_Dir (0x7072)：IO Port C Direction Register**

Read/Write direction vector from/into the direction register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOC_Dir							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOC_Dir							

- **P_IOC_Attrib (0x7073)：IO Port C Attribute Register**

Read/Write attribute vector from/into the Attribute Register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOC_Attrib							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOC_Attrib							

- **P_IOC_SPE (0x7082)：IO Port C Special Function Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	0	0
W2NEN	V2NEN	U2NEN	W2EN	V2EN	U2EN	FTIN2EN	OL2EN

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TIO1CEN	TIO1BEN	TIO1AEN	Reserved	EXINT1EN	EXINT0EN	Reserved	

B15	W2NEN	W2N pin mode selection	0: GPIO	1: W2N phase
B14	V2NEN	V2N pin mode selection	0: GPIO	1: V2N phase
B13	U2NEN	U2N pin mode selection	0: GPIO	1: U2N phase
B12	W2EN	W2 pin mode selection	0: GPIO	1: W2 phase
B11	V2EN	V2 pin mode selection	0: GPIO	1: V2 phase
B10	U2EN	U2 pin mode selection	0: GPIO	1: U2 phase
B9	FTIN2EN	External fault protection input 2 enable	0: Disable	1: Enable
B8	OL2EN	Overload protection input 2 enable	0: Disable	1: Enable
B7	TIO1CEN	P_TMR1_TGRC input capture input/PWM output pin or position detection input enable	0: Disable	1: Enable
B6	TIO1BEN	P_TMR1_TGRB input capture input/PWM output pin or position detection input enable	0: Disable	1: Enable
B5	TIO1AEN	P_TMR1_TGRA input capture input/PWM output pin or position detection input enable	0: Disable	1: Enable
B4	Reserved			
B3	EXINT1EN	External interrupt input 1 enable	0: Disable	1: Enable
B2	EXINT0EN	External interrupt input 0 enable	0: Disable	1: Enable
B1-0	Reserved			

- **P_IOD_Data (0x7078)：IO Port D Data Register**

Write data into data register and read from I/O pad. Write data into P_IOD_Data will be the same as writing into P_IOD_Buffer. To prevent unwanted operation at unmodified bit data, bit operation instruction should apply at P_IOD_Buffer instead of P_IOD_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOD_Data							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOD_Data							

- **P_IOD_Buffer (0x7079)：IO Port D Buffer Register**

Write data into the data register and read data from the I/O buffer. Writing data into P_IOD_Buffer will be the same as writing into P_IOD_Data.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOD_Buffer							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOD_Buffer							

Note: The reading of P_IOD_Data (R)(0x7078) and P_IOD_Buffer (R)(0x7079) is through different physical path. The data is from I/O pad by reading P_IOD_Data (R)(0x7078). The data is form I/O buffer by reading P_IOD_Buffer (R)(0x7079).

- **P_IOD_Dir (0x707A)：IO Port D Direction Register**

Read/Write direction vector from/into the direction register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOD_Dir							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
P_IOD_Dir							

- **P_IOD_Attrib (0x707B)：IO Port D Attribute Register**

Read/Write attribute vector from/into the Attribute Register.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOD_Attrib							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
P_IOD_Attrib							

5.8. Timer/PWM Module (TPM)

There are five TPM timer channels (PDC0, PDC1, TPM2, MCP3, and MCP4) on the SPMC75F2413A chip. MCP3 and MCP4 timer channels provide two sets of full function for three-phase, six independent PWM output capabilities. PDC0 and PDDC1 timer channels include the three programmable special function pins for input capture, output compare, PWM output, and position detection circuits. TPM2 is a general-purpose timer with input capture, compare output and PWM output capability. All of these TPM timers provide independent time base at different input clock sources. Features are listed below.

- Maximum 20 programmable PWM output pins (channel 0-4) / 8 input capture pins (channel 0-2)
- Maximum two set of 6-phase PWM output is possible to drive two AC induction or brush-less DC motors simultaneously (channel 3 and 4)
- Eight counter input clock selection for each channel
- A/D converter conversion start trigger can be generated
- PDC0 and 1 each supports 3-channel input capture, compare output, and PWM output function
- PDC0 and 1 each supports phase counting mode for quadrature phase encoder inputs
- PDC0 and 1 also support position detection function for motor control applications
- TPM2 supports 2-channel input capture, compare output, and PWM output function
- MCP3 and 4 contains PWM or logic level waveform outputs, dead-time generation, fault protection, and overload protection function
- Interrupt logics for PDC0, PDC1, TPM2, MCP3 and MCP4.

5.9. PDC TIMER 0 AND 1

5.9.1. Module Introduction

SPMC75F2413A provides two channels of 16 bit PDC (Phase Detection Control, PDC) timers used for capture function and PWM operation. In addition, supports position detection features for Brushless-DC motor application. The PDC timers are very useful for mechanical speed calculation including ACI and BLDC motor. For BLDC motor, its commutation for change current conduction is according to position information. Figure 5-22 shows the block diagram of entire PDC timers, channel 0 and channel 1. For details of PDC timer specification, please refer to Table 5-10.

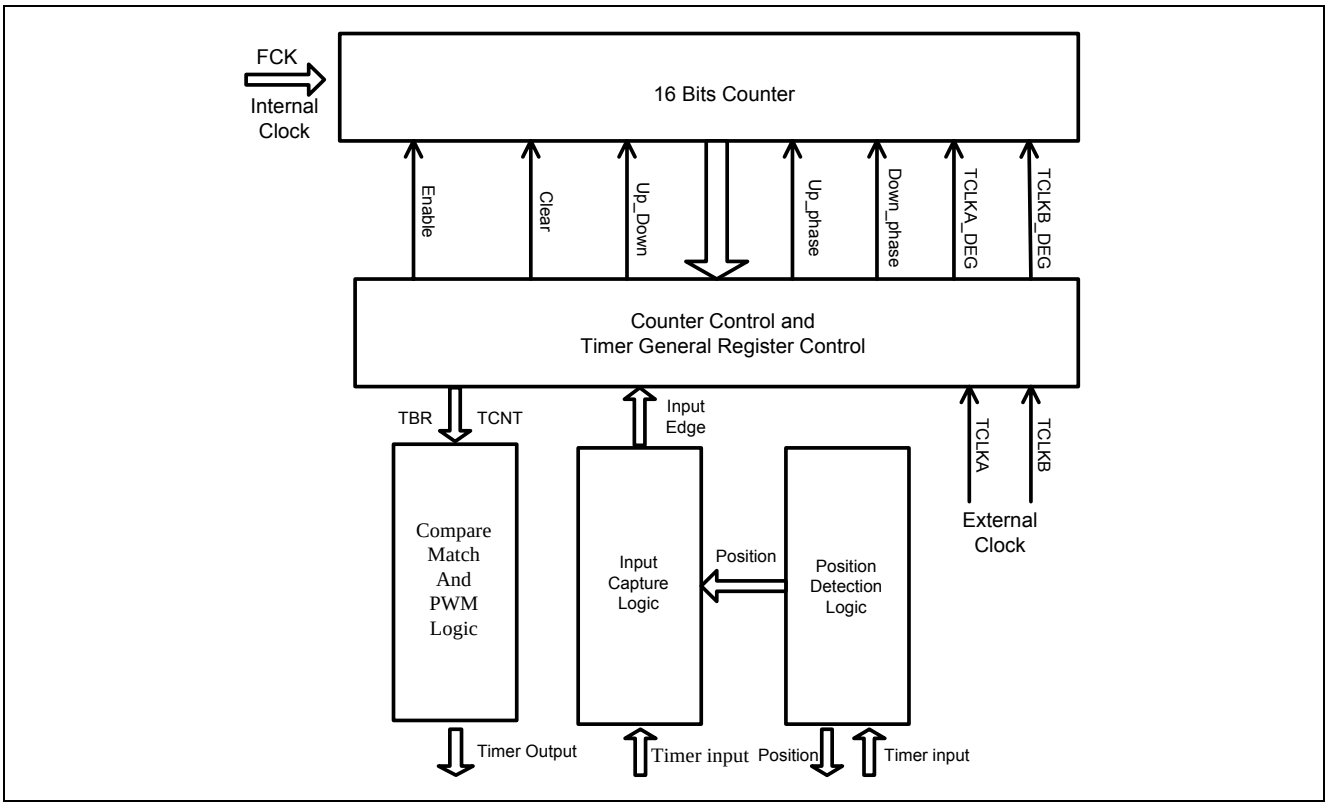


Figure 5-22 PDC timers block diagram

Table 5-10 PDC timers specification

Function	PDC Timer 0	PDC Timer 1
Clock sources	Internal clock: FCK/1, FCK/4, FCK/16, FCK/64, FCK/256, FCK/1024 External clock: TCLKA, TCLKB	
IO pins	♦ TIO0A ♦ TIO0B ♦ TIO0C	♦ TIO1A ♦ TIO1B ♦ TIO1C
Timer general register	♦ P_TMR0_TGRA ♦ P_TMR0_TGRB ♦ P_TMR0_TGRC	♦ P_TMR1_TGRA ♦ P_TMR1_TGRB ♦ P_TMR1_TGRC
Timer buffer register	♦ P_TMR0_TBRA ♦ P_TMR0_TBRB ♦ P_TMR0_TBRC	♦ P_TMR1_TBRA ♦ P_TMR1_TBRB ♦ P_TMR1_TBRC
Timer period and counter register	♦ P_TMR0_TPR ♦ P_TMR0_TCNT	♦ P_TMR1_TPR ♦ P_TMR1_TCNT
Capture sample clock	Internal clock: FCK/1, FCK/2, FCK/4, FCK/8	
Counting edge	♦ Rising ♦ Falling ♦ Both edge	
Counter clear source	♦ Cleared on TIO0A, TIO0B, and TIO0C capture input. ♦ Cleared on P_POS0_DectData position detection data changes. ♦ Cleared on P_TMR0_TPR compare matches.	♦ Cleared on TIO1A, TIO0B, and TIO0C capture input. ♦ Cleared on P_POS1_DectData position detection data changes. ♦ Cleared on P_TMR1_TPR compare matches.
Input capture function	Yes	Yes

Function		PDC Timer 0	PDC Timer 1
PWM compare match output function	1 output	Yes	Yes
	0 output	Yes	Yes
	Output Hold	Yes	Yes
Edge-aligned PWM		Yes	Yes
Center-aligned PWM		Yes	Yes
Phase counting mode		Yes, phase inputs are TCLKA/TCLKB	Yes, phase inputs are TCLKC/TCLKD
Timer buffer operation		Yes	Yes
AD convert start trigger		P_TMR0_TGRA compare match	P_TMR1_TGRA compare match
Interrupt sources		♦ Timer 0 TPR interrupt ♦ Timer 0 TGRA interrupt ♦ Timer 0 TGRB interrupt ♦ Timer 0 TGRC interrupt ♦ Timer 0 PDC interrupt ♦ Timer 0 overflow interrupt ♦ Timer 0 underflow interrupt	♦ Timer 1 TPR interrupt ♦ Timer 1 TGRA interrupt ♦ Timer 1 TGRB interrupt ♦ Timer 1 TGRC interrupt ♦ Timer 1 PDC interrupt ♦ Timer 1 overflow interrupt ♦ Timer 1 underflow interrupt

5.9.2. PDC Timer Counting Operation

Each on-chip PDC timer has the following five possible counting operations：

- ❑ Timer mode operation.
- ❑ Directional phase counting mode 1 to 4.
- ❑ Count on external clock input pin TCLKA or TCLKB.
- ❑ Edge-aligned PWM mode (continuous up counting, PWM output mode).
- ❑ Center-aligned PWM mode (continuous up/down counting, PWM output mode).

5.9.2.1. Continuous Up Counting Mode with Edge-Aligned PWM

Each timer channel can be configured as edge-aligned PWM mode by setting MODE bits in P_TMRx_Ctrl (x = 0, 1). At this mode, the counter acts as up-counting timer and counts from 0x0000 to the value of timer period register. User must configure P_TMRx_TPR (x = 0 ~ 1) register, set counter clear source (CCLS) as cleared by timer period compare match and enable Port B/C specific function for compare match output pin.

The PDC timer continuous up counting according to the input clock sources from the configuration of TMRPS that is defined in corresponding timer control register. The timer counter register will be cleared to zero when the register value matches that of the timer period register and period compare match event interrupt flag TPRIF is set. The period interrupt request is generated when PPRIE bit is set in P_TMRx_INT (x = 0, 1) register.

Once the timer counter register became as 0x0000, the underflow event flag TCUIF is set. The underflow interrupt request is generated when TCUIE bit is set in P_TMRx_INT (x = 0, 1) register.

The overflow flag is set when the value of timer counter register reaches 0xFFFF and TCVIF flag is set. The overflow interrupt request is generated when TCVIE bit is set in P_TMRx_INT (x = 0, 1) register.

The compare match event of general register occurs when timer counter register matches the content of TGRA, TGRB or TGRC register. It generates the general register compare match interrupt when TGAIE, TGBIE or TGCIE bit is set in the corresponding timer interrupt enable register.

The initial value of P_TMRx_TPR (x = 0, 1) can be any value from 0x0000 to 0xFFFF. Either the external clock input pin or internal clock source FCK can be selected as the clock source of the timer. The continuous up counting mode is extremely suitable for the generation of edge-triggered or asynchronous PWM waveforms and sampling periods in digital motor control systems. Figure 5-23 shows the normal continuous up counting mode of the PDC timer.

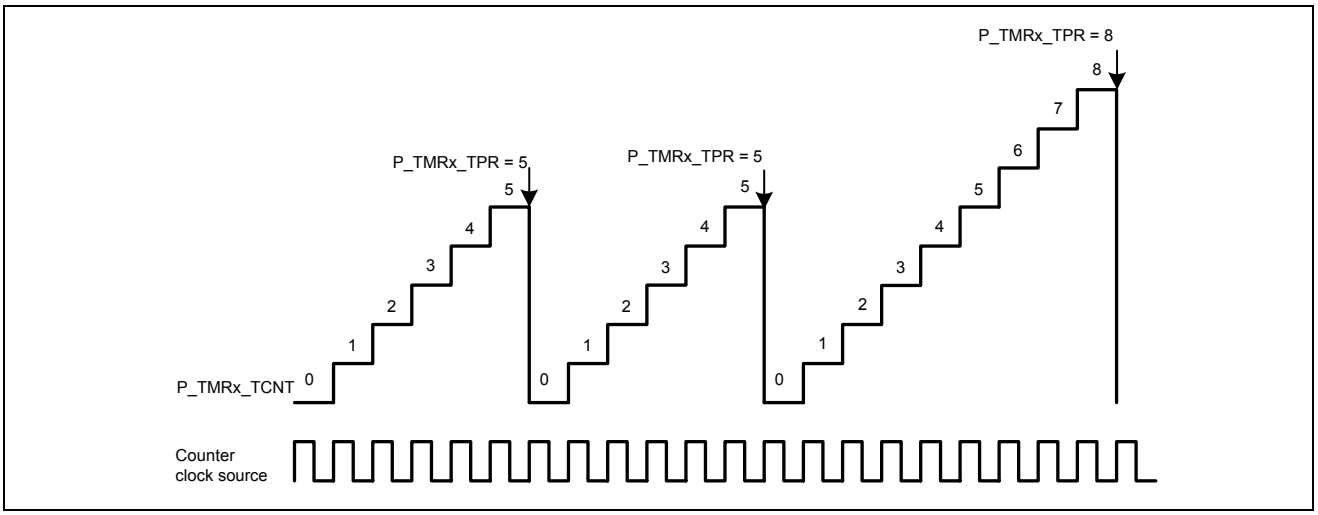


Figure 5-23 Continuous up counting example (CCLS = 111'b, CKEGS = 00'b, TMRPS = 000'b)

At edge-aligned PWM mode, user must set P_TMRx_TPR (x= 0, 1) period register and P_TMRx_TGRy (y = A, B, C) general register then set counter clear source (CCLS) as cleared by timer period compare match. The output condition of compare match can be configured by P_TMRx_IOCtrl (x= 0, 1) register.

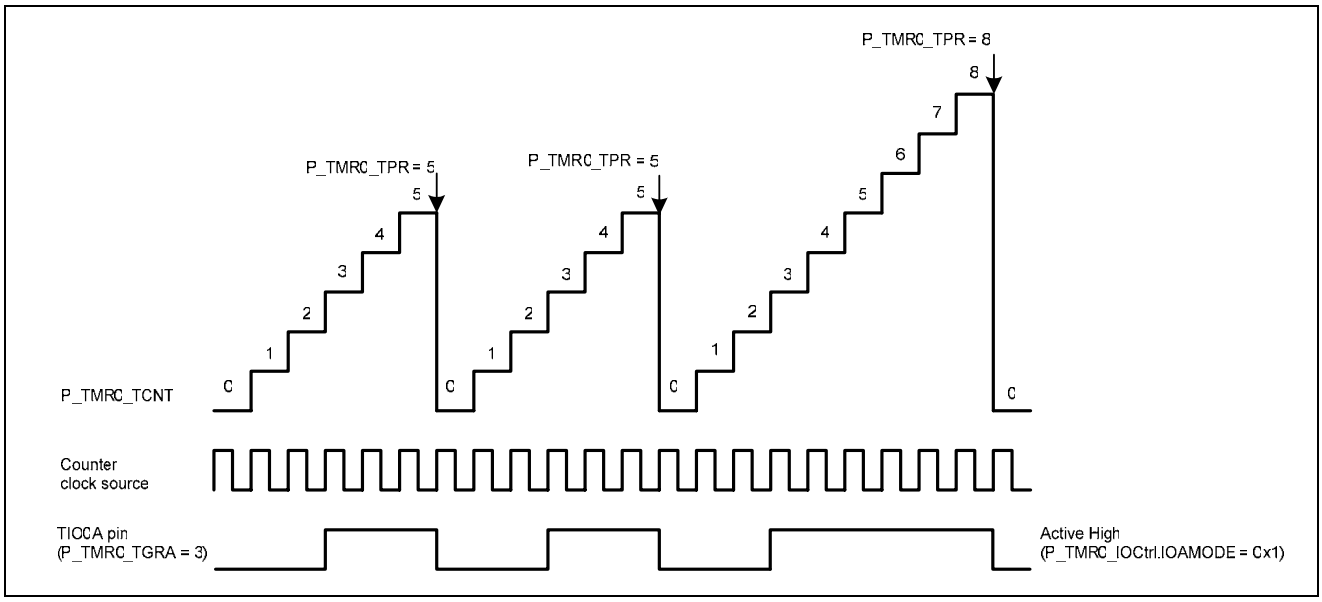


Figure 5-25

Figure 5-24 shows the normal continuous up counting mode for edge-aligned PWM generation of timer 0.

The PDC timer module has two channels and can perform PWM compare match output function up to six pins output. The output waveforms have active low at compare match, active high at compare match and output hold for the corresponding TIOxA, TIOxB, TIOxC (x = 0, 1) output pin using compare match with P_TMRx_TGRA, P_TMRx_TGRB, P_TMRx_TGRC (x = 0, 1) register respectively. Figure 5-26 shows the programming flowchart of PWM compare match output operation. Figure 5-27 is an example of edge aligned PWM. The correlations between the configuration of P_TMR0_IOCtrl and PWM output, the register TGRx and interrupt status flag TGxIF(x=A, B, C) are shown, respectively.

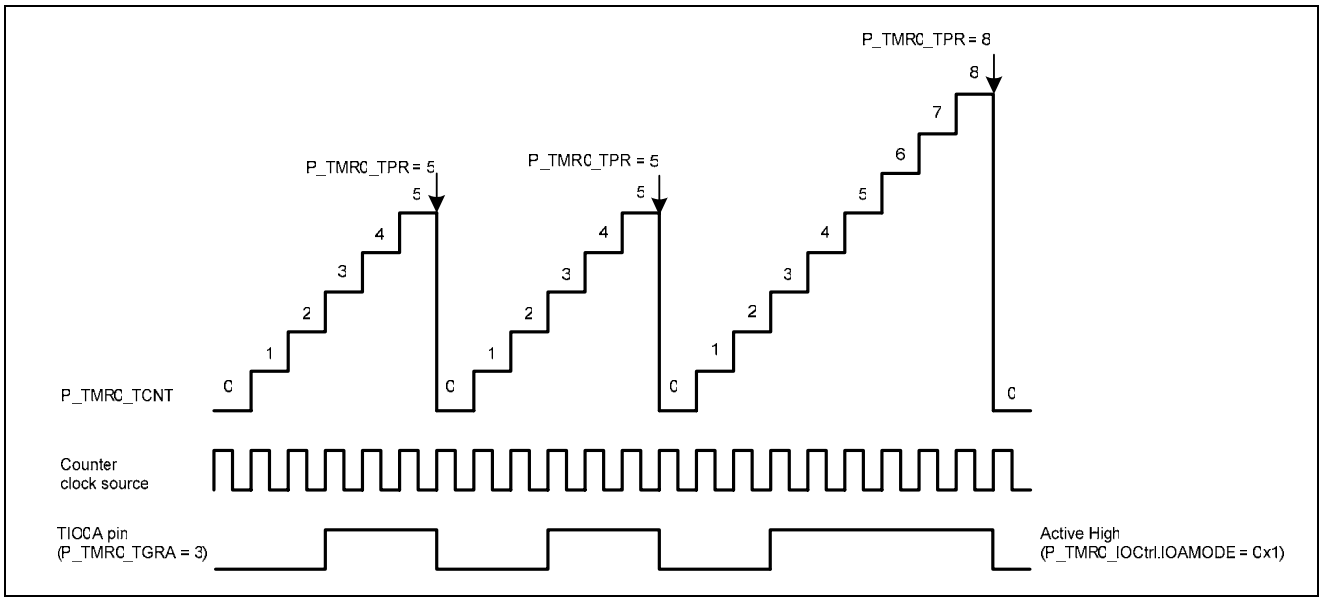
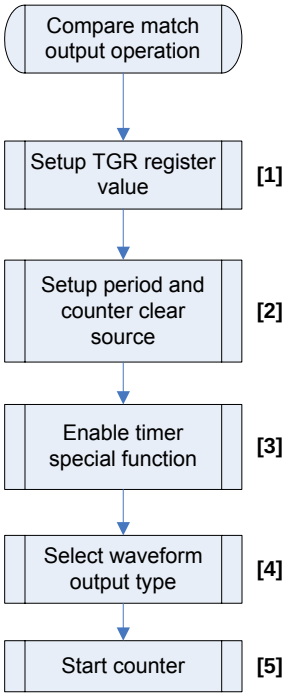


Figure 5-25 Edge-Aligned mode PWM



Descriptions:

[1.] Setup the TGRA/TGRB/TGRC value to generate the desired waveform width.

[2.] Setup the CCLS bits to 111'b so that period register determines the period and counter clear source,

[3.] Set the bits TIO0AEN, TIO0BEN, TIO0CEN to 1 in the P_IOB_SPE register and configures the corresponding IO pin to output mode.

[4.] Select compare match output mode through P_TMRx_IOCtrl (x = 0, 1) register.

[5.] Start the counting operation with the bit TMR0ST or TMR1ST is set in P_TMR_Start register.

Figure 5-26 Example programming flowchart of PWM compare match output operation

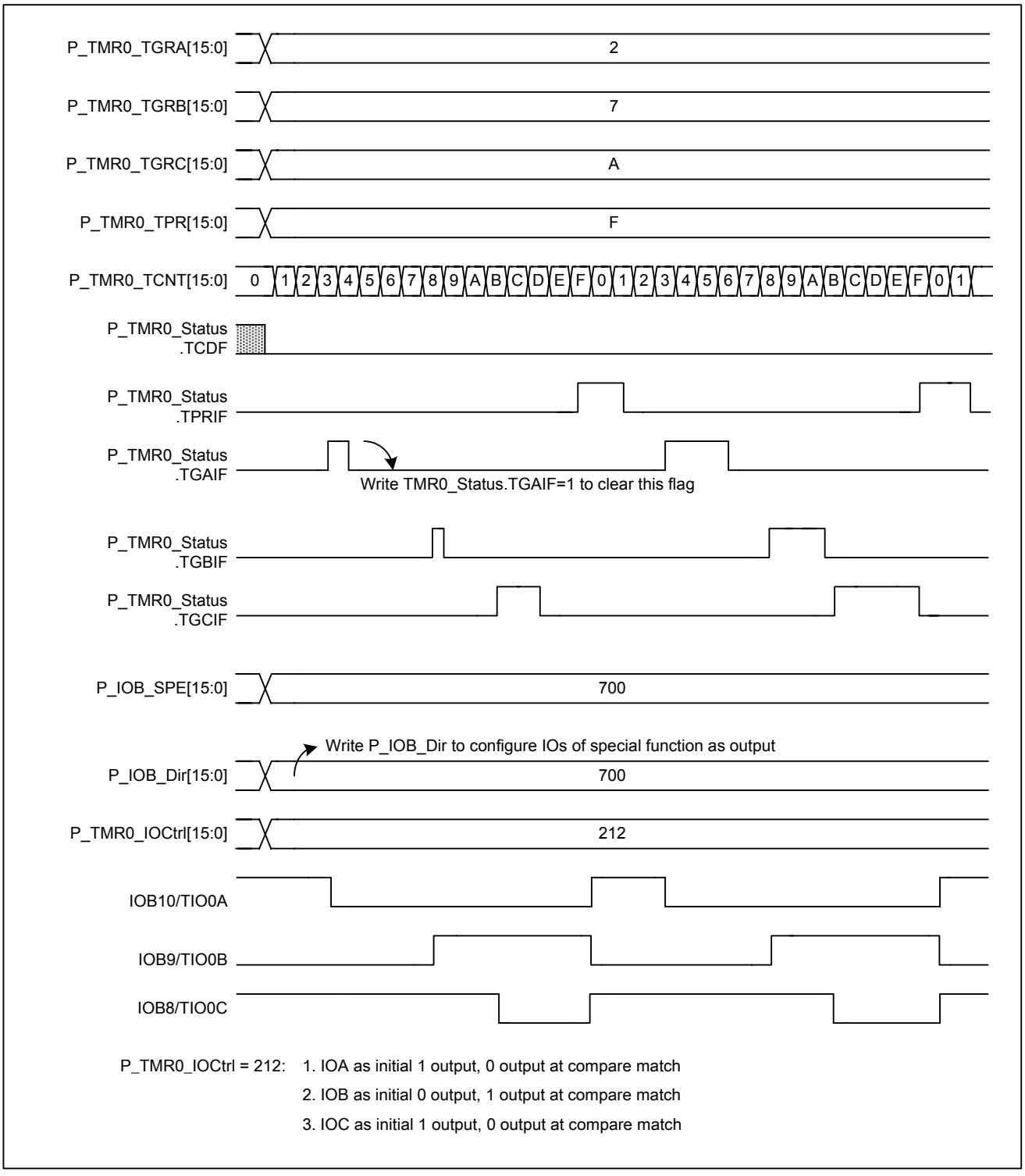


Figure 5-27 TMR0 edge aligned PWM

5.9.2.2. Timer mode Operation

The Timer mode can be selected by setting MODE in P_TMRx_Ctrl (x=0, 1). Except output waveform, it operates the same as continuous up counting mode with edge-aligned PWM. The first compare match event of general register occurs when timer counter register matches the content of TGRA, TGRB or TGRC register and the output will transits in the way set by IOAMODE, IOBMODE and IOCMODE, respectively. If compare match event occurs again, the compare match interrupt flag will be set but output waveform retain. Figure 5-28 shows the output timing in Timer mode.

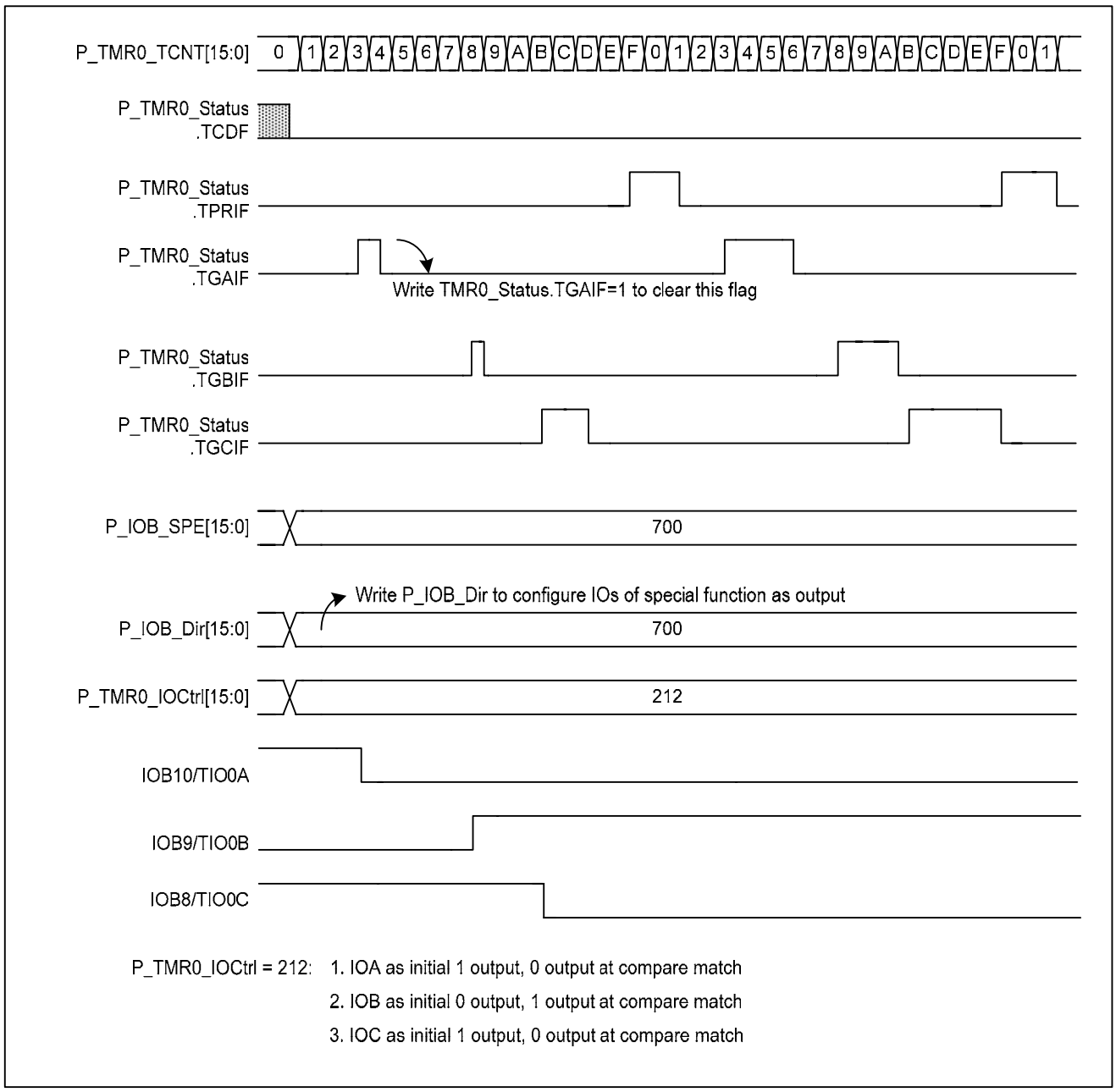


Figure 5-28 Timer mode output timing

5.9.2.3. Continuous up/down counting mode with Center-Aligned PWM

The operation of continuous up/down counting mode is the same as up counting mode except the timer period register defines the middle transition point of complete counting process. The counting direction changes from up to down when the timer counter register reaches the timer period register. The period of the timer is two times of P_TMRx_TPR (x = 0, 1) of the scaled clock input and the setting of CKEGS in the P_TMRx_Ctrl (x = 0, 1) register. Figure 5-29 shows the continuous up/down counting mode operation.

The initial value of the timer period register can be any value from 0x0000 to 0xFFFF. When the value of the timer counter register equals to timer period register, the PDC timer start to count down to zero. The period, underflow, overflow interrupts behaves the same manner as described in the continuous up counting mode. The counting direction is recorded at TCDF bit in the P_TMRx_Status (x = 0, 1) register. Either the external clock input pin or internal clock source FCK can be selected as the clock source of the timer. Figure 5-30 shows the center-aligned mode PWM at continuous up/down counting mode of timer 0.

Figure 5-31 is an example of center aligned PWM. The correlations between the configuration of P_TMR0_IOCtrl and PWM output, the register TGRx and interrupt status flag TGxIF(x=A, B, C) are shown, respectively.

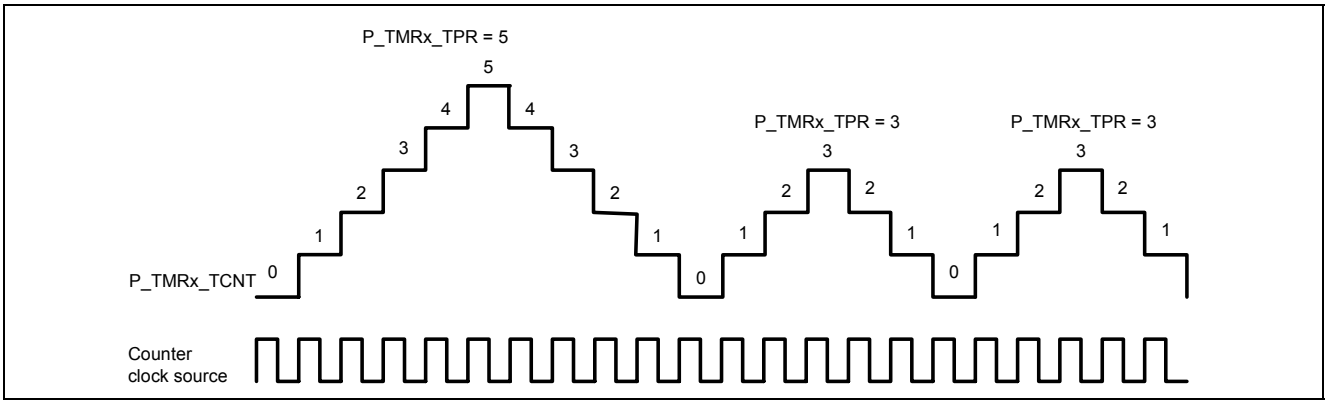


Figure 5-29 Continuous up/down counting example (CCLS = 111'b, CKEGS = 00'b, TMRPS = 000'b)

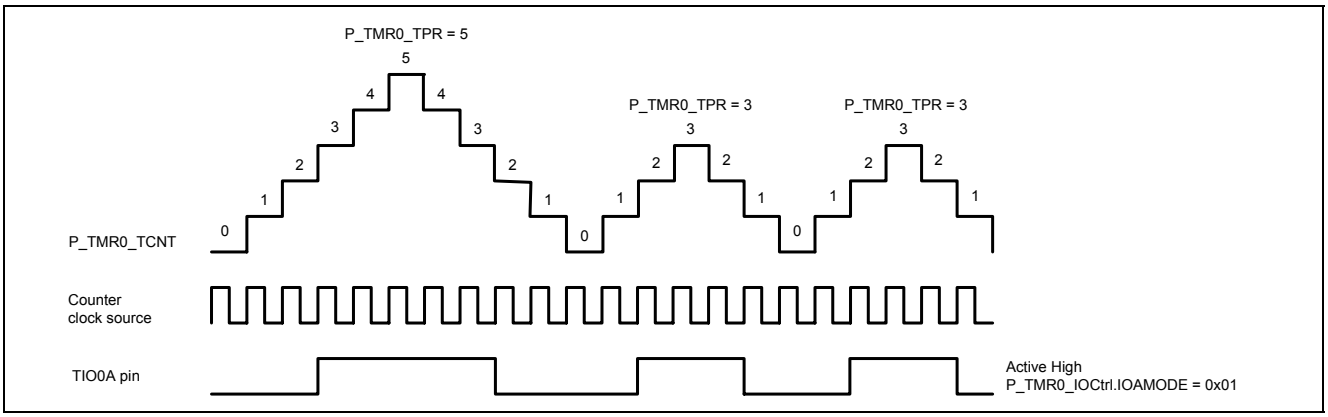


Figure 5-30 Center-aligned mode PWM

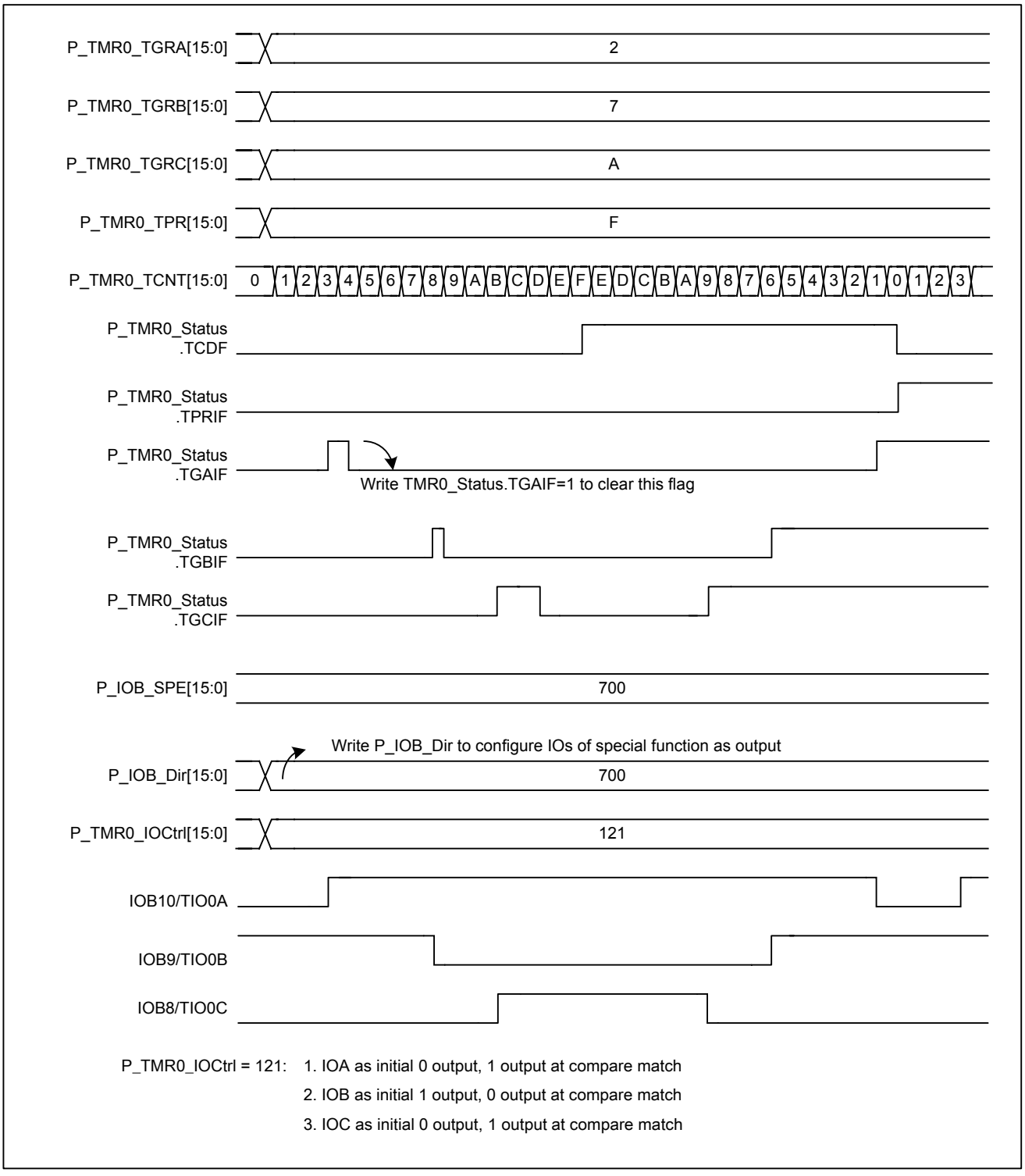


Figure 5-31 TMR0 center aligned PWM

5.9.2.4. Input Capture Operation

The capture function activation and the input edge at which the interrupt status flag issued are determined by the bits of IOAMOD, IOBMODE and IOCMODE in the P_TMRx_IOCtrl (x = 0, 1) register, respectively. It can be the rising edge, falling edge or both edge. The value of counter is always transferred to TGRx (x=A, B, C) and TBRx (x=A, B, C) at the rising and falling edge of corresponding input capture port, respectively. The counter register, P_ TMRx_TCNT (x = 0, 1) can be cleared according to the setting of CCLS in P_TMRx_Ctrl (x = 0, 1) register. The counter clear source can be one of TIO0A, TIO0B and TIO0C at the selected edge according to CLEGS in P_TMRx_Ctrl (x = 0, 1).

The powerful and flexible input capture function provides the essential feature for the motor control.

Table 5-11 shows the input capture configurations settings and results. When the input capture function is selected, the pulse width or period on input pin can be measured. Figure 5-33 shows the programming flowchart of input capture operation. Figure 5-34 is an example of input capture TIO0x (x=A, B, C). The correlations between the configuration of P_TMR0_IOCtrl and interrupt even are shown.

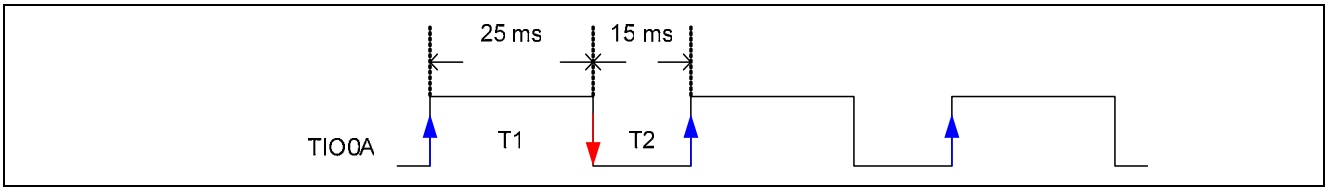


Figure 5-32 input capture signal connected to TIO0A

Table 5-11 Input capture configuration settings and results

Input capture settings			Description	Results
CLEGS	CCLS	IOAMOD		
Rising edge	TIO0A	Rising edge	Counter cleared at rising edge, interrupt at rising edge	P_TMR0_TGRA = period (40 ms) P_TMR0_TBRA = T1 (25ms)
Rising edge	TIO0A	Falling edge	Counter cleared at rising edge, interrupt at falling edge	P_TMR0_TGRA = period (40 ms) P_TMR0_TBRA = T1 (25ms)
Rising edge	TIO0A	Both edge	Counter cleared at rising edge, interrupt at both edge	P_TMR0_TGRA = period (40 ms) P_TMR0_TBRA = T1 (25ms)
Falling edge	TIO0A	Rising edge	Counter cleared at falling edge, interrupt at rising edge	P_TMR0_TGRA = T2 (15 ms) P_TMR0_TBRA = period (40ms)
Falling edge	TIO0A	Falling edge	Counter cleared at falling edge, interrupt at falling edge	P_TMR0_TGRA = T2 (15 ms) P_TMR0_TBRA = period (40ms)
Falling edge	TIO0A	Both edge	Counter cleared at falling edge, interrupt at both edge	P_TMR0_TGRA = T2 (15 ms) P_TMR0_TBRA = period (40ms)
Both edge	TIO0A	Rising edge	Counter cleared at both edge, interrupt at rising edge	P_TMR0_TGRA = T2 (15 ms) P_TMR0_TBRA = T1 (25ms)
Both edge	TIO0A	Falling edge	Counter cleared at both edge, interrupt at falling edge	P_TMR0_TGRA = T2 (15 ms) P_TMR0_TBRA = T1 (25ms)
Both edge	TIO0A	Both edge	Counter cleared at both edge, interrupt at both edge	P_TMR0_TGRA = T2 (15 ms) P_TMR0_TBRA = T1 (25ms)

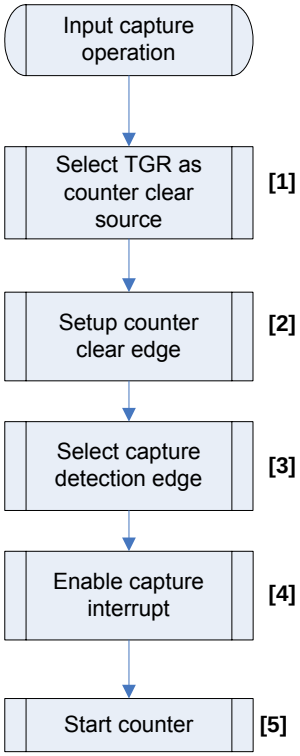


Figure 5-33 Example programming flowchart of input capture operation

Descriptions:

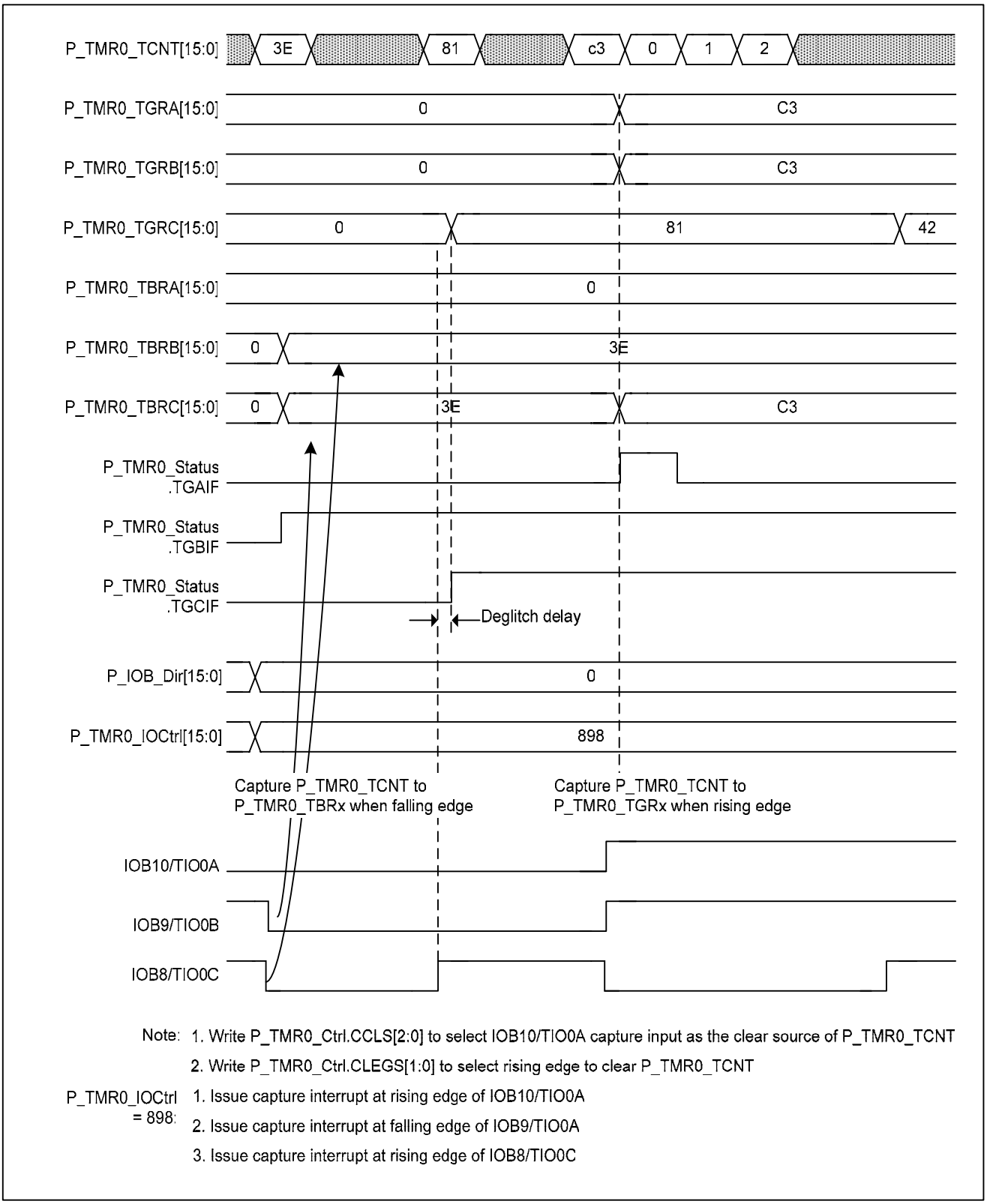
[1.] Select TIOxA, TIOxB, or TIOxC (x=0, 1) as counter clear source, write value to CCLS bits in P_TMRx_Ctrl (x = 0, 1) register.

[2.] Setup the counter clear edge by configuring CLEGS:

[3.] Select capture input interrupt edge as rising, falling, or both edge with setting of bits IOxMOD (x = A, B, C).

[4.] Enable capture interrupt in P_TMRx_INT (x = 0, 1) register if necessary.

[5.] Start the counting operation with the bit TMR0ST or TMR1ST is set in P_TMR_Start register.



Note: 1. Write P_TMR0_Ctrl.CCLS[2:0] to select IOB10/TIO0A capture input as the clear source of P_TMR0_TCNT

2. Write P_TMR0_Ctrl.CLEGS[1:0] to select rising edge to clear P_TMR0_TCNT

P_TMR0_IOCtrl = 898:

1. Issue capture interrupt at rising edge of IOB10/TIO0A
2. Issue capture interrupt at falling edge of IOB9/TIO0A
3. Issue capture interrupt at rising edge of IOB8/TIO0C

Figure 5-34 Capture input signal width and cycle

5.9.2.5. Timer 0 and 1 Control Registers

The P_TMRx_Ctrl (x = 0, 1) configures the selection of timer clock source, counter clock edge, counter clear source, counter clear edge, capture input sample clock and timer operating modes. TCLKA, TCLKB clock input will be sampled by system clock FCK. Any pulse narrower than four sampling clocks will be ignored. When programmed at counting on both edge, the input clock is halved. When MODE bits are set to phase counting mode, the counting phase input is TCLKA/TCLKB on timer 0 and TCLKC/TCLKD on timer 1. The time clock source should be assigned to internal clock in phase counting mode.

- **P_TMR0_Ctrl (0x7400): Timer 0 Control Register**
- **P_TMR1_Ctrl (0x7401): Timer 1 Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SPCK		MODE				CLEGS	

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CCLS			CKEGS		TMRPS		

B15-B14	SPCK	Capture input sample clock select	00: FCK/1	01: FCK/2
			10: FCK/4	11: FCK/8
B13-B10	MODE	Modes select	0000: Timer mode	0100: Phase counting mode 1
			0101: Phase counting mode 2	0110: Phase counting mode 3
			0111: Phase counting mode 4	1x0x: Edge-aligned PWM mode
			1x1x: Center-aligned PWM mode	
B9-B8	CLEGS	Counter clear edge in input capture mode	00: do not clear	01: rising edge
			10: falling edge	11: both edge
B7-B5	CCLS	Counter clear source select	000: TCNT clearing disabled	001: TCNT cleared by TIOxA (x = 0, 1) capture input
			010: TCNT cleared by TIOxB (x = 0, 1) capture input	011: TCNT cleared by TIOxC (x = 0, 1) capture input
			100: TCNT cleared by every P_POSx_DectData (x = 0, 1) change 6 times	101: TCNT cleared by every P_POSx_DectData (x = 0, 1) change 3 times
			110: TCNT cleared by P_POSx_DectData (x = 0, 1) position detection data change	111: TCNT cleared by P_TMRx_TPR (x = 0, 1) compare match
B4-B3	CKEGS	Clock edge select	00: Count at rising edge	01: Count at falling edge
			1X: Count at both edges	
B2-B0	TMRPS	Timer pre-scalar select	00: Counts on FCK /1	001: Counts on FCK /4
			010: Counts on FCK /16	011: Counts on FCK /64
			100: Counts on FCK /256	101: Counts on FCK /1024
			110: Counts on TCLKA pin input	111: Counts on TCLKB pin input

5.9.2.6. Timer 0 and 1 Period Register

The P_TMRx_TPR (x = 0, 1) is a 16-bit readable/writable register. It is used to set the period of PWM waveform. When P_TMRx_TCNT (x = 0, 1) register reaches P_TMRx_TPR (x = 0, 1) register value, P_TMRx_TCNT (x = 0, 1) register will be cleared to 0x0000 (up-counting mode) or start down-count (continuous up-/down-counting mode) according to MODE bits programmed in P_TMRx_Ctrl (x = 0, 1) registers. Its default value is 0xFFFF. When P_TMRx_TPR (x = 0, 1) register is set to 0x0000, the P_TMRx_TCNT (x = 0, 1) register counter will stop counting and remain at 0x0000.

- **P_TMR0_TPR (0x7435): Timer 0 Period Register**
- **P_TMR1_TPR (0x7436): Timer 1 Period Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
TMRPRD							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
TMRPRD							

5.9.2.7. Timer 0 and 1 General and Buffer Register

TGRA, TGRB, TGRC are 16-bit registers. PDC Timer has six timer general registers, three for each channel. The TGR registers are dual function 16-bit readable/writable registers, functioning as either PWM output or input capture registers.

The values in TGR and TCNT are constantly compared with each other when the TGR registers are used as PWM output registers. When the both values match, the TGAIF, TGBIF, TGCIF bits in corresponding timer interrupt status register are set to 1. Compare match outputs can be selected by TIOxA, TIOxB and TIOxC (x = 0, 1). When the TGR registers are used as input capture registers, the TCNT value is stored at the rising edge of input capture port.

When PWM mode, edge-aligned PWM mode, or center-aligned PWM mode is selected, the TGR register behaves as the duty ratio value register. Upon reset, the TGR registers are initialized to 0x0000.

When bits CCLS are set to 100'b, 101'b, 110'b, the PDC timer behaves as PDC mode used for BLDC motor application. The hall position signals are connected to TIOxA, TIOxB, TIOxC (x = 0, 1). The TCNT register is stored to TGRA register according to bits value of CCLS and CLEG bits should be assigned to clear on both edge. When position detection change event occurred, the TCNT register will be latched to TGRA then reset to 0x0000. User could use this information to read the correct TGRA value to calculate the motor speed.

The timer buffer registers TBRA, TBRB and TBRC are the double buffers of TGRA, TGRB and TGRC, respectively. The value of TGRx (x=A, B, C) can automatically be updated when the period compare match event occurs. That is, the duty ratio value will not be updated until one period ends completely. When the TBR registers are used as input capture registers, the TCNT value is stored at the falling edge of input capture port.

- **P_TMR0_TGRA (0x7440): Timer 0 General Register A**
- **P_TMR0_TGRB (0x7441): Timer 0 General Register B**
- **P_TMR0_TGRC (0x7442): Timer 0 General Register C**
- **P_TMR1_TGRA (0x7443): Timer 1 General Register A**
- **P_TMR1_TGRB (0x7444): Timer 1 General Register B**
- **P_TMR1_TGRC (0x7445): Timer 1 General Register C**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRGLR							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRGLR							

- **P_TMR0_TBRA (0x7450): Timer 0 Buffer Register A**
- **P_TMR0_TBRB (0x7451): Timer 0 Buffer Register B**
- **P_TMR0_TBRC (0x7452): Timer 0 Buffer Register C**
- **P_TMR1_TBRA (0x7453): Timer 1 Buffer Register A**
- **P_TMR1_TBRB (0x7454): Timer 1 Buffer Register B**
- **P_TMR1_TBRC (0x7455): Timer 1 Buffer Register C**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRBUF							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRBUF							

5.9.2.8. Timer 0 and 1 Input and Output Control Register

The P_TMRx_IOCtrl (x =0, 1) register controls the PWM output and input capture action type of TIOxA, TIOxB, and TIOxC (x = 0, 1) pins. By setting the CCLS and MODE bits in P_TMRx_Ctrl (x = 0, 1) register will determine the timer IO action mode. When choosing PWM output mode, the IOAMODE / IOBMODE / IOCMODE bits determines the waveform generation depending on the active clock edge. When choosing input capture mode, the IOAMODE/IOBMODE/IOCMODE bits defines the capture event including position detection changed.

- **P_TMR0_IOCtrl (0x7410): Timer 0 IO control register**
- **P_TMR1_IOCtrl (0x7411): Timer 1 IO control register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved				IOCMODE			

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
IOBMODE				IOAMODE			

B15-B12	Reserved			
B11-B8	IOCMODE	Select Timer 0/Timer 1 IOC Configuration	PWM compare match output mode：	
			0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
			Input capture mode：	
			1000: Issue input capture interrupt at rising edge	1001: Issue input capture interrupt at falling edge
			101x: Issue input capture interrupt at both edges	11xx: Input capture when Position Detection Register changes
B7-B4	IOBMODE	Select Timer 0/Timer 1 IOB Configuration	PWM compare match output mode：	
			0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
			Input capture mode：	
			1000: Issue input capture interrupt at rising edge	1001: Issue input capture interrupt at falling edge
			101x: Issue input capture interrupt at both edges	11xx: Input capture when Position Detection Register changes
B3-B0	IOAMODE	Select Timer 0/Timer 1 IOA Configuration	PWM compare match output mode：	
			0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
			Input capture mode：	
			1000: Issue input capture interrupt at rising edge	1001: Issue input capture interrupt at falling edge
			101x: Issue input capture interrupt at both edges	11xx: Input capture when Position Detection Register changes

5.9.2.9. Timer Start Register

The P_TMR_Start register selects the operation of counter start/stop for the P_TMRx_TCNT (x = 0 ~ 4). When counter operation stopped, its contents will be cleared. Set TMR0ST or TMR1ST bit to 1 would start the P_TMR0_TCNT or P_TMR1_TCNT register immediately and vice versa.

- **P_TMR_Start (0x7405): Timer Counter Start Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved			TMR4ST	TMR3ST	TMR2ST	TMR1ST	TMR0ST

B15-B5	Reserved			
B4	TMR4ST	Timer 4 counter start setting	0: Counter operation stopped	1: Performs counting operation
B3	TMR3ST	Timer 3 counter start setting	0: Counter operation stopped	1: Performs counting operation
B2	TMR2ST	Timer 2 counter start setting	0: Counter operation stopped	1: Performs counting operation
B1	TMR1ST	Timer 1 counter start setting	0: Counter operation stopped	1: Performs counting operation
B0	TMR0ST	Timer 0 counter start setting	0: Counter operation stopped	1: Performs counting operation

5.9.2.10. Timer 0 and 1 Interrupt Enable Register

The P_TMRx_INT (x = 0, 1) register is used to enable or disable A/D conversion start request by TGRA compare match, interrupt requests for position detection changes, overflow/underflow of TCNT, period register compare match and input capture/compare match of TGRA, TGRB, TGRC.

- **P_TMR0_INT (0x7420): Timer 0 Interrupt Enable Register**
- **P_TMR1_INT (0x7421): Timer 1 Interrupt Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
Reserved							PDCIE

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TADSE	TCUIE	TCVIE	TPRIE	Reserved	TGCIE	TGBIE	TGAIE

B15-B9	Reserved			
B8	PDCIE	Position detection change interrupt enable bit	0: Disable	1: Enable
B7	TADSE	A/D conversion start request by TGRA enable bit	0: Disable	1: Enable
B6	TCUIE	Underflow interrupt enable bit	0: Disable	1: Enable
B5	TCVIE	Overflow interrupt enable bit	0: Disable	1: Enable
B4	TPRIE	Timer Period Register interrupt enable bit	0: Disable	1: Enable
B3	Reserved			
B2	TGCIE	Timer General C Register interrupt enable bit	0: Disable	1: Enable
B1	TGBIE	Timer General B Register interrupt enable bit	0: Disable	1: Enable
B0	TGAIE	Timer General A Register interrupt enable bit	0: Disable	1: Enable

5.9.2.11. Timer 0 and 1 Interrupt Status Register

The interrupt status register indicates the event generation of position detection changes, an underflow/overflow of TCNT, period register compare match and input capture/compare match of TGRA, TGRB, and TGRC. These flags show the interrupt sources. An interrupt would be generated when the corresponding interrupt enable bit is set in P_TMRx_INT (x = 0, 1) register. The TCDF represents the counter direction when timer is setup to center-aligned PWM mode or phase counting mode.

- **P_TMR0_Status (0x7425): Timer 0 Interrupt Status Register**
- **P_TMR1_Status (0x7426): Timer 1 Interrupt Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0
Reserved							PDCIF

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TCDF	TCUIF	TCVIF	TPRIF	Reserved	TGCIF	TGBIF	TGAIF

B15-B9	Reserved			
B8	PDCIF※	Position detection changes interrupt flag	0: Position no changed	1: Position changed
B7	TCDF	Timer Counter Count direction flag	0: Up-counting	1: Down-counting
B6	TCUIF※	Timer Counter Underflow flag	0: Underflow not occurred	1: Underflow has occurred
B5	TCVIF※	Timer Counter Overflow flag	0: Overflow not occurred	1: Overflow has occurred
B4	TPRIF※	Timer Period Register compare match flag	0: Compare match not occurred	1: Compare match has occurred
B3	Reserved			
B2	TGCIF※	Timer General C Register input capture/compare match flag	0: Input capture/compare match not occurred	1: Input capture/compare match has occurred
B1	TGBIF※	Timer General B Register input capture/compare match flag	0: Input capture/compare match not occurred	1: Input capture/compare match has occurred
B0	TGAIF※	Timer General A Register input capture/compare match flag	0: Input capture/compare match not occurred	1: Input capture/ compare match has occurred

※: write '1' to clear this flag

5.9.2.12. Timer 0 and 1 Counter Register

The PDC timer has two TCNT counters (P_TMR0_TCNT and P_TMR1_TCNT), one for each channel. The TCNT counters are 16-bit readable registers that increment/decrement according to input clocks.

Bits TMRPS in corresponding timer control register can select input clocks. P_TMR0_TCNT and P_TMR1_TCNT increment/decrement in center-aligned PWM mode, while they only increment in other modes. The TCNT counters are initialized to 0x0000 by compare matches with corresponding TGRA, TGRB, TGRC, or input captures to TGRA, TGRB, TGRC, or P_POSx_DectData (x = 0 , 1) data changes. When the TCNT counters overflow, a TCUIF flag in timer interrupt status register for the corresponding channel is set to 1. When TCNT underflows, a TUDIF flag in timer interrupt status register is set to 1.

- **P_TMR0_TCNT (0x7430): Timer 0 Counter Register**
- **P_TMR1_TCNT (0x7431): Timer 1 Counter Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRCNT							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRCNT							

5.9.3. Phase Counting Mode Operation

In phase counting mode, the phase difference between two external clock inputs is detected and timer counter counts up or down according to the clock phase relationship. This mode can be set for PDC0 and PDC1. The general application is for two-phase quadrature encoder pulse inputs. The clock source of PDC channel 0 utilizes TCLKA and TCLKB pins and PDC channel 1 utilizes TCLKC and TCLKD pins. The SPMC75F2413A supports the following four modes directional phase counting operation. Figure 5-35 to Figure 5-38 represents the four-phase counting mode operation, and Figure 5-39 shows the programming flowchart of phase counting mode procedure.

5.9.3.1. Phase Counting Mode 1

In phase counting mode 1, the P_TMRx_TCNT (x = 0, 1) always counts up as long as the TCLKB/TCLKD clock source is leading 90 degree with TCLKA/TCLKC. On the other hand, the P_TMRx_TCNT always count down when TCLKB/TCLKD clock source is lagging 90 degree with TCLKA/TCLKC. This mode is useful for encoder equipped motor drive application. Table 5-12 shows phase counting mode 1 relationship. The phase resolution is amplified four times compared to encoder resolution specification (pulse / revolution). Figure 5-35 shows the example of phase counting 1.

Table 5-12 phase counting mode 1 relationship

TCLKA (PDC0) **TCLKC (PDC1)**	**TCLKB (PDC0)** **TCLKD (PDC1)**	**Counting Operation**
H	Rising	Up-count
L	Falling	
Rising	L	
Falling	H	
H	Falling	Down-count
L	Rising	
Rising	H	
Falling	L	

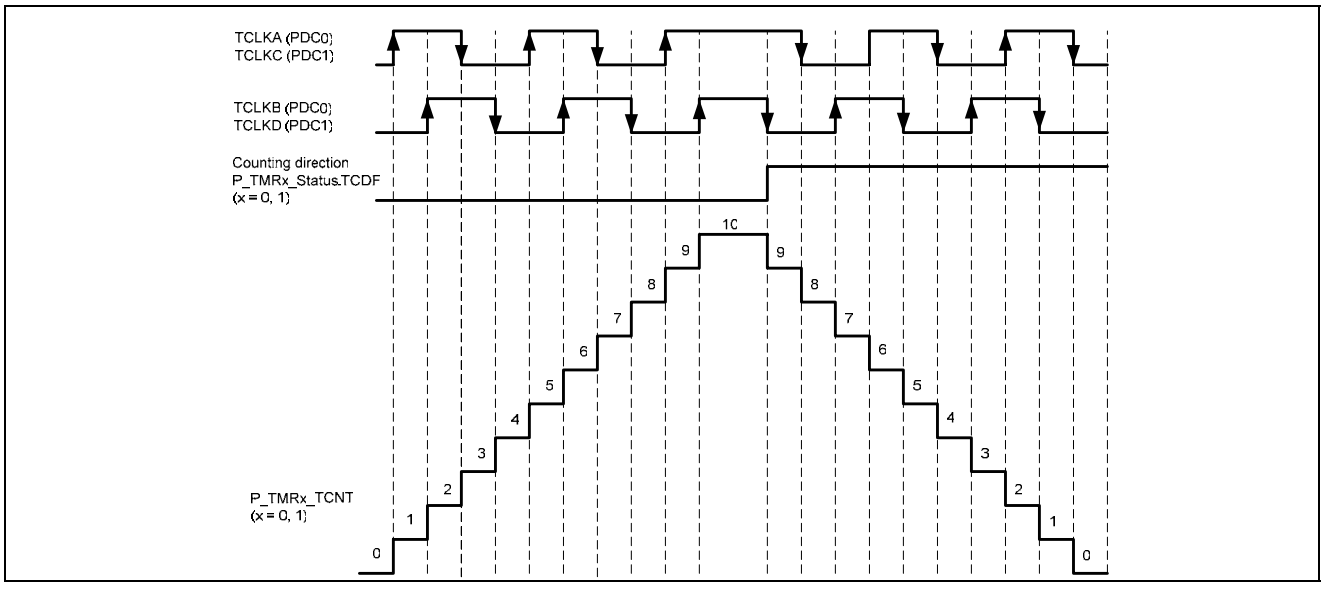


Figure 5-35 phase counting mode 1

5.9.3.2. Phase Counting Mode 2

In phase counting mode 2, the P_TMRx_TCNT (x = 0, 1) counting direction is determined by the logic level of TCLKB/TCLKD. When TCLKB/TCLKD remains logic 'H' level, the counter does the up-counting operation. If TCLKB/TCKD is logic level 'L', it does the down-counting operation. Table 5-13 shows the relationship. The counting operation is synchronous to the falling edge of TCLKA/TCLKC. Figure 5-36 shows the phase counting mode 2 examples.

Table 5-13 phase counting mode 2 relationship

TCLKA (PDC0) TCLKC (PDC1)	TCLKB (PDC0) TCLKD (PDC1)	Counting Operation
H	Rising	—
L	Falling	—
Rising	L	—
Falling	H	Up-count
H	Falling	—
L	Rising	—
Rising	H	—
Falling	L	Down-count

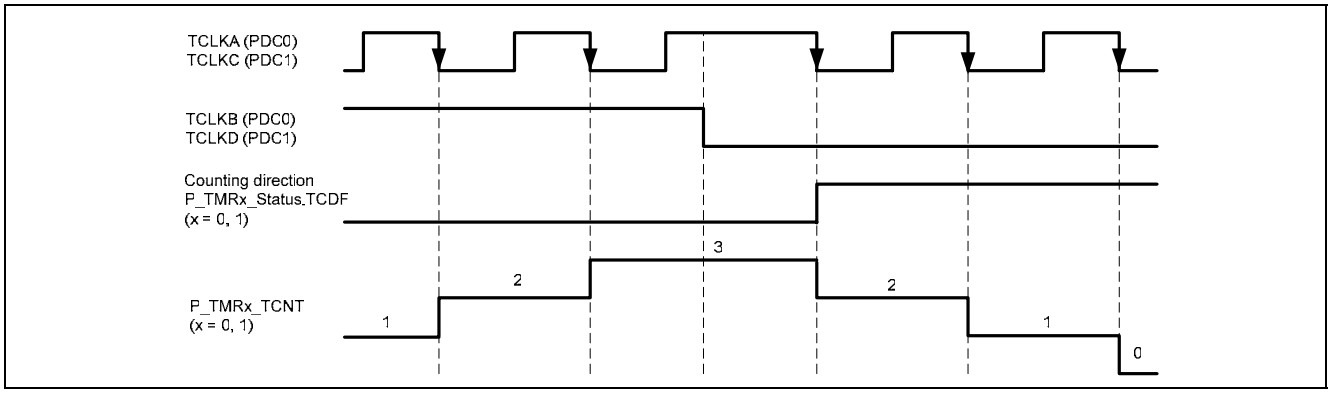


Figure 5-36 phase counting mode 2

5.9.3.3. Phase Counting Mode 3

In phase counting mode 3, the P_TMRx_TCNT (x = 0, 1) does the up counting operation when TCLKB/TCLKD remains at logic level 'H', and synchronous to the falling edge of TCLKA/TCLKC. On the other hand, the P_TMRx_TCNT (x = 0, 1) does the down counting operation in the situation of TCLKA/TCLKC at logic level 'H', and synchronous to the falling edge of TCLKB/TCLKD. The following table shows the relationship and

Figure 5-37 represents this phase counting example.

Table 5-14 phase counting mode 3 relationship

TCLKA (PDC0) TCLKC (PDC1)	TCLKB (PDC0) TCLKD (PDC1)	Counting Operation
H	Rising	—
L	Falling	—
Rising	L	—
Falling	H	Up-count
H	Falling	Down-count
L	Rising	—
Rising	H	—
Falling	L	—

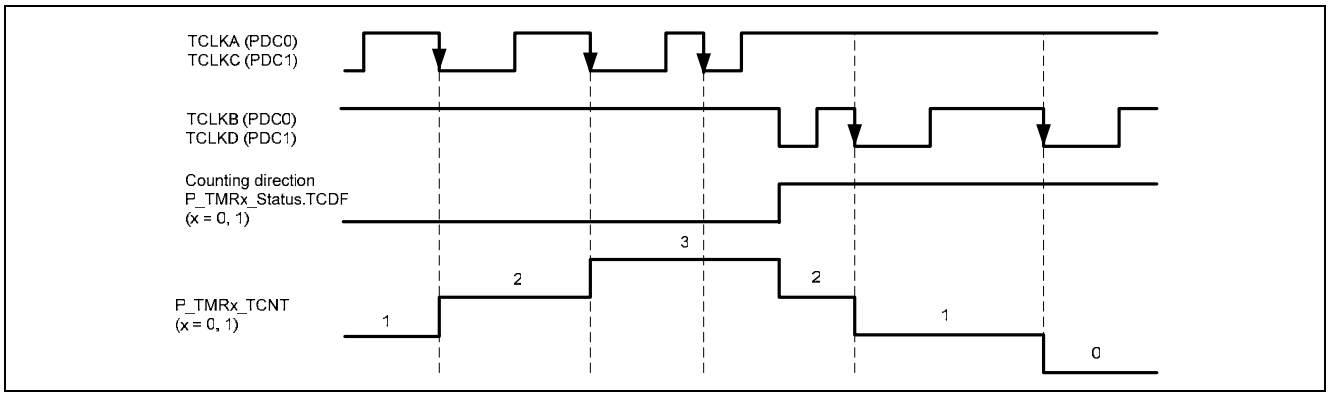


Figure 5-37 phase counting mode 3

5.9.3.4. Phase Counting Mode 4

In phase counting mode 4, the P_TMRx_TCNT counting direction is determined by the combinations of logic level and active level selection of TCLKx (x = A, B, C, D). When TCLKx (x = A, C) is at logic 'H'/'L' level and TCLKy (y = B, D) clock is in the rising/falling edge, the counter will do the up counting operation. In the case of TCLKx (x = A, C) is at logic 'H'/'L' level and TCLKy (y = B, D) clock is in the falling/rising edge; the counter will do the down counting operation. The following table shows the relationship and represents this phase counting example.

Table 5-15 phase counting mode 4 relationship

TCLKA (PDC0) TCLKC (PDC1)	TCLKB (PDC0) TCLKD (PDC1)	Counting Operation
H	Rising	Up-count
L	Falling	Up-count
Rising	L	—
Falling	H	—
H	Falling	Down-count
L	Rising	Down-count
Rising	H	—
Falling	L	—

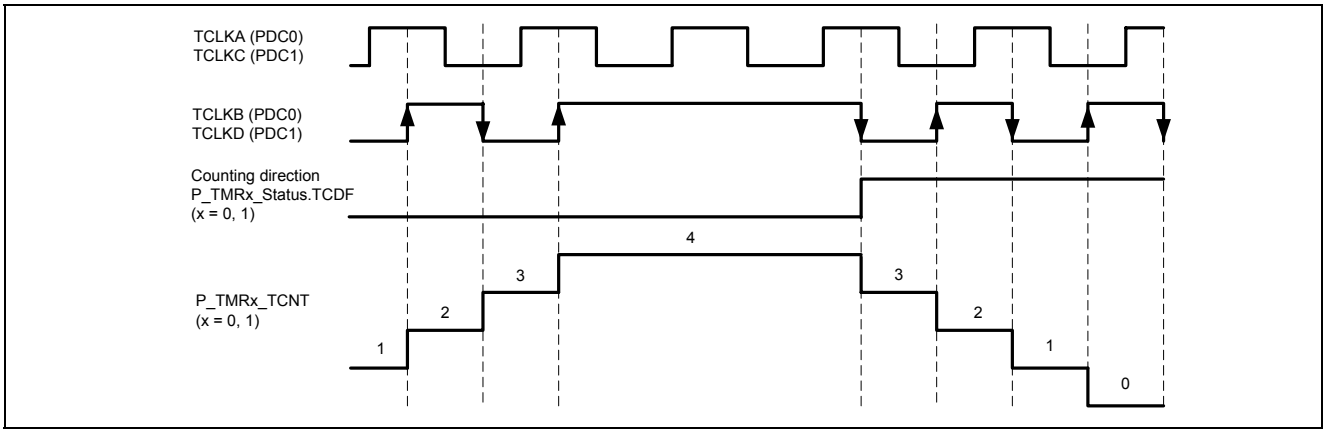
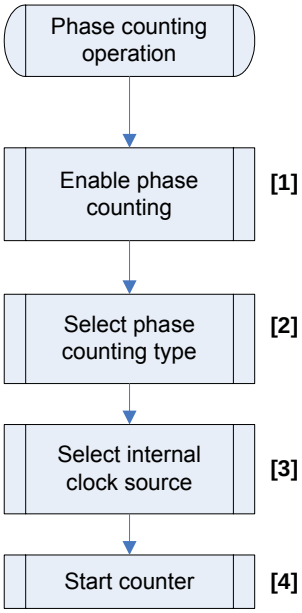


Figure 5-38 phase counting mode 4



Descriptions:

[1.] Enable phase counting mode by setting the TCLKAEN/ TCLKBEN or TCLKCEN/ TCLKDEN in the P_IOA_SPE register.

[2.] Select phase counting mode 1 to 4 by programming MODE bits in the P_TMRx_Ctrl (x = 0, 1) register.

[3.] Select the internal clock source FCK by choosing proper bit value TMRPS in the P_TMRx_Ctrl (x = 0, 1) register.

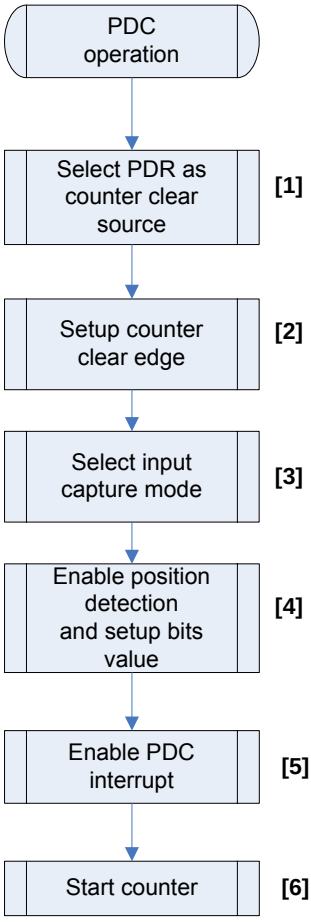
[4.] Start the counting operation with the bit TMR0ST or TMR1ST is set in P_TMR_Start register.

Figure 5-39 Example programming flowchart of phase counting operation

5.9.4. Position Detection Change (PDC) Mode Operation

The PDC timer has an extremely useful feature for position detection control used in BLDC motor driving application. The P_TMRx_TCNT (x = 0, 1) value can be transferred to TGRA, when CCLS bits is set to 100'b, 101'b or 110'b in the P_TMRx_Ctrl (x = 0, 1) register. Through the value of CCLS bits, the counter register can be stored to TGRA every six, three, one position detection data changes. Whenever the position detection changed event occurs, the counter register will be reset to 0x0000 after transferred to TGRA and PDCIF interrupt flag is set to 1. If the position detection interrupt enable bit PDCIE is set to 1 in the corresponding P_TMRx_INT (x = 0, 1) register, it would request a PDC interrupt to CPU.

Through programming the bits value of SPLCNT, SPLCK and SPLMOD, user could avoid the noise on the hall signal inputs and position detection data register P_POS0_DectData, P_POS1_DectData can latch the correct position data. Figure 5-40 shows the programming flowchart of PDC mode operation.



Descriptions:

[1.] Select the position data change is the clear source of counter register, the possible CCLS bits is 100'b, 101'b or 110'b in the P_TMRx_Ctrl (x = 0, 1) register.

[2.] Set the counter clear edge is both edge of position signal. The CLEG is set to 11'b in the P_TMRx_Ctrl (x = 0, 1) register.

[3.] Select the PDR mode in P_TMRx_IOCtrl (x = 0, 1). The IOAMODE should set to 11xx'b.

[4.] Enable the position detection logic by setting PDEN in the P_POSx_DectCtrl (x = 0, 1) register. Also configure proper bits value of SPLMOD and SPLCNT.

[5.] Enable the PDC interrupt by setting the PDCIE in P_TMRx_INT (x =0, 1) register if necessary.

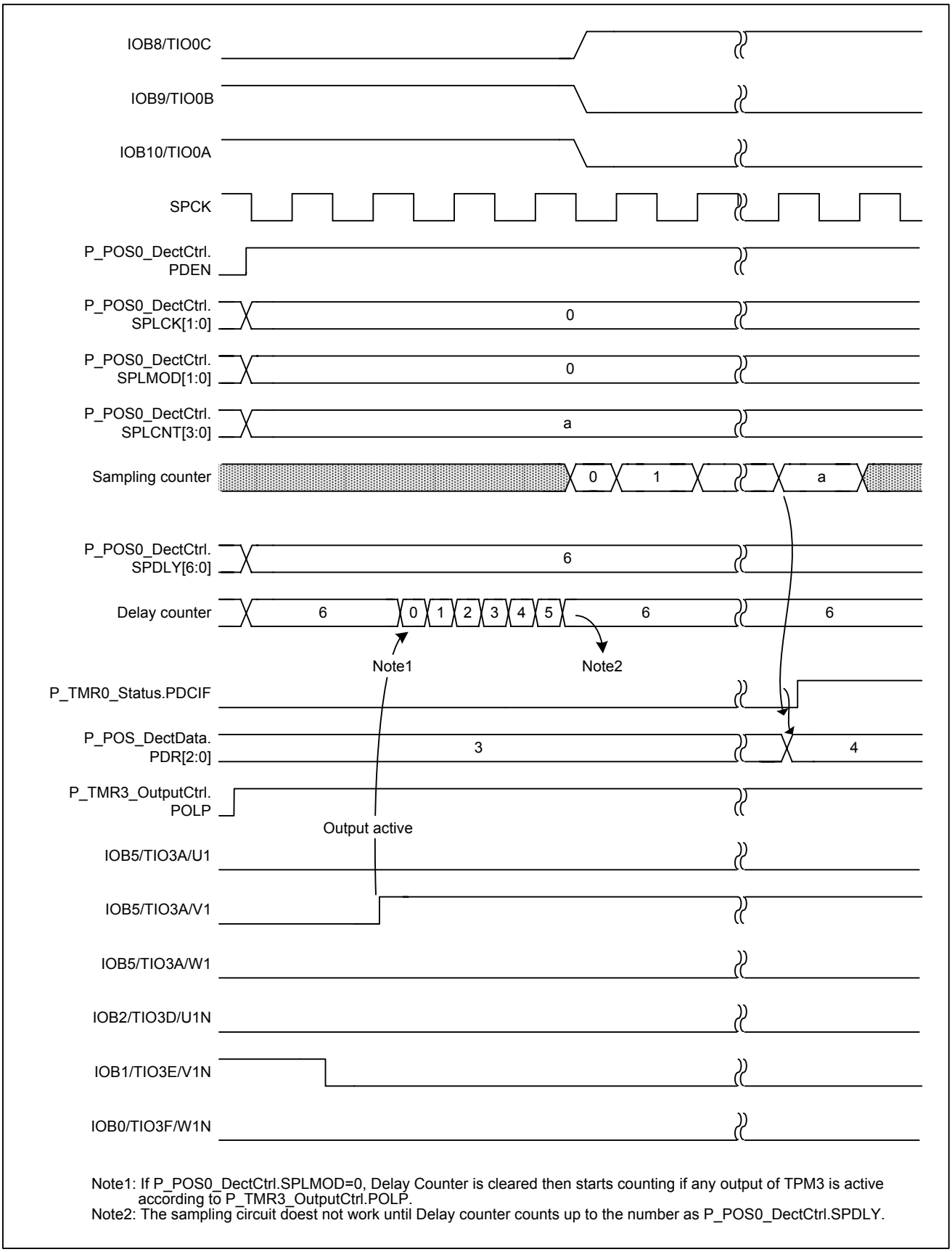
[6.] Start the counting operation with the bit TMR0ST or TMR1ST is set in P_TMR_Start register.

Figure 5-40 Example programming flowchart of PDC operation

5.9.4.1. Timer 0 and 1 Position Detection Control Register

There are two position detection control registers available in SPMC75F2413A： P_POS0_DectCtrl and P_POS1_DectCtrl are for timer 0 and timer 1, respectively. The control-registers control the sampling settings of position detection signals from TIOxA, TIOxB and TIOxC (x = 0, 1) input pins. The sampling parameters such as sampling clock, valid sampling count select, and sampling delay are all programmable.

The SPLMOD bits determine the sampling position signal condition. They can be selected from three modes：sample when PWM on, sample regularly, or sample while low side transistors are in conducting current. The SPDLY bits select the sampling delay and used in modes where sampling is made while PWM is on or lower side phase are conducting current. It helps to prevent erroneous detection due to the glitch that occurs immediately after the transistor is on.



Note1: If P_POS0_DectCtrl.SPLMOD=0, Delay Counter is cleared then starts counting if any output of TPM3 is active according to P_TMR3_OutputCtrl.POLP.
Note2: The sampling circuit doest not work until Delay counter counts up to the number as P_POS0_DectCtrl.SPDLY.

Figure 5-41 Position detection with noise filter

- **P_POS0_DectCtrl (0x7462): Timer 0 Position Detection Control Register**
- **P_POS1_DectCtrl (0x7463): Timer 1 Position Detection Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	RW	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SPLCK		SPLMOD		SPLCNT			

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
PDEN	SPDLY						

B15-B14	SPLCK	Sampling clock select	00: FCK/4	01: FCK/8
			10: FCK/32	11: FCK/128
B13-B12	SPLMOD	Sampling mode select	00: Start sampling when one of Ux/Vx/Wx/UxN/VxN/WxN (x=1,2) output is active and delay counter count to the value of SPDLY	01: Sample immediately regardless of delay counter.
			10: Start sampling when one of UxN/VxN/WxN (x=1,2) output is active and delay counter count to the value of SPDLY	11: Reserved
B11-B8	SPLCNT	Sampling count select	The valid settings are from 1 to 15 times. Note that count 0 and 1 are assumed to be one time.	
B7	PDEN	Position detection enable	0: Disable	1: Enable
B6-B0	SPDLY	Sampling delay	It is used to delay sampling in order to prevent erroneous detection due to noise that occurs immediately after any PWM output is active. The delay counter start counting when one of Ux/Vx/Wx/UxN/VxN/WxN (x=1,2) output is active.	

5.9.4.2. Timer 0 and 1 Position Detection Data Register

The current filtered position data will be latched to these registers. The sampling settings can be set in position detection control registers P_POSx_DectCtrl (x = 0, 1).

- **P_POS0_DectData (0x7464): Timer 0 Position Detection Data Register**
- **P_POS1_DectData (0x7465): Timer 1 Position Detection Data Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved					PDR		

B15-B13	Reserved	
B3-B0	**PDR**	PDR[2]: Noise filtered position detection input from pin TIO0C
		PDR[1]: Noise filtered position detection input from pin TIO0B
		PDR[0]: Noise filtered position detection input from pin TIO0A

5.10. TPM TIMER 2 MODULE

5.10.1. Introduction

SPMC75F2413A has a general-purpose 16 bit TPM (Timer PWM Mode, TPM) timer that support functions of input capture and PWM output features. The timer 2 could be used to provide a time base system for speed loop of motor control applications. It has two timer input/output pins for input capture and PWM output operations. Figure 5-42 shows the block diagram of the timer 2 module. For details of timer 2 specifications, please refer to Table 5-16.

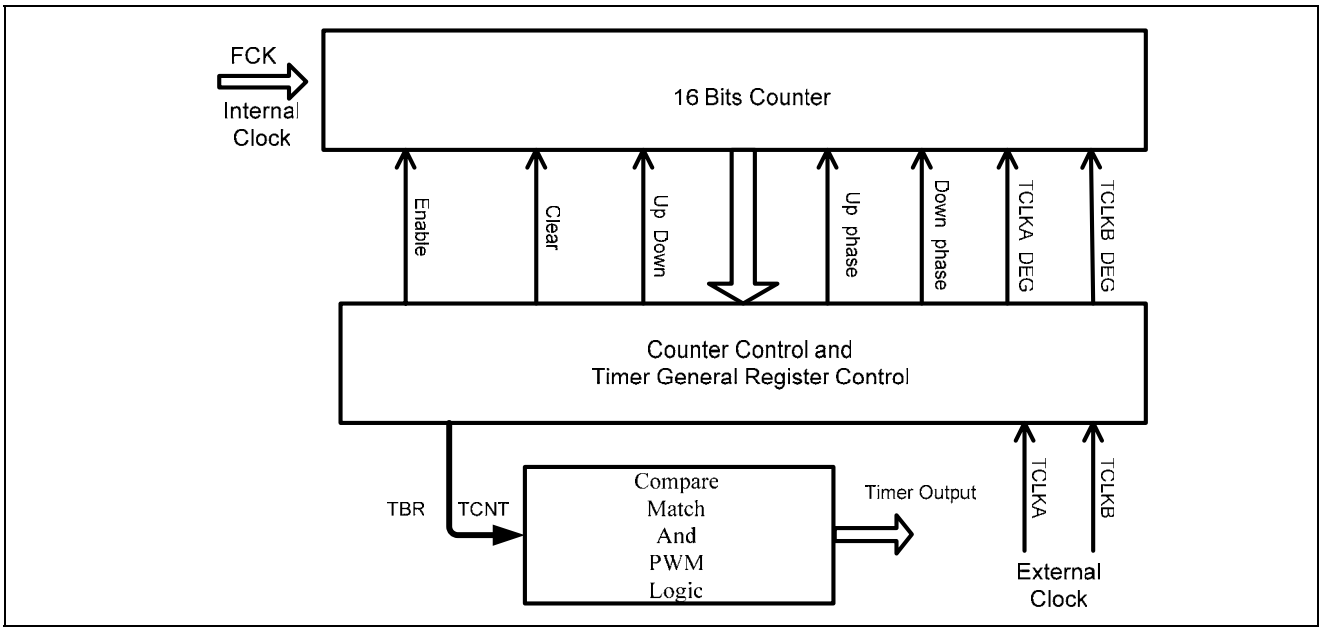


Figure 5-42 TPM timer 2 block diagram

Table 5-16 TPM Timer 2 Specification

Function		TPM Timer 2
Clock sources		Internal clock: FCK/1, FCK/4, FCK/16, FCK/64, FCK/256, FCK/1024 External clock: TCLKA, TCLKB
IO pins		TIO2A TIO2B
Timer general register		P_TMR2_TGRA P_TMR2_TGRB
Timer buffer register		P_TMR2_TBRA P_TMR2_TBRB
Timer period and counter register		P_TMR2_TPR P_TMR2_TCNT
Capture sample clock		Internal clock: FCK/1, FCK/2, FCK/4, FCK/8
Counting edge		Rising Falling Both edge
Counter clear source		Cleared on TIO2A, TIO2B capture input. Cleared on P_TMR2_TPR compare matches.
Input capture function		Yes
PWM compare match output function	1 output	Yes
	0 output	Yes
	Output Hold	Yes

Function	TPM Timer 2
Edge-aligned PWM	Yes
Center-aligned PWM	Yes
Timer buffer operation	Yes
AD convert start trigger	P_TMR2_TGRA compare match
Interrupt sources	Timer 2 TPR interrupt Timer 2 TGRA interrupt Timer 2 TGRB interrupt

5.10.2. TPM Timer 2 Counting Operation

The TPM2 is a general-purpose timer with input capture and PWM compare match output capability. TPM timer 2 provided independent time base at different input clock sources for application such as：

- ❑ The sampling and constant frequency driven features for digital control system.
- ❑ Speed loop time base of inverter motor control system.
- ❑ Timer mode operation
- ❑ Count on external clock input pin TCLKA or TCLKB
- ❑ Edge-aligned PWM mode (continuous up counting, PWM output mode)
- ❑ Center-aligned PWM mode (continuous up/down counting, PWM output mode)

5.10.2.1. Continuous Up Counting Mode with Edge-Aligned PWM

The TPM timer 2 can be configured as edge-aligned PWM mode by setting MODE bits in P_TMR2_Ctrl. At this mode, the timer counter act as up-counting timer and counting from 0x0000 to timer period register value. User must set P_TMR2_TPR register and set counter clear source (CCLS) is cleared by timer period compare match.

The timer continuous up counting according to the input clock sources from bits value TMRPS defined in corresponding timer control register. The timer counter register will be cleared to zero when the register value matches that of the timer period register and period compare match event interrupt flag TPRIF is set. The period interrupt request is generated when PPRIE bit is set in P_TMR2_INT register. The general register compare match event occurs when timer counter register matches the content of TGRA or TGRB register. It generates the general register compare match interrupt when TGAIE or TGBIE bit is set in the corresponding timer interrupt enable register.

The initial value of P_TMR2_TPR can be any value from 0x0000 to 0xFFFF. Either the external clock input pin or internal clock source FCK can be selected as the clock source of the timer. The normal continuous up counting mode is extremely suitable for the generation of edge-triggered or asynchronous PWM waveforms and sampling periods in digital motor control systems.

Figure 5-43 shows the normal continuous up counting mode of the TPM timer 2.

At edge-aligned PWM mode, user must set P_TMR2_TPR period register and P_TMR2_TGRx (x = A, B) general register then set counter clear source (CCLS) as cleared by timer period compare match. The compare match output condition set at P_TMR2_IOCtrl register.

Figure 5-44 shows the normal continuous up counting mode for edge-aligned PWM generation of timer 2.

The TPM timer 2 module can perform PWM compare match output function up to two pins output. The output waveforms have active low at compare match, active high at compare match and output hold for the corresponding TIO2A and TIO2B output pin using compare match with P_TMR2_TGRA and P_TMR2_TGRB register respectively. Figure 5-45 shows the programming flowchart of PWM compare match output operation. Figure 5-46 is an example of edge aligned PWM. The correlations between the configuration of P_TMR2_IOCtrl and PWM output, the register TGRx and interrupt status flag TGxIF(x=A, B) are shown, respectively.

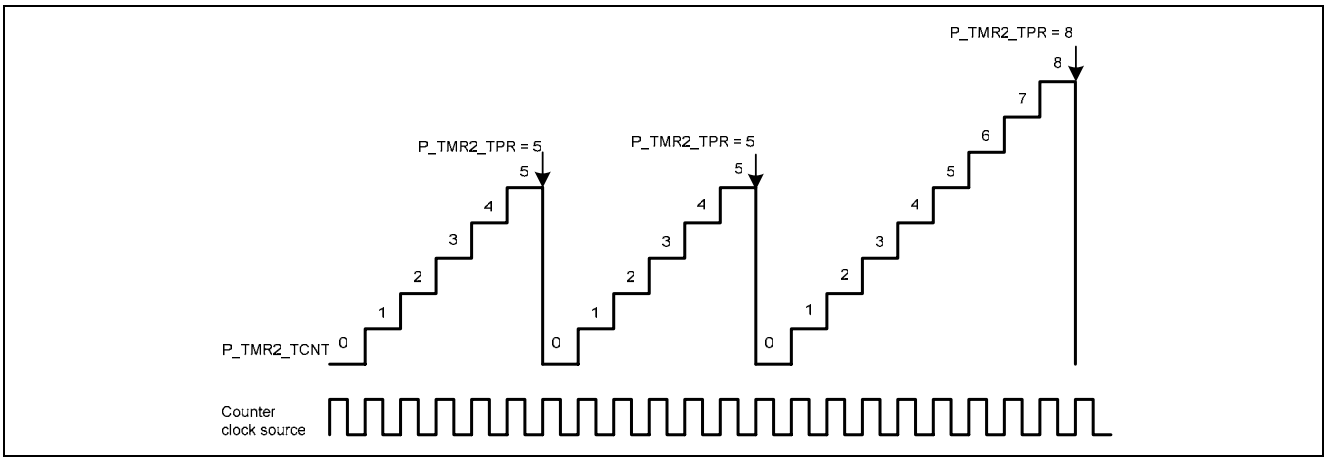


Figure 5-43 Continuous up counting example (CCLS = 111'b, CKEGS = 00'b, TMRPS = 000'b)

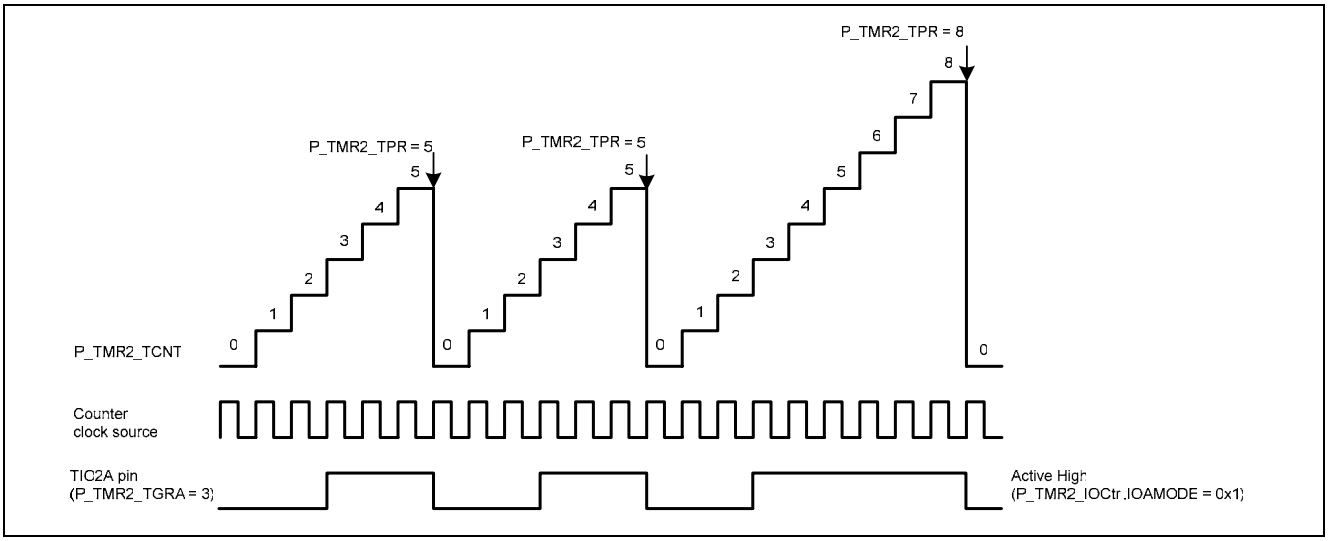
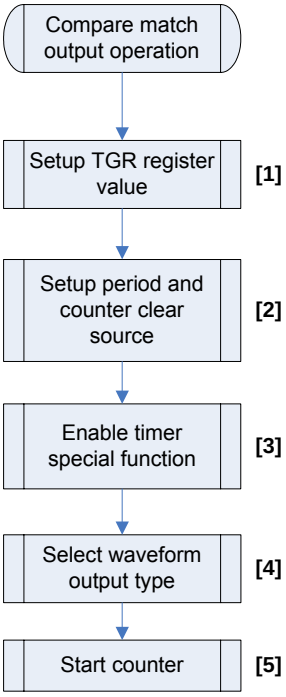


Figure 5-44 Edge-Aligned mode PWM



Descriptions:

[1.] Setup the TGRA/TGRB value to generate the desired waveform width.

[2.] Setup the CCLS bits to 111'b so that period register determines the period and counter clear source,

[3.] Set the bits TIO2AEN and TIO2BEN, to 1 in the P_IOA_SPE register and configures the corresponding IO pin to output mode.

[4.] Select compare match output mode through P_TMR2_IOCtrl register.

[5.] Start the counting operation with the bit TMR2ST is set in P_TMR_Start register.

Figure 5-45 Example programming flowchart of PWM compare match output operation

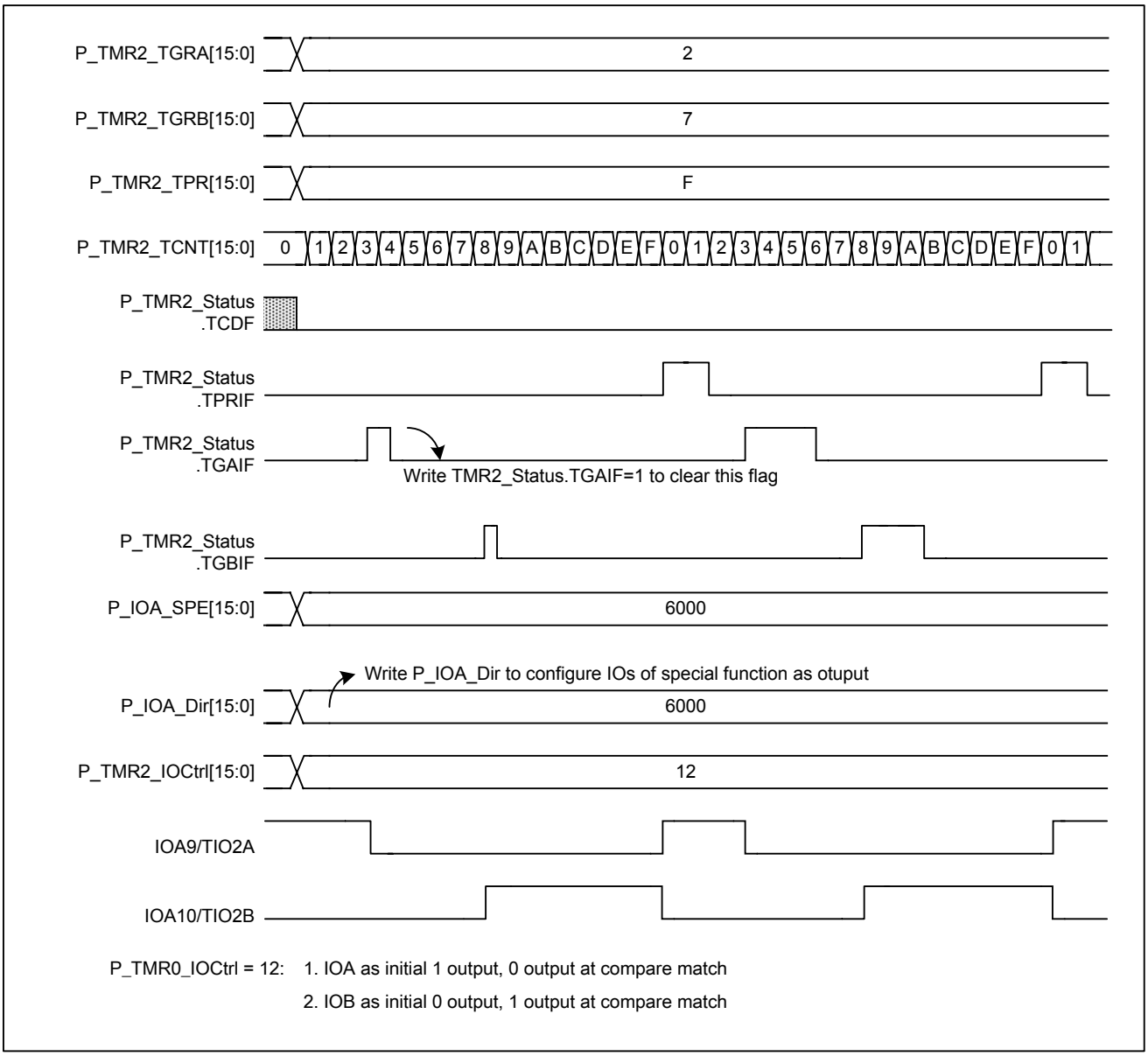


Figure 5-46 TMR2 edge aligned PWM

5.10.2.2. Timer mode Operation

The Timer mode can be selected by setting MODE in P_TMR2_Ctrl. Except output waveform, it operates the same as continuous up counting mode with edge-aligned PWM. The first compare match event of general register occurs when timer counter register matches the content of TGRA or TGRB register and the output will transits in the way set by IOAMODE, IOBMODE, respectively. If compare match event occurs again, the compare match interrupt flag will be set but output waveform retain. Figure 5-47 shows the output timing in Timer mode.

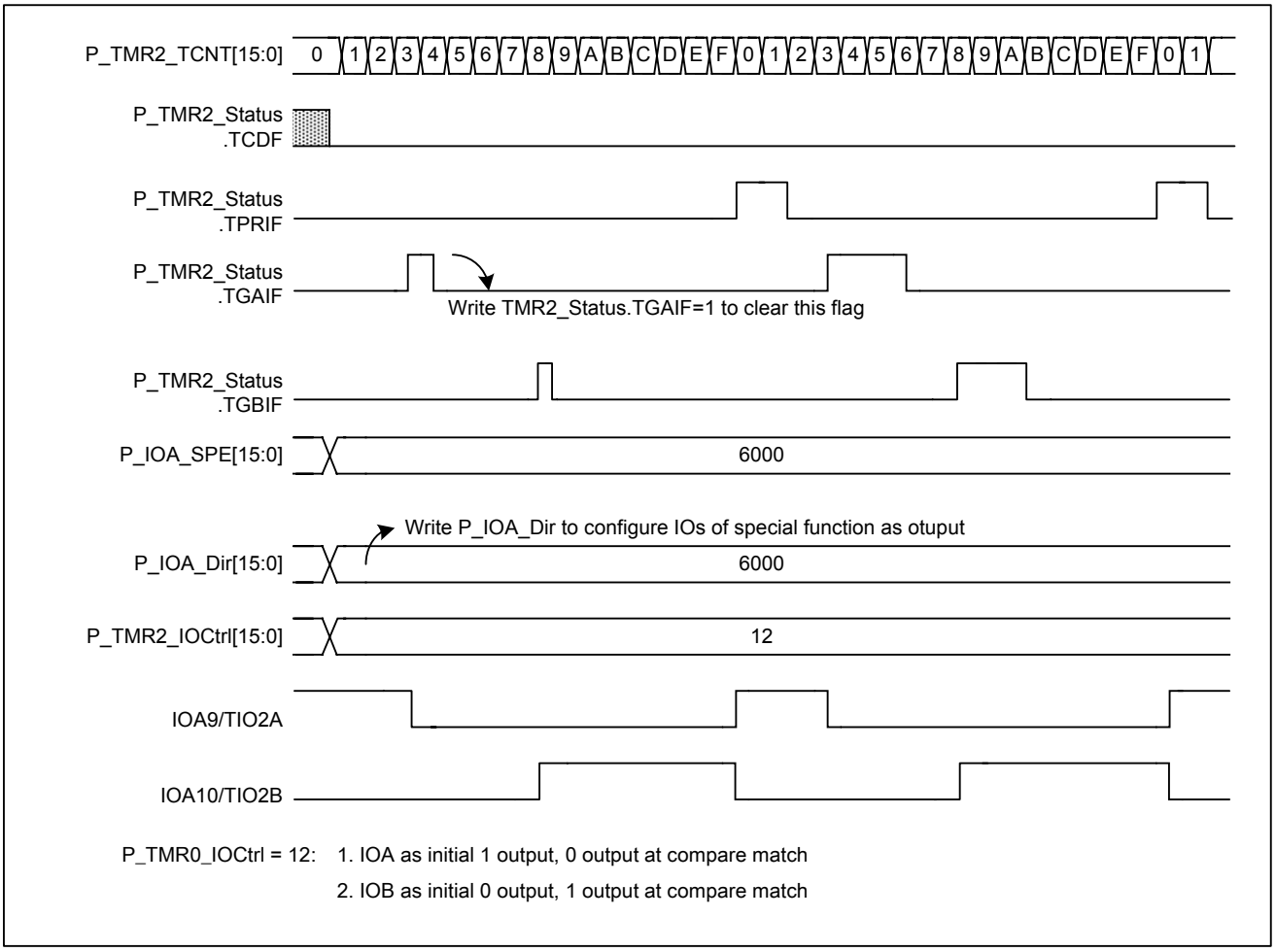


Figure 5-47 Timer mode output timing

5.10.2.3. Continuous up/down counting mode with Center-Aligned PWM

The operation of continuous up/down counting mode is the same as up counting mode except the timer period register defines the middle transition point of whole counting process. The counting direction changes from up to down when the timer counter register reaches the timer period register. The period of the timer is two times of P_TMR2_TPR of the scaled clock input and the setting of CKEGS in the P_TMR2_Ctrl register. Figure 5-48 shows the continuous up/down counting mode operation.

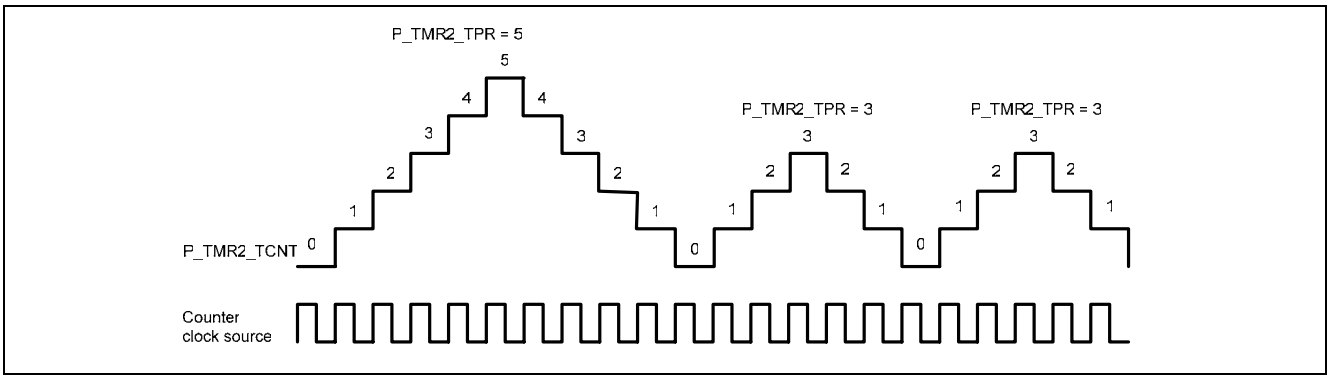


Figure 5-48 Continuous up/down counting example (CCLS = 111'b, CKEGS = 00'b, TMRPS = 000'b)

The initial value of the timer period register can be any value from 0x0000 to 0xFFFF. When the value of the timer counter register equals to timer period register, the TPM timer 2 start to count down to zero. The period interrupts behaves the same manner as described in the continuous up counting mode.

The counting direction is recorded at TCDF bit in the P_TMR2_Status register. Either the external clock input pin or internal clock source FCK can be selected as the clock source of the timer. Figure 5-49 shows the center-aligned mode PWM at continuous up/down counting mode of timer 2. Figure 5-50 is an example of center aligned PWM. The correlations between the configuration of P_TMR2_IOCtrl and PWM output, the register TGRx and interrupt status flag TGxIF(x=A, B) are shown, respectively.

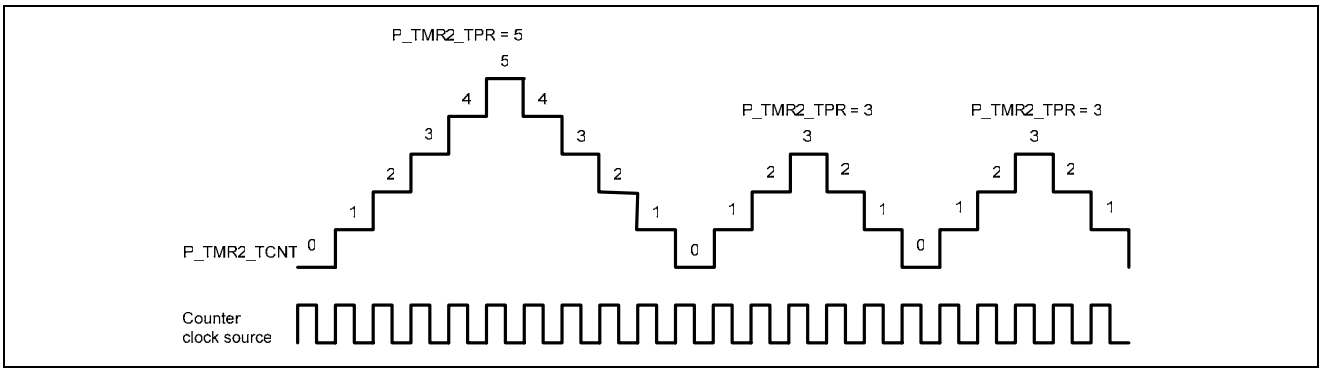


Figure 5-49 Center-Aligned mode PWM

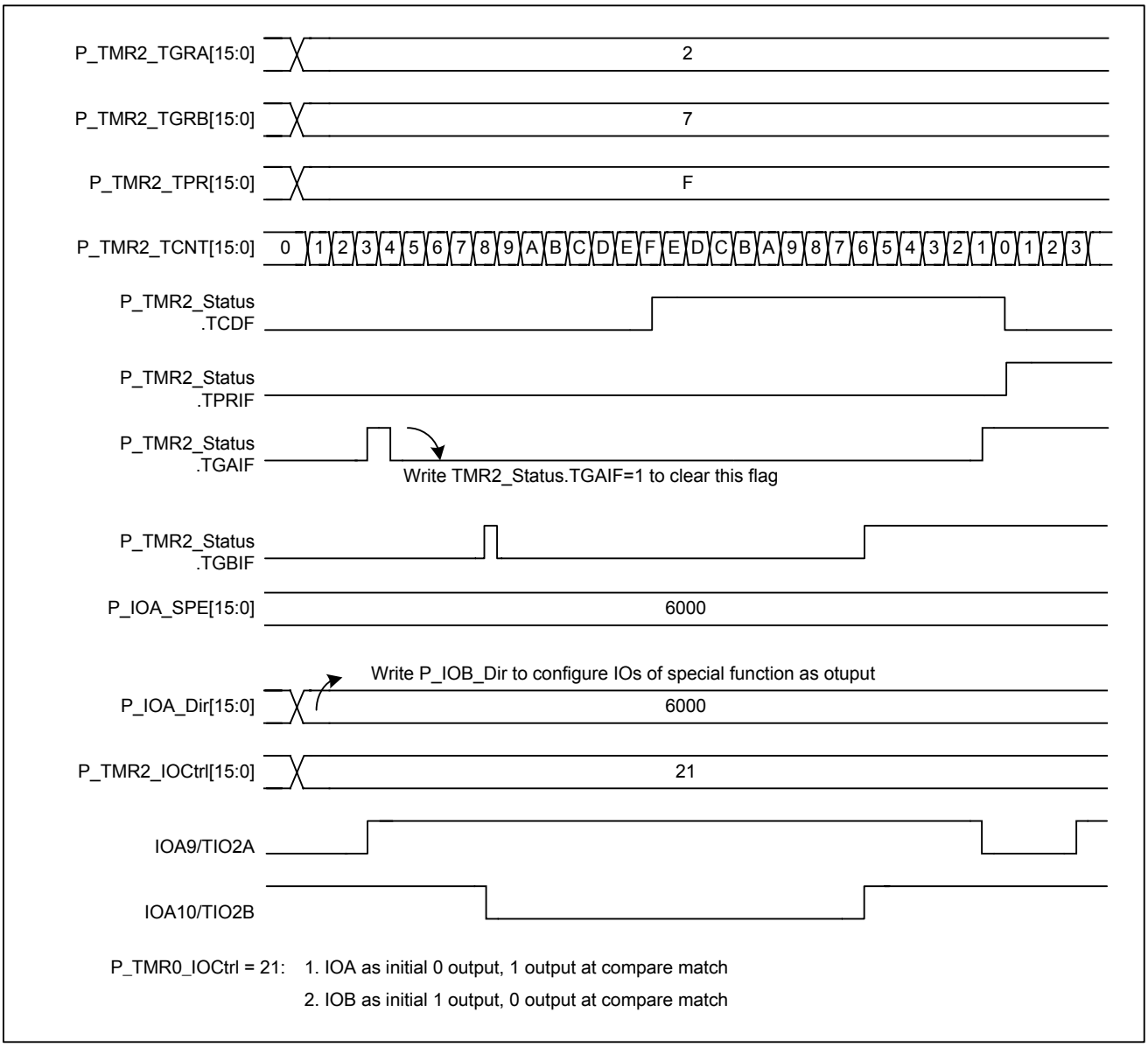


Figure 5-50 TMR2 center aligned PWM

5.10.2.4. Input Capture Operation

The capture function activation and the input edge at which the interrupt status flag issued are determined by the bits of IOAMODE and IOBMODE in the P_TMR2_IOCtrl register, respectively. It can be the rising edge, falling edge or both edge. The value of counter is always transferred to TGRx (x=A, B) and TBRx (x=A, B) at the rising and falling edge of corresponding input capture port, respectively. The counter register, P_ TMR2_TCNT can be cleared according to the setting of CCLS in P_TMR2_Ctrl register. The counter clear source can be one of TIO0A and TIO0B at the selected edge according to CLEGS in P_TMR2_Ctrl.

Table 5-17 shows the input capture configurations settings and results. When the input capture function is selected, the pulse width or period can be measured presents on input pin. Figure 5-52 shows the programming flowchart of input capture operation. Figure 5-53 is an example of input capture TIO0x (x=A, B). The correlations between the configuration of P_TMR2_IOCtrl and interrupt even are shown.

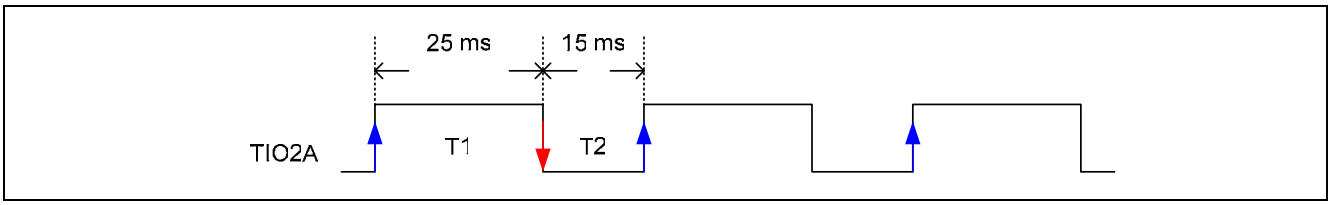


Figure 5-51 input capture signal connected to TIO2A

Table 5-17 input capture configuration settings and results

Input capture settings			Description	Results
CLEGS	CCLS	IOAMODE		
Rising edge	TIO2A	Rising edge	Counter cleared at rising edge, interrupt at rising edge	P_TMR2_TGRA = period (40 ms) P_TMR2_TBRA = T1 (25ms)
Rising edge	TIO2A	Falling edge	Counter cleared at rising edge, interrupt at falling edge	P_TMR2_TGRA = period (40 ms) P_TMR2_TBRA = T1 (25ms)
Rising edge	TIO2A	Both edge	Counter cleared at rising edge, interrupt at both edge	P_TMR2_TGRA = period (40 ms) P_TMR2_TBRA = T1 (25ms)
Falling edge	TIO2A	Rising edge	Counter cleared at falling edge, interrupt at rising edge	P_TMR2_TGRA = T2 (15 ms) P_TMR2_TBRA = period (40ms)
Falling edge	TIO2A	Falling edge	Counter cleared at falling edge, interrupt at falling edge	P_TMR2_TGRA = T2 (15 ms) P_TMR2_TBRA = period (40ms)
Falling edge	TIO2A	Both edge	Counter cleared at falling edge, interrupt at both edge	P_TMR2_TGRA = T2 (15 ms) P_TMR2_TBRA = period (40ms)
Both edge	TIO2A	Rising edge	Counter cleared at both edge, interrupt at rising edge	P_TMR2_TGRA = T2 (15 ms) P_TMR2_TBRA = T1 (25ms)
Both edge	TIO2A	Falling edge	Counter cleared at both edge, interrupt at falling edge	P_TMR2_TGRA = T2 (15 ms) P_TMR2_TBRA = T1 (25ms)
Both edge	TIO2A	Both edge	Counter cleared at both edge, interrupt at both edge	P_TMR2_TGRA = T2 (15 ms) P_TMR2_TBRA = T1 (25ms)

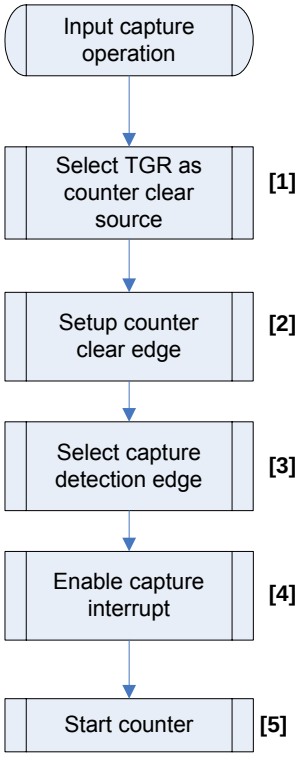


Figure 5-52 Example programming flowchart of input capture operation

Descriptions:

[1.] Select TIO2A or TIO2B as counter clear source, and then write value to CCLS bits in P_TMR2_Ctrl register.

[2.] Setup the counter clear edge by configuring CLEGS:

[3.] Select capture input interrupt edge as rising, falling, or both edge with setting of bits IOxMOD (x = A, B).

[4.] Enable capture interrupt in P_TMR2_INT register if necessary.

[5.] Start the counting operation with the bit TMR2ST set in P_TMR_Start register.

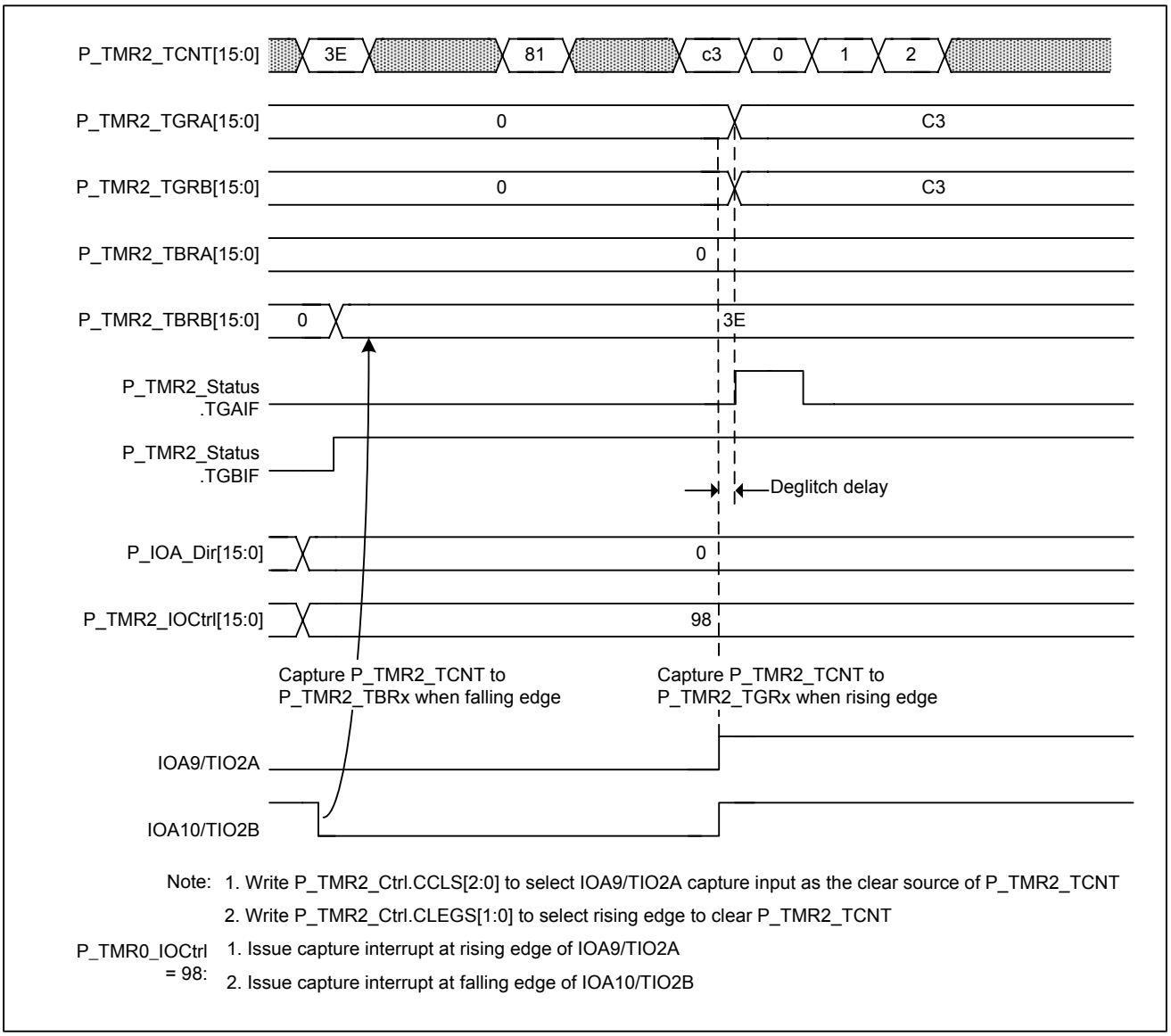


Figure 5-53 Capture input signal width and cycle

5.10.2.5. Timer 2 Control Registers

The P_TMR2_Ctrl configures the selection of timer clock source, counter clock edge, counter clear source, counter clear edge, and capture input sample clock and timer operating modes. TCLKA, TCLKB clock input will be sampled by system clock FCK. When programmed at counting on both edge, the input clock is halved. Any pulse narrower than four sampling clocks will be ignored.

- **P_TMR2_Ctrl (0x7402): Timer 2 Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SPCK		MODE				CLEGS	

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CCLS			CKEGS		TMRPS		

B15-B14	SPCK	Capture input sample clock select	00: FCK/1	01: FCK/2
			10: FCK/4	11: FCK/8
B13-B10	MODE	Modes select	0xxx: Timer mode	1x0x: Edge-aligned PWM mode
			1x1x: Center-aligned PWM mode	
B9-B8	CLEGS	Counter clear edge in input capture mode	00: do not clear	01: rising edge
			10: falling edge	11: both edge
B7-B5	CCLS	Counter clear source select	000: TCNT clearing disabled	001: TCNT cleared by TIO2A capture input
			010: TCNT cleared by TIO2B capture input	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: TCNT cleared by P_TMR2_TPR compare match
B4-B3	CKEGS	Clock edge select	00: Count at rising edge	01: Count at falling edge
			1X: Count at both edges	
B2-B0	TMRPS	Timer pre-scalar select	000: Counts on FCK /1	001: Counts on FCK /4
			010: Counts on FCK /16	011: Counts on FCK /64
			100: Counts on FCK /256	101: Counts on FCK /1024
			110: Counts on TCLKA pin input	111: Counts on TCLKB pin input

5.10.2.6. Timer 2 Period Register

The P_TMR2_TPR is a 16-bit readable/writable register. It is used to set the period of PWM waveform. When P_TMR2_TCNT register reaches P_TMR2_TPR register value, P_TMR2_TCNT register will be cleared to 0x0000 (up-counting mode) or start down-count (continuous up-/down-counting mode) according to MODE bits programmed in P_TMR2_Ctrl register. Its default value is 0xFFFF. When P_TMR2_TPR register is set to 0x0000, the P_TMR2_TCNT register counter will stop counting and remain at 0x0000.

- **P_TMR2_TPR (0x7437): Timer 2 Period Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
TMRPRD							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
TMRPRD							

5.10.2.7. Timer 2 General and Buffer Register

TGRA, TGRB are 16-bit registers. The TPM timer 2 has two timer general registers. The TGR registers are dual function 16-bit readable/writable registers, functioning as either PWM compare match or input capture registers.

The values in TGR and TCNT are constantly compared with each other when the TGR registers are used as PWM compare match output registers. When the both values match, the TGAIF or TGBIF bit in corresponding timer interrupt status register is set to 1. Compare match outputs can be selected by TIO2A and TIO2B.

When the TGR registers are used as input capture registers, the TCNT value is stored at the rising edge of input capture port.

When PWM mode, edge-aligned PWM mode, or center-aligned PWM mode is selected, the TGR register behaves as the duty ratio value register. Upon reset, the TGR registers are initialized to 0x0000.

The timer buffer registers TBRA and TBRB are the double buffers of TGRA and TGRB, respectively. The value of TGRx (x=A, B)

can automatically be updated when the period compare match event occurs. That is, the duty ratio value will not be updated until one period ends completely. When the TBR registers are used as input capture registers, the TCNT value is stored at the falling edge of input capture port.

- **P_TMR2_TGRA (0x7446): Timer 2 General Register A**
- **P_TMR2_TGRB (0x7447): Timer 2 General Register B**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRGLR							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRGLR							

- **P_TMR2_TBRA (0x7456): Timer 2 Buffer Register A**
- **P_TMR2_TBRB (0x7457): Timer 2 Buffer Register B**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRBUF							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRBUF							

5.10.2.8. Timer 2 Input and Output Control Register

The P_TMR2_IOCtrl register controls the PWM compare match output and input capture action type of TIO2A and TIO2B pins. By setting the CCLS and MODE bits in P_TMR2_Ctrl register will determine the timer IO action mode. When choosing PWM compare match output mode, the IOAMODE/IOBMODE bits determines the waveform generation depending on the active clock edge. When choosing input capture mode, the IOAMODE/IOBMODE bits defines the capture event.

- **P_TMR2_IOCtrl (0x7412): Timer 2 IO control register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
IOBMODE				IOAMODE			

B15-B8	Reserved			
B7-B4	IOBMODE	Select Timer 0/Timer 1 IOB Configuration	PWM compare match output mode:	
			0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match

			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
			Input capture mode：	
			1000: Issue input capture interrupt at rising edge	1001: Issue input capture interrupt at falling edge
			101x: Issue input capture interrupt at both edges	11xx: Input capture when Position Detection Register changes
B3-B0	IOAMODE	Select Timer 0/Timer 1 IOA Configuration	PWM compare match output mode：	
			0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
			Input capture mode：	
			1000: Issue input capture interrupt at rising edge	1001: Issue input capture interrupt at falling edge
			101x: Issue input capture interrupt at both edges	11xx: Input capture when Position Detection Register changes

5.10.2.9. Timer 2 Start Register

The P_TMR_Start register selects the operation of counter start/stop for the P_TMRx_TCNT (x = 0 ~ 4). When counter operation stopped, its contents will be cleared. Set TMR2ST bit to 1 would start the P_TMR2_TCNT register immediately and vice versa.

- **P_TMR_Start (0x7405): Timer Counter Start Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved			TMR4ST	TMR3ST	TMR2ST	TMR1ST	TMR0ST

B15-B5	Reserved			
B4	TMR4ST	Timer 4 counter start setting	0: Counter operation stopped	1: Performs counting operation
B3	TMR3ST	Timer 3 counter start setting	0: Counter operation stopped	1: Performs counting operation
B2	TMR2ST	Timer 2 counter start setting	0: Counter operation stopped	1: Performs counting operation
B1	TMR1ST	Timer 1 counter start setting	0: Counter operation stopped	1: Performs counting operation
B0	TMR0ST	Timer 0 counter start setting	0: Counter operation stopped	1: Performs counting operation

5.10.2.10. Timer 2 Interrupt Enable Register

The P_TMR2_INT register is used to enable or disable A/D conversion start request by TGRA compare match, interrupt requests for period register compare match and input capture/compare match of TGRA or TGRB.

- **P_TMR2_INT (0x7422): Timer 2 Interrupt Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R	R	R/W	R	R	R/W	R/W
0	0	0	0	0	0	0	0
TADSE	Reserved		TPRIE	Reserved		TGBIE	TGAIE

B15-8	Reserved			
B7	TADSE	A/D conversion start request by TGRA enable bit	0: Disable	1: Enable
B6-B5	Reserved			
B4	TPRIE	Timer Period Register interrupt enable bit	0: Disable	1: Enable
B3-B2	Reserved			
B1	TGBIE	Timer General B Register interrupt enable bit	0: Disable	1: Enable
B0	TGAIE	Timer General A Register interrupt enable bit	0: Disable	1: Enable

5.10.2.11. Timer 2 Interrupt Status Register

The interrupt status register indicates the event generation of a period registers compare match and input capture/compare match of TGRA or TGRB. These flags show the interrupt sources. An interrupt would be generated when the corresponding interrupt enable bit is set in P_TMR2_INT register. The TCDIF represents the counter direction when timer is setup to center-aligned PWM mode.

- **P_TMR2_Status (0x7427): Timer 2 Interrupt Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R	R	R/W	R	R	R/W	R/W
0	0	0	0	0	0	0	0
TCDF	Reserved		TPRIF	Reserved		TGBIF	TGAIF

B15-8	Reserved			
B7	TCDF	Timer Count direction flag	0: Up-counting	1: Down-counting
B6-B5	Reserved			
B4	TPRIF※	Timer Period Register compare match flag	0: Compare match not occurred	1: Compare match has occurred
B3-B2	Reserved			
B1	TGBIF※	Timer General B Register input capture/compare match flag	0: Input capture/compare match not occurred	1: Input capture/compare match has occurred
B0	TGAIF※	Timer General A Register input capture/compare match flag	0: Input capture/compare match not occurred	1: Input capture/compare match has occurred

※: write '1' to clear this flag

5.10.2.12. Timer 2 Counter Register

The TPM timer 2 has a 16 bit counter P_TMR2_TCNT register. It is a readable register that increments/decrements according to input clocks.

Bits TMRPS in corresponding timer control register can select input clocks. P_TMR2_TCNT can increment or decrement in center-aligned PWM mode, although they only increment in other modes. The P_TMR2_TCNT register is reset to 0x0000 by compare matches with corresponding TGRA, TGRB or input captures to TGRA, TGRB.

- **P_TMR2_TCNT (0x7432): Timer 2 Counter Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRCNT							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRCNT							

5.11. MCP TIMER 3 AND 4 MODULE

5.11.1. Introduction

There are two channels of 16bit MCP (Motor Control PWM) timers, MCP timer 3 and MCP timer 4 on the SPMC75F2413A chip. The MCP timers provide two independent set of full function for three-phase, six programmable PWM waveform output capabilities. The MCP timer 3 should work with PDC timer 0 and MCP timer 4 works with PDC timer 1 to form the speed closed loop control for BLDC and ACI motor applications. This MCP timer module has totally twelve timer output pins for motor control operations. Figure 5-54 shows the block diagram of the MCP timer 3 and 4 module. For details of timer specifications, please refer to Table 5-18.

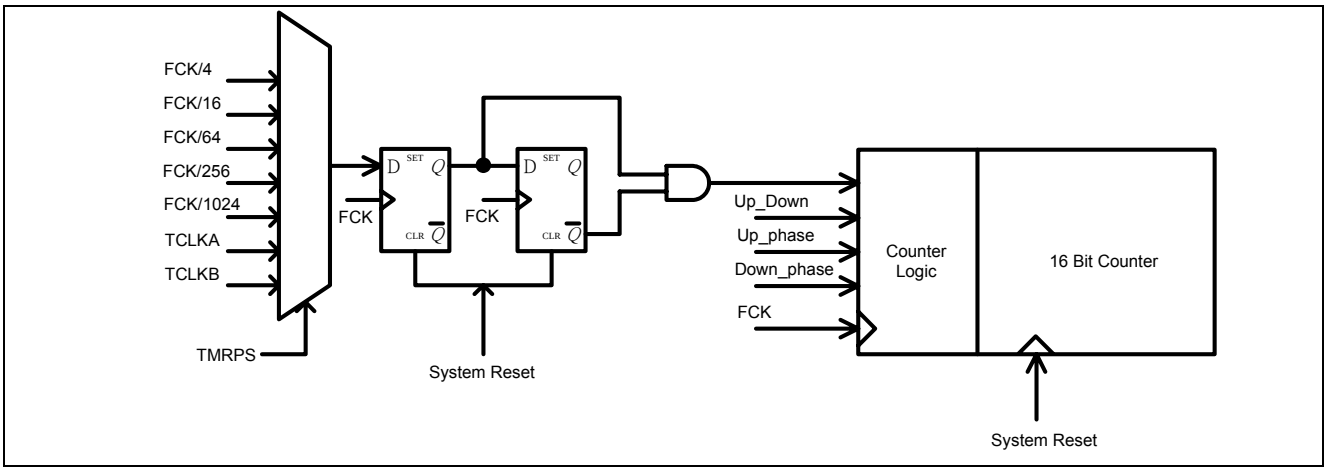


Figure 5-54 MCP timer 3 and 4 block diagram

Table 5-18 MCP timer 3 and 4 specification

Function	MCP Timer 3	MCP Timer 4
Clock sources	Internal clock: FCK/1, FCK/4, FCK/16, FCK/64, FCK/256, FCK/1024 External clock: TCLKA, TCLKB	
Output pins	◆ TIO3A/U1 ◆ TIO3B/V1 ◆ TIO3C/W1	◆ TIO4A/U2 ◆ TIO4B/V2 ◆ TIO4C/W2

Function		MCP Timer 3	MCP Timer 4
		◆ TIO3D/U1N ◆ TIO3E/V1N ◆ TIO3F/W1N	◆ TIO4D/U2N ◆ TIO4E/V2N ◆ TIO4F/W2N
Timer general register		◆ P_TMR3_TGRA ◆ P_TMR3_TGRB ◆ P_TMR3_TGRC ◆ P_TMR3_TGRD	◆ P_TMR4_TGRA ◆ P_TMR4_TGRB ◆ P_TMR4_TGRC ◆ P_TMR4_TGRD
Timer buffer register		◆ P_TMR3_TBRA ◆ P_TMR3_TBRB ◆ P_TMR3_TBRC	◆ P_TMR4_TBRA ◆ P_TMR4_TBRB ◆ P_TMR4_TBRC
Interrupt period		Interrupt every one, two, four and eight period	
Counting edge		◆ Rising ◆ Falling ◆ Both edge	
Counter clear source		Clear on P_TMR3_TPR compare match	Clear on P_TMR4_TPR compare match
PWM compare match output function	1 output	Yes	Yes
	0 output	Yes	Yes
	Output Hold	Yes	Yes
BLDC motor drive PWM		Yes	Yes
ACI motor drive PWM		Yes	Yes
Edge-aligned PWM		Yes	Yes
Center-aligned PWM		Yes	Yes
Complementary PWM		Yes	Yes
Timer buffer operation		Yes, but not P_TMR3_TGRD	Yes, but not P_TMR4_TGRD
AD convert start trigger		P_TMR3_TGRD compare match	P_TMR4_TGRD compare match
PWM duty partial load prevention		Yes, through P_TMR_LDOK register	Yes, through P_TMR_LDOK register
PWM output enable control		Yes, through P_TMR_Output register	Yes, through P_TMR_Output register
PWM waveform control	Forced H	Yes	Yes
	Forced L	Yes	Yes
	Active H	Yes	Yes
	Active L	Yes	Yes
UVW phase synchronization		◆ P_POS0_DectData register change ◆ P_TMR3_TGRB compare match ◆ P_TMR3_TGRC compare match	◆ P_POS1_DectData register change ◆ P_TMR4_TGRB compare match ◆ P_TMR4_TGRC compare match
Duty Mode		Use P_TMR3_TGRA register or thee timer general register	Use P_TMR4_TGRA register or thee timer general register
MCP registers write protection		Yes, through P_TPWM_Write register	Yes, through P_TPWM_Write register
External fault input pin		FTIN1	FTIN2
External overload input pin		OL1	OL2
Interrupt source		◆ Timer 3 TPR interrupt ◆ Timer 3 TGRA interrupt ◆ External fault input 1 interrupt ◆ External overload input 1 interrupt ◆ MCP3 PWM output short interrupt	◆ Timer 4 TPR interrupt ◆ Timer 4 TGRA interrupt ◆ MCP4 external fault input 2 interrupt ◆ External overload input 2 interrupt ◆ MCP4 PWM output short interrupt

5.11.2. MCP Timer 3 and 4 Counting Operation

The on-chip MCP timer 3 and 4 have the following five possible counting operations：

- ❑ Timer mode operation.
- ❑ Count on external clock input pin TCLKA or TCLKB.
- ❑ Edge-aligned PWM mode (continuous up counting, PWM output mode).
- ❑ Center-aligned PWM mode (continuous up/down counting, PWM output mode).
- ❑ Complementary PWM mode w/o dead-time control.

5.11.2.1. Continuous Up Counting Mode with Edge-Aligned PWM

Each MCP timer channel can be configured as edge-aligned PWM mode by setting MODE bits in P_TMR0_Ctrl. At this mode, the timer counter act as up-counting timer and counting from 0x0000 to timer period register value. User must set P_TMRx_TPR (x = 3 ~ 4) register and set counter clear source (CCLS) as cleared by timer period compare match and also needs to setup proper bits value of PRDINT in the P_TMRx_Ctrl (x = 3, 4) register.

The MCP timer continuous up counting according to the input clock sources from bits value TMRPS defined in corresponding timer control register. The timer counter register will be cleared to zero when the register value matches that of the timer period register and period compare match event interrupt flag TPRIF is set. The period interrupt request is generated when PPRIE bit is set in P_TMRx_INT (x = 3, 4) register.

The initial value of P_TMRx_TPR (x = 3, 4) can be any value from 0x0000 to 0xFFFF. Either the external clock input pin or internal clock source FCK can be selected as the clock source of the timer. The normal continuous up counting mode is extremely suitable for the generation of edge-triggered or asynchronous PWM waveforms and sampling periods in digital motor control systems. Figure 5-55 shows the normal continuous up counting mode of the MCP timer 3.

At edge-aligned PWM mode, user must configure P_TMRx_TPR (x= 3, 4) period register and P_TMRx_TGRy (y = A, B, C) general register, then set counter clear source (CCLS) as cleared by timer period compare match. The output conditions of compare match are configured by setting P_TMRx_IOCtrl (x= 3, 4) register.

Figure 5-56 shows the normal continuous up counting mode for edge-aligned PWM generation of timer 3.

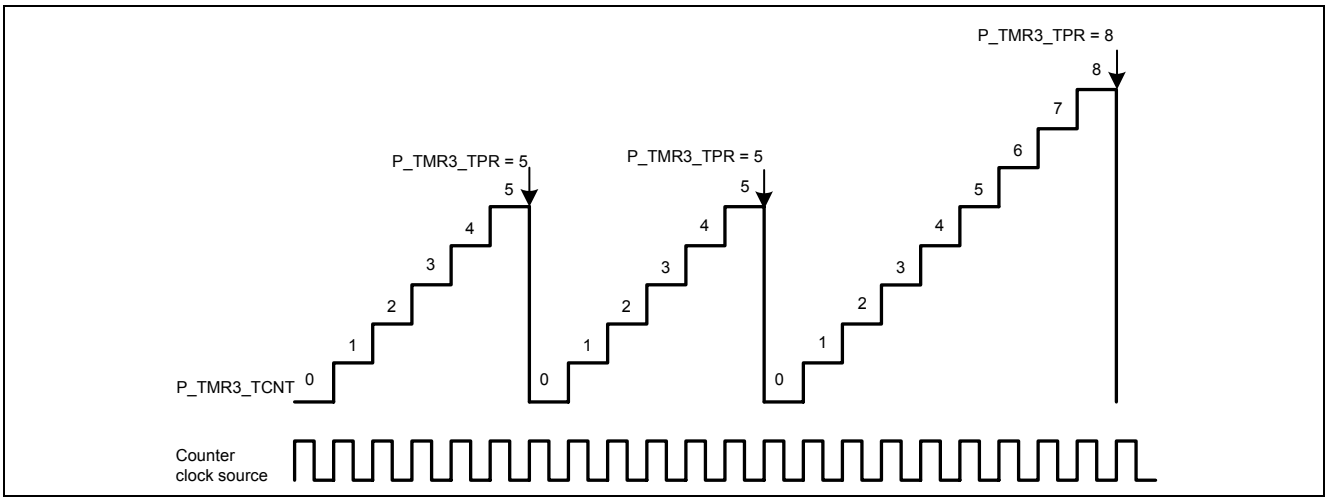


Figure 5-55 Continuous up counting example (CCLS = 111'b, CKEGS = 00'b, TMRPS = 000'b)

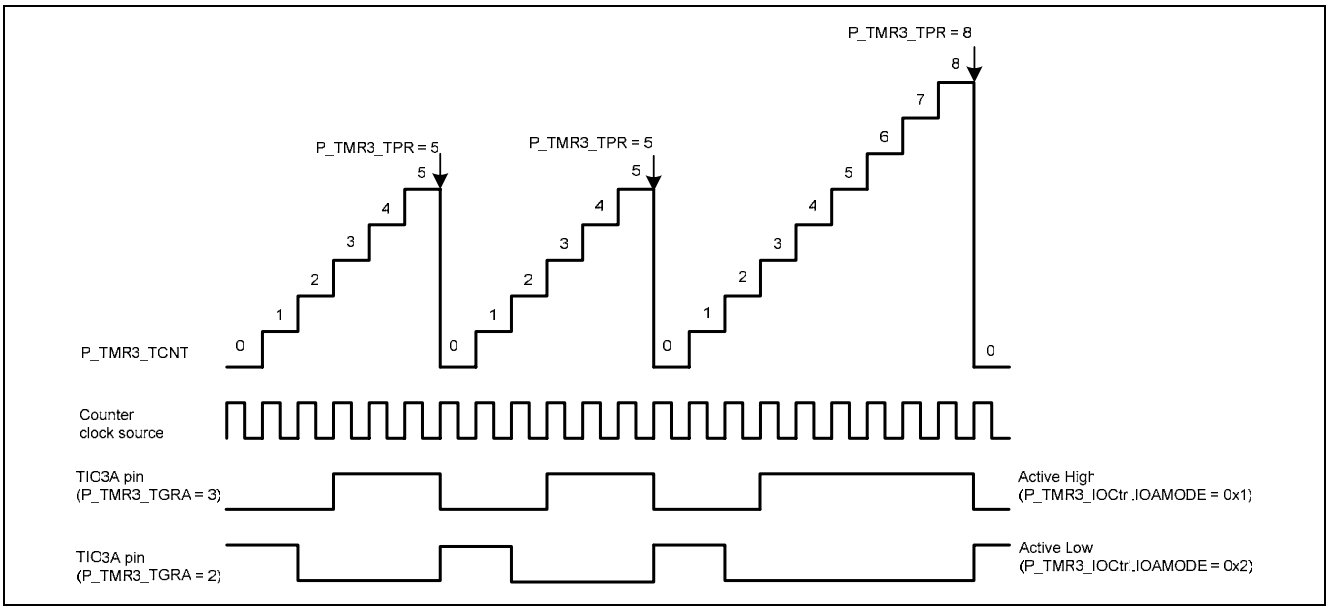


Figure 5-56 Edge-Aligned mode PWM

5.11.2.2. Timer mode Operation

The Timer mode can be selected by setting MODE in P_TMRx_Ctrl (x=3, 4). Except output waveform, it operates the same as continuous up counting mode with edge-aligned PWM. The first compare match event of general register occurs when timer counter register matches the content of TGRA, TGRB or TGRC register and the output will transits in the way set by IOAMODE, IOBMODE and IOCMODE, respectively. If compare match event occurs again, the compare match interrupt flag will be set but output waveform retain.

5.11.2.3. Continuous up/down counting mode with Center-Aligned PWM

The operation of continuous up/down counting mode is the same as up counting mode except the timer period register defines the middle transition point of the whole counting process. The counting direction changes from up to down when the timer counter register reaches the timer period register. The period of the timer is two times of P_TMRx_TPR (x = 3, 4) of the scaled clock input and the setting of CKEGS in the P_TMRx_Ctrl (x = 3, 4) register. Figure 5-57 shows the continuous up/down counting mode operation.

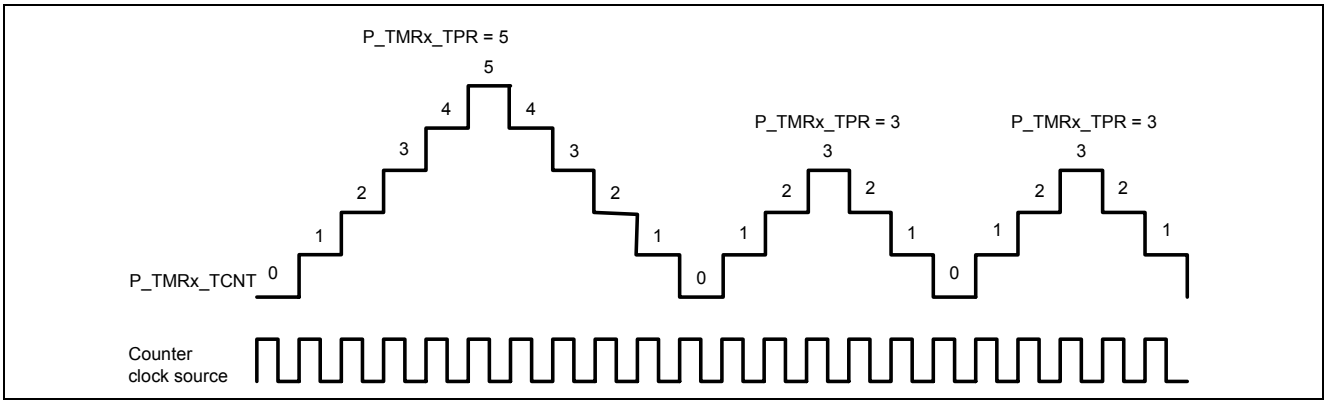


Figure 5-57 Continuous up/down counting example (CCLS = 111'b, CKEGS = 00'b, TMRPS = 000'b)

The initial value of the timer period register can be any value from 0x0000 to 0xFFFF. When the value of the timer counter register equals to timer period register, the MCP timer start to count down to zero. The period interrupt behaves the same manner as described in the continuous up counting mode.

The counting direction is recorded at TCDF bit in the P_TMRx_Status (x = 3, 4) register. Either the external clock input pin or internal clock source FCK can be selected as the clock source of the timer. Figure 5-58 shows the center-aligned mode PWM at continuous up/down counting mode of timer 3.

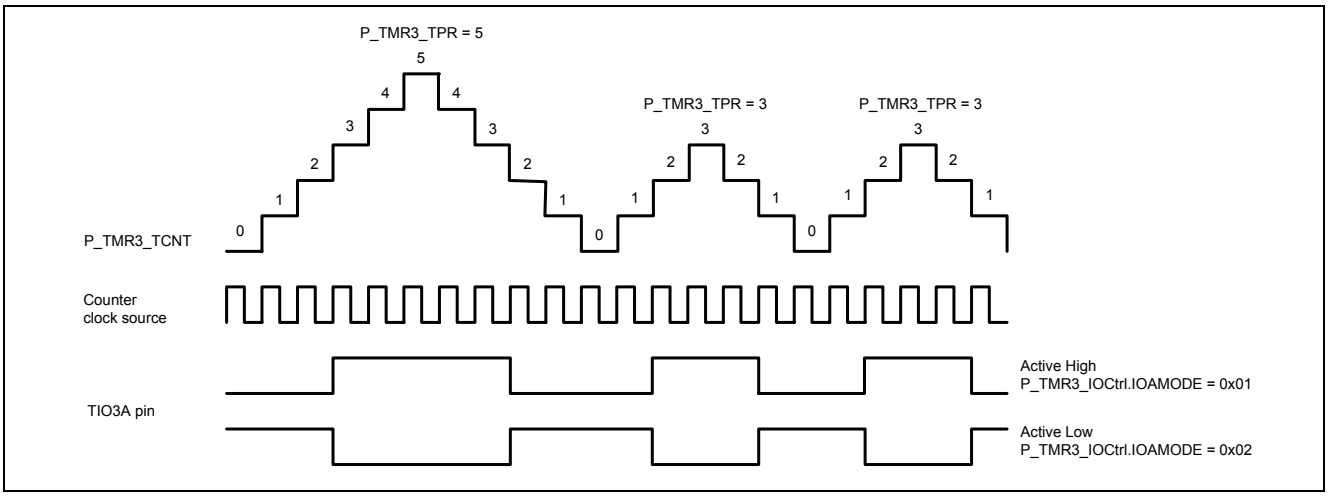


Figure 5-58 Center-Aligned mode PWM

5.11.2.4. Timer/PWM Module Write Enable Control Register

User must write 0x5A01 to P_TPWM_Write register to enable the timer 3 and write 0x5A02 to P_TPWM_Write to enable timer 4 for timer PWM generation. The P_TPWM_Write register provides a way to prevent the settings of timer 3 or 4 being miswritten due to CPU runaway. To modify the setting of timer 3 or timer 4, the corresponding TMR3/4WE bit must be set to '1'. Registers concerned with TMR3WE and TMR4WE are listed below. The recommended procedure of P_TPWM_Write register is first to read the content then does logical OR operation on control words (0x5A01 or 0x5A02). Write back the result to P_TPWM_Write last.

The TMR3WE and TMR4WE control the MCP registers respectively as follows:

TMR3WE bit controls the write operation of following registers：
P_TMR3_Ctrl, P_TMR3_IOCtrl, P_TMR3_INT, P_TMR3_Status, P_TMR3_DeadTime, P_TMR_Start, P_TMR_Output

TMR4WE bit controls the write operation of following registers：
P_TMR4_Ctrl, P_TMR4_IOCtrl, P_TMR4_INT, P_TMR4_Status, P_TMR4_DeadTime, P_TMR_Start, P_TMR_Output

- **P_TPWM_Write (0x7409): Timer/PWM Module Write Enable Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
Reserved						TMR4WE	TMR3WE

B15-8	WECHK	Write enable check bits pattern. To properly enable TMR4WE and TMR3WE, these bits must be written to '0x5A'. Otherwise, the control bits will not be set. These bits will be read as '0'.		
B7-2	Reserved			
B1	TMR4WE	Timer 4 setting registers write enable select bit	0: Disable	1: Enable
B0	TMR3WE	Timer 3 setting registers write enable select bit	0: Disable	1: Enable

5.11.2.5. Timer 3 and 4 Control Registers

The P_TMRx_Ctrl (x = 3, 4) configures the selection of timer clock source, counter clock edge, counter clear source, counter clear edge, TPR interrupt frequency and timer operating modes. TCLKA, TCLKB clock input will be sampled by system clock FCK. Any pulse narrower than four sampling clocks will be ignored. The MCP timer 3 and 4 does not support input capture mode. When programmed at counting on both edge, the input clock is halved.

- **P_TMR3_Ctrl (0x7403): Timer 3 Control Register**
- **P_TMR4_Ctrl (0x7404): Timer 4 Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
PRDINT		MODE				Reserved	

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CCLS			CKEGS		TMRPS		

B15-B14	PRDINT	TPR interrupt frequency select	00: Interrupt every period	01: Interrupt once every 2 periods
			10: Interrupt once every 4 periods	11: Interrupt once every 8 periods
B13-B10	MODE	Modes select	0xxx: Timer mode	1x0x: Edge-aligned PWM mode
			1x1x: Center-aligned PWM mode	
B9-B8	Reserved			
B7-B5	CCLS	Counter clear source select	000: TCNT clearing disabled	001: Reserved
			010: Reserved	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: TCNT cleared by P_TMRx_TPR (x = 3, 4) compare match
B4-B3	CKEGS	Clock edge select	00: Count at rising edge	01: Count at falling edge
			1X: Count at both edges	
B2-B0	TMRPS	Timer pre-scalar select	000: Counts on FCK /1	001: Counts on FCK /4
			010: Counts on FCK /16	011: Counts on FCK /64
			100: Counts on FCK /256	101: Counts on FCK /1024
			110: Counts on TCLKA pin input	111: Counts on TCLKB pin input

5.11.2.6. Timer 3 and 4 Period Register

The P_TMRx_TPR (x = 3, 4) is a 16-bit readable/writable register. It is used to set the period of PWM waveform. When P_TMRx_TCNT (x = 3, 4) register reaches P_TMRx_TPR (x = 3, 4) register value, P_TMRx_TCNT (x = 3, 4) register will be cleared to 0x0000 (up-counting mode) or start down-count (continuous up-/down-counting mode) according to MODE bits programmed in P_TMRx_Ctrl (x = 3, 4) registers. Its default value is 0xFFFF. When P_TMRx_TPR (x = 3, 4) register is set to 0x0000, the P_TMRx_TCNT (x = 3, 4) register counter will stop counting and remain at 0x0000.

- **P_TMR3_TPR (0x7438): Timer 3 Period Register**
- **P_TMR4_TPR (0x7439): Timer 4 Period Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
TMRPRD							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1
TMRPRD							

5.11.2.7. Timer Load-OK Register

In PWM output mode, to prevent partial duty parameters from being loaded incorrectly, correct updating procedures must be followed. The correct updating procedures are first update P_TMR3/4_TGRA-C, then set corresponding LDOK bit to '1'. Once LDOK bit has been set, all duty parameters are considered to be ready, and will be loaded to TGR when counter has been cleared. Then LDOK bit will be cleared to '0' when counter has been cleared. During LDOK be set to '1', the contents of P_TMR3/4_TGRA-C will not be altered by writing to these registers. To correctly set the LDOK bits, the pattern '101010' must be written to P_TMR_LDOK bit 7 to bit 2, otherwise the LDOK bits will not be updated. For example, to set LDOK0 to '1', 0x00A9 must be written to P_TMR_LDOK.

- **P_TMR_LDOK (0x740A): Timer Load-OK Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
TLDCHK						LDOK1	LDOK0

B15-B8	Reserved		
B7-B2	TLCKHK	Timer load register check bits	To change the settings of P_TMR_LDOK, "101010" must be written to these bits. Otherwise LDOK1 and LDOK0 will not be changed. These bits will be read as '0'.
B1	LDOK1	P_TMR4_TGRA-C ok to load bit	This bit determines whether the values in P_TMR4_TGRA-C are ready to be loaded to PWM module. The values in P_TMR4_TGRA-C will not be loaded to PWM module until this bit has been set to '1'. After the values have been loaded, this bit will be cleared automatically. Note that when this bit has been set, the values in P_TMR4_TGRA-C will not be changed by writing to these registers.
B0	LDOK0	P_TMR3_TGRA-C ok to load bit	This bit determines whether the values in P_TMR3_TGRA-C are ready to be loaded to PWM module. The values in P_TMR3_TGRA-C will not be loaded to PWM module until this bit has been set to '1'. After the values have been loaded, this bit will be cleared automatically. Note that when this bit has been set, the values in P_TMR3_TGRA-C will not be changed by writing to these registers.

5.11.2.8. Timer 3 and 4 General and Buffer Register

The TGRA, TGRB and TGRC registers are dual function 16-bit readable/writable registers, functioning as compare match registers. The values in TGR and TCNT are constantly compared with each other when the TGR registers are used as compare match registers. When edge-aligned PWM or center-aligned PWM mode is selected, the TGR register controls duty ratio of PWM output. Upon reset, the TGR registers are initialized to 0x0000.

The bit TGDIF in P_TMRx_Status (x=3, 4) will be set when TCNT counter value matches the content of P_TMRx_TGRD(x = 3, 4) register and this event could trigger an ADC to start a conversion. Remarkably, the TGRD doest not derive any output waveform.

The timer buffer registers TBRA, TBRB and TBRC are the double buffers of TGRA, TGRB and TGRC, respectively. The value of TGRx (x=A, B, C) can automatically be updated when the period compare match event occurs. That is, the duty ratio value will not be updated until one period ends completely.

- **P_TMR3_TGRA (0x7448): Timer 3 General Register A**
- **P_TMR3_TGRB (0x7449): Timer 3 General Register B**
- **P_TMR3_TGRC (0x744A): Timer 3 General Register C**
- **P_TMR3_TGRD (0x744B): Timer 3 General Register D**
- **P_TMR4_TGRA (0x744C): Timer 4 General Register A**
- **P_TMR4_TGRB (0x744D): Timer 4 General Register B**
- **P_TMR4_TGRC (0x744E): Timer 4 General Register C**
- **P_TMR4_TGRD (0x744F): Timer4 General Register D**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRGLR							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRGLR							

- **P_TMR3_TBRA (0x7458): Timer 3 Buffer Register A**
- **P_TMR3_TBRB (0x7459): Timer 3 Buffer Register B**
- **P_TMR3_TBRC (0x745A): Timer 3 Buffer Register C**
- **P_TMR4_TBRA (0x745C): Timer 4 Buffer Register A**
- **P_TMR4_TBRB (0x745D): Timer 4 Buffer Register B**
- **P_TMR4_TBRC (0x745E): Timer 4 Buffer Register C**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRBUF							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
TMRBUF							

5.11.2.9. Timer 3 and 4 Input and Output Control Register

The P_TMRx_IOCtrl (x =3, 4) register controls the action type of PWM compare match output in TIOxA, TIOxB, and TIOxC (x = 3, 4) pins. By setting the CCLS and MODE bits in P_TMRx_Ctrl (x = 3, 4) register will determine the timer action mode. When choosing PWM compare match output mode, the IOAMODE/IOBMODE/IOCMODE bits determines the waveform generation depending on the active clock edge. The MCP 3 and 4 does not have the setting for input capture operation and bits value 1xxx'b of IOAMODE/IOBMODE/IOCMODE are invalid.

- **P_TMR3_IOCtrl (0x7413): Timer 3 IO control register**
- **P_TMR4_IOCtrl (0x7414): Timer 4 IO control register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved				IOCMODE			

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
IOBMODE				IOAMODE			

B15-B12	Reserved			
B11-B8	IOCMODE	Select Timer 0/Timer 1 IOC Configuration	0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
B7-B4	IOBMODE	Select Timer 0/Timer 1 IOB Configuration	0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	
B3-B0	IOAMODE	Select Timer 0/Timer 1 IOA Configuration	0000: Initial output 0, 0 output at compare match	0001: Initial output 0, 1 output at compare match
			0010: Initial output 1, 0 output at compare match	0011: Initial output 1, 1 output at compare match
			01xx: Output hold	

5.11.2.10. Timer Start Register

The P_TMR_Start register selects the operation of counter start/stop for the P_TMRx_TCNT (x = 0 ~ 4). When counter operation stopped, its contents will be cleared. Setting TMR3ST or TMR4ST bit to 1 would start the P_TMR3_TCNT or P_TMR4_TCNT register immediately and vice versa.

- **P_TMR_Start (0x7405): Timer Counter Start Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved			TMR4ST	TMR3ST	TMR2ST	TMR1ST	TMR0ST

B15-B5	Reserved			
B4	TMR4ST	Timer 4 counter start setting	0: Counter operation stopped	1: Performs counting operation
B3	TMR3ST	Timer 3 counter start setting	0: Counter operation stopped	1: Performs counting operation
B2	TMR2ST	Timer 2 counter start setting	0: Counter operation stopped	1: Performs counting operation
B1	TMR1ST	Timer 1 counter start setting	0: Counter operation stopped	1: Performs counting operation
B0	TMR0ST	Timer 0 counter start setting	0: Counter operation stopped	1: Performs counting operation

- **P_TMR3_INT (0x7423): Timer 3 Interrupt Enable Register**
- **P_TMR4_INT (0x7424): Timer 4 Interrupt Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R	R	R/W	R/W	R	R	R
0	0	0	0	0	0	0	0
TADSE	Reserved		TPRIE	TGDIE	Reserved		

B15-8	Reserved			
B7	TADSE※	A/D conversion start request by TGRD enable bit	0: Disable	1: Enable
B6-B5	Reserved			
B4	TPRIE	Timer Period Register interrupt enable bit	0: Disable	1: Enable
B3	TGDIE※	Timer General D Register interrupt enable bit	0: Disable	1: Enable
B2-B0	Reserved			

※ Please refer to Timer 3 and 4 Interrupt Status Register.

5.11.2.11. Timer 3 and 4 Interrupt Status Register

The interrupt status register indicates the event generation of period register compare match and compare match of TGRD. These flags show the interrupt sources. An interrupt would be generated when the corresponding interrupt enable bit is set in P_TMRx_INT (x = 3, 4) register. The TCDF represents the counter direction when timer is setup to center-aligned PWM mode. The bit TGDIF in P_TMRx_Status (x=3, 4) will be set when timer counter register matches the content of P_TMRx_TGRD(x = 3, 4) register and this event could trigger an ADC to start a conversion.

- **P_TMR3_Status (0x7428): Timer 3 Interrupt Status Register**
- **P_TMR4_Status (0x7429): Timer 4 Interrupt Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R	R	R/W	R/W	R	R	R
0	0	0	0	0	0	0	0
TCDF	Reserved		TPRIF	TGDIF	Reserved		

B15-8	Reserved			
B7	TCDF	Timer Count direction flag	0: Up-counting	1: Down-counting
B6-B5	Reserved			
B4	TPRIF※	Timer Period Register compare match flag.	0: Compare match not occurred	1: Compare match has occurred
B3	TGDIF※	Timer General D Register compare match flag	0: Compare match not occurred	1: Compare match has occurred
B2-B0	Reserved			

※: write '1' to clear this flag

5.11.2.12. Timer 3 and 4 Counter Register

The MCP timer 3 and timer 4 have two TCNT counters (P_TMR3_TCNT and P_TMR4_TCNT), one for each channel. The TCNT counters are 16-bit readable registers that increment/decrement according to input clocks.

Bits TMRPS in corresponding timer control register can select input clocks. P_TMR3_TCNT and P_TMR4_TCNT increment/decrement in center-aligned PWM mode, while they only increment in other modes. The TCNT counters are initialized to 0x0000 when TCNT value matches the period register.

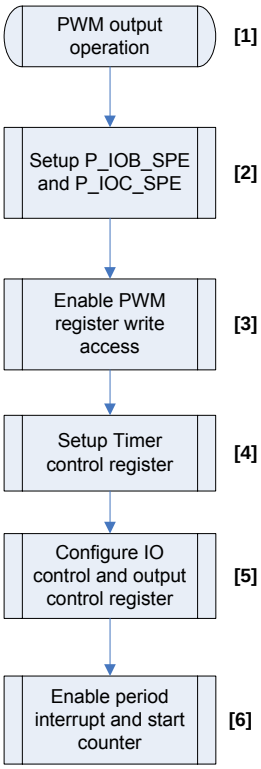
- **P_TMR3_TCNT (0x7433): Timer 3 Counter Register**
- **P_TMR4_TCNT (0x7434): Timer 4 Counter Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRCNT							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
TMRCNT							

5.11.2.13. PWM Output Operation

The MCP timer module has two channels and can perform PWM function up to twelve pins output. The output waveforms have active low at compare match, active high at compare match , forced high and forced low for the corresponding TIOxA, TIOxB, TIOxC, TIOxD, TIOxE and TIOxF (x = 3, 4) output pin using compare match with P_TMRx_TGRA, P_TMRx_TGRB, P_TMRx_TGRC (x = 3, 4) register respectively. Figure 5-59 shows the programming flowchart of PWM operation.



Descriptions:

[1.] Program the PWM specified GPIO pins as output port and fault input pin if necessary.

[2.] Enable the special function of PWM of P_IOB_SPE and P_IOC_SPE.

[3.] Write control word to P_TPWM_Write register to enable the write access.

[4.] Setup the CCLS bits to 111'b so that period register determines the period and counter clear source.

[5.] Select compare match output mode through P_TMRx_IOCtrl (x = 3, 4) register and choose desired PWM waveform through P_TMRx_OutputCtrl (x = 3, 4) register.

[6.] Enable period interrupt and start the counting operation with the bit TMR3ST or TMR4ST is set in P_TMR_Start register.

Figure 5-59 Example programming flowchart of PWM operation

5.11.2.14. Timer Output Enable Register

This register enables/disables the PWM outputs of the specified MCP3 and/or MCP4 timer module. The PWM output will be high-impedance if disabled. Note that this register only takes effect when TIO3A to TIO3F or TIO4A to TIO4F are set to be output pins in special function mode.

- **P_TMR_Output (0x7406): Timer Output Enable Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved		TMR4FOE	TMR4EOE	TMR4DOE	TMR4COE	TMR4BOE	TMR4AOE

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved		TMR3FOE	TMR3EOE	TMR3DOE	TMR3COE	TMR3BOE	TMR3AOE

B15-B14	Reserved			
B13	TMR4FOE	Timer 4 IOF Output enable (TIO4F)	0: Disable	1: Enable
B12	TMR4EOE	Timer 4 IOE Output enable (TIO4E)	0: Disable	1: Enable
B11	TMR4DOE	Timer 4 IOD Output enable (TIO4D)	0: Disable	1: Enable
B10	TMR4COE	Timer 4 IOC Output enable (TIO4C)	0: Disable	1: Enable
B9	TMR4BOE	Timer 4 IOB Output enable (TIO4B)	0: Disable	1: Enable
B8	TMR4AOE	Timer 4 IOA Output enable (TIO4A)	0: Disable	1: Enable
B7-B6	Reserved			
B5	TMR3FOE	Timer 3 IOF Output enable (TIO3F)	0: Disable	1: Enable
B4	TMR3EOE	Timer 3 IOE Output enable (TIO3E)	0: Disable	1: Enable

B3	TMR3DOE	Timer 3 IOD Output enable (TIO3D)	0: Disable	1: Enable
B2	TMR3COE	Timer 3 IOC Output enable (TIO3C)	0: Disable	1: Enable
B1	TMR3BOE	Timer 3 IOB Output enable (TIO3B)	0: Disable	1: Enable
B0	TMR3AOE	Timer 3 IOA Output enable (TIO3A)	0: Disable	1: Enable

5.11.2.15. Timer 3 and 4 Output Control Register

The configuration of MCP timer 3 and 4 output control registers is essential to the PWM waveform type used for motor drive applications. The DUTYMODE bit determines which registers used for PWM determines duty ratio. Generally speaking, when driving a BLDC motor with 120 degree PWM mode only P_TMRx_TGRA(x = 3, 4) is the need to setup the duty register. In other words, all of the three P_TMRx_TGRA/P_TMRx_TGRB/P_TMRx_TGRC (x = 3, 4) registers required for 180 degree PWM, including BLDC and ACI motor. The POLP bit determines the PWM active level for IGBT/MOSFET switching device. The UPWM, VPWM and WPWM can be forced H/L or active H/L waveform on specified pin. The bits of POLP, WPWM/VWPM/UPWM and WOC/VOC/UOC make different results in the PWM waveform generation.

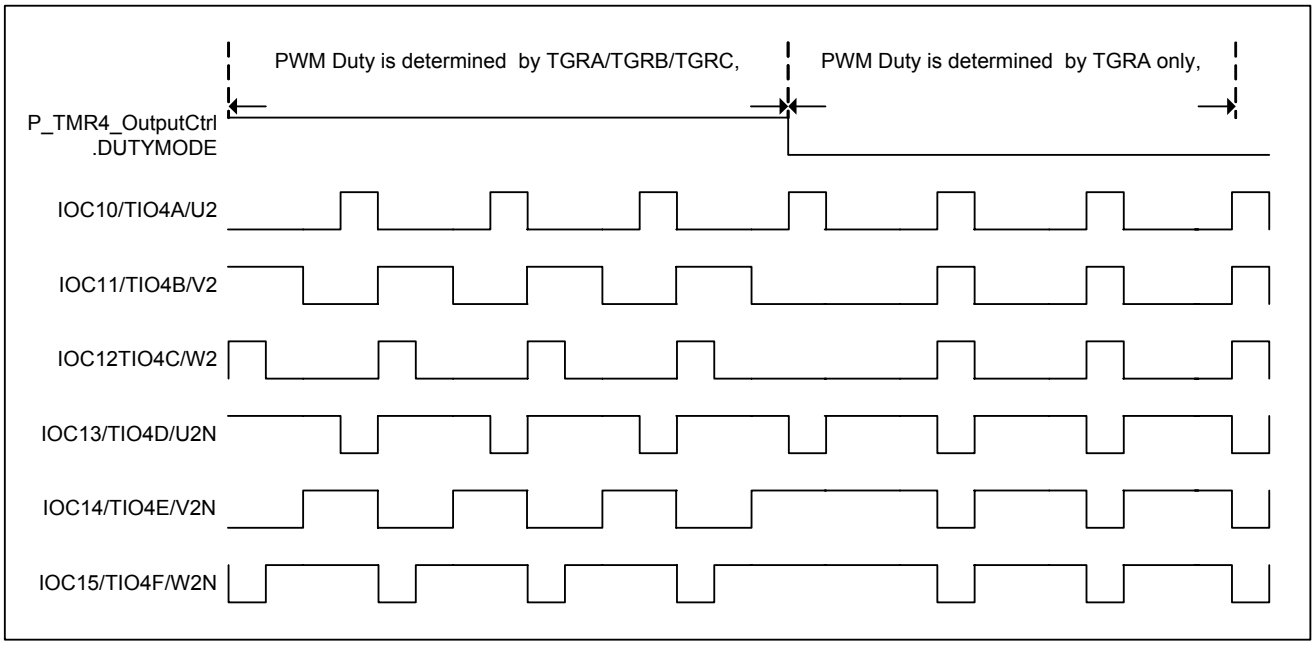


Figure 5-60 PWM output timing with different duty mode selection

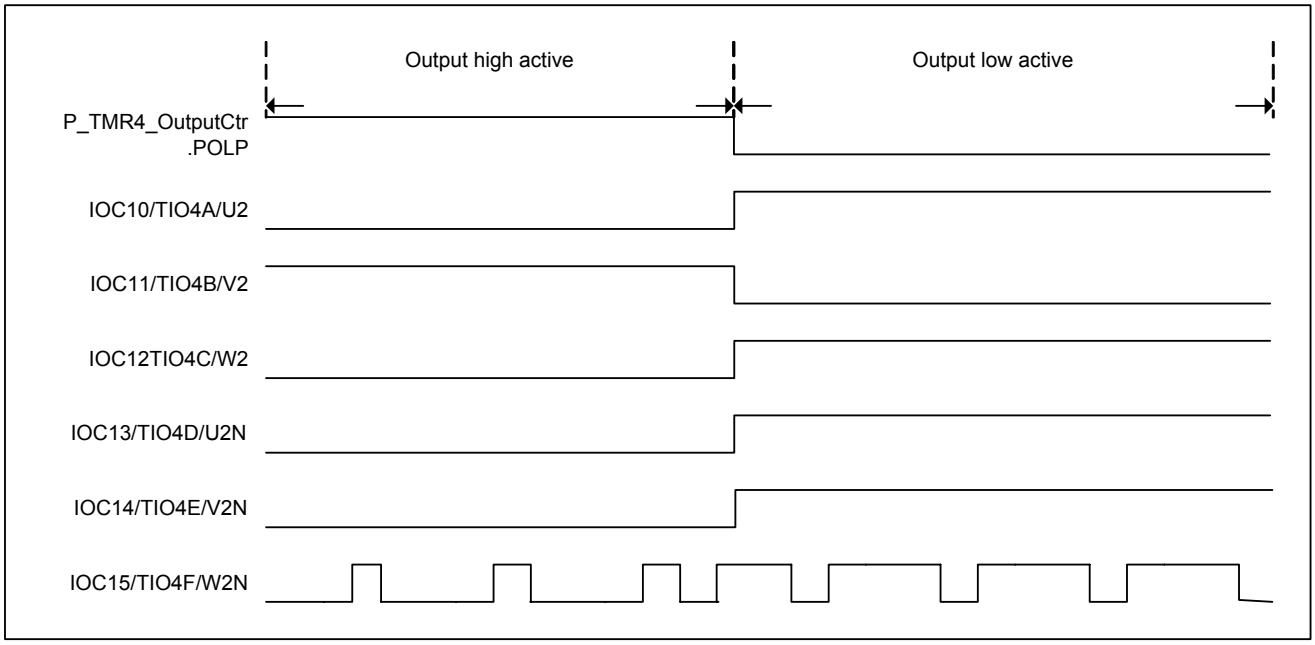


Figure 5-61 Output polarity timing

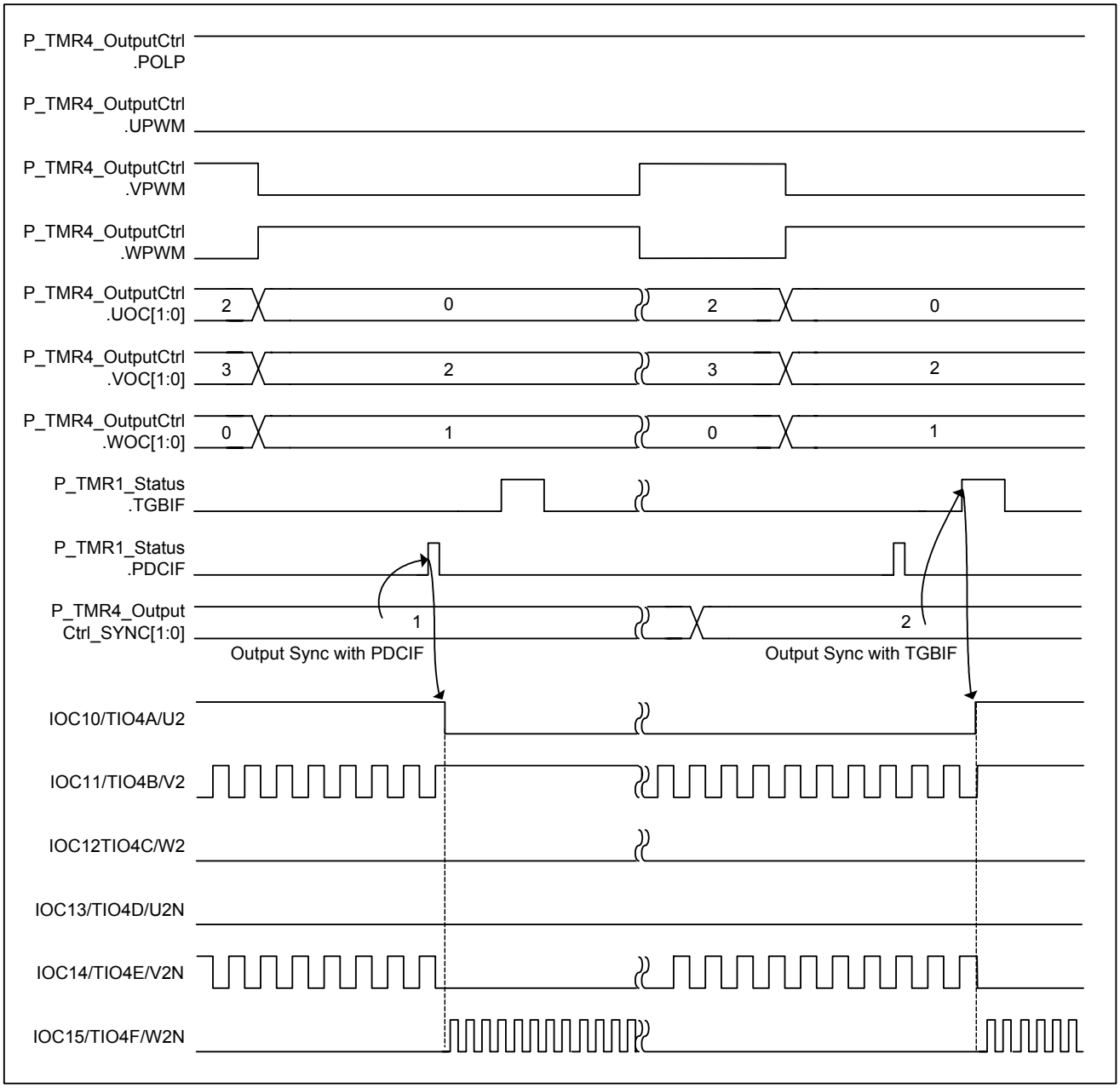


Figure 5-62 PWM Sync mode

- **P_TMR3_OutputCtrl (0x7407): Timer 3 Output Control Register**
- **P_TMR4_OutputCtrl (0x7408): Timer 4 Output Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	RW	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
DUTYMODE	POLP	Reserved			WPWM	VPWM	UPWM

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SYNC		WOC		VOC		UOC	

B15	DUTYMODE	Duty mode select	0: U phase in common (same as TGRA register)	1: Three phases independent
B14	POLP	Phase polarity select	0: Active low	1: Active high
B13-B11	Reserved			
B10	WPWM	W phase PWM output select	0: H/L level output	1: PWM waveform output
B9	VPWM	V phase PWM output select	0: H/L level output	1: PWM waveform output
B8	UPWM	U phase PWM output select	0: H/L level output	1: PWM waveform output
B7-B6	SYNC	UVW phases output synchronization source select	00: No sync	01: Synchronized to P_POSx_DectData (x = 0, 1) register change
			10: Synchronized to TGRB register compare match of PDCx (x = 0, 1)	11: Synchronized to TGRC register compare match of PDCx (x = 0, 1)

B5-B4 WOC — W phase output control

POLP=1 (Active high)				
WOC[1:0]	WPWM = 1 (PWM output)		WPWM = 0 (H/L output)	
	W phase	WN phase	W phase	WUN phase
00	CPWM	PWM	L	L
01	L	PWM	L	H
10	PWM	L	H	L
11	PWM	CPWM	H	H
POLP=0 (Active Low)				
00	PWM	CPWM	H	H
01	H	CPWM	H	L
10	CPWM	H	L	H
11	CPWM	PWM	L	L

B3-B2 VOC — V phase output control

POLP=1 (Active high)				
VOC[1:0]	VPWM = 1 (PWM output)		VPWM = 0 (H/L output)	
	V phase	VN phase	V phase	VN phase
00	CPWM	PWM	L	L
01	L	PWM	L	H
10	PWM	L	H	L
11	PWM	CPWM	H	H
POLP=0 (Active Low)				
00	PWM	CPWM	H	H
01	H	CPWM	H	L
10	CPWM	H	L	H
11	CPWM	PWM	L	L

B1-B0 UOC — U phase output control

POLP=1 (Active high)				
UOC[1:0]	UPWM = 1 (PWM output)		UPWM = 0 (H/L output)	
	U phase	UN phase	U phase	UN phase
00	CPWM	PWM	L	L
01	L	PWM	L	H
10	PWM	L	H	L
11	PWM	CPWM	H	H
POLP=0 (Active Low)				
00	PWM	CPWM	H	H
01	H	CPWM	H	L
10	CPWM	H	L	H
11	CPWM	PWM	L	L

5.11.2.16. Timer 3 and 4 Dead Time and Control Register

In complementary PWM mode, each pairs of the complement PWM channel can be used to drive the high side and low side transistors. The PWM signal of each pairs should be totally logic opposite in non-deal case, but actually condition is not. To prevent the active time of PWM signal between low side and high side PWM are overlapping, the dead time unit must be used in complementary PWM mode.

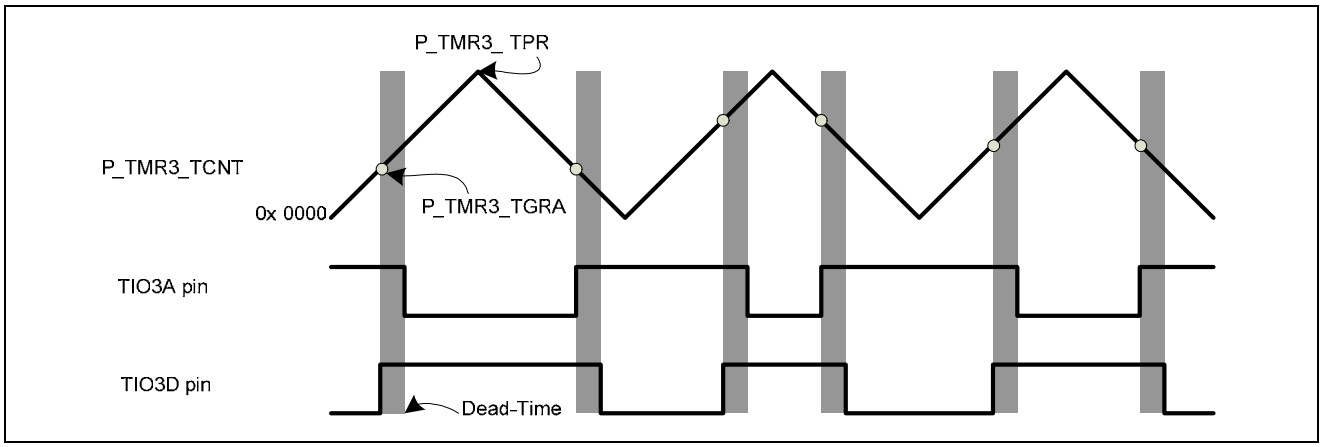


Figure 5-64

Figure 5-63 shows the center-aligned complementary PWM with dead time inserted of timer 3.

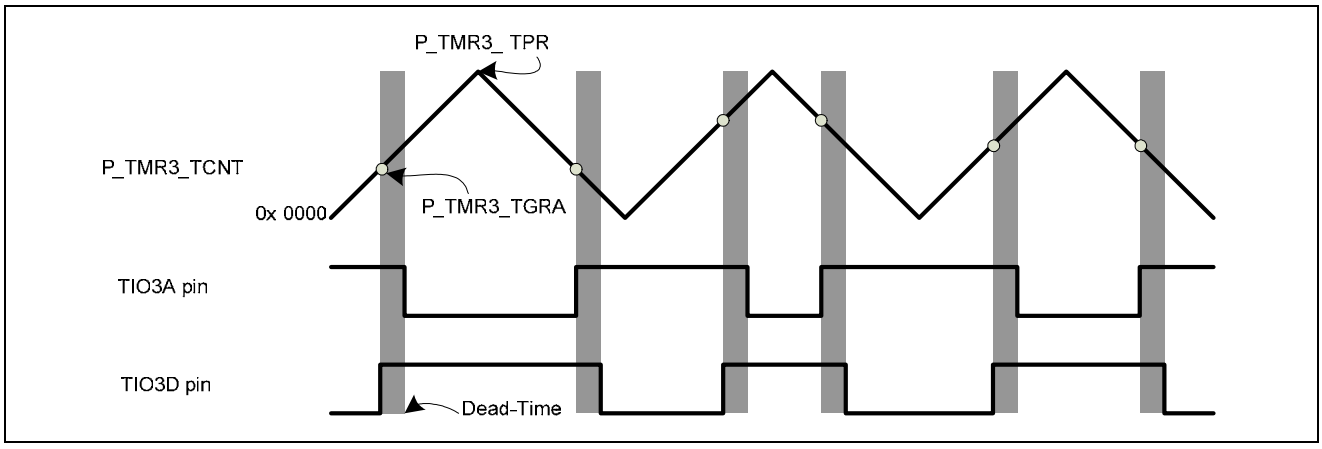


Figure 5-64 Active-low PWM mode of dead-time generation

There are two dead-time timer control registers in the SPMC75F2413A : P_TMR3_DeadTime and P_TMR4_DeadTime, for MCP channel 3 and channel 4. The dead-time timer only works when programmed in complementary PWM mode. The dead-time timer unit will delay the active edge for positive or lower phase output and affected by the setting of POLP bit in the P_TMRx_OutputCtrl (x = 3, 4) register. Three phase dead time feature could be independent enable or disable and the dead time interval is determined through DTP bits at FCK/4 clock source.

- **P_TMR3_DeadTime (0x7460): Timer 3 Dead Time and Control Register**
- **P_TMR4_DeadTime (0x7461): Timer 4 Dead Time and Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R/W	RW	R/W	R	R	R	R
0	0	0	0	0	0	0	0
Reserved	DTWE	DTVE	DTUE	Reserved			

B7	B6	B5	B4	B3	B2	B1	B0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved	DTP						

B15	Reserved			
B14	DTWE	Dead-time timer enable for W phases	0: Disable	1: Enable
B13	DTVE	Dead-time timer enable for V phases	0: Disable	1: Enable
B12	DTUE	Dead-time timer enable for U phases	0: Disable	1: Enable
B11-B7	Reserved			
B6-B0	DTP	Dead-time timer period	These bits select the dead-time period. Dead time can be set from 0 to 127 FCK/4 clocks	

5.11.2.17. Timer Fault Input Control Register

The fault protection input can be used to establish a high-impedance state for protection by applying an active low state on FTINT1-2 pins summarized in Table 5-19. Also, an interrupt will be generated simultaneously. The PWM outputs will remain in high-impedance state until released. Additionally, the output compare mode can be activated to compare the complementary PWM output pairs such as U1 and U1N, etc., conducting at the same time.

Also note that the OCLS bit in P_Faultx_Ctrl (x = 1, 2) register determines the PWM output compare polarity level; developer must properly select the PWM protection polarity to ensure the safety of the driver circuits of target system. User should aware that the fault input protection only works with complementary PWM mode.

Clearing OSF and FTPINIF, releasing fault protection state (PWM high-impedance state) can only be made by a power-on reset or software release procedures. External reset pin reset will not release this fault protection state!

Table 5-19 Fault input and PWM output pins combinations

Pin Name	**Pin State**	**Description**
FTIN1	Input	Input request to set U1, V1, W1, U1N, V1N, W1N output high-impedance
FTIN2	Input	Input request to set U2, V2, W2, U2N, V2N, W2N output high-impedance
PWM Output Pairs Combination	**Pin State at fault**	**Description**
U1, U1N	Input Floating	All PWM output pins of MCP3 will be set to high-impedance state if these two pins output low/high level, which is determined by P_Fault1_Ctrl.OCLS, simultaneously for more than one clock cycle
V1, V1N	Input Floating	
W1, W1N	Input Floating	
U2, U2N	Input Floating	All PWM output pins of MCP4 will be set to high-impedance state if these two pins output low/high level, which is determined by P_Fault2_Ctrl.OCLS, simultaneously for more than one cycle
V2, V2N	Input Floating	
W2, W2N	Input Floating	

The PWM output will be halted (set to high-impedance state) under following circumstances.

- ❑ FTIN1-2 pin input low-level state. The valid FTINT input can be set for holding low for FCK/4 x (1~15).
- ❑ The complementary PWM output can be set to high-impedance state if upper and lower phase simultaneously output active-level for more than 1 system clock cycle.
- ❑ PLL or oscillator stopped
- ❑ Fast Interrupt Request (FIQ) will be generated.

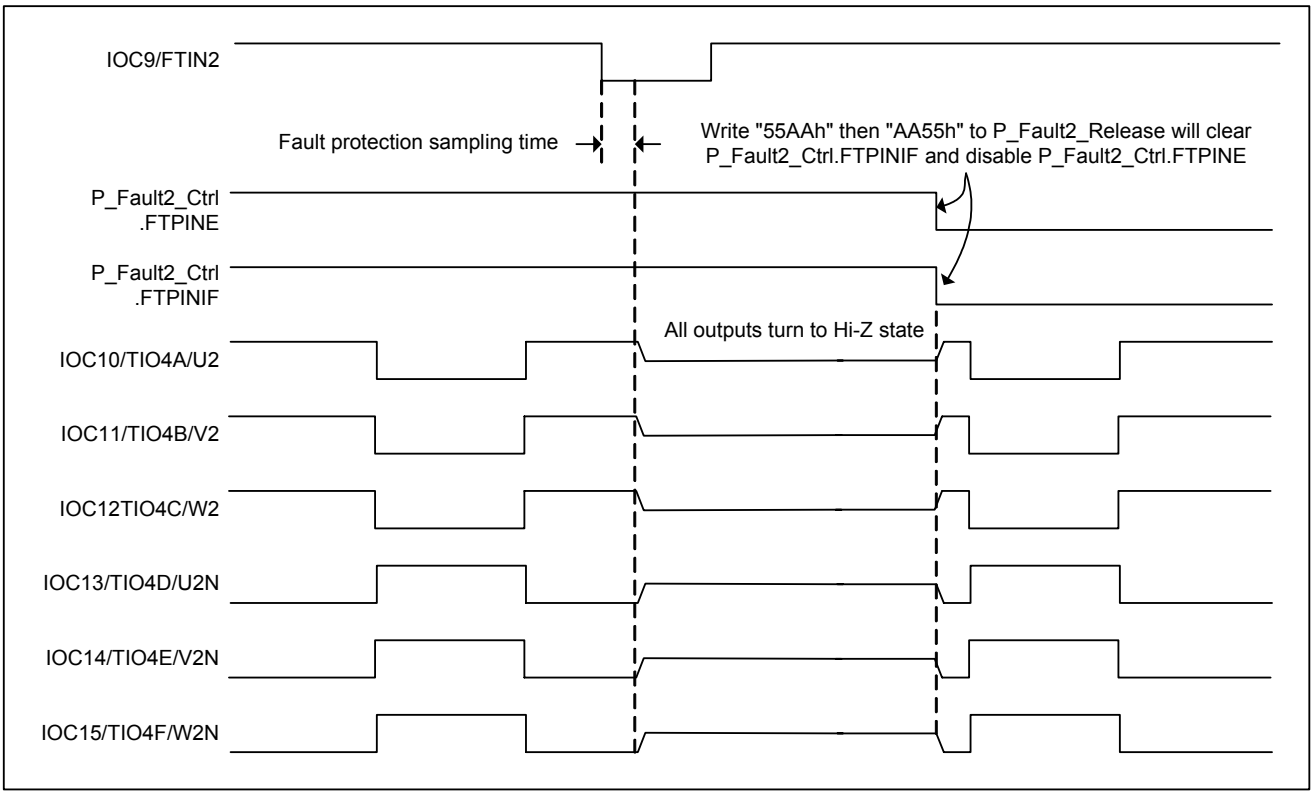


Figure 5-65 Fault error timing

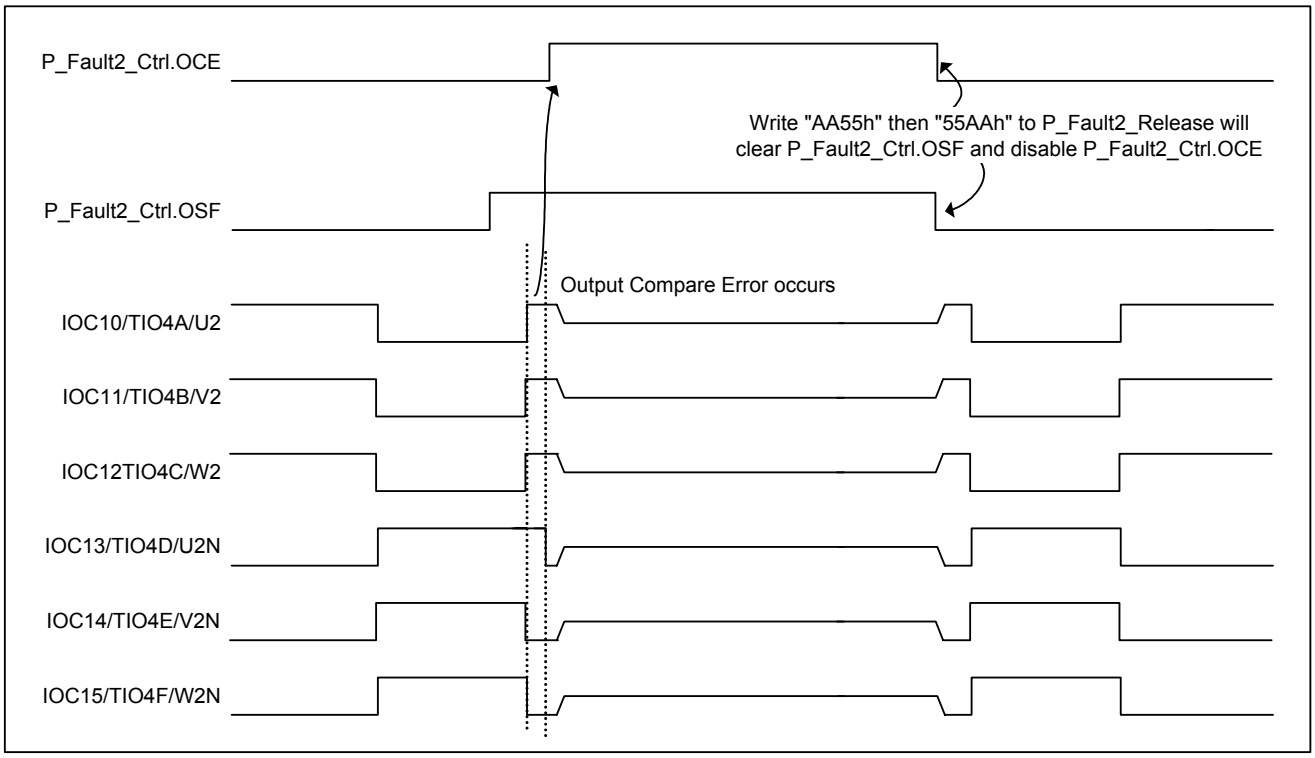


Figure 5-66 Output compare error

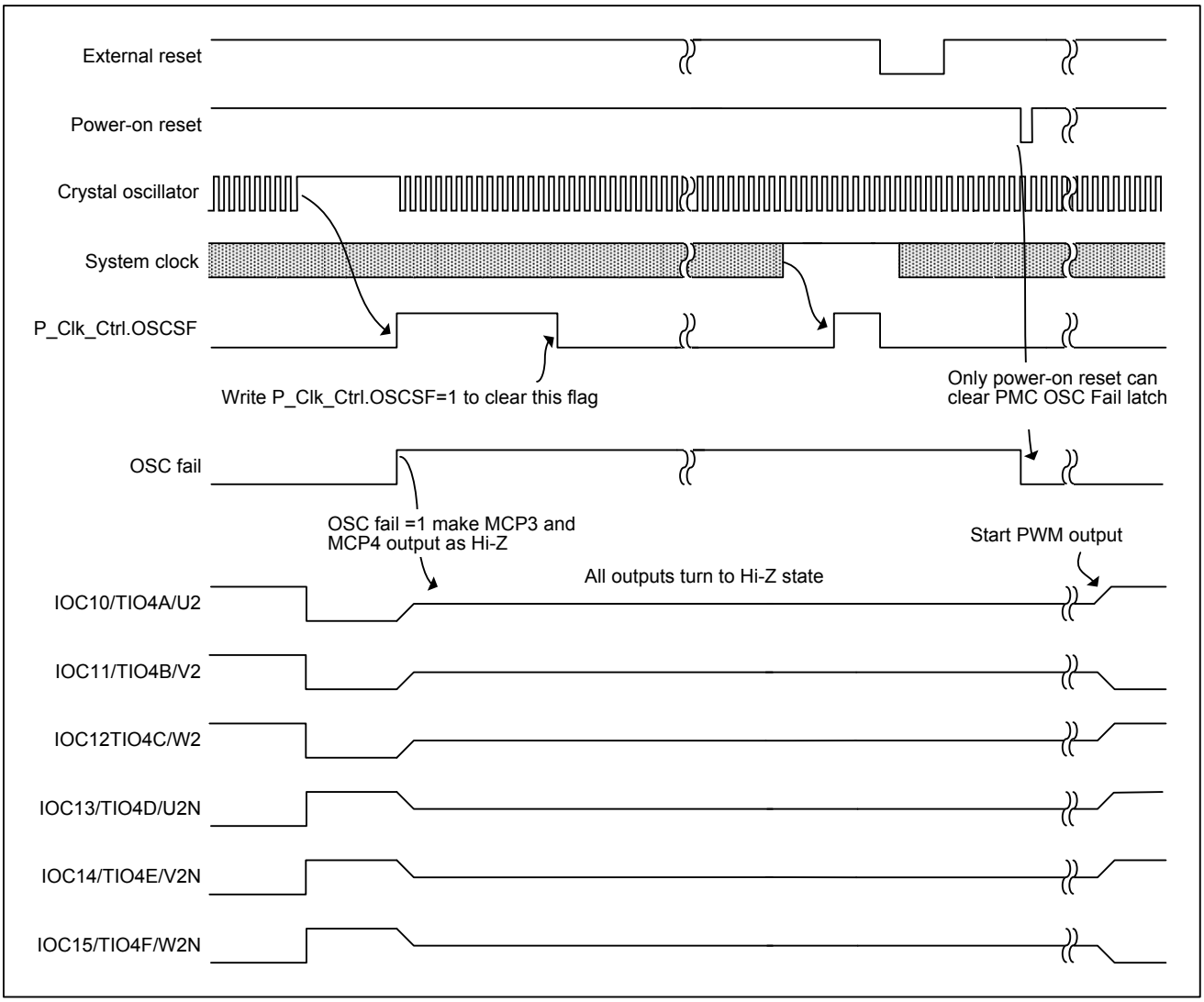


Figure 5-67 Oscillator stopped timing

- **P_Fault1_Ctrl (0x7466): Fault input 1 Control and Status Register**
- **P_Fault2_Ctrl (0x7467): Fault input 2 Control and Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	RW	R/W	R/W	R	R	R	R
0	0	0	0	0	0	0	0
OCE	OCIE	OCLS	OSF	Reserved			

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
FTPINE	FTPINIE	FTPINIF	Reserved	FTCNT			

B15	OCE	Output compare enable	0: Disable	1: Enable
B14	OCIE	Output compare interrupt enable	0: Disable	1: Enable
B13	OCLS	Output compare polarity level select	0: Compare low-level	1: Compare high-level
B12	OSF†	Output short flag	Software needs to set the OCE bit to '1' again to active the output short protection function after this flag is cleared.	
B11-B8	Reserved			

B7	FTPINE	Fault input pin 1/2 enable	0: Disable	1: Enable
B6	FTPINIE	Fault input 1/2 interrupt enable	0: Disable	1: Enable
B5	FTPINIF‡	Fault input 1/2 status flag	0: Not occurred	1: Occurred
B4	Reserved			
B3-B0	FTCNT	Fault protection sampling time	FCK/4 * n, n = 1 to 15. User should note that setting the FTCNT value to 0 will always make the external fault input interrupt happen even the FTIN1/2 pin is at logic high state. If FTPINIE bit is set, FTPINIF will not be able to be cleared and the interrupt routine executed recursively due to incorrect FTCNT setting. This will cause the system unpredictable.	

※: write '1' to clear this flag

† : write "0xAA55" then "0x55AA" to P_Faultx_Release (x = 1, 2) will clear this flag and also disable output compare.

‡ : write "0x55AA" then "0xAA55" to P_Faultx_Release (x = 1, 2) will clear this flag and also disable fault input pin.

5.11.2.18. Timer Fault Release Register

To release the PWM output high-impedance state caused by fault input, first check the asserted fault pin input flag FTPINIF in P_Faultx_Ctrl (x = 1, 2) register, then write "0x55AA" and "0xAA55" sequentially to its corresponding fault release P_Faultx_Release (x = 1, 2) register.

To release the PWM output high-impedance state from PWM output short-circuit logic detection presents inside the chip, first check output short flag OSF in P_Faultx_Ctrl (x = 1, 2) register, then write "0xAA55" and "0x55AA" sequentially to its corresponding fault release P_Faultx_Release (x = 1, 2) register.

To release the PWM high-impedance state caused because oscillator fail, first clear oscillator fail flag OSCSF in P_Clk_Ctrl register, then write "0x5555" and "0xAAAA" sequentially to its corresponding fault release P_Faultx_Release (x = 1, 2) register.

- **P_Fault1_Release(0x746A): Fault 1 Flag Release Register**
- **P_Fault2_Release(0x746B): Fault 2 Flag Release Register**

B15	B14	B13	B12	B11	B10	B9	B8
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
FTRR							

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
FTRR							

B15-B0	FTRR	**FTRR**: Fault release control words

5.11.2.19. Timer Overload Protection Control and Status Register

The SPMC75F2413A devices contain an overload protection circuit. The circuit starts operating when the overload protection input (OL) is pulled low. The overload protection input is sampled by clock FCK/4. Sampling number can be set from 0 to 15 times. There are three methods to deactivate overload protection: deactivate by a timer, deactivate by PWM synchronous, or deactivate manually. These methods can be used when the overload protection input has been released back to high.

The output disabled phases during overload protection are to disable no phases, all phases, PWM phases, or all upper/all lower phases. When to disable all upper or all lower phases is selected (P_OLx_Ctrl.OLMD = 3, x = 1, 2), motor drive PWM output is determined by their turn-on status immediately before being disabled. When two or more upper phases are active, all upper phases are turned on and all lower phases are turned off; when two or more lower phases are active, all upper phases are turned off and all lower phases are turned on. Table 5-20 and Table

5-21 show the overload function behavior depending on POLP bit in P_TMRx_OutputCtrl (x = 3, 4) register and OLMD bit when such condition happened. To disable a phase means to put the phase in inactive level.

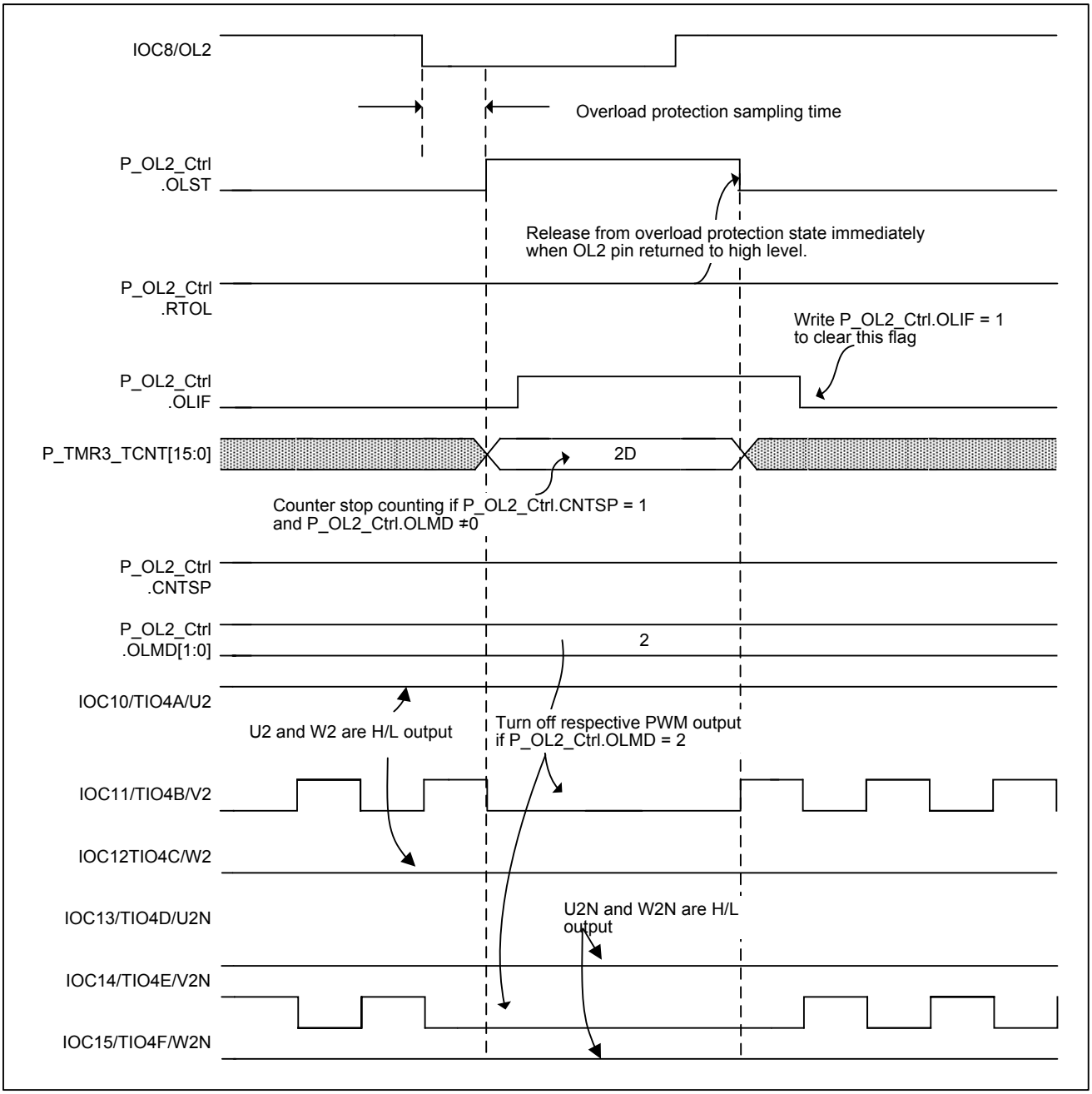


Figure 5-68 Stop PWM output only when overload occurs

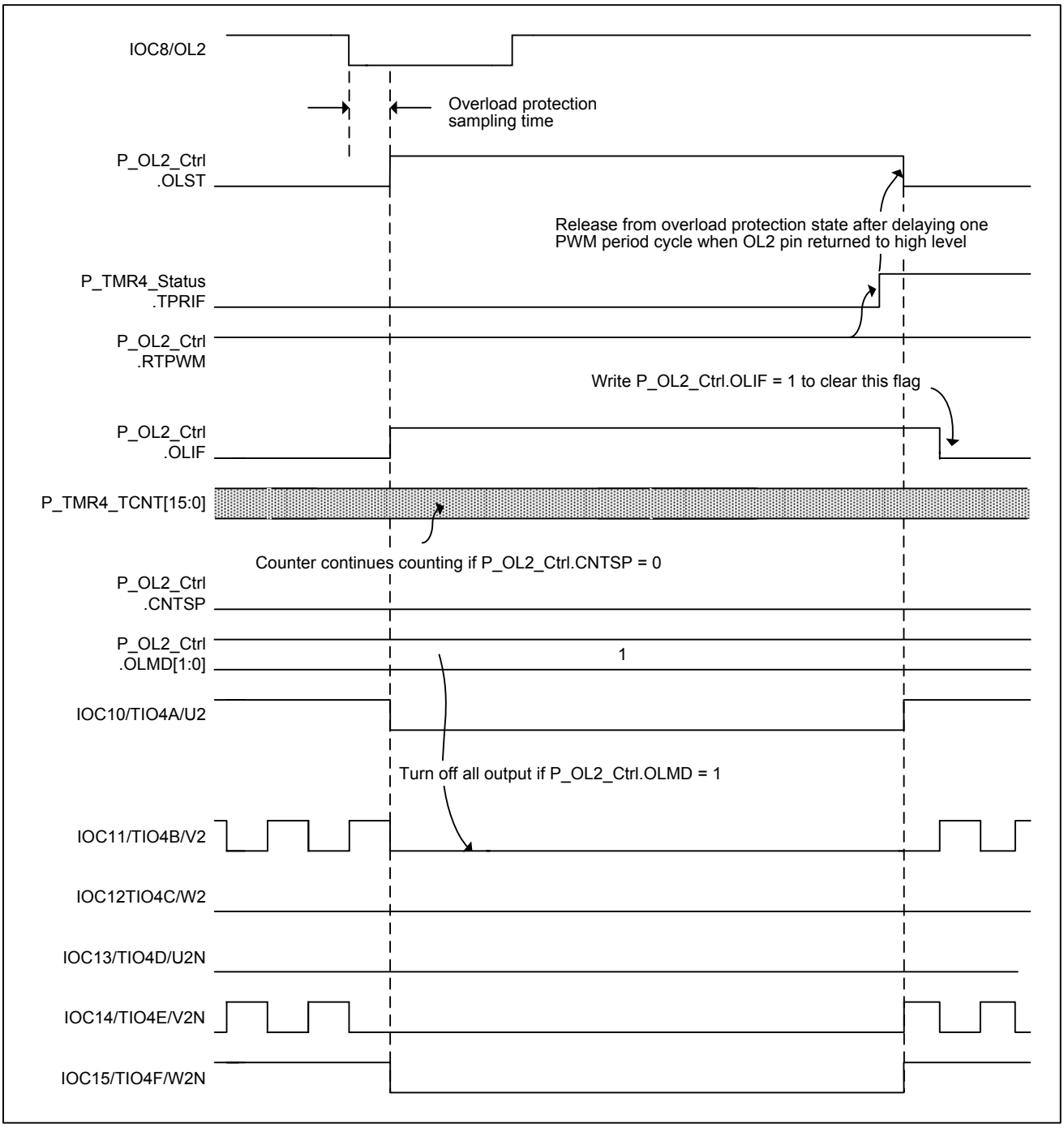


Figure 5-69 Stop all output when overload occurs

Table 5-20 Overload protection interrupt when POLP = 1

POLP = 1 OLMD		TIOxA ~ TIOxF Phase Output State (x = 3, 4)	Overload Protection Interrupt Capability
0	0	No phases disabled	No
0	1	All phases disabled	Yes
1	0	PWM/CPWM phases disabled. (Refer to P_TMRx_OutputCtrl)	Yes
1	1	(1) Any upper two phases are detected as high level, and then disable all lower phases.	Issue overload protection interrupt when any upper two phases or lower two phases are detected as high level,

POLP = 1 OLMD		TIOxA ~ TIOxF Phase Output State (x = 3, 4)	Overload Protection Interrupt Capability
		(2) Any lower two phases are detected as high level, and then disable all upper phases. If either condition (1) or (2) is not satisfied, no phases are disabled.	otherwise no interrupt is issued.

Table 5-21 Overload protection interrupt when POLP = 0

POLP = 1 OLMD		TIOxA ~ TIOxF Phase Output State (x = 3, 4)	Overload Protection Interrupt Capability
0	0	No phases disabled	No
0	1	All phases disabled	Yes
1	0	PWM/CPWM phases disabled. (Refer to P_TMRx_OutputCtrl)	Yes
1	1	(1) Any upper two phases are detected as low level, and then disable all lower phases. (2) Any lower two phases are detected as low level, and then disable all upper phases. If either condition (1) or (2) is not satisfied, no phases are disabled.	Issue overload protection interrupt when Any upper two phase are detected as low level, otherwise no interrupt is issued.

- **P_OL1_Ctrl(0x7468): Overload Input 1 Control and Status Register**
- **P_OL2_Ctrl(0x7469): Overload input 2 Control and Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	RW	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
OLEN	CNTSP	OLMD		OLST	RTTMB	RTPWM	RTOL

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
OLIE	OLIF	Reserved		OLCNT			

B15	OLEN	Overload protection enable	0: Disable	1: Enable
B14	CNTSP	Stop PWM counter (P_TMR3_TCNT/P_TMR4_TCNT) during overload protection occurring	0: Do not stop	1: Stop the counter
B13-B12	OLMD	Output disabled phases during overload protection occurring	00: No phases disabled	01: All phases disabled, i.e. on turn-off state
			10: PWM phases disabled	11: All upper or all lower phases are disabled depending on the active phases
B11	OLST	Overload protection status	0: No operation	1: Under protection
B10	RTTMB	Release from TGRB selection	0: keep overload protection	1: Release from overload protection after P_TMRx_TGRB (x = 0, 1) register compare match occurred when OLx (x = 1, 2) pin returned to high level.

B9	RTPWM	Release from PWM selection	0: keep overload protection	1: Release from overload protection state after delaying one PWM period cycle when OLx (x = 1, 2) pin returned to high level.
B8	RTOL	Release from OL pin selection	0: keep overload protection	1: Release from overload protection state immediately when OLx (x = 1, 2) pin returned to high level.
B7	OLIE	Overload interrupt enable bit	0: Disable	1: Enable
B6	OLIF※	Overload interrupt flag	0: Not occurred	1: Has occurred
B5-B4	Reserved			
B3-B0	OLCNT	Overload protection sampling time.	FCK/4 * n, n = 1 to 15. User should note that setting the OLCNT value to 0 will always make the external fault input interrupt happen even the OL1/2 pin is at logic high state. If OLIE bit is set, OLIF will not be able to be cleared and the interrupt routine executed recursively due to incorrect OLCNT setting. This will cause the system unpredictable.	

※: write '1' to clear this flag

5.12. Compare Match Timer

The device has a compare match timer (CMT) comprising two 16-bit timer channels. Each channel has a 16-bit up-count counter and can generate interrupt at set intervals. The clock input source can be selected from $F_{CK}/1$, $F_{CK}/2$, $F_{CK}/4$, $F_{CK}/8$, $F_{CK}/16$, $F_{CK}/64$, $F_{CK}/256$, or $F_{CK}/1024$. The compare match interrupt will be set if the register value of P_CMTx_TCONT (x=0, 1) matches that of P_CMTx_TPR (x=0, 1), respectively. The counters will start counting when STx (x=0, 1) in P_CMT_Start is set, independently.

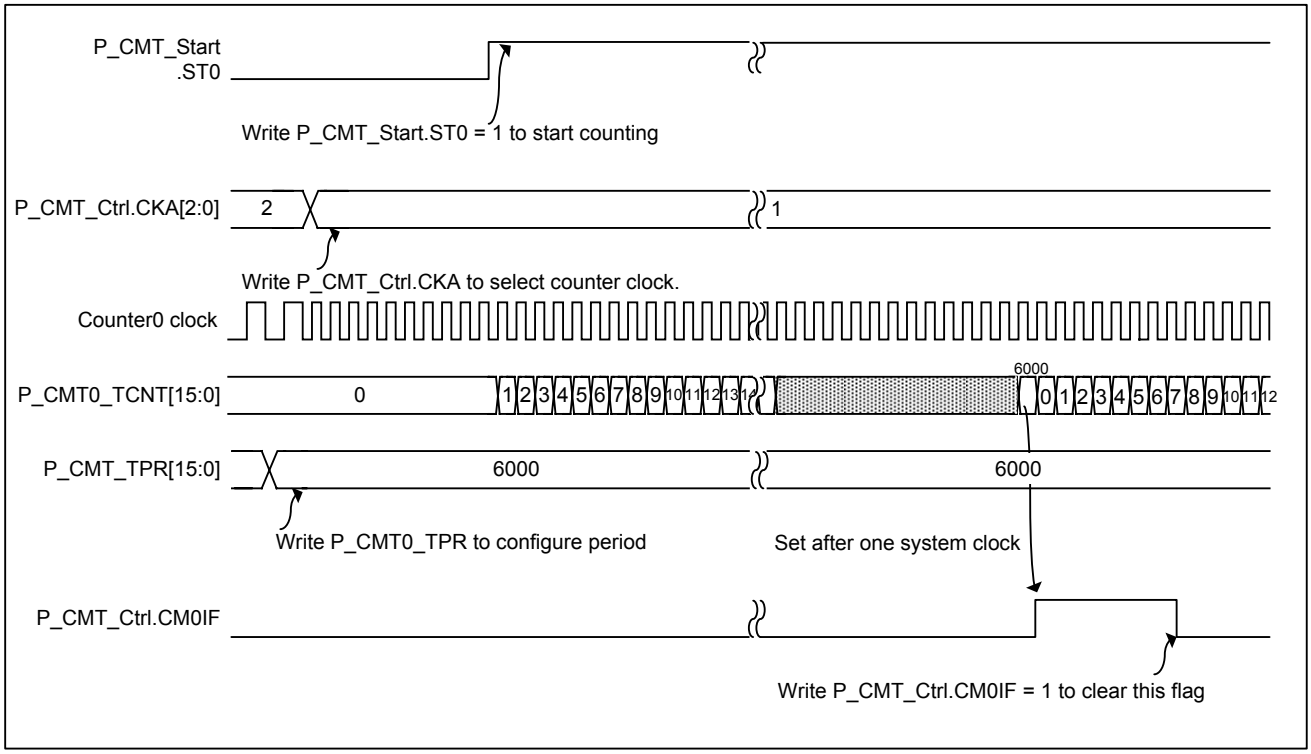


Figure 5-70 CMT timing

- **P_CMT_Start (0x7500)：Compare Match Timer Start Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0
Reserved						ST1	ST0

B15-B2	Reserved			
B1	ST1	Compare match timer 1 counter start	0: P_CMT1_TCNT counter operation stopped, and cleared to 0x0000	1: P_CMT1_TCNT counter operation enabled
B0	ST0	Compare match timer 0 counter start	0: P_CMT0_TCNT counter operation stopped, and cleared to 0x0000	1: P_CMT0_TCNT counter operation enabled

- **P_CMT_Ctrl (0x7501)：Compare Match Timer Control and Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CM1IF	CM1IE	Reserved			CKB		

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CM0IF	CM0IE	Reserved			CKA		

B15	CM1IF※	CMT1 compare match interrupt flag	0: Not matched	1: Matched
B14	CM1IE	CMT1 compare match interrupt enable	0: CMT1 compare match interrupt disable	1: CMT1 compare match interrupt enable
B13-B11	Reserved			
B10-B8	CKB	CMT1 clock select bits	000: FCK / 1	001: FCK / 2
			010: FCK / 4	011: FCK / 8
			100: FCK / 16	101: FCK / 64
			110: FCK / 256	111: FCK / 1024
B7	CM0IF※	CMT0 compare match interrupt flag	0: Not matched	1: Matched
B6	CM0IE	CMT0 compare match interrupt enable	0: CMT0 compare match interrupt disable	1: CMT0 compare match interrupt enable
B5-B3	Reserved			
B10-B8	CKA	CMT0 clock select bits	000: FCK / 1	001: FCK / 2
			010: FCK / 4	011: FCK / 8
			100: FCK / 16	101: FCK / 64
			110: FCK / 256	111: FCK / 1024

※: write '1' to clear this flag

- **P_CMT0_TCNT (0x7508)：Compare Match Timer 0 Counter Register**
- **P_CMT1_TCNT (0x7509)：Compare Match Timer 1 Counter Register**

Compare match timer counter is a 16-bit register used as an up-counter. The initial value is 0x0000.

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
CMTCNT							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
CMTCNT							

- **P_CMT0_TPR (0x7510)：Compare Match Timer 0 Period Register**
- **P_CMT1_TPR (0x7511)：Compare Match Timer 1 Period Register**

The compare match timer period register is a 16-bit register used to set the period for compare match function. The initial value is 0x0000. The P_CMTx_TCNT (x = 0, 1) will be cleared to 0x0000 when a new value has been written to P_CMTx_TPR (x = 0, 1).

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CMTPR							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CMTPR							

5.13. Time Base Module

The Time Base Module is used to produce the reference clock needed by other modules on the chip. It comprises a 16-bit ripple counter, can generate reference clocks from $F_{CK}/2$, $F_{CK}/4$ ~ $F_{CK}/1024$ ~ $F_{CK}/65536$. Only the clocks of $F_{CK}/2$, $F_{CK}/4$ ~ $F_{CK}/1024$ supply the peripherals of SPMC75F2413A chip. Time base counter can be cleared by writing 0x5555 to Time Base Reset Register (P_TMB_Reset). The peripherals using the clock source provided by the time base module will be a concern if user intends to clear time base.

By using the divider of the Time Base Module, a 50% duty cycle pulse can be produced to drive a buzzer device. The selected time base clock is sent to pin IOC4/BZO.

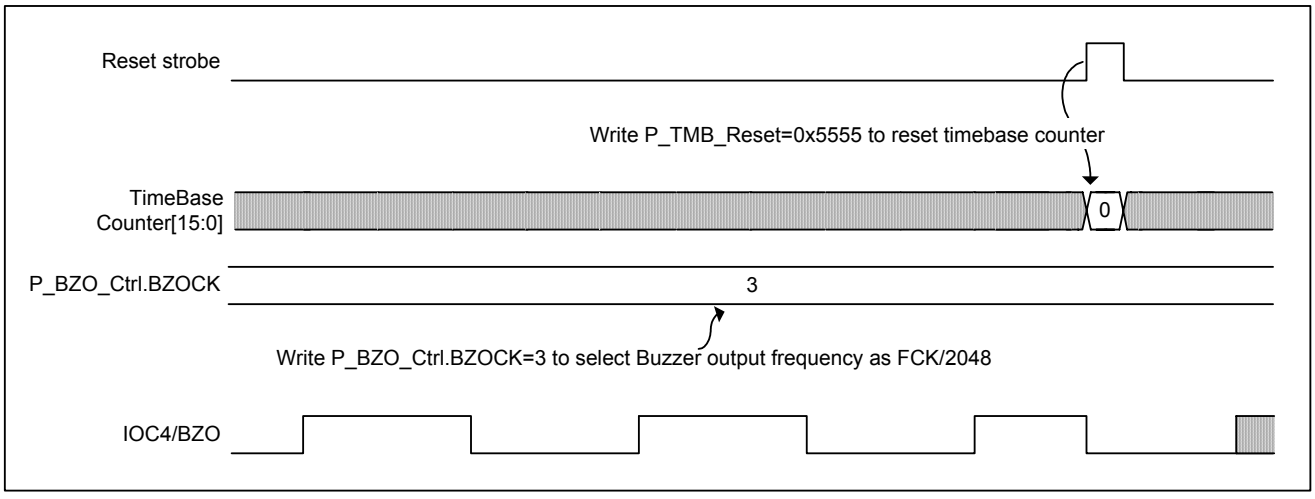


Figure 5-71 Timebase and buzzer output timing

- **P_TMB_Reset (0x70B8)：Time Base Reset Register**

Write 0x5555 to this register to reset the time base counter register to initial the clock sources of all peripherals on the chip.

B15	B14	B13	B12	B11	B10	B9	B8
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
TBRR							

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	W	W	W
0	0	0	0	0	0	0	0
TBRR							

- **P_BZO_Ctrl (0x70B9)： Buzzer Output Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CMTPR							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
CMTPR							

B15	BZOEN	Buzzer output enable select bit	0: Disable	1: Enable
B14-B2	Reserved			
B1-B0	BZOCK	Buzzer output frequency select bits	00: FCK / 16384	01: FCK / 8192
			10: FCK / 4096	11: FCK / 2048

5.14. Serial Communication Interface

The SPMC75F2413A supports two serial communication interfaces: SPI (Standard Peripheral Interface) and UART (Universal Asynchronous Receiver/Transceiver).

5.14.1. SPI (Standard Peripheral Interface)

The SPMC75F2413A devices include the three-pin SPI module. The SPI is a high-speed synchronous serial I/O that allows a serial of bit stream to be transmitted out or received into the device at a programmable transfer rate. The SPI supports full-duplex synchronous transfer between a master device and a slave device. The SPMC75F2413A supports both master and slave modes. The parameters such as operation mode, clock frequency, clock phase, and clock polarity are user programmable. The SPI module provides the following features:

- Three external pins:
  - SCK: clock input/output pin (shared with IOB11)
  - SDO: data output pin (shared with IOB13)
  - SDI: data input pin (shared with IOB12)
- Supports full-duplex synchronous transfer
- Two operation modes: master and slave
- Baud rate: 6 programmable transfer rate / Max. 6Mbps at 24MHz CPU clock
- Data word length: 8-bit
- Programmable clock phase and clock polarity settings
- Selectable data strobe time: input data bit sampled at the middle/end of data output time
- Three selectable sampling clock sources for noise immunity

The function diagram of SPI module is as follows.

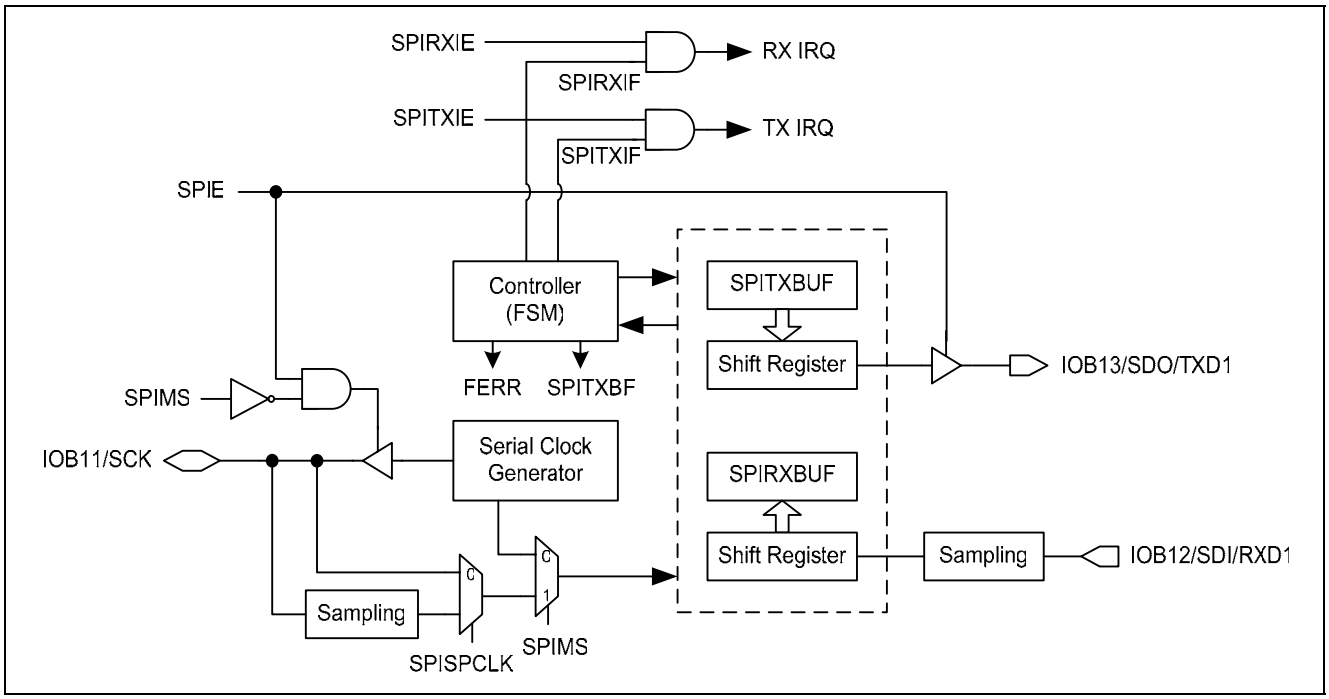


Figure 5-72 Function block diagram of SPI interface

5.14.2. SPI Operation

5.14.2.1. SPI Master Mode

As in master mode, the shifting clock (SPICLK) is generated by SPI module. There are two control bits to control the clock phase (SPIPHA) and polarity (SPIPOL) in the P_SPI_Ctrl register. The transmission starts immediately from data is written to the P_SPI_TxBuf register.

After software writes one byte through P_SPI_TxBuf register, the data is latched into its internal transmission buffer. If the shift register is not shifting data, the data will be loaded to the shift register and start transmitting at the next SCLK phase. On the other hand, if the shift register is busy in shifting data (SPITXBF flag is set in P_SPI_TxStatus register), the new data will not be shifted out until the present byte has been shifted out.

The SPI shifts the data from MSB to LSB through the SPIDO pin. The 8-bit data is shifted out after eight SCLK cycles. At the same time, the data is also shifted in through SDI pin. When each 8-bit transfer is completed, the SPITXIF bit in P_SPI_TxStatus register will be set; besides, a SPI interrupt will be generated if the SPITXIE bit is set to '1' in P_SPI_TxStatus register.

In contrast, while SPI interface is received one byte successfully, the received data will be latched into reception buffer. At that time, SPIRXIF bit in P_SPI_RxStatus register will be set and a SPI interrupt will be issued to CPU if the SPIRXIE bit in the P_SPI_RxStatus register is set.

The following diagram depicts the timing scheme on SPI master mode for different operation types (polarity control bit equals "1" or "0", phase control bit equals "1" or "0", and sample strobe control bit equals "1" or "0").

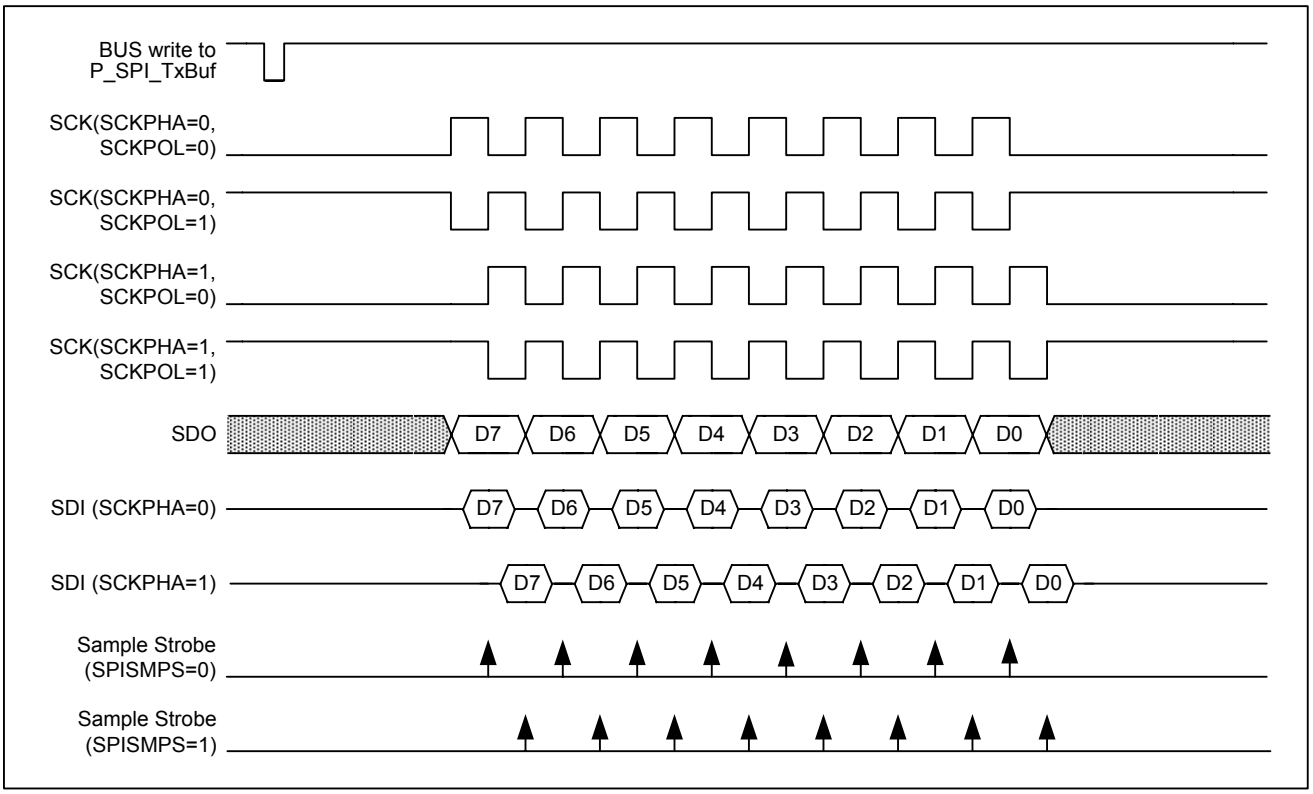


Figure 5-73 SPI mode timing, Master Mode

5.14.2.2. SPI Slave Mode

In slave mode, the shifting clock SCLK comes from external SPI master, so the transmission starts from the first external SCLK event. To transmit, the firmware should write the data to its transmitting buffer before the first SCK comes from the master. Both master and slave devices must be programmed with the same SCLK phase and polarity for transmitting and receiving data.

If the clock phase bit (SPIPHA) is “1”, the first data bit to be shifted out starts right after the command written to P_SPI_TxBUF register. If the clock phase bit (SPIPHA) is “0”, the first data bit to be shifted will start after first SCLK edge.

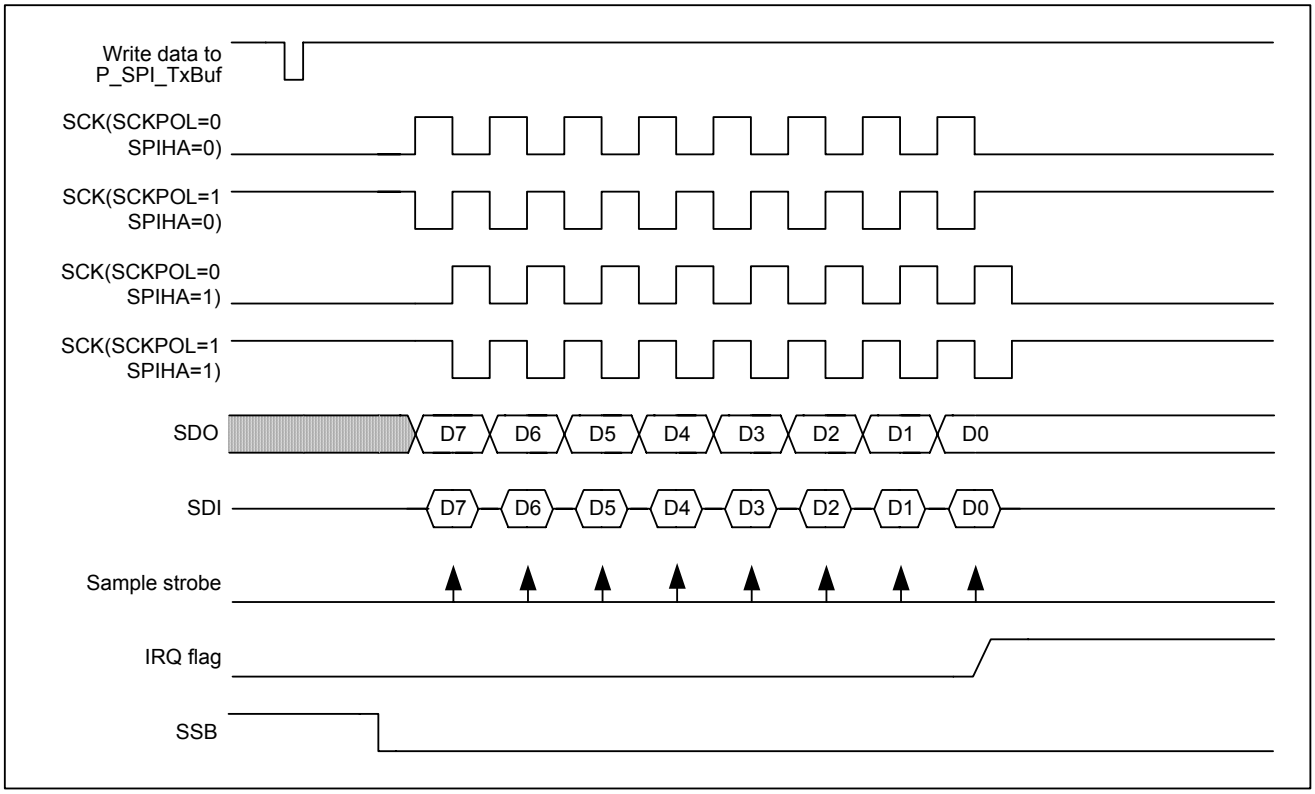


Figure 5-74 SPI mode timing, Slave Mode, SPIPHA = 0

- **P_SPI_Ctrl (0x7140): SPI Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R	R	R	W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SPIE	Reserved			SPIRST	SPISPCLK		SPIMS

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
Reserved		SPIPHA	SPIPOL	SPISMPS	SPIFS		

B15	SPIE	SPI enable	0: Disable	1: Enable
B14-B12	Reserved			
B11	SPIRST	Write 1 to reset. It only generate one pulse to reset the SPI module except for the register setting		
B10-B9	SPISPCLK	Sampling clock select bits	00: no sampling	01: FCK
			10: FCK/2	11: FCK/4
B8	SPIMS	SPI mode selection	0: Master mode	1: Slave mode
B7-B6	Reserved			
B5	SPIPHA	SPI clock phase. SPI clock phase select, see SPI Master Mode Timing		
B4	SPIPOL	SPI clock polarity. SPI clock polarity select, see SPI Master Mode Timing		
B3	SPISMPS	SPI sample mode selection for master mode	0: input data bit sampled at the middle of data output time	1: input data bit sampled at the end of data output time
B2-B0	SPIFS	Master mode clock frequency selection	000: FCK/4	001: FCK/8
			010: FCK/16	011: FCK/32
			100: FCK/64	1xx: FCK/128

- **P_SPI_TxStatus (0x7141): SPI Transmit Status Register**

The SPITXBF will be set when P_SPI_TxBUF is written and be cleared immediately when the session of SPI transmission starts.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R	R	R	R	R
0	0	0	0	0	0	0	0
SPITXIF	SPITXIE	SPITXBF	Reserved				

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B15	SPITXIF※	SPI Transmit interrupt flag	0: Not occur	1: Happened, write 1 to clear
B14	SPITXIE	SPI Transmit interrupt enable	0: Disable	1: Enable
B13	SPITXBF	Transmission buffer full flag	1: Transmission buffer full	0: Transmission buffer is empty
B12-B0	Reserved			

※: write '1' to clear this flag

- **P_SPI_TxBuf (0x7142): SPI Transmission Buffer Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SPITXBUF							

B15-B8	Reserved	
B7-B0	SPITXBUF	Write data sends to SPIDO pin

- **P_SPI_RxStatus (0x7143): SPI Receive Status Register**

The FERR will be set when reception buffer receives the new data before reading the former out. It will be cleared immediately when reading P_SPI_RxBuf.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R	R	R	R/W	R	R
0	0	0	0	0	0	0	0
SPIRXIF	SPIRXIE	Reserved			FERR	Reserved	

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B15	SPIRXIF※	SPI receive interrupt flag	0: Not occur	1: Happened, write 1 to clear
B14	SPIRXIE	SPI receive interrupt enable	0: Disable	1: Enable
B13-B11	Reserved			
B10	FERR	Buffer full and overwrite error bit	0: No overwrite error occurs	1: overwrite error happened
B9-B0	Reserved			

※: write '1' to clear this flag

- **P_SPI_RxBuf (0x7144): SPI Reception Buffer Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
SPIRXBUF							

B15-B8	Reserved	
B7-B0	SPIRXBUF	Read data from SPIDI pin

5.14.3. UART (Universal Asynchronous Receiver/Transceiver)

The UART module built in SPMC75F2413A performs serial-to-parallel conversion on data received from an external device and it performs parallel-to-serial conversion on data transmitted to the external device. This module provides the following features:

- Four external pins:
  - RXD1: data reception pin 1 (shared with IOB12)
  - TXD1: data transmission pin 1 (shared with IOB13)
  - RXD2: data reception pin 2 (shared with IOC0)
  - TXD2: data transmission pin 2 (shared with IOC1)
- Provides standard asynchronous, full-duplex communication
- Programmable trans-receive baud rate
- Parity can be even, odd or disabled for generation and detection
- Stop bit width can be 1 or 2 bits
- Support transmitting interrupt
- Support receiving interrupt
- High noise rejection for bit receiving (majority decision of 3 consecutive samples in the middle of received bit time)
- Framing and Parity error detection during reception
- Overrun detection
- Programmable baud rate from 300 bps to 115200 bps
- Support Transmission/Reception data channel selection between TXD1/RXD1 and TXD2/RXD2. Any one of the transmission channels can cooperate with one of reception channels.

Figure 5-75 and Figure 5-76 shows the block diagram and the data format for UART, respectively.

5.14.4. UART Operation

There exists a baud rate register and a 16-bit timer to generate the baud rate. Each times the timer increments from its maximum count (0xFFFF), a clock is sent to the baud rate circuit. The clock is through divid-by-16 counter to generate the baud rate. The timer is reloaded automatically the value in baud rate register.

Baud Rate = FCK / [16 x (65536 – P_UART_BaudRate)]

The content in baud rate register is taken as a 16-bit unsigned number. To derive the required baud rate register values from a known baud rate, use the equation and refer to Table 5-22:

P_UART_BaudRate = 65536 – FCK / (16 x Baud Rate)

Table 5-22 P_UART_BaudRate setup value at FCK = 24.0 MHz

Baud Rate	Baud Rate Timer Reload Register Value @ 24MHz
115200 bps	0xFFF3
57600 bps	0xFFE6
19200 bps	0xFFB2
9600 bps	0xFF64
4800 bps	0xFEC8
2400 bps	0xFD8F
1200 bps	0xFB1E
600 bps	0xF63C
300 bps	0xEC78

The UART begins transmitting after the first rollover of the divide-by-16 counter after the software writes to the P_UART_Data register. The UART transmits data on the TXD2/TXD1 pin in the following order: start bit, 8 data bits (LSB first), parity bit (Parity Enable mode only), stop bit. The TXIF bit in P_UART_Status register is set after 2 FCK cycles when the stop bit is transmitted. The TXIF bit is cleared automatically after the software writes to the P_UART_Data register. Figure 5-77 shows the data transmission timing.

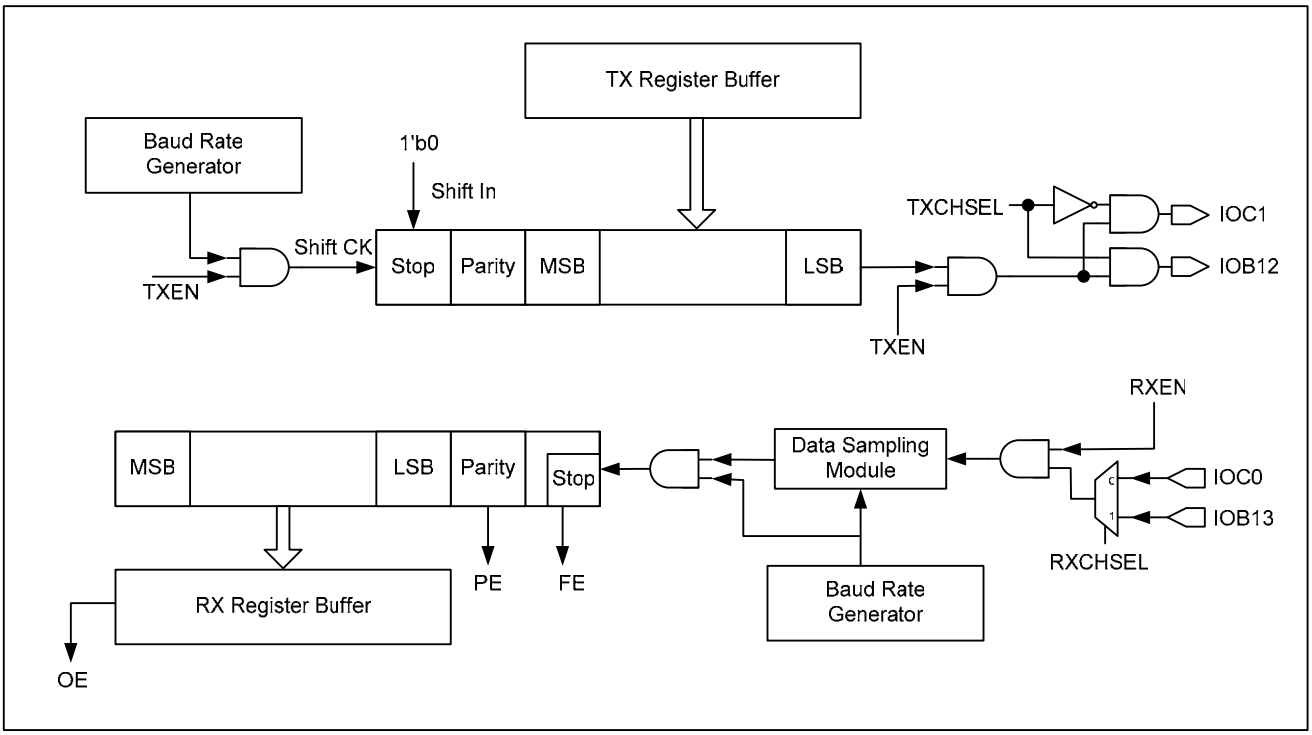


Figure 5-75 UART block diagram

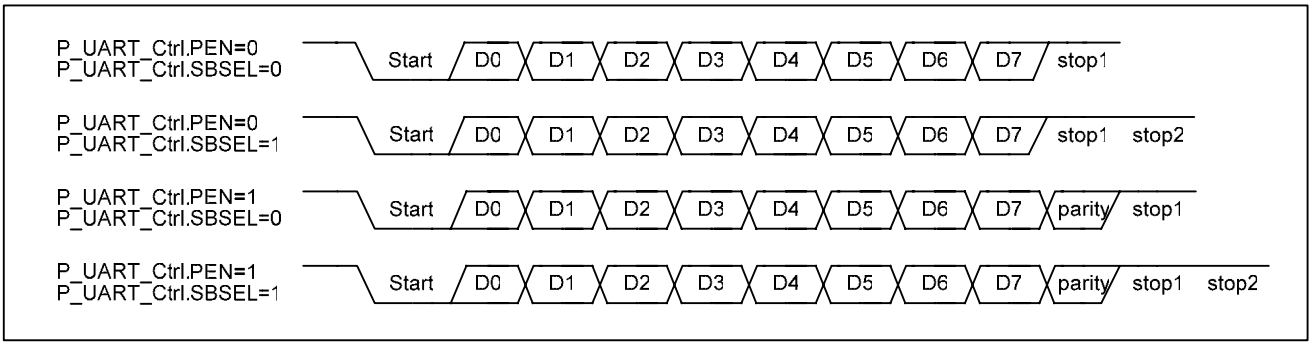


Figure 5-76 UART Data Format

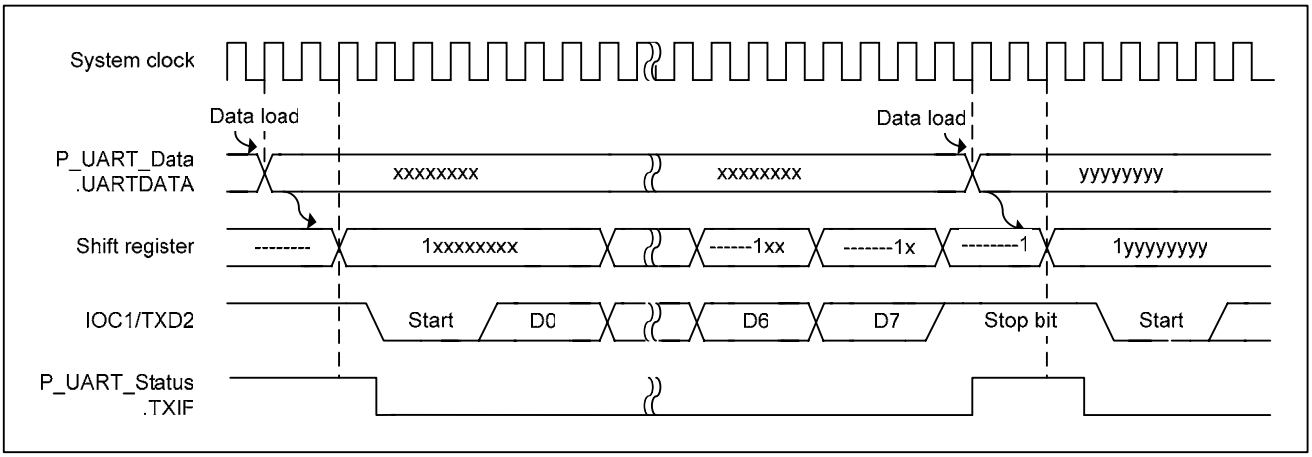


Figure 5-77 Data Transmission Timing

Reception begins at the falling edge of a start bit received on RXD2/RXD1 pin, when enabled by the RXEN bit in P_UART_Ctrl register. For this purpose, RXD2/RXD1is sampled 16 times per bit for any baud rate. When a falling edge of a start bit is detected, the divide-by-16 counter used to generate the receiving clock is reset to align the counter rollover to the bit boundaries. For noise rejection, the serial port establishes the content of each received bit by a majority decision of 3 consecutive samples in the middle of each bit time. This is especially true for the start bit. If the falling edge on RXD2/RXD1is not verified by a majority decision of 3 consecutive samples logic low level, then the serial port stops reception and waits for another falling edge on RXD2/RXD1.

Figure 5-78 shows the data sampling scheme. After receiving the stop bit, the UART module writes the received byte to the P_UART_Data register and set the RXIF and RXBF bit. The serial port then waits for another high-to-low transition on the RXD1/ RXD2 pin. Figure 5-79 shows the data reception timing.

If the received byte is not read out before the next reception finished, the data will be over-written by the new received. In every reception session, RXBF is checked after receiving the stop bit. If the RXBF bit is set, the OE will be set to record this overrun error event. Remarkably, the OE will be cleared automatically if the error check success in the following session. Figure 5-80 shows the overrun error timing.

The parity and frame check is used for improving the reliability of reception. The parity can be even or odd according to the configuration of P_UART_Ctrl.PSEL. The parity check is performed after receiving parity bit if P_UART_Ctrl.PEN is enabled. The PE bit will be set if any parity error. Please refer to Figure 5-81 for timing diagram. The Stop Bit is the part of the UART data formation. If the reception session fails to receive Stop Bit, the integrity of the data frame is lost. The FE bit is set to record this frame error event. Figure 5-82 shows the frame error timing. Remarkably, PE and FE will be clear automatically if the error checks success in the following session, respectively.

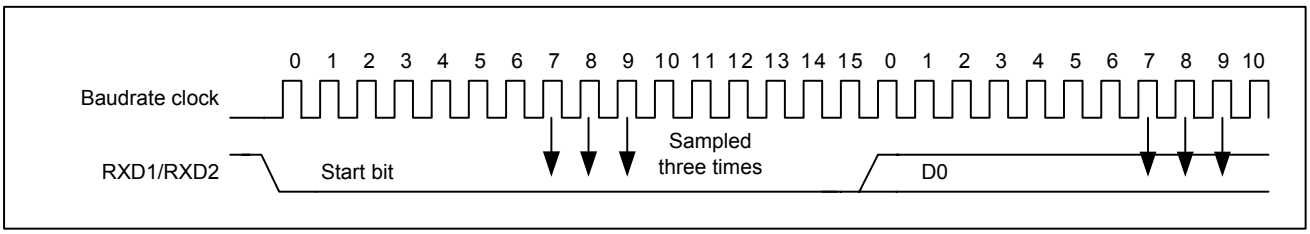


Figure 5-78 Data sampling scheme

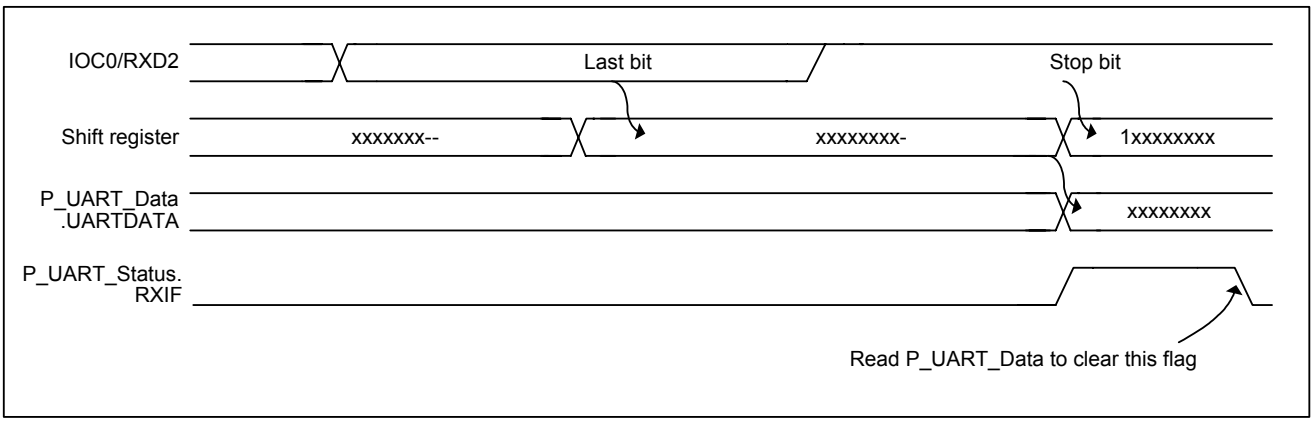


Figure 5-79 RX buffer full

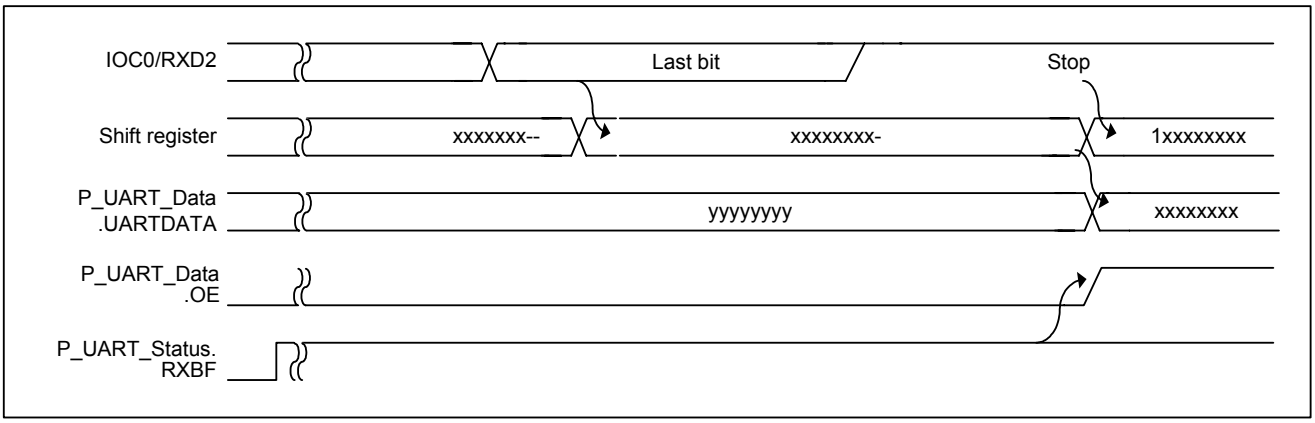


Figure 5-80 Overrun error timing

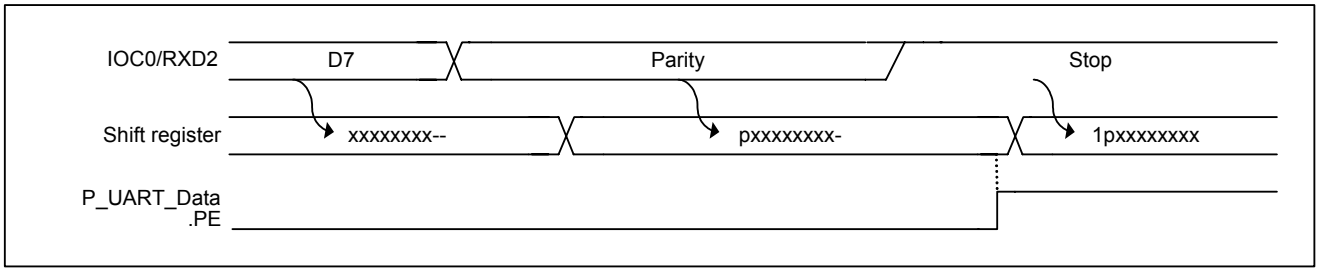


Figure 5-81 Parity Error timing

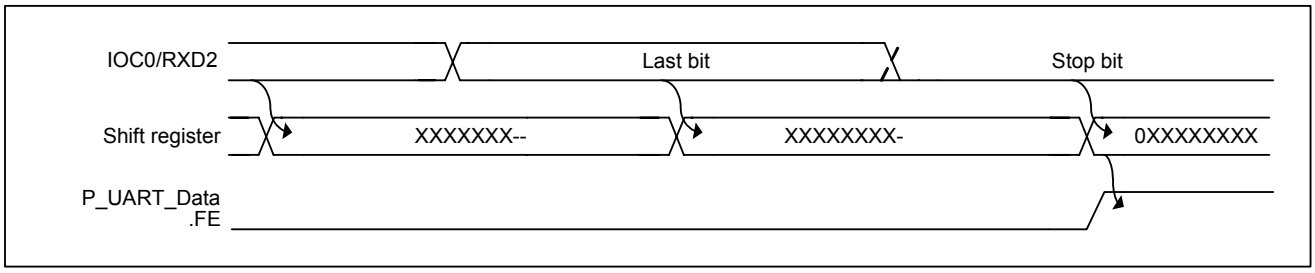


Figure 5-82 Frame Error timing

- **P_UART_Data (0x7100): UART Data Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved				OE	Reserved	FE	PE

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
UARTDATA							

B15-B12	Reserved			
B11	OE	Overrun Error (Ready-only)	0: Not Occurred	1: Occurred
B10	Reserved			
B9	PE	Parity Error (Ready-only)	0: Not Occurred	1: Occurred
B8	FE	Frame Error (Ready-only)	0: Not Occurred	1: Occurred
B7-B0	UARTDATA	UART Data Read/Write Register		

Note: Read-only error flags in bit [11:8] have the same function with control register bits located in bit[3:0] of P_UART_RXStatus register.

- **P_UART_RXStatus (0x7101): UART Reception Error Flag Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	Bb2	B1	B0
R/W	R/W	R/W	R/W	R/W	R	R/W	R/W
0	0	0	0	0	0	0	0
Reserved				OE	Reserved	FE	PE

B15-B4	Reserved			
B3	OE	Overrun Error	Read 0: Not Occurred	Read 1: Occurred
B2	Reserved			
B1	FE	Parity Error	Read 0: Not Occurred	Read 1: Occurred
B0	PE	Frame Error	Read 0: Not Occurred	Read 1: Occurred

- **P_UART_Ctrl (0x7102): UART Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R	R/W	W	R/W	R/W	R
0	0	0	0	0	0	0	0
RXIE	TXIE	RXEN	TXEN	Reset	TXCHSEL	RXCHSEL	Reserved

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R/W	R/W	R/W	R
0	0	0	0	0	0	0	0
Reserved				SBSEL	PSEL	PEN	Reserved

B15	RXIE	Receive Interrupt Enable	0: Disabled	1: Enabled
B14	TXIE	Transmit Interrupt Enable	0: Disabled	1: Enabled
B13	RXEN	UART reception enable	0: Disabled	1: Enabled
B12	TXEN	UART transmission enable	0: Disabled	1: Enabled
B11	Reset	Software reset		
B10	TXCHSEL	Transmission data channel selection	0: UART transmission to TXD2 on IOC1 pin	1: UART transmission to TXD1 on IOB12 pin
B9	RXCHSEL	Reception data channel selection	0: UART reception from RXD2 on IOC0 pin	1: UART reception from RXD1 on IOB13 pin
B8-B4	Reserved			
B3	SBSEL	Stop Bit Size Selection.	0: 1 Stop Bit	1: 2 Stop Bit
B2	PSEL	Parity Selection	0: Odd Parity (if PEN= 1)	1: Even Parity (if PEN= 1)
B1	PEN	Parity Enable	0: Disabled	1: Enabled
B0	Reserved			

- **P_UART_BaudRate(0x7103): UART Baud Rate Setup Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
UARTBUD							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
UARTBUD							

B15-B0	UARTBUD	UART Baud Rate Divisor	Baud Rate = CPUCLK / [16 x (65536 – P_UART_BaudRate)] The value of P_UART_BaudRate register is calculated as follows: P_UART_BaudRate = 65536 – CPUCLK / (16 x Baud Rate)

- **P_UART_Status (0x7104): UART Status Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	1	0	0	0	0	0	0
RXIF	TXIF	Reserved					

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved	RXBF	Reserved		BY	Reserved		

B15	RXIF	Receive Interrupt Flag	1: a valid byte received complete, an interrupt is asserted if RXIE bit is set as '1'	0: no reception interrupt
B14	TXIF	Transmit Interrupt Flag	1: transmitter is ready, an interrupt is asserted if TXIE bit is set as '1'	0: transmitter is not ready
B13-B7	Reserved			
B6	RXBF	Receiving buffer full flag	0: reception buffer is not full	1: Reception buffer is full
B5-B4	Reserved			
B3	BY	Transmitting busy flag.	0: transmitter is ready	1: Transmitter is busy
B2-B0	Reserved			

5.15. Analog-to-Digital Converter (ADC)

SPMC75F2413A embeds an 8-channel ADC with 10-bit resolution. The channel inputs AN7 – AN0 of ADC shares with GPIO pins IOA7 – IOA0, respectively. When corresponding ADC channel is enabled, each pin can be controlled to disable digital function through the register, P_ADC_Channel. The output of sample hold is converted from the analog signal fed into the converter. This converter generates a result via successive approximation. The analog top reference voltage is selectable through the pin VEXTREF. The A/D Converter used for the SPMC75F2413 contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor after activation A/D conversion. The block diagram of A/D converter is shown in Figure 5-83. Figure 5-84 shows the timing diagram of ADC. The ADC has the following features:

- 10-bit resolution
- Max. 100kHz conversion rate
- 8 selectable input channels AN[7:0], shared pin with IOA[7:0]
- External reference input pin VEXTREF
- Four selectable ADC conversion clock: FCK/8, FCK/16, FCK/32, FCK/64
- Provides conversion complete interrupt
- Multiple triggers to start a conversion
  - Software immediate start
  - TGRA compare match on PDC0, PDC1, TPM2 and TGRD compare match on MCP3, and MCP4 timers

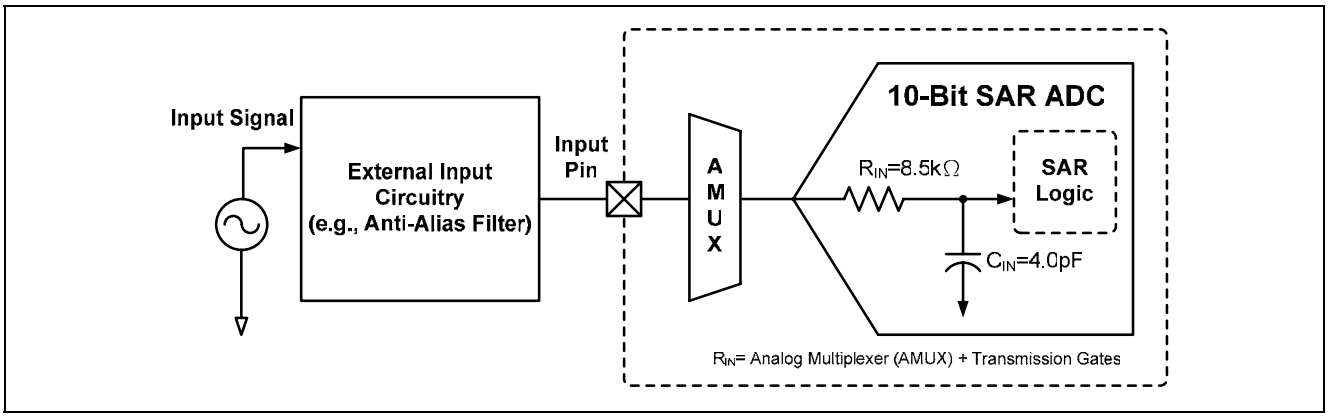
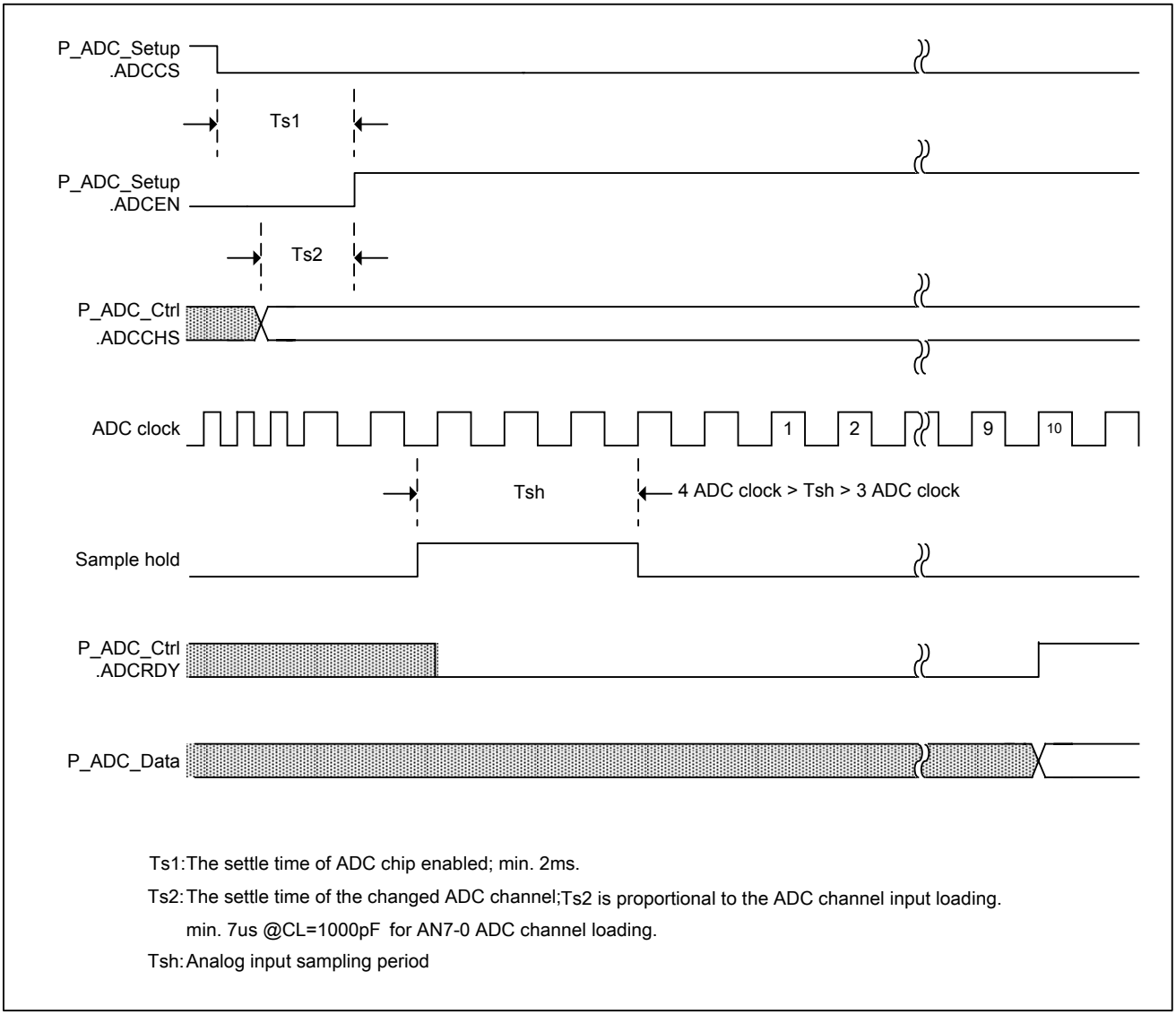


Figure 5-83 ADC equivalent circuit for SPMC75F2413A



Ts1: The settle time of ADC chip enabled; min. 2ms.

Ts2: The settle time of the changed ADC channel;Ts2 is proportional to the ADC channel input loading. min. 7us @CL=1000pF for AN7-0 ADC channel loading.

Tsh: Analog input sampling period

Figure 5-84 ADC timing diagram

The bit ADCCS is set initially to turn on the internal bias in ADC and off if Standby mode for power saving. ADCEN is the control bit to enable ADC function. The ADC clock is configured by ADCFS in P_ADC_Setup. The derived clock frequency is suggested to be less 1.5MHz for conversion precision. The ways to starting conversion have tree methods: external conversion request, auto sampling signal from Timer/PWM module (TPM) and manual ADC conversion. These can be configured by the bits ADCEXTRG and ASPEN in P_ADC_Setup, and ADCSTR in P_ADC_Ctrl. The conversion ready status ADCRDY and interrupt flag ADCIF will set if conversion ready. The converted data can acquired through P_ADC_Data(R). The example of ADC operation is shown in Figure 5-85.

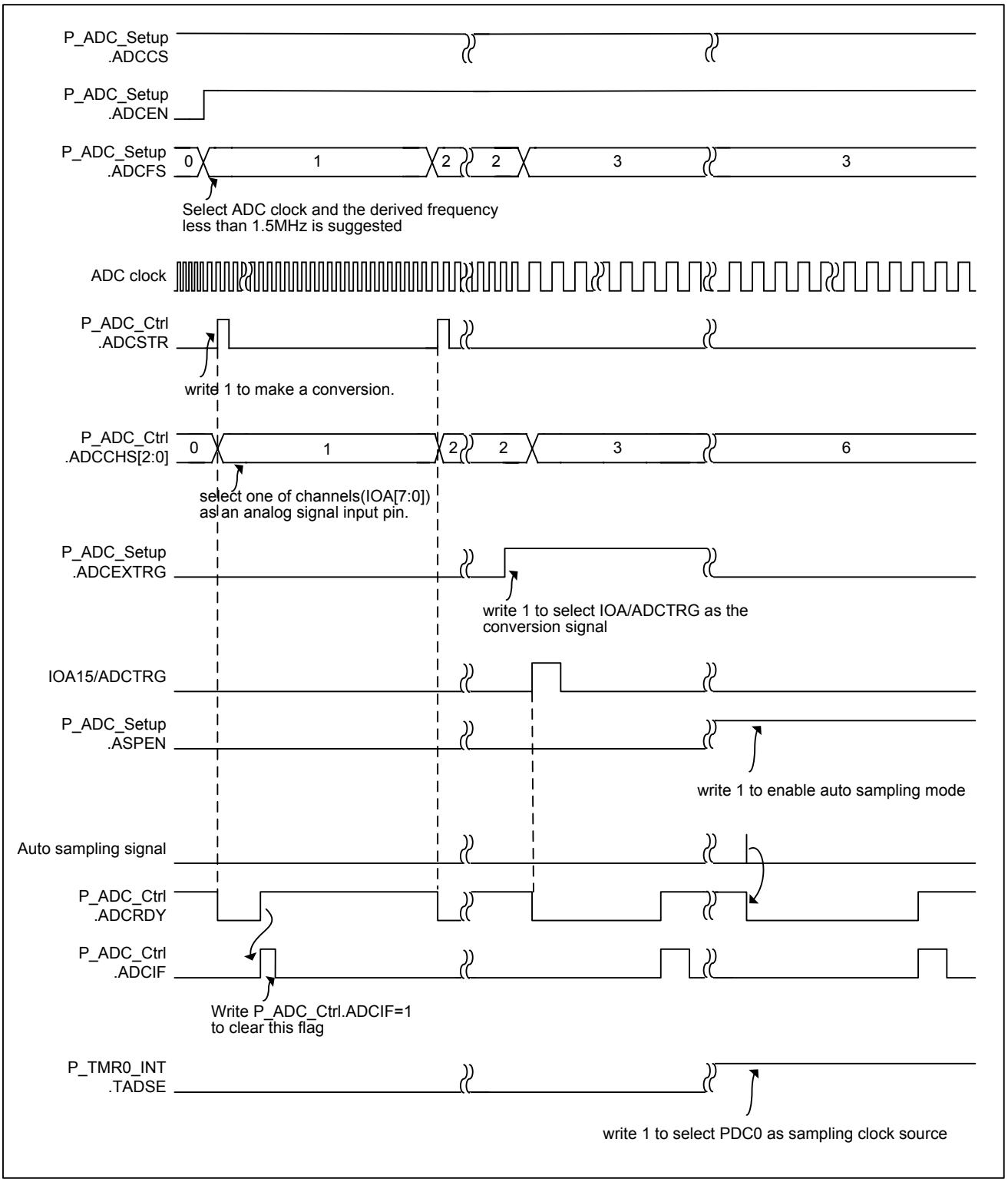


Figure 5-85 AD conversion timing

- **P_ADC_Setup (0x7160)：ADC Setup Register**

The P_ADC_Setup register control the ADC block power on or off, ADC conversion clock and event selection to trigger the start operation of ADC. User should note that the when power-on-reset occurred, the ADC block is power on (ADCCS bit is 1) and ADC function is off (ADCEN bit is 0). At meanwhile, the P_ADC_Data value is 0xFFC0 for the purpose of power saving but without ADC conversion ready signal (ADCRDY in P_ADC_Ctrl register is 0). If user sets the ADCEN to 1 at this time, the ADC block will generate the ADCRDY signal and also set the ADCIF bit in P_ADC_Ctrl register. To prevent read the incorrect ADC value; do not read the first ADC data after the ADCEN is set to 1.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0
ADCCS	ADCEN	Reserved			ADCFS		ADCEXTRG

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
ASPEN	Reserved						

B15	ADCCS	ADC power on	0: un-select ADC block	1: select ADC block
B14	ADCEN	ADC converter enable	0: disable ADC block	1: enable ADC block
B13-B11	Reserved			
B10-B9	ADCFS†	A/D converter clock selection	00: CPUCLK /8	01: CPUCLK /16
			10: CPUCLK /32	11: CPUCLK /64
B8	ADCEXTRG	External ADC conversion request trigger from a high pulse on IOA15 pad	1: Enable	0: Disable
B7	ASPEN※	Auto Sampling mode enable	0: Disable	1: Enable
B6-B0	Reserved			

† Configure ADCFS to let derived frequency is less than 1.5MHz.
※ Please refer to the bit TADSE in P_TMRx_INT (x=0~4)

- **P_ADC_Ctrl(0x7161)： ADC Control Register**

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
ADCIF	ADCIE	Reserved					

B7	B6	B5	B4	B3	B2	B1	B0
R	R/W	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0
ADCRDY	ADCSTR	Reserved			ADCCHS		

B15	ADCIF※	ADC interrupt flag	0: interrupt Not happened	1: interrupt happen
B14	ADCIE	ADC interrupt enable	0: disable	1: enable
B13-B8	Reserved			
B7	ADCRDY	ADC conversion ready	0: conversion not ready, AD data not effect	1: conversion ready, AD data is valid
B6	ADCSTR	Manual start ADC Conversion	0: No Effect	1: START
B5-B3	Reserved			
B2-B0	ADCCHS	Select ADC converter channel input	000: ADC Channel0 (IOA0)	001: ADC Channel1 (IOA1)
			010: ADC Channel2 (IOA2)	011: ADC Channel3 (IOA3)
			100: ADC Channel4 (IOA4)	101: ADC Channel5 (IOA5)
			110: ADC Channel6 (IOA6)	111: ADC Channel7 (IOA7)

※: write '1' to clear this flag

- **P_ADC_Channel(0x7166) ：ADC Input Channels Select Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
Reserved							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
ADCCH7	ADCCH6	ADCCH5	ADCCH4	ADCCH3	ADCCH2	ADCCH1	ADCCH0

B15-B8	Reserved			
B7	ADCCH7	ADC Input Channel 7 Enable	1: IOA7 as ADC channel 7	0: IOA7 as GPIO
B6	ADCCH6	ADC Input Channel 6 Enable	1: IOA6 as ADC channel 6	0: IOA6 as GPIO
B5	ADCCH5	ADC Input Channel 5 Enable	1: IOA5 as ADC channel 5	0: IOA5 as GPIO
B4	ADCCH4	ADC Input Channel 4 Enable	1: IOA4 as ADC channel 4	0: IOA4 as GPIO
B3	ADCCH3	ADC Input Channel 3 Enable	1: IOA3 as ADC channel 3	0: IOA3 as GPIO
B2	ADCCH2	ADC Input Channel 2 Enable	1: IOA2 as ADC channel 2	0: IOA2 as GPIO
B1	ADCCH1	ADC Input Channel 1 Enable	1: IOA1 as ADC channel 1	0: IOA1 as GPIO
B0	ADCCH0	ADC Input Channel0 Enable	1: IOA0 as ADC channel 0	0: IOA0 as GPIO

- **P_ADC_Data (0x7162) ：ADC Data Register**

B15	B14	B13	B12	B11	B10	B9	B8
R	R	R	R	R	R	R	R
1	1	1	1	1	1	1	1
ADCDATA							

B7	B6	B5	B4	B3	B2	B1	B0
R	R	R	R	R	R	R	R
1	1	0	0	0	0	0	0
ADCDATA		Reserved					

B15-B6	ADDATA	ADC conversion data		
B5-B0	Reserved			

5.16. Watchdog Timer (WDT)

The purpose of a watchdog timer is to monitor if the system operates normally. Within a certain period, watchdog counter must be cleared. If the watchdog timer is not cleared, CPU assumes the program has been running in an abnormal condition and therefore, CPU will reset the system to the initial state and start running the program from beginning. It protects the system from incorrect code execution by launching a system reset when the watchdog timer overflows as a result of failure of software to clear the timer within selection time. For SPMC75F2413A devices, watchdog function can be enabled or disabled by P_System_Option.WDG.

The device includes a watchdog timer (WDT) to monitor abnormal software run-away. A system or CPU reset will be generated if it is not periodically cleared by software. The watchdog timer is an eight-bit counter. Its clock can be selected from eight different sources. When a counter overflow occurs, a watchdog reset will be generated. A watchdog reset can issue a system reset or CPU reset according to control register settings. To further ensure the settings of watchdog control register will not be modified accidentally, a special bit pattern must be written to the unused bits of watchdog control register when the settings is to be changed. Otherwise a watchdog reset will be generated if the unused bits of watchdog control register are not properly written.

Following are the eight watchdog time-out selections.

Table 5-23 WDT Time-out selections

WDPS	WDT Clock Rate (Hz)	Time-out Time (F_{CK}=24MHz)
000	F_{CK}/65536	699.05ms
001	F_{CK}/32768	349.52ms
010	F_{CK}/16384	174.76ms
011	F_{CK}/8192	87.38ms
100	F_{CK}/4096	43.69ms
101	F_{CK}/2048	21.84ms
110	F_{CK}/1024	10.92ms
111	F_{CK}/512	5.46ms

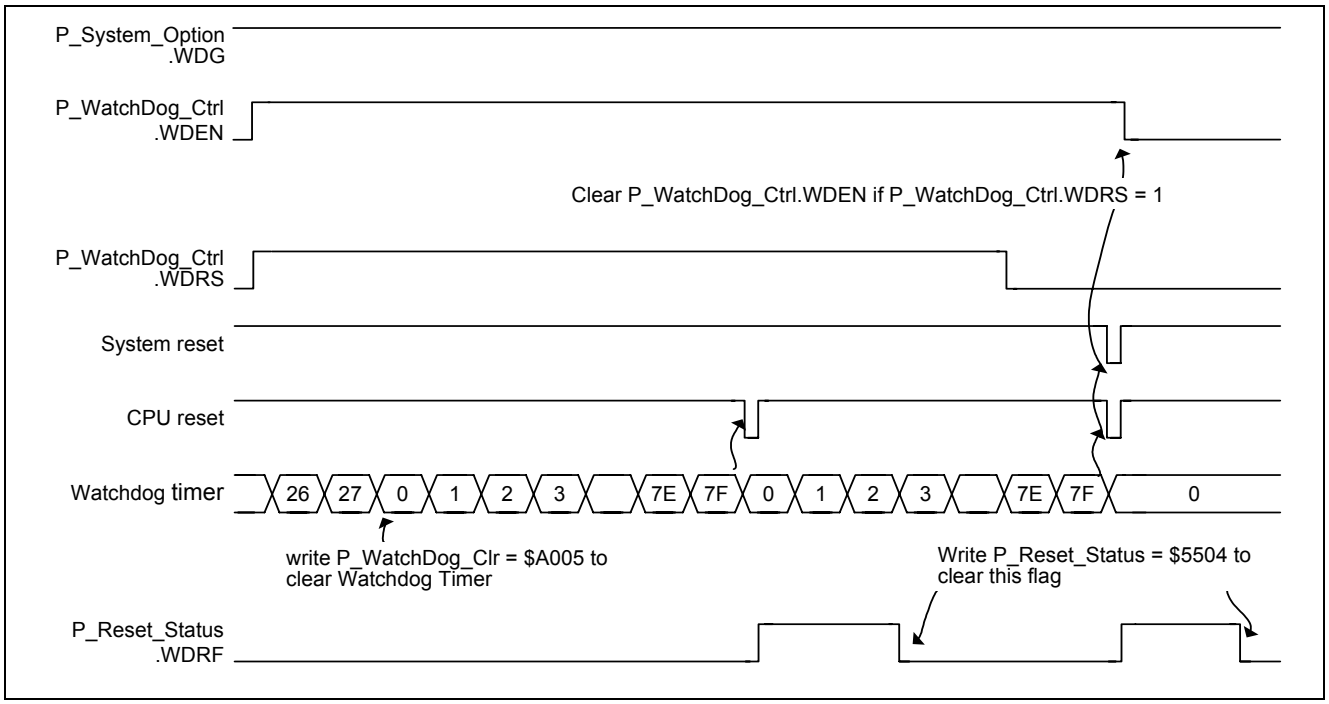


Figure 5-86 Watchdog Timing Diagram

- **P_WatchDog_Ctrl (0x700A)：Watchdog Control Register**

This register provides the watchdog clear timer and on/off function for firmware setting.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R	R	R	R	R	R
0	0	0	0	0	0	0	0
WDEN	WDRS	Reserved					

B7	B6	B5	B4	B3	B2	B1	B0
W	W	W	W	W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
WDCHK					WDPS		

B15	WDEN※	Watchdog timer enable bit	0: Disable	1: Enable
B14	WDRS	Watchdog reset select bit	0: System reset	1: CPU reset
B13-B8	Reserved			
B7-B3	WDCHK	Watchdog control register check bits	To change the settings of P_WatchDog_Ctrl register, “10101” must be written to these bits. Otherwise a watchdog reset will be generated. These bits will be read as ‘0’	
B2-B0	WDPS	Watchdog Timer Time-out Selections	Please see Table 5-23	

※ If WDEN is set, this bit can only be cleared by system reset event, which is reset CPU and peripherals. Please refer to Table 5-7.

- **P_WatchDog_Clr (0x700B)：Watchdog Clear Register**

P_WatchDog_Clr register is used to clear watchdog timer, Write 0xA005 to clear watchdog timer. A watchdog reset will be generated if other value has been written.

B15	B14	B13	B12	B11	B10	B9	B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
WDTCLR							

B7	B6	B5	B4	B3	B2	B1	B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0
WDTCLR							

Note: Please the bit WDRF in P_Reset_Status for reference.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Min.	Typ.	Max.	Unit
DC Supply Voltage	V_{DD}		-	6.0(V_+)	V
Input Voltage Range	V_{IN}	-0.5	-	V_+ + 0.5	V
Current into Vdd Pin	I_{VDD}	-	-	80	mA
Current out of Vss Pin	I_{VSS}	-	-	80	mA
Current soured by each I/O port	I_{OHR}	-	-	15	mA
Current sunk by each I/O port	I_{OLR}	-	-	15	mA
Operating Temperature	T_A	-40	-	+85	℃
Storage Temperature	T_{STO}	-50	-	+150	℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see DC Characteristics.

6.2. DC Characteristics (VDD = 4.5~5.5V, T_A = -40~85°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	4.5	5.0	5.5	V	
LVR voltage	V_{LVR}	3.60	4.09	4.50	V	
Operating current	I_{OP}	-	-	35	mA	VDD = 5.0V, 6MHz X'tal, F_{CK}=24MHz
Wait current	I_{WAIT}	-	-	25	mA	PLL on, CPU off
Standby current	I_{STB}	-	-	150	uA	All off, VDD = 5.0V, T_A = 25℃
Input High Level	V_{IH}	0.7VDD	-	-	V	All input
Input Low Level	V_{IL}	-	-	0.3VDD	V	All input
Output High Current	I_{OH1}	-2.0	-	-	mA	VDD = 4.5V, V_{OH} = 4.0V (Normal drive I/O)
	I_{OH2}	-4.0	-	-		VDD = 4.5V, V_{OH} = 4.0V (Large drive I/O)※
Output Low Current	I_{OL1}	2.0	-	-	mA	VDD = 4.5V, V_{OL} = 0.5V (Normal drive I/O)
	I_{OL2}	10	-	-		VDD = 4.5V, V_{OL} = 0.5V (Large drive I/O)※
Input Pull-low Resistance	R_{PL}	-	100	-	KΩ	VDD = 5.0V, V_O = VDD
Input Pull-high Resistance	R_{PH}	-	100	-	KΩ	VDD = 5.0V, V_O = VSS

Note1: Data in "Typ" column is at 25°C unless otherwise stated.

Note2: Large drive I/O pins: IOA[15:8], IOB[5:0], IOB[15:12], IOC[3:0], IOC[15:10]

6.3. AC Characteristics (VDD = 4.5~5.5V, T_A = -40~85°C)

Characteristics	Symbol	Unit			Unit
		Min.	Typ.	Max.	
Input Clock Frequency (Crystal)	F_{CK}	3.0	-	6.0	MHz
PLL Output Frequency	F_{PLL}	12	-	24	MHz
Power-on Timer Period and Time of Wakeup from Standby Mode	T_{PORT}	-	82	200	mS
RESETB Pulse Width (low)	T_{RSTB}	-	7.0	15	uS

6.4. Analog Interface Electrical Characteristics (VDD = 5.0V, T_A = -40ºC~85ºC)

Mnemonic	Description		Symbol	Min.	Typ.	Max.	Unit	Condition
A/D Converter	Resolution		N_{R_AD}	-	-	10	Bit	
	Top Reference Voltage		V_{RT}	2 (Note 1)	-	VDD	V	
	Top Reference Voltage Supply Current		I_{RT}	-	500	-	uA	
	Analog Input Voltage		V_{AIN}	0	-	VDD/V_{RT}	V	
	Conversion Rate		F_{AD}	50	100	200	KHz	VDD=5.0V@24.0MHz
	Analog Input Impedance (Note 2)		$R_{AIN(Note\ 2)}$	-	-	30	KΩ	
	Accuracy	Integral Linearity Error	E_{INL_AD}	-	±1.0	±2.0	LSB (Note 3)	
		Differential Linearity Error	E_{DNL_AD}	-	±1.0	±2.0	LSB	
		Zero Offset Error	E_{ZOE_AD}	-	-	±1.5	LSB	
		Full Scale Error	E_{FSE_AD}	-	-	±1.5	LSB	
		Total Error	E_{ALL_AD}	-	-	±3.0	LSB	

Note1: The ADC performance is limited by the system's noise level, so the SPMC751F2413A can not guarantee the 10-bit accuracy when VEXTREF is 2.0V.

Note2: Analog input voltage might not stabilize within the analog input sampling period (>1.5uSec) if the output impedance of the external circuit for the analog input is high enough. Therefore, it is recommended to keep the output impedance of the external circuit low. It is recommended that the impedance is less than 30KΩ. Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.01uF to 0.1uF for the analog input pin. Figure 5-83 shows ADC equivalent circuit for reference.

Note3: LSB means Least Significant Bit. With VEXTREF=5.0V, 1LSB=5.0V/2^10=4.883 mV.

7. SPMC75F2413A EVM BOARD V1.1 SCHEMATIC

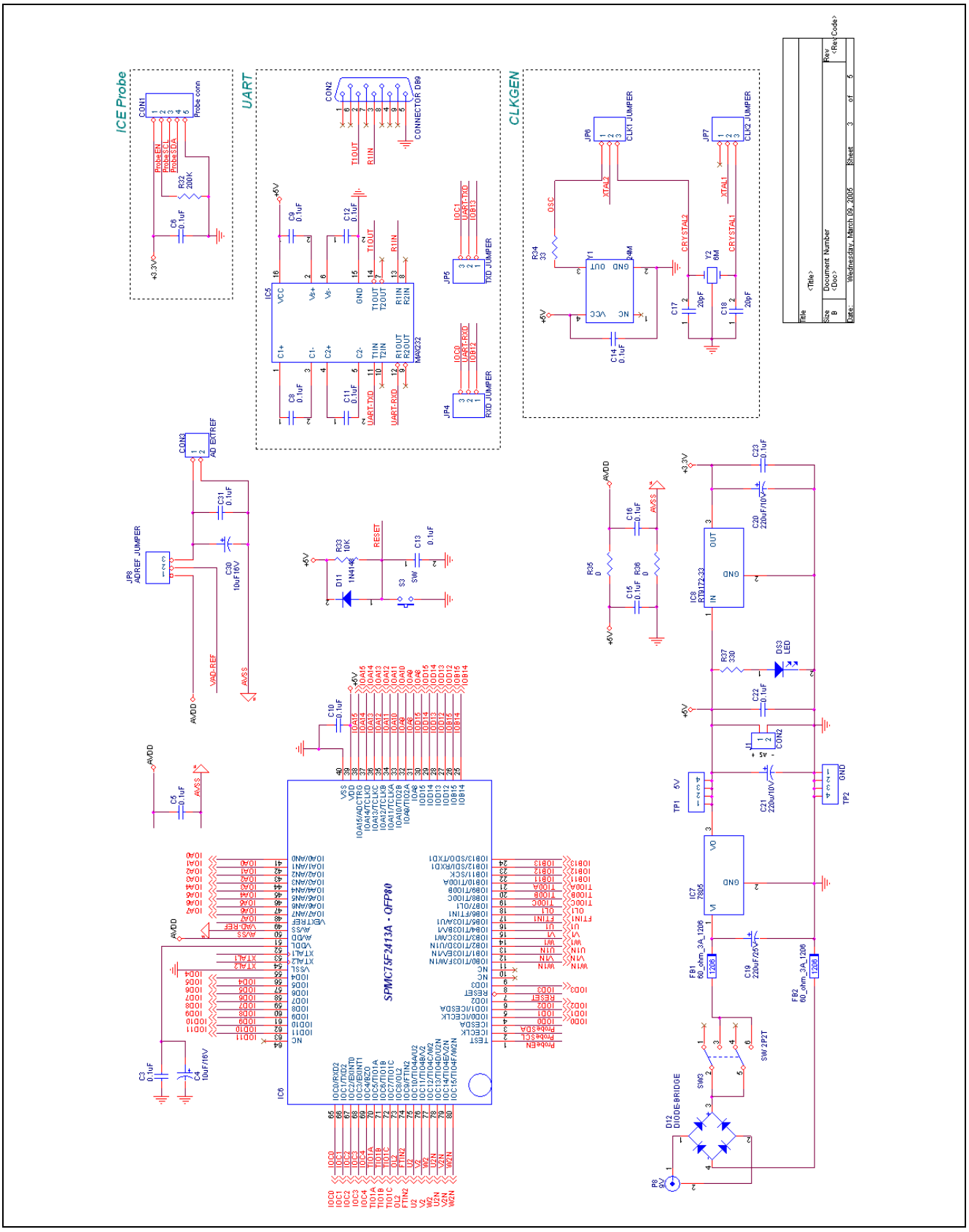


Figure 7-1 SPMC75F2413A EVM board circuit part I

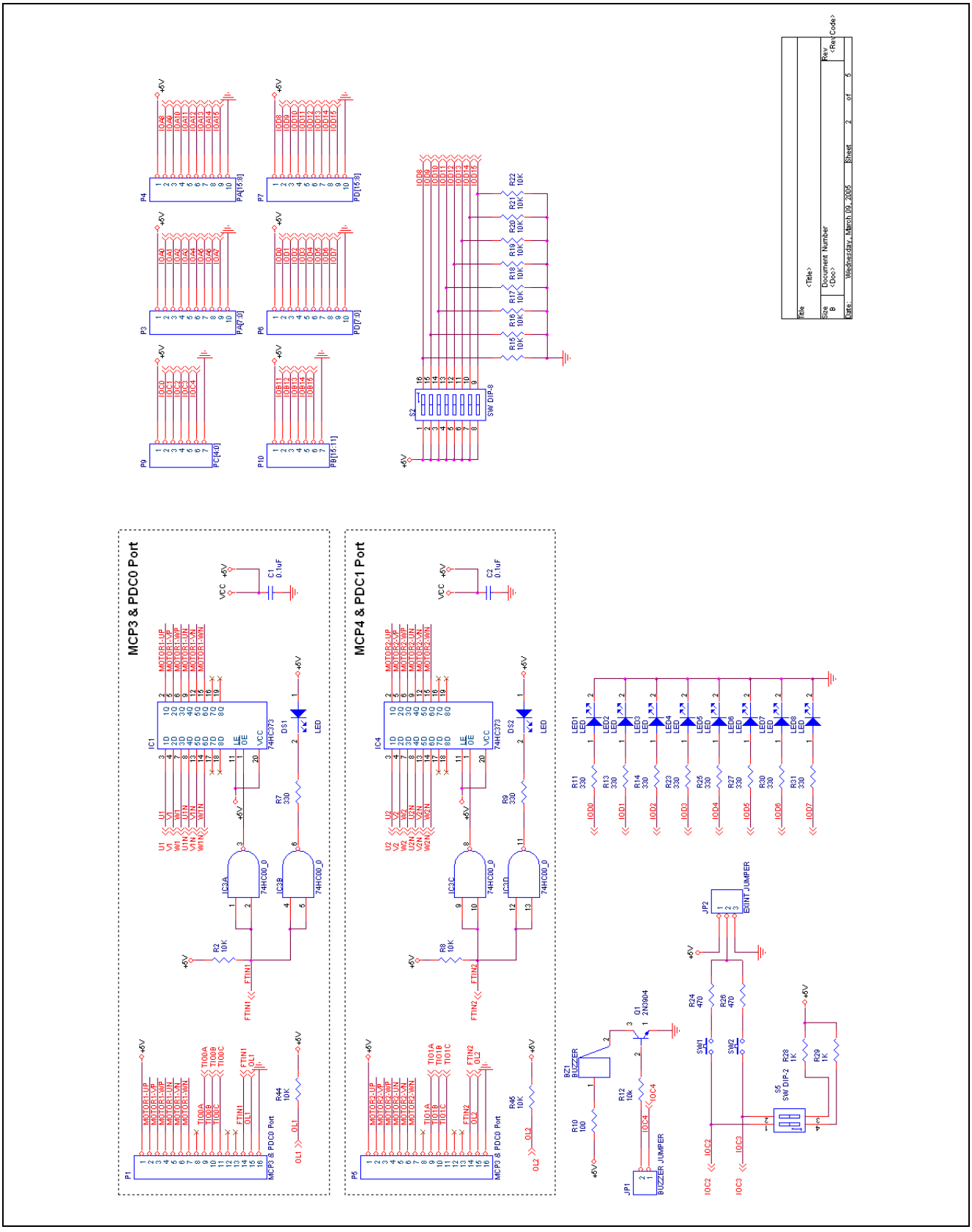


Figure 7-2 SPMC75F2413A EVM board circuit part II

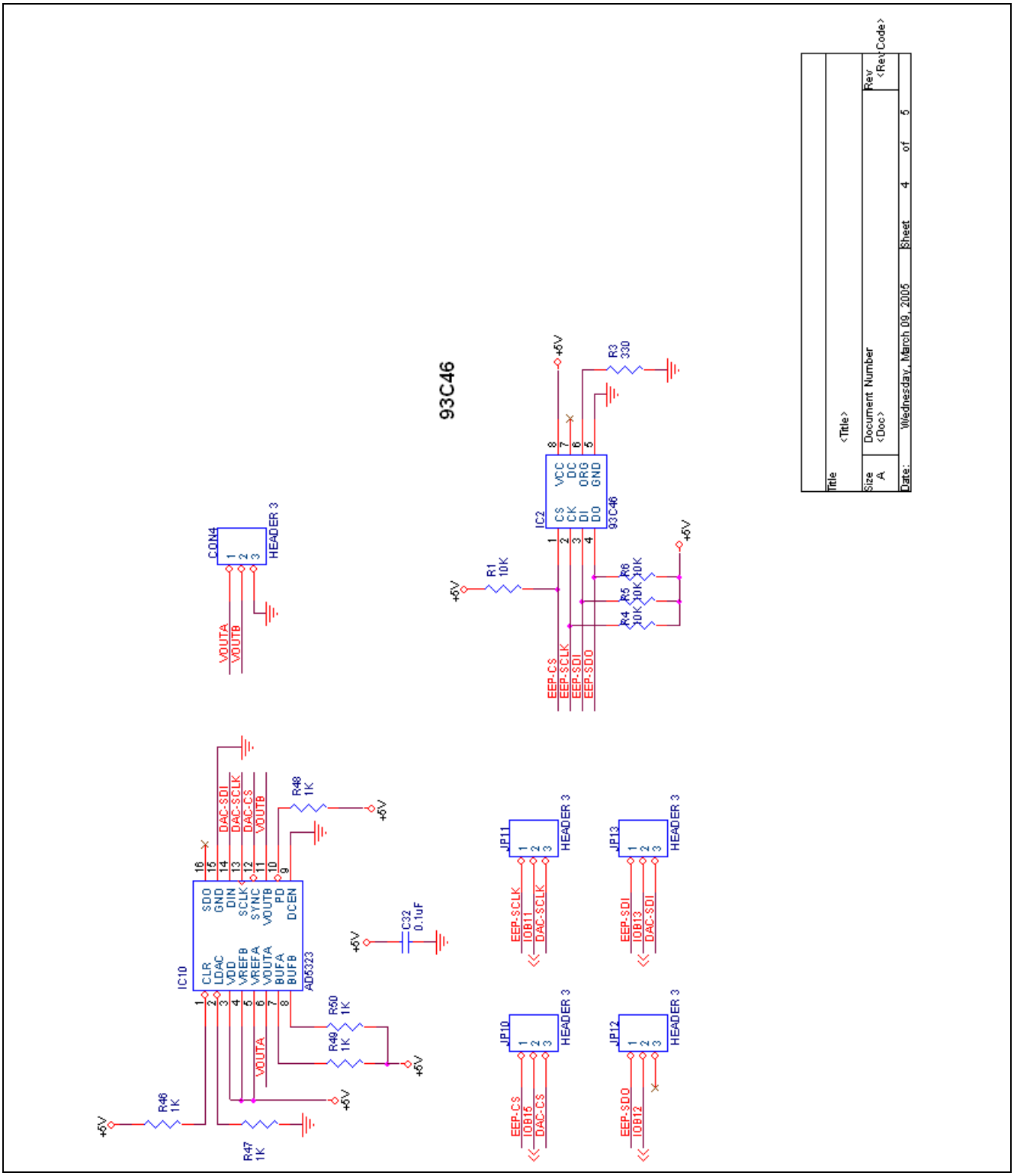
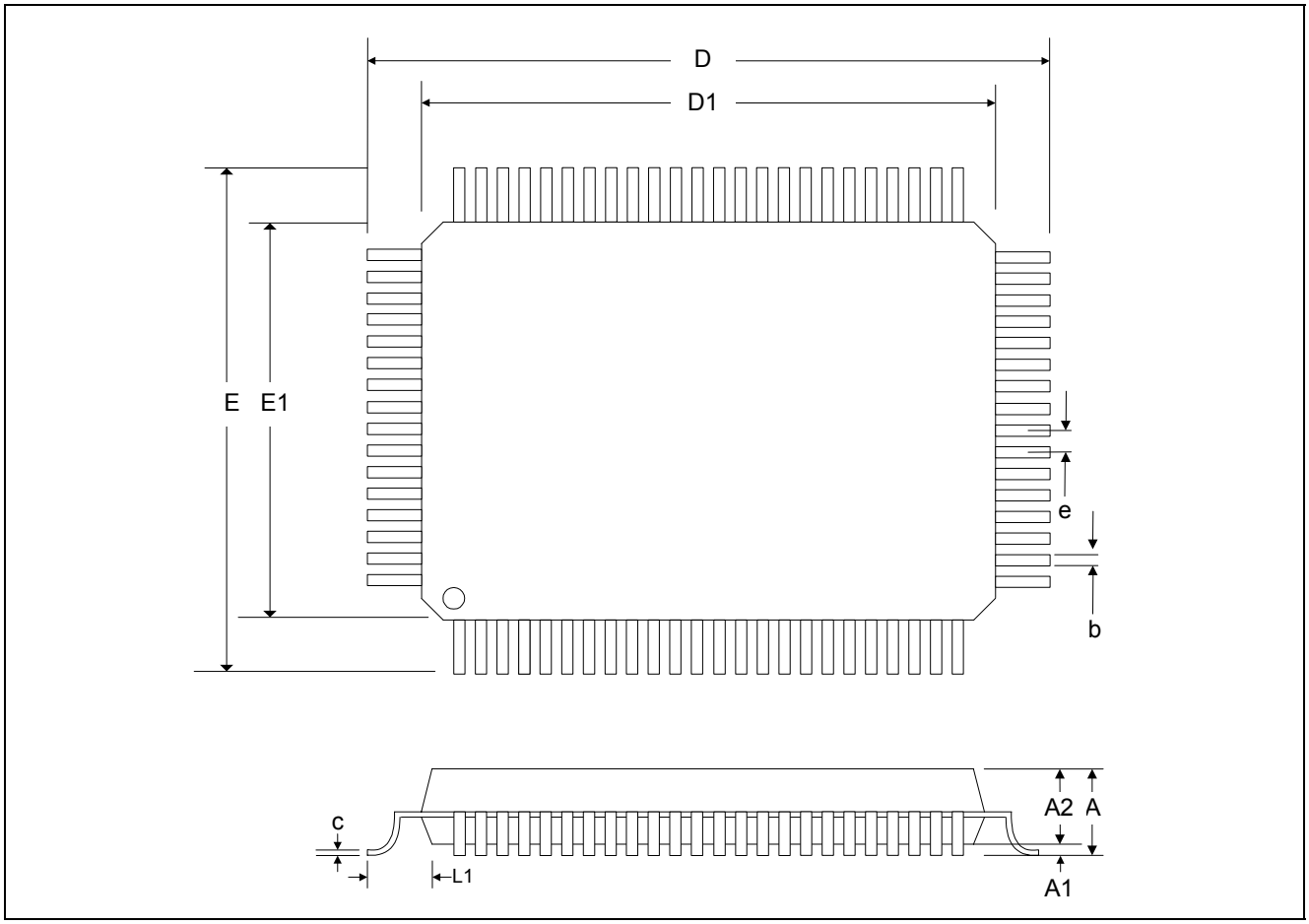


Figure 7-3 SPMC75F2413A EVM board circuit part III

8. PACKAGE/PAD LOCATIONS

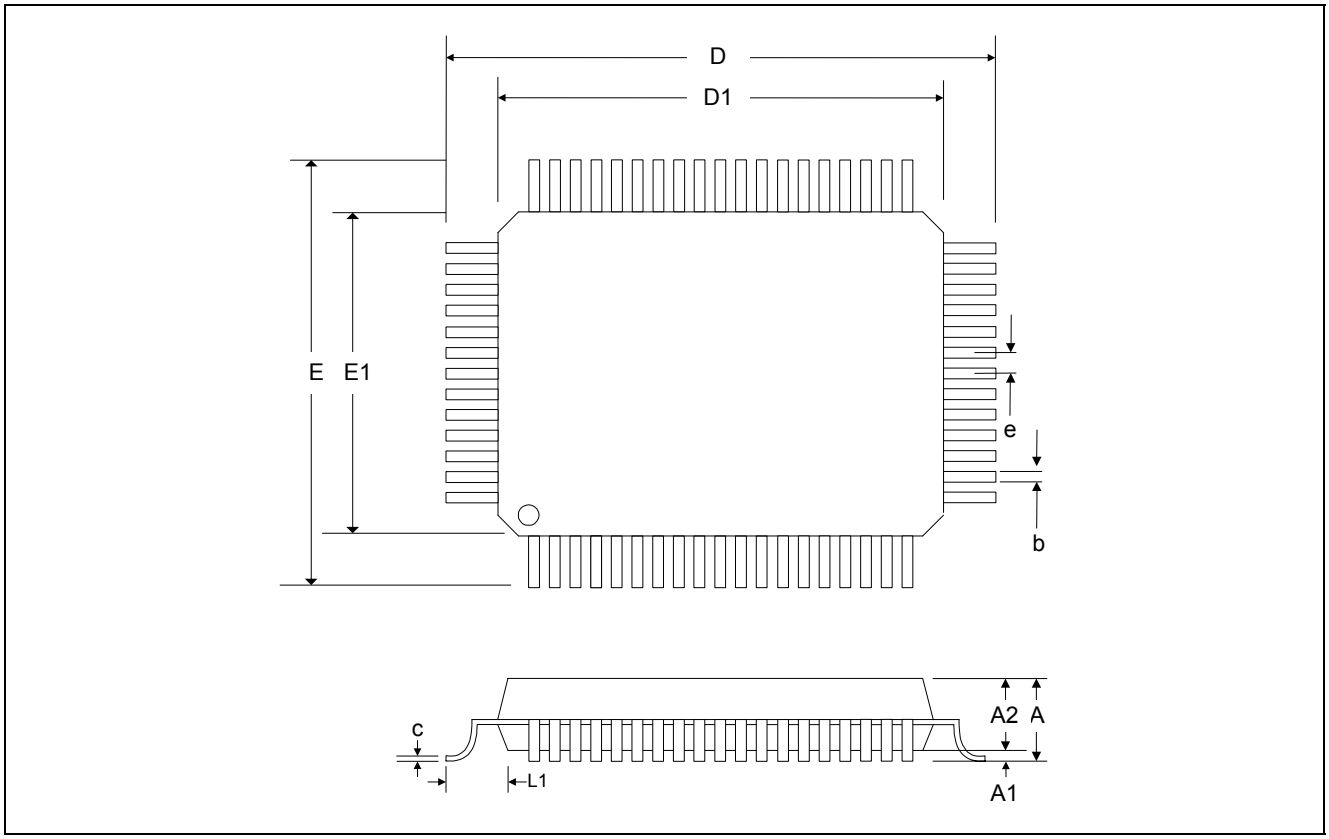
8.1. Package Information

8.1.1. 80 PIN QFP



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	0.134
A1	0.010	-	-
A2	0.098	0.107	0.114
b	0.012	0.014	0.018
c	0.004	0.006	0.009
D	0.913 BSC.		
D1	0.787 BSC.		
E	0.677 BSC.		
E1	0.551 BSC.		
e	0.031 BSC.		
L1	0.063 REF		

8.1.2. 64 PIN QFP



Symbol	Dimension in inch		
	Min.	Typ.	Max.
A	-	-	0.134
A1	0.010	-	-
A2	0.098	0.107	0.114
b	0.014	0.015	0.020
C	0.004	0.006	0.009
D	0.913 BSC.		
D1	0.787 BSC.		
E	0.677 BSC.		
E1	0.551 BSC.		
e	0.039 BSC.		
L1	0.063 REF		

8.2. Ordering Information

Product Number	Package Type
SPMC75F2413A - PQ05	Package form - QFP 80
SPMC75F2413A - PQ04	Package form - QFP 64

8.3. Storage Condition and Period for Package

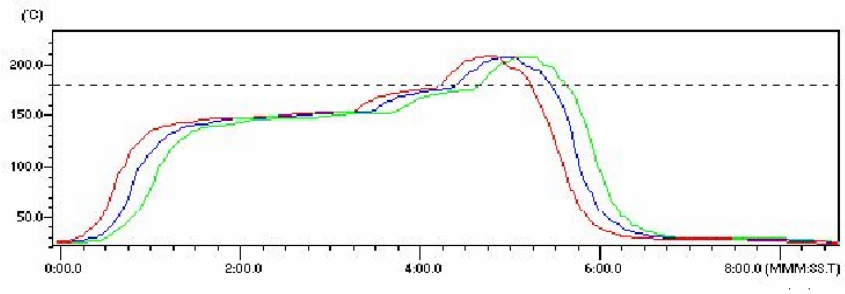
Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
QFP	LEVEL 3	220 +5/-0℃	168Hrs @ ≦30℃/ 60% R.H.	Yes

Note1: Please refer to IPC/JEDEC standard J-STD-020A and EIA JEDEC stand JFSD22-A112
Note2: or refer to the "CAUTION Note" on dry pack bag.

8.4. Recommended SMT Temperature Profile

This "Recommended" temperature profile is a rough guideline for SMT process reference. Most of SUNPLUSIT leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF(Pre-Plated Frame) product with 63/37 solder paste, we recommend 240℃~245℃ for peak temperature.

Recommended Reflow Profile for 63/37 Solder Paste or Cu lead frame

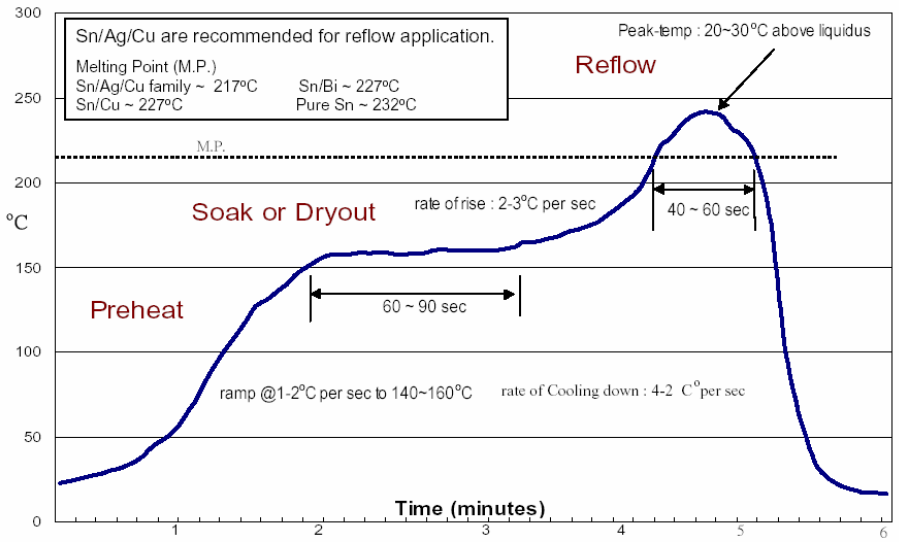


This profile is designed for use with Sn63 or Sn62 and can serve as a general guideline in establishing a reflow profile.

Reflow Profile:

- Heating-up @1~3°C per sec to 140°C
- Preheat @ 140-150°C for 120 ~ 160 sec
- Ramp @ 2~3 °C per sec to peak temperature (220 ~ 225 °C), Temperature over 183°C for 45~ 75 sec
- Cooling down to room temperature @4~2°C per sec to avoid undesired intermatalic compound layer.

Recommended Reflow Profile for Lead-free Solder Paste or PPF lead frame



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10. REVISION HISTORY

Date	Revision #	Description	Page
Feb. 15, 2006	1.1	Modify the Conversion Rate (F_{AD})	141
JUL. 20, 2005	1.0	1. Rewrite the chapters for TPM0 ~ TPM4 module. 2. Supply detailed timing diagrams for every topic. 3. Change Operating current, Wait current and Standby current in 6.26.2 4. Add T_{PORT} and T_{RSTB} in 6.36.3. 5. Add analog interface electrical characteristics in 6.4. 6. Add I_{VDD}, I_{VSS}, I_{OHR}, I_{OLR} in 6.1.	55~117 33~136 139 139 140 139
JUN. 17, 2004	0.1	Original	33