TJA1082

FlexRay node transceiver

Rev. 01 — 1 July 2009 | Preliminary data sheet

1. General description

The TJA1082 FlexRay node transceiver is compatible with the FlexRay electrical physical layer specification V2.1 Rev. B (see Ref. 1). It also incorporates features and parameters anticipated to be included in V3.0, currently being finalized. It is primarily intended for communication systems operating at between 2.5 Mbit/s and 10 Mbit/s, and provides an advanced interface between the protocol controller and the physical bus in a FlexRay network. The TJA1082 offers an optimized solution for Electronic Control Unit (ECU) applications that do not need enhanced power management and are typically switched by ignition or activated by a dedicated wake-up line.

The TJA1082 provides differential transmit capability to the network and differential receive capability to the FlexRay controller. It offers excellent EMC performance as well as high ESD protection.

The TJA1082 actively monitors system performance using dedicated error and status information (readable by any microcontroller), as well as internal voltage and temperature monitoring.

2. Features

2.1 Optimized for time triggered communication systems

- Compliant with Electrical Physical Layer specification 2.1 Rev. B
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
- Data transfer at 2.5 Mbit/s, 5 Mbit/s and 10 Mbit/s
- Supports 60 ns minimum bit time at 400 mV differential voltage
- Very low ElectroMagnetic Emission (EME) to support unshielded cable
- Differential receiver with high common-mode range for excellent ElectroMagnetic Immunity (EMI)
- Auto I/O level adaptation to host controller supply voltage V_{IO}
- Can be used in 14 V and 42 V powered systems
- Instant shut down interface (BGE pin)

2.2 Low power management

- Very low current consumption in Standby mode
- Remote wake-up via wake-up symbol or dedicated FlexRay data frames on the bus lines

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2.3 Diagnosis and robustness

- Enhanced supply voltage monitoring on V_{CC} and V_{IO}
- Two error diagnosis modes: status register readout via Serial Peripheral Interface (SPI) or simple error indication via ERRN pin
- Overtemperature detection
- Short-circuit detection on bus lines
- Power-on flag
- Clamping diagnosis for pins TXEN and BGE
- Bus pins protected against ±8 kV ESD pulses according to IEC61000-4 and HBM
- Bus pins protected against transients in automotive environment (ISO 7637 class C compliant)
- Bus pins short-circuit proof to battery voltage (14 V and 42 V) and ground
- Maximum differential voltage between pins BP or BM and any other pin of ±60 V
- Bus lines remain passive when the transceiver is not powered
- No reverse currents from the digital input pins to V_{IO} or V_{CC} when the transceiver is not powered
- Two error diagnosis modes:
  - Status register readout via SPI
  - Simple error indication via ERRN pin

2.4 FlexRay conformance classes

- Bus driver - bus guardian interface
- Bus driver logic level adaptation

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	**Description**	**Version**
TJA1082TT	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Block diagram

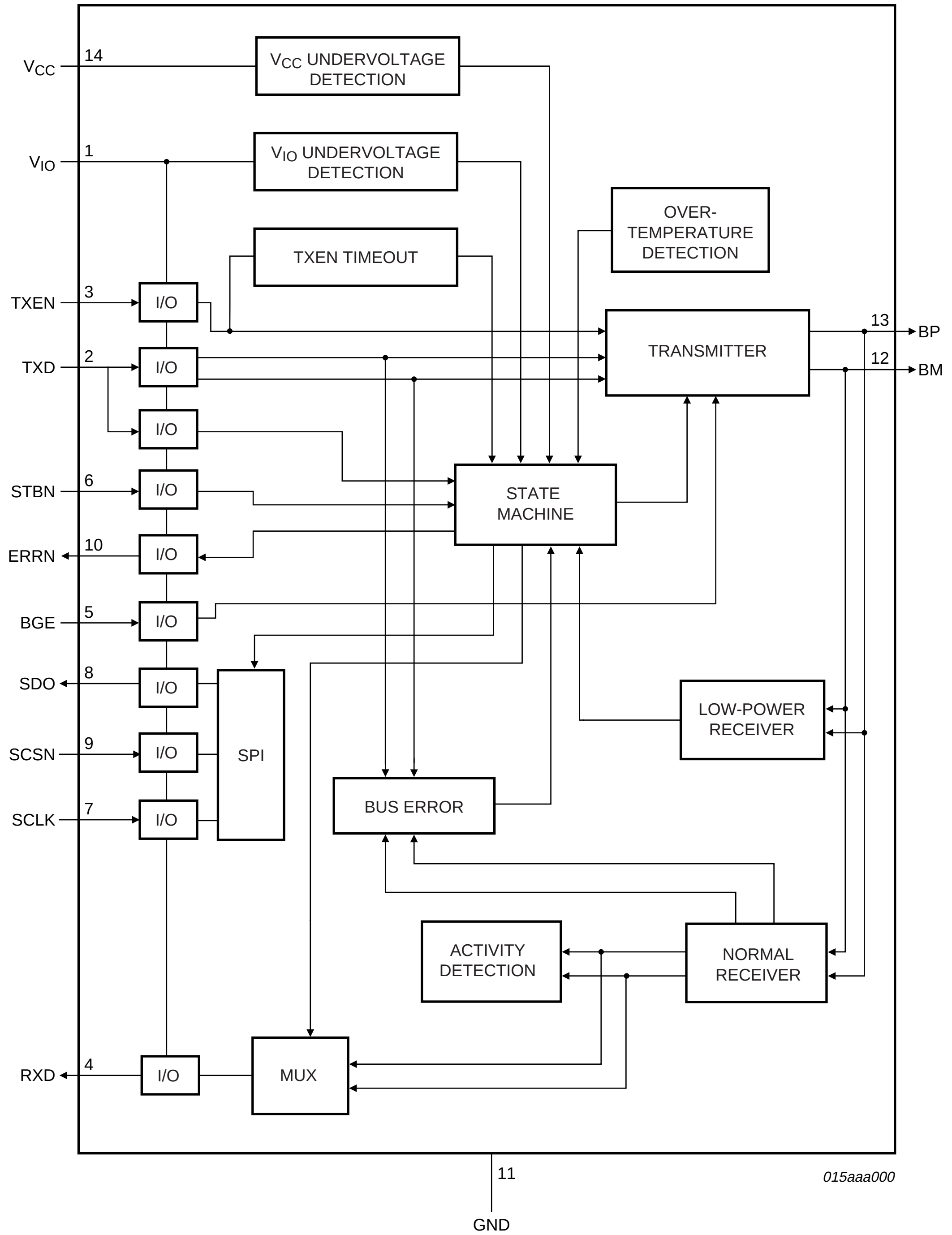


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

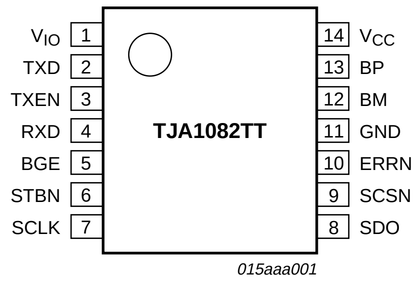


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
V_{IO}	1	P	supply voltage for V_{IO} voltage level adaptation
TXD	2	I	transmit data input; internal pull-down
TXEN	3	I	transmitter enable input; when HIGH transmitter disabled; internal pull-up
RXD	4	O	receive data output
BGE	5	I	bus guardian enable input; when LOW transmitter disabled; internal pull-down
STBN	6	I	mode control input; transceiver in Normal mode when HIGH; internal pull-down
SCLK	7	I	SPI clock signal; internal pull-up
SDO	8	O	SPI data output
SCSN	9	I	SPI chip select input; internal pull-up/pull-down
ERRN	10	O	error diagnosis output and wake-up indication
GND	11	P	ground
BM	12	I/O	bus line minus
BP	13	I/O	bus line plus
V_{CC}	14	P	supply voltage (+5 V)

6. Functional description

6.1 Power modes

The TJA1082 features three power modes: Normal, Standby and Power-off. Normal and Standby modes can be selected via the STBN input (HIGH for Normal mode) once the transceiver has been powered up. See Table 3 for a detailed description of pin signaling in the three power modes.

Table 3. Pin signalling in the different power modes

Mode	STBN	UV at V_{IO}	UV at V_{CC}	ERRN LOW	ERRN HIGH	RXD LOW	RXD HIGH	SDO	Biasing BP, BM	UV-det	Trans-mitter	Low-power receiver
Normal	HIGH	no	no	error flag set	error flag reset	bus DATA_0	bus DATA_1 or idle	high-impedance (in simple error indication mode) or enabled (in SPI mode)	V_{CC} / 2	enabled	enabled	enabled[1]
Standby	LOW	no	no	wake flag set	wake flag reset	wake flag set	wake flag reset		GND		disabled	enabled[2]
	LOW	no	yes[3]	wake flag set[4]	wake flag reset[4]	wake flag set[4]	wake flag reset[4]					disabled
	HIGH	no	yes[3]	error flag set	error flag reset	wake flag set[4]	wake flag reset[4]					
	X	yes[5]	no	LOW		LOW		high-impedance				enabled[2]
	X	yes[5]	yes[3]	LOW		LOW						disabled
Power-off[6]	X	X[5]	yes	high-impedance		HIGH			GND[7]	disabled		disabled

[1] The wake flag is set if a valid wake-up event is detected while switching to Standby mode.

[2] The wake flag is set if a valid wake-up event is detected.

[3] $V_{uvd(VCC)} > V_{CC} > V_{th(det)POR}$.

[4] Pins ERRN and RXD will reflect the state of the wake flag prior to the undervoltage event.

[5] The internal signals at pins STBN, BGE and TXD are set LOW; the internal signals at pins TXEN, SCLK and SCSN are set HIGH.

[6] $V_{CC} < V_{th(rec)POR}$ at power-up and $V_{CC} < V_{th(det)POR}$ at power-down (see Figure 6 and Figure 7).

[7] Except when V_{CC} = 0; in this case the biasing of BP and BM is floating.

6.1.1 Normal mode

In Normal mode, the transceiver transmits and receives data via the bus lines BP and BM. The transmitter and the normal receiver are enabled, along with the undervoltage detection function. The timing diagram for Normal mode is illustrated in Figure 3.

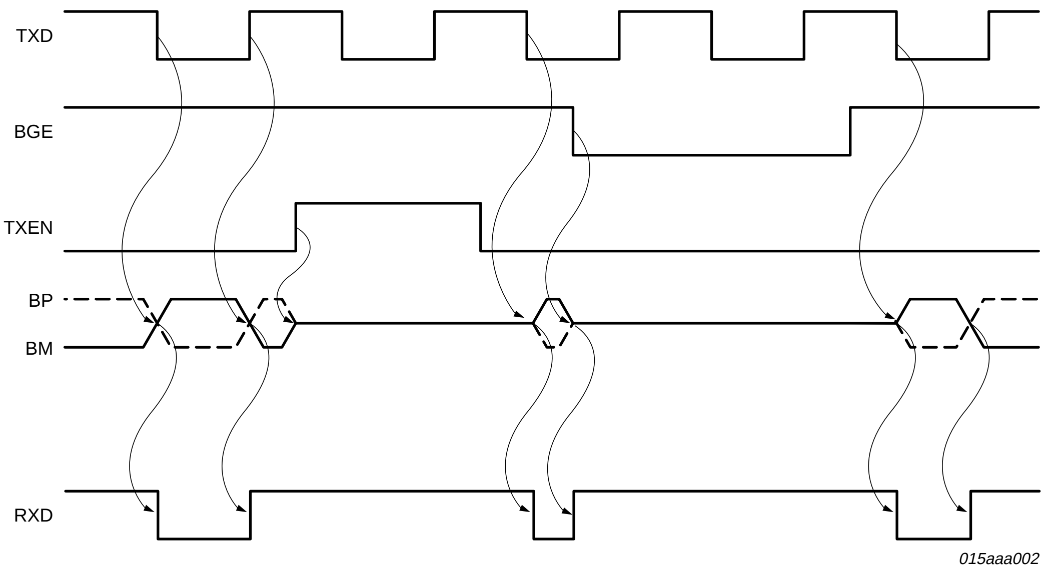


Fig 3. Timing diagram in Normal mode

Table 4 describes the behavior of the transmitter in Normal mode, when the temperature flag (TEMP HIGH) is not set and with no time-out on pin TXEN. Transmitter behavior is illustrated in Figure 14.

Table 4. Transmitter operation in Normal mode

BGE	TXEN	TXD	Bus state	Transmitter
L	X	X	idle	transmitter is disabled
X	H	X	idle	transmitter is disabled
H	L	H	DATA_1	transmitter is enabled; the bus lines are actively driven; BP is driven HIGH and BM is driven LOW
H	L	L	DATA_0	transmitter is enabled; the bus lines are actively driven; BP is driven LOW and BM is driven HIGH

The transmitter is activated during the first LOW level on pin TXD while pin BGE is HIGH and pin TXEN is LOW.

In Normal mode, the normal receiver output is connected directly to pin RXD (see Table 5). Receiver behavior is illustrated in Figure 15.

Table 5. Behavior of normal receiver in Normal mode

Bus state	RXD
DATA_0	L
DATA_1	H
idle	H

When V_{IO} and V_{CC} are within their operating ranges, pin ERRN indicates the status of the error flag. See Section 6.7 for a detailed description of error signalling in Normal mode.

6.1.1.1 Bus activity and idle detection

In Normal mode, bus activity and bus idle are detected as follows:

- Bus activity is detected when the absolute differential voltage on the bus lines is higher than $|V_{i(dif)det(act)}|$ for $t_{det(act)(bus)}$:
  - If the differential voltage on the bus lines is higher than $V_{IH(dif)}$ after bus activity has been detected, pin RXD goes HIGH.
  - If the differential voltage on the bus lines is lower than $V_{IL(dif)}$ after bus activity has been detected, pin RXD goes LOW.
- Bus idle is detected when the absolute differential voltage on the bus lines is lower than $|V_{i(dif)det(act)}|$ for $t_{det(idle)(bus)}$. This results in pin RXD being switched HIGH or staying HIGH.

6.1.2 Standby mode

Standby mode is a low-power mode featuring very low current consumption. In Standby mode, the transceiver is unable to transmit or receive data since both the transmitter and the normal receiver are switched off. The low-power receiver is activated to monitor the bus for wake-up activity, provided an undervoltage has not been detected on pin V_{CC}.

The low power receiver is deactivated if an undervoltage is detected on pin V_{CC} - with the result that the wake flag will not be set if a wake-up pattern or dedicated data frame is received.

Pins ERRN and RXD indicate the status of the wake flag when V_{IO} and V_{CC} are within their operating ranges. See Table 3 for a description of pins ERRN and RXD when an undervoltage is detected on pin V_{IO} or pin V_{CC}.

The status register cannot be read via the SPI interface if an undervoltage is detected on pin V_{IO}.

The BGE input has no effect In Standby mode.

6.1.3 Power-off mode

The transmitter and the two receivers (normal and low-power) are deactivated in Power-off mode. As a result, the wake flag will not be set if a wake-up pattern or dedicated data frame is received. If the voltage at V_{CC} rises above $V_{th(rec)POR}$, the transceiver switches to Standby mode and the digital section is reset. If V_{CC} subsequently drops below $V_{th(det)POR}$, the transceiver reverts to Power-off mode (see Section 6.2).

The status register cannot be read via the SPI interface in Power-off mode.

6.1.4 State transitions

Figure 4 shows the TJA1082 state transition diagram. The timing diagram for the ERRN indication signal during transitions between Normal and Standby modes, when the error flag is set and the wake flag is not set, is illustrated in Figure 5 and described in Table 6.

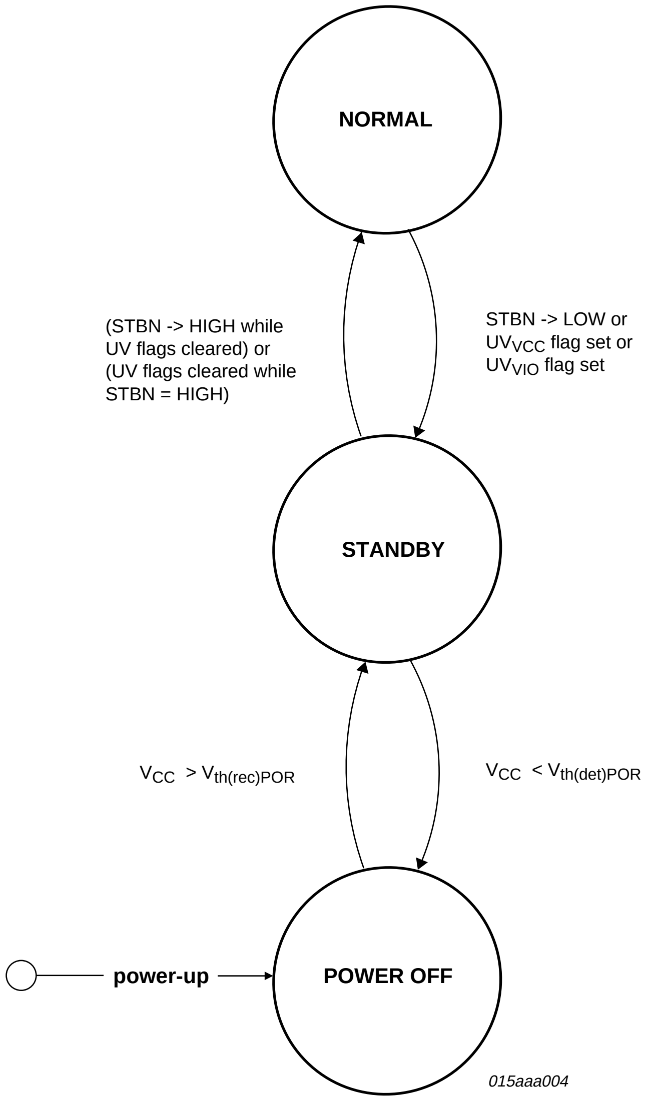


Fig 4. State transitions diagram

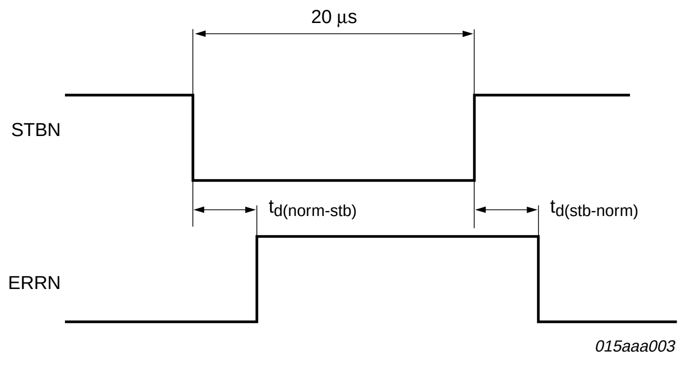


Fig 5. State transitions timing (bus error flag set)

Table 6. State transitions

→ indicates the action that initiates a transaction; →1 and →2 are the consequences of a transaction.

Transition	UVV_{IO} flag[1]	UVV_{CC} flag[1]	wake flag[1]	PWON flag[1]	STBN	VCC level
Normal to Standby	cleared	cleared	cleared	cleared	→ L	$V_{CC} > V_{uvd(VCC)}$
	→ set	cleared	cleared	cleared	H	$V_{CC} > V_{uvd(VCC)}$
	cleared	→ set	cleared	cleared	H	$V_{uvd(VCC)} > V_{CC} > V_{th(det)POR}$
Standby to Normal	cleared	cleared	1 → cleared	2 → cleared	→ H	$V_{CC} > V_{uvd(VCC)}$
	→ cleared	cleared	1 → cleared	2 → cleared	H	$V_{CC} > V_{uvd(VCC)}$
	cleared	→ cleared	1 → cleared	2 → cleared	H	$V_{uvd(VCC)} > V_{CC} > V_{th(det)POR}$
Standby to Power-off	X	set	X	X	X	→ $V_{CC} < V_{th(det)POR}$
Power-off to Standby	X	set	X	1 → set	X	→ $V_{CC} > V_{th(rec)POR}$

[1] See Table 7 for set and reset conditions of all flags.

6.2 Power-up and power-down behavior

6.2.1 Power-up

The TJA1082 has two supply pins: V_{CC} (+5 V) and V_{IO} (for the voltage level adaptation). The ramp up of the different power supplies can vary, depending on the state or value of a number of signals and parameters.The power-up behavior of the TJA1082 is not affected by the sequence in which power is supplied to these pins or by the voltage ramp up.

As an example, Figure 6 shows one possible power supply ramp-up scenario. The digital section of the TJA1082 is supplied by V_{CC}. The voltage on pin V_{CC} ramps up before the voltage on pin V_{IO}. As long as the voltage on V_{CC} remains below the power-on reset recovery threshold, $V_{th(rec)POR}$, the internal state machine will not be active and the transceiver will be totally passive, remaining in Power-off mode. As soon as the voltage crosses the $V_{th(rec)POR}$ threshold, the internal state machine starts running, setting the PWON flag and switching the TJA1082 to Standby mode. This initializes the V_{CC} and V_{IO} under-voltage flags to the set state (since both V_{CC} and V_{IO} are actually in undervoltage state just after power-on).

Once both V_{IO} and V_{CC} have reached their operating ranges in Standby mode (above $V_{uvd(VIO)}$ and $V_{uvd(VCC)}$ respectively), the under-voltage flags are reset and the transceiver enters the mode indicated by STBN (Normal or Standby).

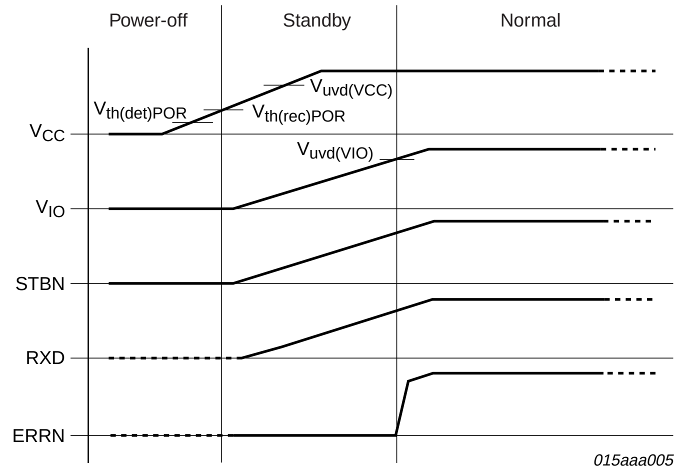


Fig 6. Power-up behavior (example)

6.2.2 Power-down

The behavior of the TJA1082 during power-down is illustrated in Figure 7.

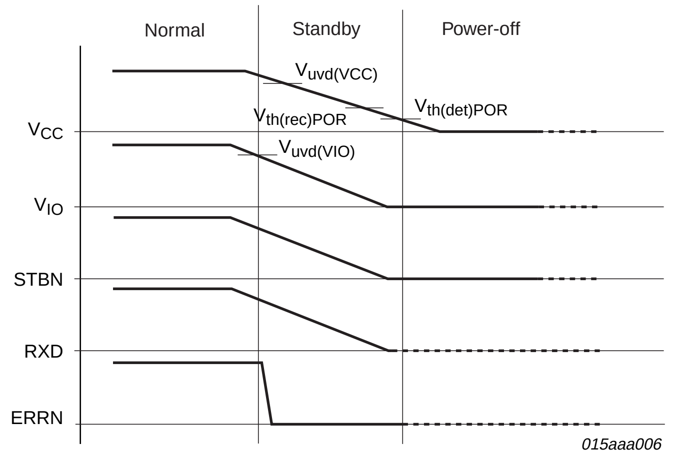


Fig 7. Power-down behavior (example)

6.3 Remote wake-up

6.3.1 Bus wake-up via wake-up pattern

A valid remote wake-up event occurs when a wake-up pattern is received. A wake-up pattern consists of at least two consecutive wake-up symbols. A wake-up symbol consists of a DATA_0 phase lasting longer than $t_{det(wake)}$, followed by an idle phase lasting longer than $t_{det(wake)idle}$, provided both wake-up symbols occur within a time span of $t_{det(wake)tot}$ (see Figure 8). The transceiver will also wake up if the idle phases are replaced by DATA_1 phases.

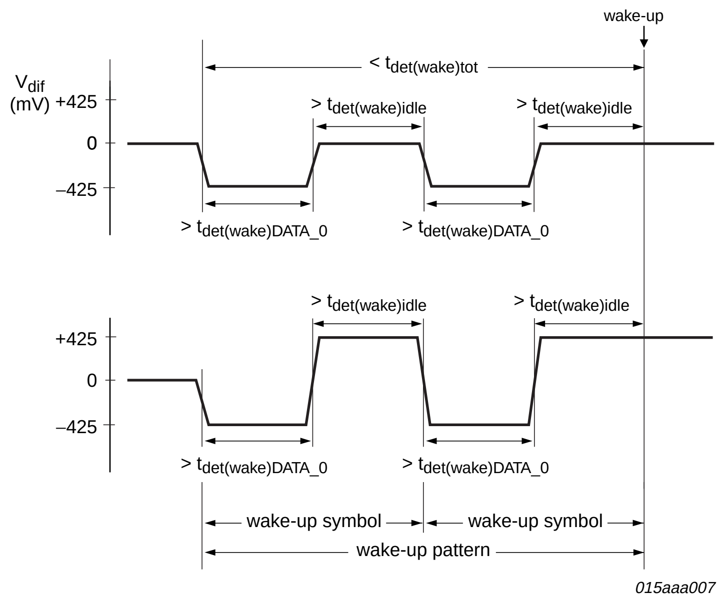


Fig 8. Bus wake-up timing

The wake-up mechanism of the TJA1082 follows the state transition diagram shown in Figure 9. See Ref. 1 for more details of the wake-up mechanism.

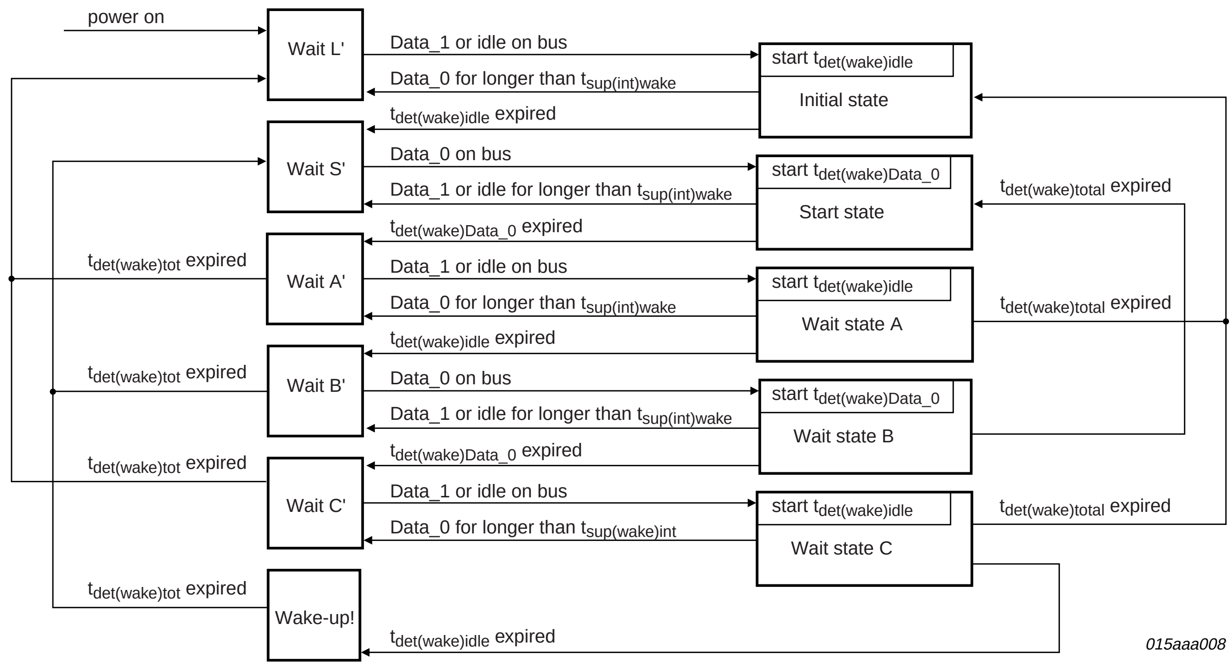


Fig 9. Wake-up state machine

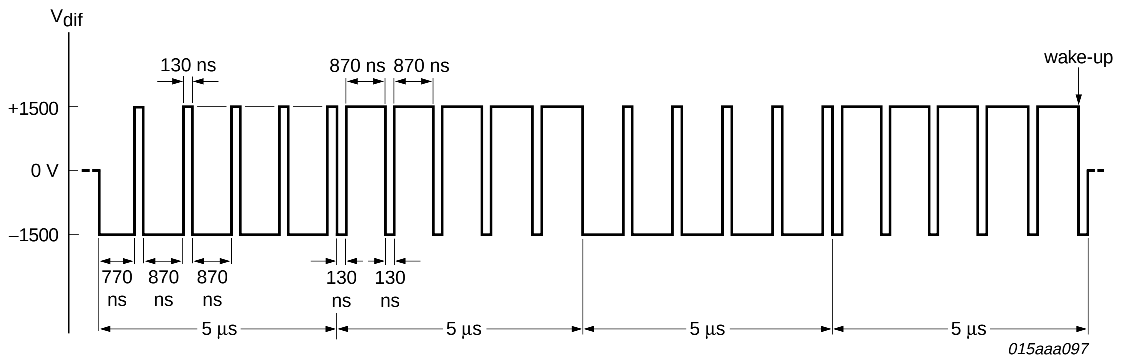
6.3.2 Bus wake-up via dedicated FlexRay data frame

The TJA1082 wake flag is set when a dedicated data frame emulating a valid wake-up pattern, as shown in Figure 10, is received.

The Data_0 and Data_1 phases of the emulated wake-up symbol are interrupted by the Byte Start Sequence (BSS) preceding each byte in the data frame. With a data rate of 10 Mbit/s, the interruption will have a maximum duration of 130 ns and will not prevent the transceiver from recognizing the wake-up pattern in the payload.

For longer interruptions at lower data rates (5 Mbit/s and 2.5 Mbit/s), the wake-up pattern should be used (see Section 6.3.1).

The wake flag will not be set if an invalid wake-up pattern is received. See Ref. 1 for more details on invalid wake-up patterns.



The duration of each interruption is 130 ns.

The transition time from DATA_0 to DATA_1 and vice versa is about 20 ns.

The TJA1082 wake-up flag is set on receipt of the following frame payload:

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

Fig 10. Minimum bus pattern for bus wake-up via dedicated FlexRay data frame

6.4 Bus error detection

The TJA1082 detects the following bus errors during transmission:

- Short-circuit BP-BM at the ECU connector or on the bus
- Short-circuit BP-GND at the ECU connector or on the bus
- Short-circuit BM-GND at the ECU connector or on the bus
- Short-circuit BP-V_{CC} at the ECU connector or on the bus
- Short-circuit BM-V_{CC} at the ECU connector or on the bus

The bus error flag is not set when a wake-up pattern or a FlexRay Collision Avoidance Symbol (CAS) is being transmitted or received.

6.5 Fail silent behavior

Three mechanisms guarantee the ‘fail silent’ behavior of the TJA1082:

- The TXEN Clamped flag is set if pin TXEN goes LOW for longer than $t_{detCL(TXEN)}$ in Normal mode; the transmitter will be disabled.
- The BGE Clamped flag is set if pin BGE goes HIGH for longer than $t_{detCL(BGE)}$ in Normal mode; no action will be taken.
- If a loss-of-ground occurs at the transceiver, resulting in the TJA1082 switching to Power-off mode, no current will flow out of the digital input pins (TXD, TXEN, BGE, STBN, SCLK, SCSN); see Table 3 for details of the behavior of the bus pins.

6.6 TJA1082 flags and Status Register

The TJA1082 has 11 status/error flags. These are described in Table 7.

Table 7. TJA1082 flags and set/reset conditions

Flag name	Flag type	Flag description	Set condition	Reset condition[1]	Consequence of flag set
bus wake	status flag	indicates if a wake-up event has occurred	wake-up event on bus in Standby mode[2]	transition to Normal mode	RXD → LOW; ERRN → LOW [3]
Normal mode	status flag	indicates if the transceiver is in Normal mode	entering Normal mode	leaving Normal mode	-
transmitter enabled	status flag	indicates the transmitter status	transmitter enabled[4]	transmitter disabled	-
BGE clamped	status flag	indicates if pin BGE is clamped	BGE HIGH for longer than $t_{detCL(BGE)}$[5]	BGE LOW[5]	-
PWON	status flag	indicates when the digital section is initialized	$V_{CC} > V_{th(rec)POR}$	transition to Normal mode	-
bus error	error flag	indicates if a bus error has been detected	bus error detected[5]	no bus error detected or positive edge on TXEN[5]	ERRN → LOW [6]
TEMP HIGH	error flag	indicates if the max. junction temperature has been reached	$T_{vj} > T_{j(dis)(high)}$[5]	TXEN = HIGH while $T_{vj} < T_{j(dis)(high)}$[5]	ERRN → LOW [6]; transmitter disabled
TXEN clamped	error flag	indicates if pin TXEN is clamped	TXEN LOW for longer than $t_{detCL(TXEN)}$[5]	TXEN = HIGH[5]	ERRN → LOW [6]; transmitter disabled
UVV_{CC}	error flag	indicates if there is an undervoltage at pin V_{CC}	$V_{CC} < V_{uvd(VCC)}$ for longer than $t_{det(uv)(VCC)}$	$V_{CC} > V_{uvd(VCC)}$ for longer than $t_{rec(uv)(VCC)}$	ERRN → LOW [6]; entering Standby mode
UVV_{IO}	error flag	indicates if there is an undervoltage at pin V_{IO}	$V_{IO} < V_{uvd(VIO)}$ for longer than $t_{det(uv)(VIO)}$	$V_{IO} > V_{uvd(VIO)}$ for longer than $t_{rec(uv)(VIO)}$	ERRN → LOW [6]; entering Standby mode
SPI error	error flag	indicates if an SPI error has occurred	SPI error detected[8]	falling edge on SCSN	ERRN → LOW [7]

[1] All flags, with the exception of the PWON flag, are reset after a power-on reset.

[2] If an undervoltage has not been detected on pin V_{CC}.

[3] If STBN = LOW.

[4] If BGE = HIGH, the Normal mode flag is set, the TEMP HIGH flag is not set and the TXEN clamped flag is not set.

[5] Flag can only be set or reset in Normal mode or on leaving Normal mode.

[6] If STBN = HIGH.

[7] If STBN = HIGH in SPI mode

[8] The SPI error flag is set when:

a) more than 16 falling edges occur on pin SCLK while pin SCSN = LOW

b) less than 16 falling edges occur on pin SCLK while pin SCSN = LOW.

The TJA1082 contains a 16-bit status register, of which bits S0 to S4 reflect the state of the status flags, bits S5 to S10 reflect the state of the error flags and bit S15 is a parity bit. All flags can be individually read out on pin SDO via a 16-bit SPI interface when the transceiver is configured in SPI mode. The status register bits are described in Table 8.

Table 8. TJA1082 status register

Status bit	Flag name	Set condition	Reset condition
S0	bus wake	bus wake flag set	bus wake flag cleared
S1	Normal mode	Normal mode flag set	Normal mode flag cleared
S2	transmitter enabled	transmitter enabled flag set	transmitter enabled flag cleared
S3	BGE clamped	BGE clamped flag set	BGE clamped flag cleared
S4	PWON	PWON flag set	PWON flag cleared and successful readout[1]
S5	bus error	bus error flag set	bus error flag cleared and successful readout[1]
S6	TEMP HIGH	TEMP HIGH flag set	TEMP HIGH flag cleared and successful readout[1]
S7	TXEN clamped	TXEN clamped flag set	TXEN clamped flag cleared and successful readout[1]
S8	UVV_{CC}	UVV_{CC} flag set	UVV_{CC} flag cleared and successful readout[1]
S9	UVV_{IO}	UVV_{IO} flag set	UVV_{IO} flag cleared and successful readout[1]
S10	SPI error	SPI error flag set	SPI error flag cleared and successful readout[1]
S11	reserved	always LOW	
S12	reserved	always HIGH	
S13	reserved	always LOW	
S14	reserved	always HIGH	
S15	parity bit	odd parity of status bits	even parity of status bits

[1] Also cleared during Power-off.

6.7 Error signalling

The TJA1082 provides two modes for error indication:

- Simple error indication mode
- SPI mode (default mode)

SPI mode is active on power-up.

To switch to simple error indication mode, SCSN has to be held LOW (connected to GND) and SCLK held HIGH (connected to V_{IO}) for longer than $t_{det(L)(SCLK)}$ (provided an undervoltage has not occurred).

When the TJA1082 is in simple error indication mode, a rising edge on SCSN initiates a transition to SPI mode (provided an undervoltage has not occurred).

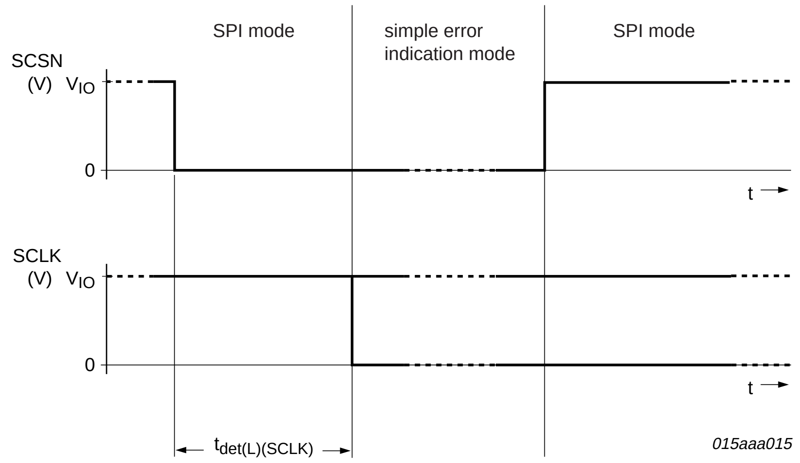


Fig 11. State transitions timing (bus error flag set)

If an undervoltage condition is detected, it will not be possible to switch between SPI mode and simple error indication mode.

6.7.1 SPI mode

The error flag information in the status register is latched in SPI mode. This means that the status bit is reset once the status register has been completely read out (provided the corresponding error flag has been reset). If an error condition is detected in Normal mode, pin ERRN goes LOW (provided one of the error bits, S5-S10, is set). Pin ERRN goes HIGH again once all the error bits (S5-S10) have been reset.

6.7.2 Simple error indication mode

If an error condition is detected in Normal mode, pin ERRN goes LOW once the relevant error flag has been set. Pin ERRN goes HIGH again when all error conditions have been cleared and all flags have been reset. Error flags are not latched. It is not possible to read-out the status bits in this mode.

6.8 SPI interface

The TJA1082 includes a 16-bit SPI interface to enable a host to read the status register when the transceiver is in SPI mode (see Section 6.7).

While pin SCSN is HIGH, the SDO output will be in a high-impedance state. To begin a status register readout, the host must force pin SCSN LOW. This will cause the SDO pin to output a LOW level by default. The data at pin SDO is then shifted out on the rising edge of the clock signal on pin SCLK.

The status bits shifted out at SDO are active HIGH. The status bits are refreshed and pin SDO returned to a high-impedance state once the status register has been read successfully (after exactly 16 clock cycles) and SCSN has been forced HIGH again. Clock signals on SCLK will be ignored while SCSN is HIGH. The timing diagram for the SPI readout is illustrated in Figure 12.

The SLCK period ranges from 500 ns to100 µs (10 kbit/s to 2 Mbit/s)

If SCSN remains LOW for longer than 16 clock cycles, it recognized as an SPI error. When this happens, the SPI error flag is set and pin SDO goes to a high-impedance state until the next falling edge on pin SCSN.

An SPI error will also be assumed if fewer than 16 clock cycles are received while SCSN is LOW. If this happens, the SPI error flag will be set.

All status bits will be refreshed once the status register has been successfully read.

When the transceiver is in simple error indication mode the SDO output will be in a high-impedance state and pin SCSN will be in pull-down mode. In SPI mode pin SCSN will be in pull-up mode.

SPI readout is not possible when the transceiver has detected an undervoltage on V_{IO}.

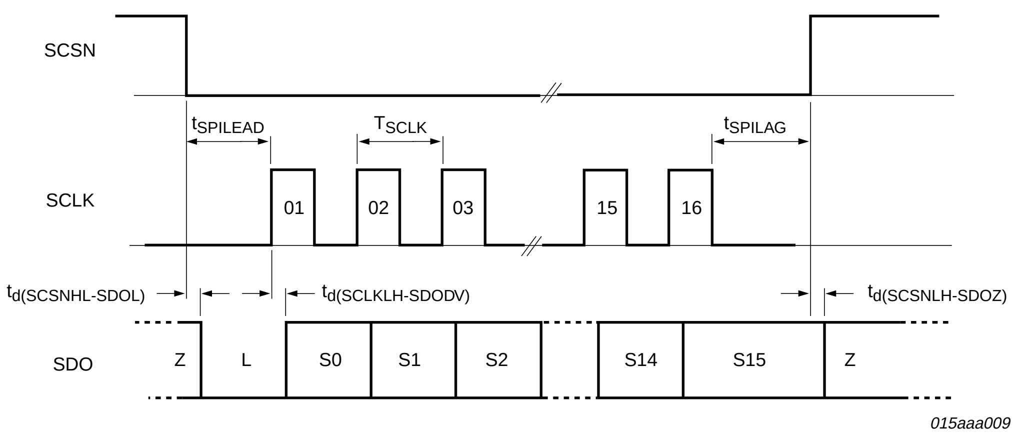


Fig 12. SPI readout timing diagram

7. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	no time limit	–0.3	+5.5	V
		operating range	4.75	5.25	V
V_{IO}	supply voltage on pin V_{IO}	no time limit	–0.3	+5.5	V
		operating range	2.8	5.25	V
V_{ERRN}	voltage on pin ERRN	no time limit	–0.3	V_{IO} + 0.3	V
V_{RXD}	voltage on pin RXD	no time limit	–0.3	V_{IO} + 0.3	V
V_{SDO}	voltage on pin SDO	no time limit	–0.3	V_{IO} + 0.3	V
V_{TXEN}	voltage on pin TXEN	no time limit	–0.3	+5.5	V
V_{TXD}	voltage on pin TXD	no time limit	–0.3	+5.5	V
V_{STBN}	voltage on pin STBN	no time limit	–0.3	+5.5	V
V_{SCSN}	voltage on pin SCSN	no time limit	–0.3	+5.5	V
V_{SCLK}	voltage on pin SCLK	no time limit	–0.3	+5.5	V
V_{BGE}	voltage on pin BGE	no time limit	–0.3	+5.5	V

Table 9. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BP}	voltage on pin BP	no time limit (with respect to pins BM and GND)		–60	+60	V
V_{BM}	voltage on pin BM	no time limit (with respect to pins BP and GND)		–60	+60	V
$I_{I(ERRN)}$	input current on pin ERRN	no time limit; V_{IO} = 0 V		–10	10	mA
$I_{I(RXD)}$	input current on pin RXD	no time limit; V_{IO} = 0 V		–10	10	mA
$I_{I(SDO)}$	input current on pin SDO	no time limit; V_{IO} = 0 V		–10	10	mA
V_{trt}	transient voltage	on pins BP and BM	[1]	–200	+200	V
T_{stg}	storage temperature			–55	+150	°C
T_{vj}	virtual junction temperature		[2]	–40	+150	°C
V_{ESD}	electrostatic discharge voltage	IEC61000-4-2 on pins BP and BM to ground	[3]	–8.0	+8.0	kV
		HBM on pins BP and BM to ground	[4]	–8.0	+8.0	kV
		HBM on any other pin	[4]	–4.0	+4.0	kV
		MM on all pins	[5]	–200	+200	V
		CDM on all pins	[6]	–1000	+1000	V

[1] According to ISO 7637, part 3 test pulses a and b; Class C; see Figure 17; R_{bus} = 45 Ω; C_{bus} = 100 pF.

[2] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature T_{vj} is: $T_{vj} = T_{amb} + TD \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[3] IEC61000-4-2: C = 150 pF; R = 330 Ω.

[4] HBM: C = 100 pF; R = 1.5 kΩ.

[5] MM: C = 200 pF; L = 0.75 µH; R = 10 Ω.

[6] CDM: R = 1 Ω.

8. Thermal characteristics

Table 10. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	130	K/W

9. Static characteristics

Table 11. Static characteristics

All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = –40 °C to +150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Pin V_{CC}						
I_{CC}	supply current	Standby mode with no undervoltage; $T_{vj} \leq 85$ °C	-	20	30	µA
		Standby mode with no undervoltage; $T_{vj} \leq 150$ °C	-	20	40	µA
		Power-off mode; $T_{vj} \leq 85$ °C	-	20	30	µA
		Power-off mode; $T_{vj} \leq 150$ °C	-	20	40	µA
		Normal mode; V_{BGE} = 0 V or $V_{TXEN} = V_{IO}$	-	-	15	mA
		Normal mode; $V_{BGE} = V_{IO}$; V_{TXEN} = 0 V; $R_{bus} \geq 45$ Ω	-	-	35	mA
		Normal mode; $V_{BGE} = V_{IO}$; V_{TXEN} = 0; V; R_{bus} > 10 MΩ	-	-	15	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		4.5	-	4.724	V
$V_{uvr(VCC)}$	undervoltage recovery voltage on pin V_{CC}		4.525	-	4.749	V
$V_{uvhys(VCC)}$	undervoltage hysteresis voltage on pin V_{CC}		20	-	240	mV
$V_{th(det)POR}$	power-on reset detection threshold voltage		3.75	-	4.15	V
$V_{th(rec)POR}$	power-on reset recovery threshold voltage		3.85	-	4.25	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		100	-	500	mV
Pin V_{IO}						
I_{IO}	supply current on pin V_{IO}	Normal mode; $V_{TXEN} = V_{IO}$; $V_{BGE} = V_{IO}$; R_{RXD} > 10 MΩ	-	-	1000	µA
		Normal mode; V_{TXEN} = 0 V; $V_{BGE} = V_{IO}$; R_{RXD} > 10 MΩ	-	-	1000	µA
		Standby mode with no undervoltage	-	3	7	µA
		Power-off mode; V_{IO} = 5 V	-	3	7	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.6	-	2.779	V
$V_{uvr(VIO)}$	undervoltage recovery voltage on pin V_{IO}		2.62	-	2.799	V
$V_{uvhys(VIO)}$	undervoltage hysteresis voltage on pin V_{IO}		20	-	190	mV
Pin SCSN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		–0.3	-	$0.3V_{IO}$	V

Table 11. Static characteristics *...continued*

All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = −40 °C to +150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	Simple error indication mode. $V_{SCSN} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	SPI mode; $V_{SCSN} = 0.3V_{IO}$	−15	-	−3	µA
I_r	reverse current	Power-off mode; to V_{CC} / V_{IO}; V_{SCSN} = 5 V; $V_{CC} = V_{IO}$ = 0 V	−5	0	+5	µA
Pin SCLK						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{SCLK} = V_{IO}$	−1	0	+1	µA
I_{IL}	LOW-level input current	$V_{SCLK} = 0.3V_{IO}$	−15	-	−3	µA
I_r	reverse current	Power-off mode; to V_{CC} / V_{IO}; V_{SCLK} = 5 V; $V_{CC} = V_{IO}$ = 0 V	−5	0	+5	µA
Pin STBN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{STBN} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	V_{STBN} = 0 V	−1	0	+1	µA
I_r	reverse current	Power-off mode; to V_{CC} / V_{IO}; V_{STBN} = 5 V; $V_{CC} = V_{IO}$ = 0 V	−5	0	+5	µA
Pin TXEN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{TXEN} = V_{IO}$	−1	0	+1	µA
I_{IL}	LOW-level input current	$V_{TXEN} = 0.3V_{IO}$	−300	-	−50	µA
I_r	reverse current	Power-off mode; to V_{CC} / V_{IO}; V_{TXEN} = 5 V; $V_{CC} = V_{IO}$ = 0 V	−5	0	+5	µA
Pin BGE						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	5.5	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{BGE} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	V_{BGE} = 0 V	−1	0	+1	µA
I_r	reverse current	Power-off mode; to V_{CC} / V_{IO}; V_{BGE} = 5 V; $V_{CC} = V_{IO}$ = 0 V	−5	0	+5	µA
Pin TXD						
V_{IH}	HIGH-level input voltage	Normal mode	$0.7V_{IO}$	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage	Normal mode	−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_{TXD} = 0.7V_{IO}$	3	-	15	µA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	−1	0	+1	µA
I_r	reverse current	Power-off mode; to V_{CC} / V_{IO}; V_{TXD} = 5 V; $V_{CC} = V_{IO}$ = 0 V	−5	0	+5	µA

Table 11. Static characteristics *...continued*

All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = –40 °C to +150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_i	input capacitance	with respect to all other pins at ground; V_{TXD} = 100 mV; f = 5 MHz	[1]	-	-	10	pF
Pin RXD							
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO} - 0.4$ V; $V_{IO} = V_{CC}$		–15	-	–1.7	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V		2	-	20	mA
Pin ERRN							
I_{OH}	HIGH-level output current	$V_{ERRN} = V_{IO} - 0.4$ V; $V_{IO} = V_{CC}$		–1500	-	–100	µA
I_{OL}	LOW-level output current	V_{ERRN} = 0.4 V		200	-	1700	µA
I_L	leakage current	$V_{ERRN} \leq V_{IO}$; $V_{CC} < V_{th(det)POR}$		–5	-	+5	µA
Pin SDO							
I_{OH}	HIGH-level output current	$V_{SDO} = V_{IO} - 0.4$ V		–8	-	–0.5	mA
I_{OL}	LOW-level output current	V_{SDO} = 0.4 V		0.8	-	9	mA
I_L	leakage current	high-impedance state; 0 V < V_{SDO} < V_{IO}		–5	-	+5	µA
Pins BP and BM							
$V_{o(idle)(BP)}$	idle output voltage on pin BP	Normal mode; $V_{TXEN} = V_{IO}$; R_{bus} = 45 Ω		$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
		Standby mode with no undervoltage on pin V_{CC}		–0.1	0	+0.1	V
$V_{o(idle)(BM)}$	idle output voltage on pin BM	Normal mode; $V_{TXEN} = V_{IO}$; R_{bus} = 45 Ω		$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
		Standby mode with no undervoltage on pin V_{CC}		–0.1	0	+0.1	V
$I_{o(idle)BP}$	idle output current on pin BP	Normal and Standby modes with no undervoltage; –60 V ≤ V_{BP} ≤ +60 V		–7.5	-	+7.5	mA
$I_{o(idle)BM}$	idle output current on pin BM	Normal and Standby modes with no undervoltage; –60 V ≤ V_{BM} ≤ +60 V		–7.5	-	+7.5	mA
$V_{o(idle)(dif)}$	differential idle output voltage	Normal mode; R_{bus} = 45 Ω		–25	0	+25	mV
$V_{OH(dif)}$	differential HIGH-level output voltage	Normal mode; 40 Ω ≤ R_{bus} ≤ 55 Ω; C_{bus} = 100 pF		600	-	1500	mV
$V_{OL(dif)}$	differential LOW-level output voltage	Normal mode; 40 Ω ≤ R_{bus} ≤ 55 Ω; C_{bus} = 100 pF		–1500	-	–600	mV
$V_{IH(dif)}$	differential HIGH-level input voltage	Normal mode; –10 V ≤ V_{BP} ≤ +15 V –10 V ≤ V_{BM} ≤ +15 V		150	225	300	mV
$V_{IL(dif)}$	differential LOW-level input voltage	Normal mode; –10 V ≤ V_{BP} ≤ +15 V –10 V ≤ V_{BM} ≤ +15 V		–300	–225	–150	mV
		Standby mode with no undervoltage on pin V_{CC}; –10 V ≤ V_{BP} ≤ +15 V; –10 V ≤ V_{BM} ≤ +15 V		–400	–225	–125	mV
$\|V_{i(dif)det(act)}\|$	activity detection differential input voltage (absolute value)			150	225	300	mV

Table 11. Static characteristics *…continued*

All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = −40 °C to +150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\|I_{O(sc)}\|$	short-circuit output current (absolute value)	on pin BP; −5 V ≤ V_{BP} ≤ +60 V		-	-	35	mA
		on pin BM; −5 V ≤ V_{BM} ≤ +60 V		-	-	35	mA
		on pins BP and BM; V_{BP} = V_{BM}; −5 V ≤ V_{BP} ≤ +60 V; −5 V ≤ V_{BM} ≤ +60 V		-	-	35	mA
$R_{i(BP)}$	input resistance on pin BP	R_{bus} = ∞ Ω		10	20	40	kΩ
$R_{i(BM)}$	input resistance on pin BM	R_{bus} = ∞ Ω		10	20	40	kΩ
$R_{i(dif)(BP-BM)}$	differential input resistance between pin BP and pin BM	R_{bus} = ∞ Ω		20	40	80	kΩ
$I_{LI(BP)}$	input leakage current on pin BP	Power-off mode; V_{CC} = V_{IO} = 0 V; 0 V ≤ V_{BP} ≤ 5 V		−5	0	+5	μA
		loss of ground; V_{BP} = V_{BM} = 0 V; all other pins connected to 16 V via 0 Ω	[1]	−1600	-	+1600	μA
$I_{LI(BM)}$	input leakage current on pin BM	Power-off mode; V_{CC} = V_{IO} = 0 V; 0 V ≤ V_{BM} ≤ 5 V		−5	0	+5	μA
		loss of ground; V_{BP} = V_{BM} = 0 V; all other pins connected to 16 V via 0 Ω	[1]	−1600	-	+1600	μA
$V_{cm(bus)(DATA\_0)}$	DATA_0 bus common-mode voltage	Normal mode; R_{bus} = 45 Ω		$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
$V_{cm(bus)(DATA\_1)}$	DATA_1 bus common-mode voltage	Normal mode; R_{bus} = 45 Ω		$0.4V_{CC}$	$0.5V_{CC}$	$0.6V_{CC}$	V
$\Delta V_{cm(bus)}$	bus common-mode voltage difference	Normal mode; DATA_1 − DATA_0; R_{bus} = 45 Ω		−25	0	+25	mV
$\Delta V_{cm(act-idle)}$	active to idle common-mode voltage difference	Normal mode; R_{bus} = 45 Ω		−300	0	+300	mV
$\|\Delta V_{i(dif)(H-L)}\|$	differential input volt. diff. betw. HIGH- and LOW-levels (abs. value)	(V_{BP} + V_{BM})/2 = 2.5 V		-	-	10	%
$\Delta V_{i(dif)(H-L)}$	differential input voltage difference between HIGH-level and LOW-level	Normal mode; −10 V ≤ V_{BP} ≤ +15 V −10 V ≤ V_{BM} ≤ +15 V		-	-	60	mV
$C_{i(BP)}$	input capacitance on pin BP	with respect to all other pins at ground; V_{BP} = 100 mV; f = 5 MHz	[1]	-	-	15	pF
$C_{i(BM)}$	input capacitance on pin BM	with respect to all other pins at ground; V_{BM} = 100 mV; f = 5 MHz	[1]	-	-	15	pF
$C_{i(dif)(BP-BM)}$	differential input capacitance between pin BP and pin BM	with respect to all other pins at ground; V_{BP} = 100 mV V_{BM} = 100 mV; f = 5 MHz	[1]	-	-	5	pF
Temperature protection							
$T_{j(dis)(high)}$	high disable junction temperature			180	-	200	°C

[1] Guaranteed by design.

10. Dynamic characteristics

Table 12. Dynamic characteristics
All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = –40 °C to + 150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pins BP and BM							
$t_{d(TXD-bus)}$	delay time from TXD to bus	Normal mode	[1][2]				
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns
$\Delta t_{d(TXD-bus)}$	delay time difference from TXD to bus	Normal mode; between DATA_0 and DATA_1	[1][2]	–4	-	+4	ns
$t_{d(bus-RXD)}$	delay time from bus to RXD	Normal mode; C_{RXD} = 15 pF; $(V_{BP} + V_{BM})/2$ = 2.5 V	[3]				
		DATA_0		-	-	50	ns
		DATA_1		-	-	50	ns
		Normal mode; C_{RXD} = 25 pF; $(V_{BP} + V_{BM})/2$ = 2.5 V	[3]				
		DATA_0		-	-	60	ns
		DATA_1		-	-	60	ns
$\Delta t_{d(bus-RXD)}$	delay time difference from bus to RXD	Normal mode; between DATA_0 and DATA_1; $(V_{BP} + V_{BM})/2$ = 2.5 V	[3]				
		C_{RXD} = 15 pF		–5	-	5	ns
		C_{RXD} = 25 pF		–6	-	6	ns
$t_{d(TXEN-busidle)}$	delay time from TXEN to bus idle	Normal mode; V_{TXD} = 0 V		-	-	75	ns
$t_{d(TXEN-busact)}$	delay time from TXEN to bus active	Normal mode; V_{TXD} = 0 V		-	-	75	ns
$\lvert\Delta t_{d(TXEN-bus)}\rvert$	delay time difference from TXEN to bus (absolute value)	Normal mode; between TXEN to bus active and TXEN to bus idle; V_{TXD} = 0 V	[4]			50	ns
$t_{d(BGE-busidle)}$	delay time from BGE to bus idle	Normal mode; V_{TXD} = 0 V		-	-	75	ns
$t_{d(BGE-busact)}$	delay time from BGE to bus active	Normal mode; V_{TXD} = 0 V		-	-	75	ns
$t_{r(dif)(bus)}$	bus differential rise time	DATA_0 to DATA_1; 20 % to 80 %; R_{bus} = 45 Ω; C_{bus} = 100 pF	[5]	3.75	-	18.75	ns
$t_{f(dif)(bus)}$	bus differential fall time	DATA_1 to DATA_0; 80 % to 20 %; R_{bus} = 45 Ω; C_{bus} = 100 pF	[5]	3.75	-	18.75	ns
$\Delta t_{(r-f)(dif)}$	difference between differential rise and fall time	on bus; 80 % to 20 % R_{bus} = 45 Ω; C_{bus} = 100 pF	[5]	–3	-	3	ns
$t_{f(bus)(idle-act)}$	bus fall time from idle to active	bus idle to DATA_0; R_{bus} = 45 Ω; C_{bus} = 100 pF; –30 mV > V_{dif} > –300 mV	[5][6]	-	-	30	ns
$t_{f(bus)(act-idle)}$	bus fall time from active to idle	DATA_1 to bus idle; R_{bus} = 45 Ω; C_{bus} = 100 pF; 300 mV > V_{dif} > 30 mV	[5][6]	-	-	30	ns

Table 12. Dynamic characteristics *…continued*

All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = −40 °C to + 150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{r(bus)(act-idle)}$	bus rise time from active to idle	DATA_0 to bus idle; R_{bus} = 45 Ω; C_{bus} = 100 pF; −300 mV < V_{dif} < −30 mV	[5][6]	-	-	30	ns
Wake-up detection							
$t_{det(wake)DATA\_0}$	DATA_0 wake-up detection time	Standby mode with no undervoltage on pin V_{CC}; −10 V ≤ V_{BP} ≤ +15 V; −10 V ≤ V_{BM} ≤ +15 V	[7]	1	-	4	μs
$t_{det(wake)idle}$	idle wake-up detection time	Standby mode with no undervoltage on pin V_{CC}; −10 V ≤ V_{BP} ≤ +15 V; −10 V ≤ V_{BM} ≤ +15 V	[7]	1	-	4	μs
$t_{det(wake)tot}$	total wake-up detection time	Standby mode with no undervoltage on pin V_{CC}; −10 V ≤ V_{BP} ≤ +15 V; −10 V ≤ V_{BM} ≤ +15 V	[7]	50	-	115	μs
$t_{sup(int)wake}$	wake-up interruption suppression time	Standby mode with no undervoltage on pin V_{CC}; −10 V ≤ V_{BP} ≤ +15 V; −10 V ≤ V_{BM} ≤ +15 V	[8]	130	-	-	ns
Undervoltage							
$t_{det(uv)(VCC)}$	undervoltage detection time on pin V_{CC}	0 V ≤ V_{IO} ≤ 5.5 V; V_{CC} = 4.4 V		2	-	100	μs
$t_{rec(uv)(VCC)}$	undervoltage recovery time on pin V_{CC}	0 V ≤ V_{IO} ≤ 5.5 V; V_{CC} = 4.85 V		2	-	100	μs
$t_{det(uv)(VIO)}$	undervoltage detection time on pin V_{IO}	$V_{th(det)POR}$ < V_{CC} < 5.5 V; V_{IO} = 2.5 V		5	-	100	μs
$t_{rec(uv)(VIO)}$	undervoltage recovery time on pin V_{IO}	$V_{th(det)POR}$ < V_{CC} < 5.5 V; V_{IO} = 2.9 V		5	-	100	μs
Activity detection							
$t_{det(act)(bus)}$	activity detection time on bus pins	Normal mode; V_{dif}: 0 mV → 400 mV; (V_{BP} + V_{BM})/2 = 2.5 V	[6]	100	-	250	ns
$t_{det(idle)(bus)}$	idle detection time on bus pins	Normal mode; V_{dif}: 400 mV → 0 mV; (V_{BP} + V_{BM})/2 = 2.5 V	[6]	100	-	250	ns
$\|\Delta t_{det(act-idle)}\|$	active to idle detection time difference (absolute value)	Normal mode; on bus pins; (V_{BP} + V_{BM})/2 = 2.5 V		-	-	150	ns
ERRN signalling							
$t_{det(L)(SCLK)}$	LOW-level detection time on pin SCLK	Normal or Standby mode with no undervoltage on pin V_{IO}		95	-	310	μs
SPI							
$t_{d(SCSNHL-SDOL)}$	SCSN falling edge to SDO LOW-level delay time	$V_{uvd(VIO)}$ < V_{IO} < 5.5 V; 4.5 V < V_{CC} < 5.5 V; C_{SDO} = 50 pF	[9]	-	-	250	ns

Table 12. Dynamic characteristics *…continued*

All parameters are guaranteed for V_{CC} = 4.5 V to 5.25 V; V_{IO} = 2.6 V to 5.25 V; T_{vj} = –40 °C to + 150 °C and R_{bus} = 45 Ω unless otherwise specified. All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(SCLKLH-SDODV)}$	SCLK rising edge to SDO data valid delay time	$V_{uvd(VIO)} < V_{IO} < 5.5$ V; 4.5 V < V_{CC} < 5.5 V; C_{SDO} = 50 pF	[9]	-	-	200	ns
$t_{d(SCSNLH-SDOZ)}$	SCSN rising edge to SDO three-state delay time	$V_{uvd(VIO)} < V_{IO} < 5.5$ V; 4.5 V < V_{CC} < 5.5 V; C_{SDO} = 50 pF	[9]	-	-	500	ns
T_{SCLK}	SCLK period	$V_{uvd(VIO)} < V_{IO} < 5.5$ V; 4.5 V < V_{CC} < 5.5 V; C_{SDO} = 50 pF	[9]	0.5	-	100	µs
$t_{SPILEAD}$	SPI enable lead time	$V_{uvd(VIO)} < V_{IO} < 5.5$ V; 4.5 V < V_{CC} < 5.5 V; C_{SDO} = 50 pF	[9]	250	-	-	ns
t_{SPILAG}	SPI enable lag time	$V_{uvd(VIO)} < V_{IO} < 5.5$ V; 4.5 V < V_{CC} < 5.5 V; C_{SDO} = 50 pF	[9]	250	-	-	ns
RXD							
t_r	rise time	20 % to 80 %; C_{RXD} = 15 pF	[4]	-	-	5	ns
		20 % to 80 %; C_{RXD} = 25 pF	[4]	-	-	9	ns
t_f	fall time	80 % to 20 %; C_{RXD} = 15 pF	[4]	-	-	5	ns
		80 % to 20 %; C_{RXD} = 25 pF	[4]	-	-	9	ns
$\Delta t_{(r-f)}$	difference between rise and fall time	C_{RXD} = 15 pF	[4]	–4	-	4	ns
		C_{RXD} = 25 pF	[4]	–7	-	7	ns
Bus error flag							
$t_{d(norm-stb)}$	normal mode to standby delay time	bus error flag set		3	-	10	µs
$t_{d(stb-norm)}$	standby to normal mode delay time	bus error flag set		3	-	10	µs
Miscellaneous							
$t_{detCL(TXEN)}$	TXEN clamp detection time	4.5 V < V_{CC} < 5.5 V		1500	-	2600	µs
$t_{detCL(BGE)}$	BGE clamp detection time	4.5 V < V_{CC} < 5.5 V		1500	-	2600	µs

[1] Rise and fall time (10 % to 90 %) of $t_{r(TXD)}$ and $t_{f(TXD)}$ = 5 ±1 ns.

[2] See Figure 14.

[3] See Figure 15.

[4] Guaranteed by design.

[5] See Figure 17.

[6] $V_{dif} = V_{BP} - V_{BM}$.

[7] See Figure 8.

[8] See Figure 10.

[9] See Figure 12.

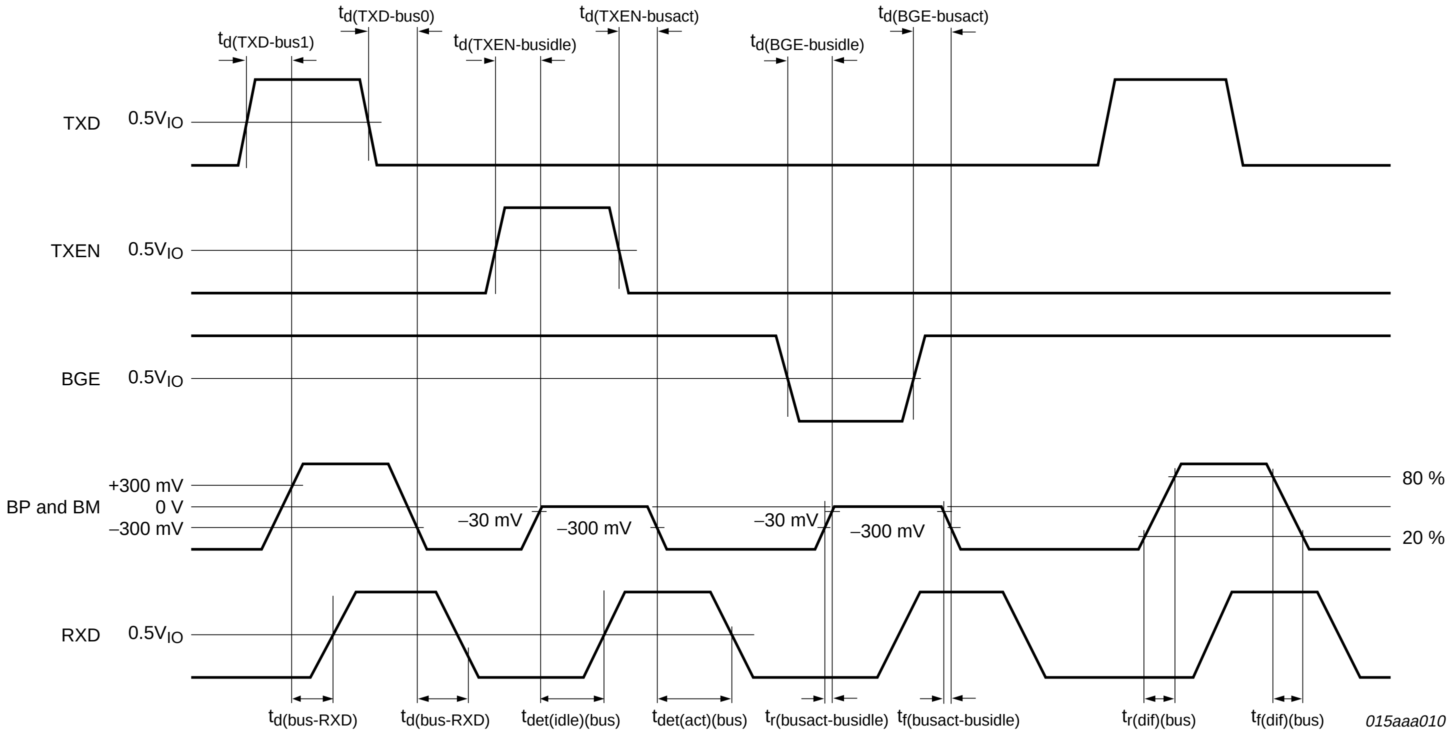
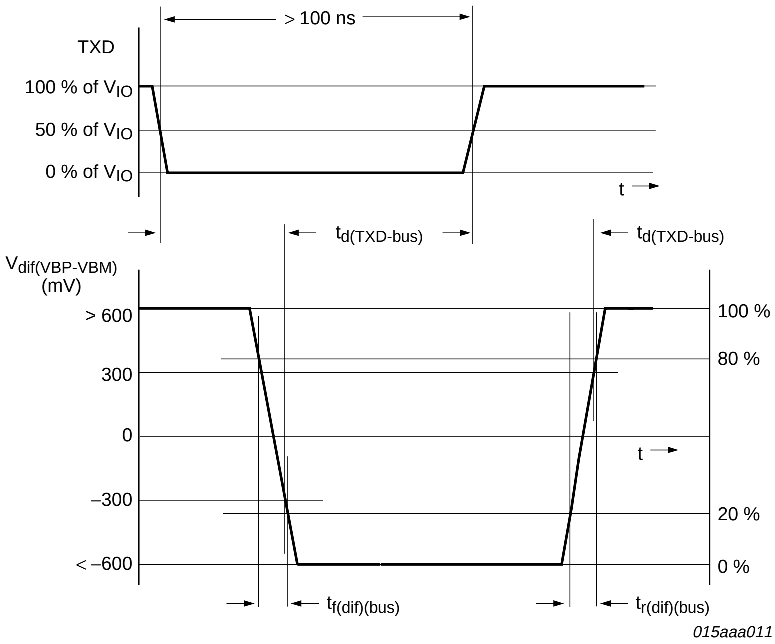
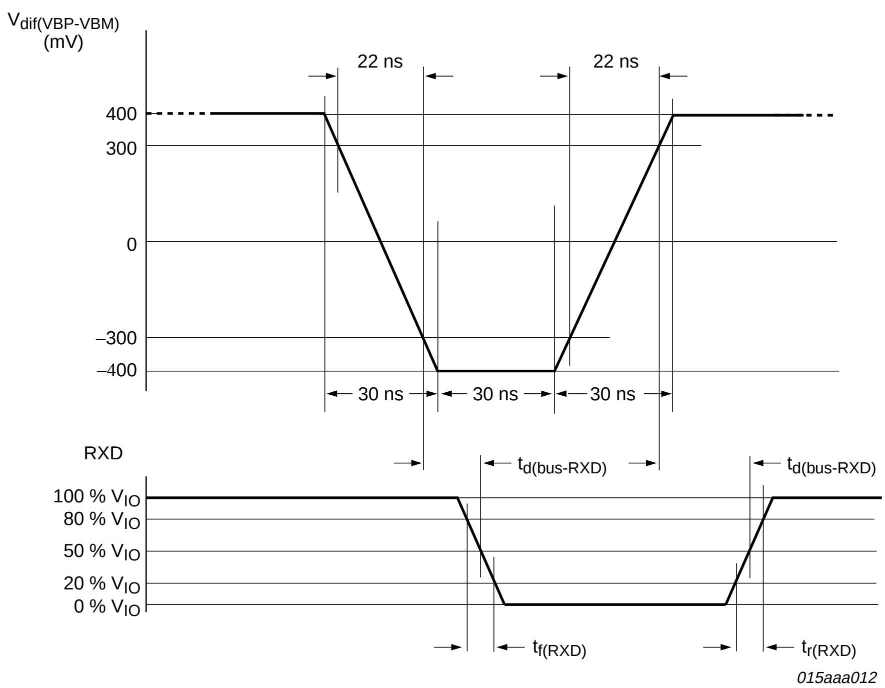


Fig 13. Detailed timing diagram



V_{dif} is the transmitter test signal.

Fig 14. Transmitter timing diagram



V_{dif} is the receiver test signal.

Fig 15. Normal receiver timing diagram

11. Test information

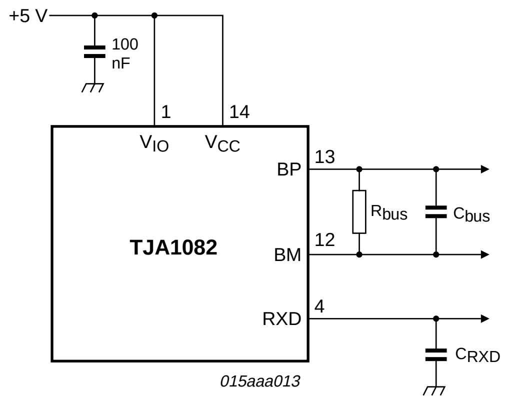
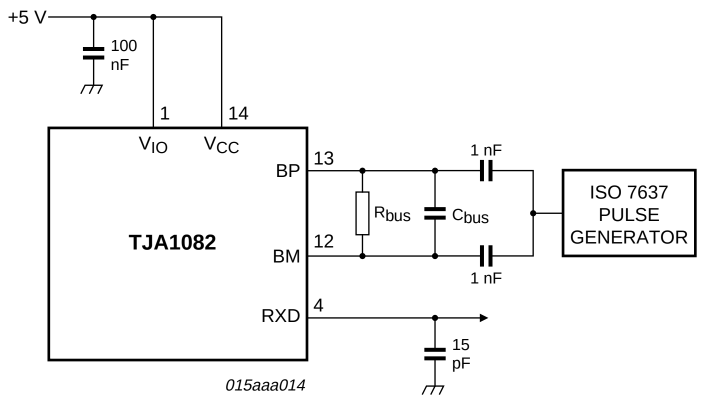


Fig 16. Test circuit for dynamic characteristics



The waveforms of the applied transients are in accordance with ISO 7637, test pulses 1, 2, 3a, 3b, 4 and 5.

Test conditions:

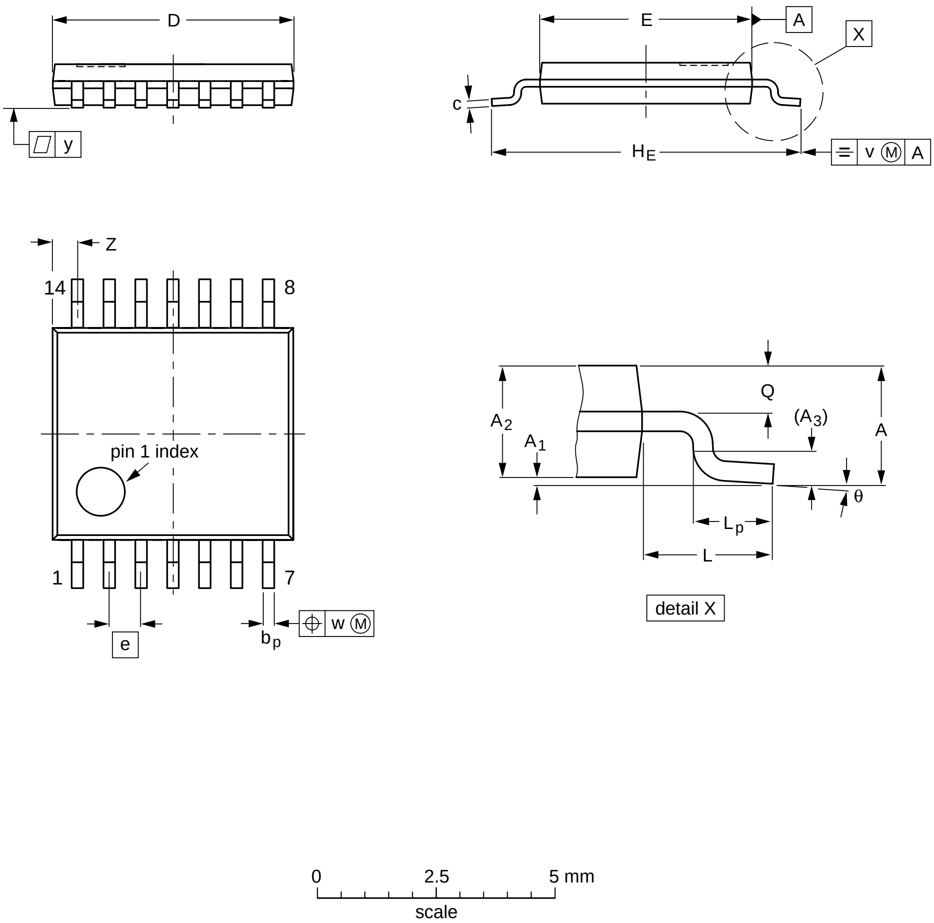
Normal mode: bus idle

Normal mode: bus active; TXD at 5 MHz and TXEN at 1 kHz

Fig 17. Test circuit for automotive transients

12. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT402-1 (TSSOP14)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 13 and 14

Table 13. SnPb eutectic process (from J-STD-020C)

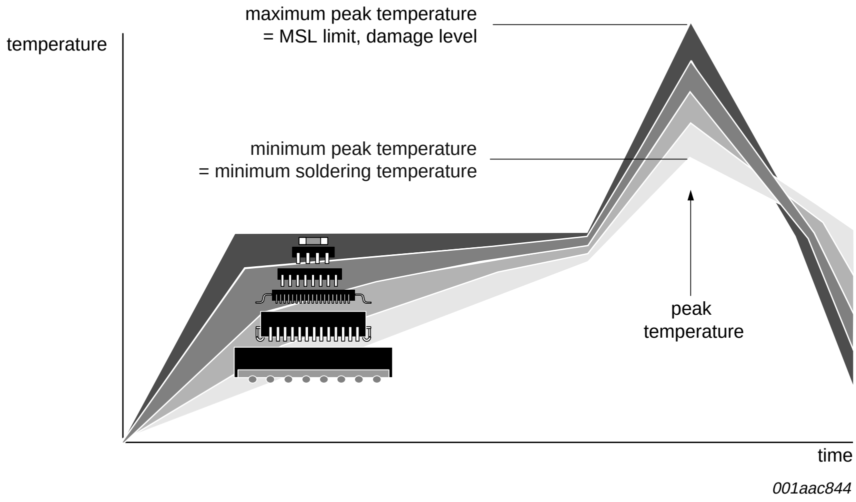
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 14. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Fig 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 15. Abbreviations

Abbreviation	Description
CAN	Controller Area Network
CDM	Charged Device Model
ECU	Engine Control Unit
EMC	ElectroMagnetic Compatibility
EME	ElectroMagnetic Emission
EMI	ElectroMagnetic Immunity
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
PWON	Power-on

15. References

[1] **EPL —** FlexRay Communications System Electrical Physical Layer Specification Version 2.1 Rev. B, FlexRay Consortium, Nov 2006

[2] **AN —** Application hint AN10365 - Surface mount reflow soldering description

16. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1082_1	20090701	Preliminary data sheet	-	-

17. Legal information

18. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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