

**Low Phase Noise LVDS VCXO (100MHz to 200MHz)**

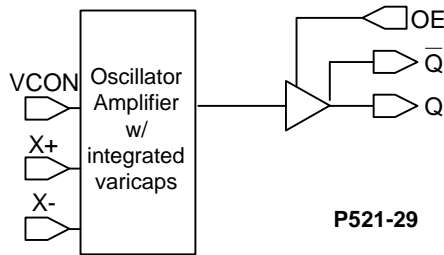
**FEATURES**

- 100MHz to 200MHz Fundamental Mode Crystal.
- Output range: 100MHz – 200MHz.
- Complementary LVDS outputs.
- Selectable OE Logic (enable high or enable low).
- Integrated variable capacitors.
- High pull linearity: < 5%.
- +/- 125 ppm pull range
- Supports 2.5V or 3.3V-Power Supply.
- Available in die form.
- Thickness 10 mil.

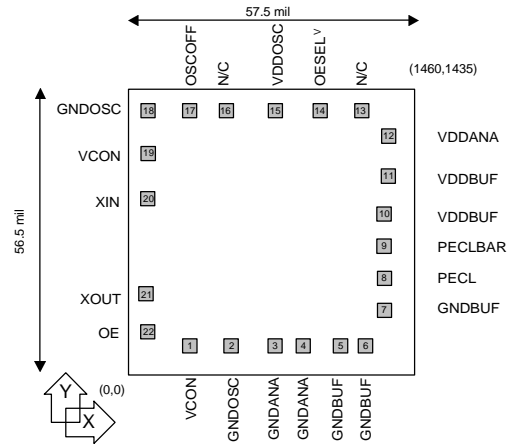
**DESCRIPTIONS**

P521-29 is a VCXO IC specifically designed to pull high frequency fundamental crystals. Its internal varicaps allow an on chip frequency pulling, controlled by the VCON input. The chip provides a low phase noise, low jitter LVDS differential clock output.

**BLOCK DIAGRAM**



**DIE CONFIGURATION**



**DIE SPECIFICATIONS**

Name	Value
Size	56.5 x 57.5 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

**OUTPUT ENABLE LOGIC SELECTION**

OESEL (Pad #14)	OCTRL (Pad #22)	State
0 (Default)	0	Tri-state
	1 (Default)	Output enabled
1	0 (Default)	Output enabled
	1	Tri-state

Pad #14, 22: Bond to GND to set to "0", bond to VDD to set to "1"  
No connection results to "default" setting through internal pull-up/down.  
Pad #22: Logical states defined by CMOS V<sub>IH</sub> and V<sub>IL</sub> levels.

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### PAD ASSIGNMENT AND DESCRIPTION

Pad #	Name	X (μm)	Y (μm)	Description
1	VCON	329.6	110.1	Control Voltage input. Use this pin to change the output frequency by varying the applied Control Voltage.
2	GNDOSC	498.3	110.0	GND connection for oscillator circuitry.
3	GNDANA	696.2	110.0	GND connection for analog circuitry.
4	GNDANA	825.0	110.0	GND connection for analog circuitry.
5	GNDBUF	973.6	110.0	GND connection for output buffer circuitry.
6	GNDBUF	1150.0	109.1	GND connection for output buffer circuitry.
7	GNDBUF (optional)	1183.6	302.2	GND connection for output buffer circuitry.
8	LVDS	1183.6	452.3	LVDS output
9	LVDSBAR	1183.6	613.5	LVDS complementary output.
10	VDDBUF (optional)	1182.4	745.9	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
11	VDDBUF	1252.4	903.6	VDD connection for output buffer circuitry. VDDBUF should be separately decoupled from other VDDs whenever possible.
12	VDDANA	1252.4	1081.3	VDD connection for analog circuitry. VDDANA should be separately decoupled from other VDDs whenever possible.
13	Not used	1058.5	1221.6	
14	OESEL	864.5	1221.6	Selector input to choose the OE control logic. See table on page 1.
15	VDDOSC	624.0	1222.7	VDD connection for oscillator circuitry. VDDOSC should be separately decoupled from other VDDs whenever possible.
16	Not used	467.1	1222.6	
17	OSCOFF	271.1	1222.6	Oscillator Off Selection input pad. When low, turns off the oscillator when output is disabled. When high (default), oscillator running when output is disabled. Internal pull-up
18	GNDOSC (optional)	109.4	1222.9	GND connection for oscillator circuitry.
19	VCON	108.9	1062.1	Control Voltage input. Use this pin to change the output frequency by varying the applied Control Voltage (internally connected to pad 1).
20	XIN	109.0	865.8	Crystal oscillator input pad.
21	XOUT	108.6	358.4	Crystal oscillator output pad.
22	OECTRL	108.6	146.5	OE input pad. See table on page 1.

Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

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### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature	$T_A$	0	70	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

#### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Parallel Fundamental Mode	100		200	MHz
Crystal Loading Rating	$C_L (xtal)$	Die at VCON = 1.65V		7.5		pF
Interelectrode Capacitance	$C_0$				3.5	pF
Crystal Pullability	$C_0/C_1 (xtal)$	AT cut			250	-
Recommended ESR	$R_E$	AT cut			30	$\Omega$

#### 3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid		10		ms
VCXO Tuning Range		XTAL $C_0/C_1 < 250$	250*			ppm
CLK output pullability		$0V \leq VCON \leq 3.3V$ at room temperature		$\pm 80^*$		ppm
On-chip Varicaps control range		$VCON = 0$ to 3.3V		4 – 18*		pF
Linearity				4*	5*	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		k $\Omega$
VCON modulation BW		$0V \leq VCON \leq 3.3V, -3dB$	25			kHz

**Note:** Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

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### 4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I <sub>DD</sub>	at 3.3V @ 155MHz			45	mA
Output valid after OE enabled		Oscillator off		10		ms
		Oscillator on			1	
Operating Voltage	V <sub>DD</sub>		2.25		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS)	45	50	55	%
Short Circuit Current				±50		mA

### 5. Jitter specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 155MHz	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 10,000 cycles		2.5		ps
Period jitter peak-to-peak at 155MHz			18.5	20	
Accumulated jitter RMS at 155MHz	At 155.52MHz, with capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.5		ps
Accumulated jitter peak-to-peak at 155MHz			24	27	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.5		ps
Integrated jitter RMS at 155MHz	Integrated 12 kHz to 20 MHz		0.25	0.35	ps

Measured on Wavecrest SIA 3000

### 6. Phase noise specifications

PARAMETERS	FREQUENCY	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	UNITS
Phase Noise relative to carrier	155.52MHz	-75	-100	-125	-140	-145	-150	dBc/Hz

Note: Phase Noise measured at VCON = 0V

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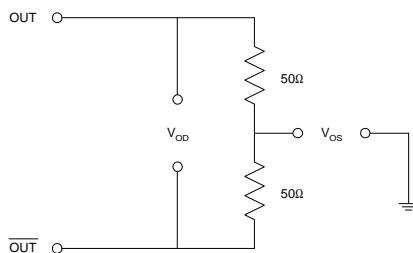
**7. LVDS Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	$V_{OD}$	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
$V_{DD}$ Magnitude Change	$\Delta V_{OD}$		-50		50	mV
Output High Voltage	$V_{OH}$			1.4	1.6	V
Output Low Voltage	$V_{OL}$		0.9	1.1		V
Offset Voltage	$V_{OS}$		1.125	1.2	1.375	V
Offset Magnitude Change	$\Delta V_{OS}$		0	3	25	mV
Power-off Leakage	$I_{OXD}$	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		$\pm 1$	$\pm 10$	$\mu A$
Output Short Circuit Current	$I_{OSD}$			-5.7	-8	mA

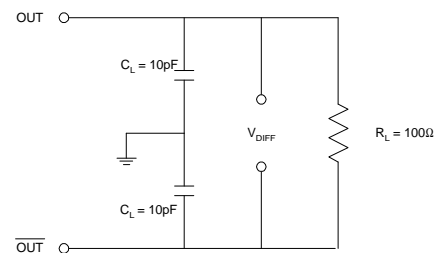
**8. LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform

