

CTLDM7002A-M621H

**SURFACE MOUNT
N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**



Top View Bottom View

TLM621H CASE

- Device is **Halogen Free** by design

APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

MAXIMUM RATINGS: ($T_A=25^{\circ}\text{C}$)

Drain-Source Voltage
Drain-Gate Voltage
Gate-Source Voltage
Continuous Drain Current
Continuous Source Current (Body Diode)
Maximum Pulsed Drain Current
Maximum Pulsed Source Current
Power Dissipation (Note 1)
Operating and Storage Junction Temperature
Thermal Resistance (Note 1)



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DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM7002A-M621H is a very low profile (0.4mm) Silicon N-Channel Enhancement-mode MOSFET in a small, thermally efficient, 1.5mm x 2mm TLM™ package.

MARKING CODE: CND

FEATURES:

- Low $r_{DS(ON)}$
- Low $V_{DS(ON)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small, Very Low Profile, TLM™

SYMBOL		UNITS
V_{DS}	60	V
V_{DG}	60	V
V_{GS}	40	V
I_D	280	mA
I_S	280	mA
I_{DM}	1.5	A
I_{SM}	1.5	A
P_D	1.6	W
T_J, T_{stg}	-65 to +150	$^{\circ}\text{C}$
θ_{JA}	75	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=20\text{V}, V_{DS}=0$		100	nA
I_{DSS}	$V_{DS}=60\text{V}, V_{GS}=0$		1.0	μA
I_{DSS}	$V_{DS}=60\text{V}, V_{GS}=0, T_J=125^{\circ}\text{C}$		500	μA
$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=10\text{V}$	500		mA
BV_{DSS}	$V_{GS}=0, I_D=10\mu\text{A}$	60		V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	2.5	V
$V_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$		1.0	V
$V_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		0.15	V
V_{SD}	$V_{GS}=0, I_S=400\text{mA}$		1.2	V

Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

R2 (17-February 2010)

CTLDM7002A-M621H

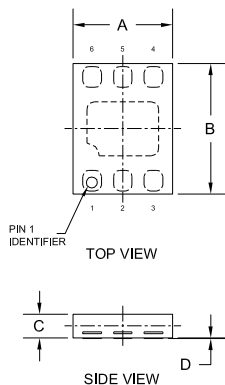
SURFACE MOUNT N-CHANNEL ENHANCEMENT-MODE SILICON MOSFET



ELECTRICAL CHARACTERISTICS - Continued: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$		2.0	Ω
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=500\text{mA}$, $T_J=125^{\circ}\text{C}$		3.5	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$		3.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}$, $I_D=50\text{mA}$, $T_J=125^{\circ}\text{C}$		5.0	Ω
g_{FS}	$V_{DS}=10\text{V}$, $I_D=200\text{mA}$	80		mS
C_{rss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		5.0	pF
C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		50	pF
C_{oss}	$V_{DS}=25\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		15	pF
t_{on} , t_{off}	$V_{DD}=30\text{V}$, $V_{GS}=10\text{V}$, $I_D=200\text{mA}$, $R_G=25\Omega$, $R_L=150\Omega$		20	ns

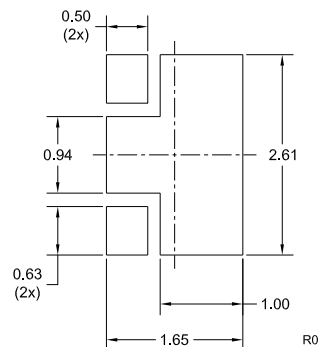
TLM621H CASE - MECHANICAL OUTLINE



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

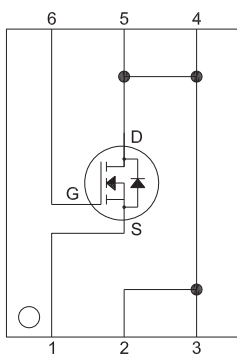
TLM621H (REV:R0)

OPTIONAL MOUNTING PADS (Dimensions in mm)



For standard mounting refer to TLM621H Package Details

PIN CONFIGURATION



LEAD CODE:

- 1) Source
- 2) Drain
- 3) Drain
- 4) Drain
- 5) Drain
- 6) Gate

MARKING CODE: CND

*Exposed pad P internally connected to pins 2, 3, 4, and 5.

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