PRODUCT SUMMARY



CX805-30 Baseband Processor for Multiband GSM and GPRS Applications

Applications

- GSM handsets and modules (900/1800/1900 MHz)
- GPRS handsets and modules (900/1800/1900 MHz)
- Bluetooth[™]-enabled wireless headset modules

Features

- 0.25 μm CMOS process technology
- ARM7 TDMI core
- Skyworks DSP core with all memory on-chip
- GPRS class 10 and circuit-switched data (14.4 kbps) data services
- Half-rate, full-rate, and enhanced full-rate speech coders
- Voice features such as voice recognition, conversation record, and voice memo
- Hardware accelerator for GPRS encryption algorithms (GEA 1 and 2)
- Integrated Real-Time Clock (RTC)
- Interface to handset MMI peripherals such as keypad, Liquid Crystal Diode (LCD), annunciator
- Interfaces to Skyworks IA and PMIC devices
- Interface to Subscriber Identity Module (SIM)
- Addresses up to 16 MB of external memory (Flash or SRAM)
- Application Interfaces:
- Serial/RS-232
- Infra-red Data Adapter (IrDA)
- Low power operation. 3 V I/Os and an on-chip supplied 2.5 V core
- Eight Chip Select (CS) signals for external memory
- 16-bit data bus, 24-bit address bus

Description

The Skyworks CX805-30 Baseband Processors (BPs) are highly integrated, dual core processors optimized for use in Global System for Mobile communications (GSM) and General Packet Radio Service (GPRS) cellular handset applications. The CX805-30 is the baseband portion of the Skyworks GSM/GPRS System Solution.

Both the Digital Signal Processor (DSP) core and the ARM7 THUMB[™] Reduced Instruction Set Computing (RISC) architecture are well suited to meet the needs of low power, high performance embedded systems such as cellular phones. The BP operates over a range of 2.7 V to 3.3 V.

The baseband processing tasks are divided between the DSP and ARM7 processor cores. The DSP core executes the physical layer, layer 1, processing functions, and the ARM microcontroller core executes Layer 2 and Layer 3 protocol software and the Man-Machine Interface (MMI) functions. The two cores communicate through a dedicated block of dual port memory. Each of the functional blocks in the device can be individually powered down to ensure minimum current consumption in the idle or standby mode.

The CX805-30 ARM and DSP peripherals are shown in Table 1. The CX805-30 family of devices is available in four package configurations as noted below. A block diagram for the CX805-30 device family is shown in Figure 1.

- The CX80501-31 is a 12 x 12 mm, 0.8 mm pitch, 160-pin Fine Pitch Ball Grid Array (FPBGA). The CX80501-31 supports up to Class 8 GPRS operation. The package, shipping, and tape and reel dimensions are shown in Figure 2, Figure 3 and Figure 4.
- The CX80501-32 is a 10 x 10 mm, 0.5 mm pitch, 180-pin FPBGA. The CX80501-32 supports up to Class 8 GPRS operation. The package, shipping, and tape and reel dimensions are shown in Figure 5, Figure 6 and Figure 7.
- The CX80502-33/-35 is a 12 x 12 mm, 0.8 mm pitch, 160-pin FPBGA. The CX80502-33/-35 supports up to Class 10 GPRS operation. The package, shipping, and tape and reel dimensions are shown in Figure 2, Figure 3 and Figure 4.
- The CX80502-34/-36 is a 10 x 10 mm, 0.5 mm pitch, 180-pin FPBGA. The CX80502-34/-36 supports up to Class 10 GPRS operation. The package, shipping, and tape and reel dimensions are shown in Figure 5, Figure 6 and Figure 7.

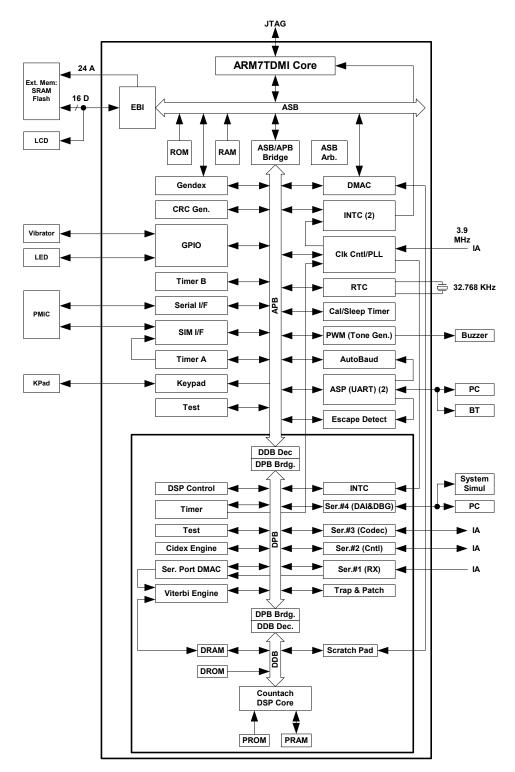
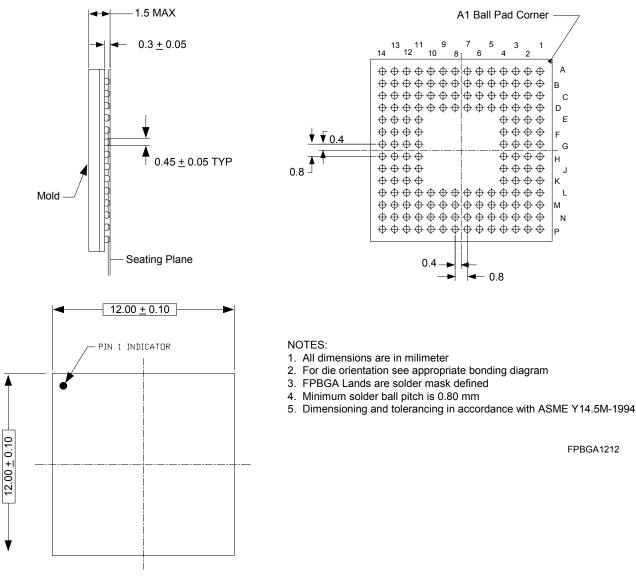
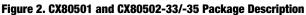
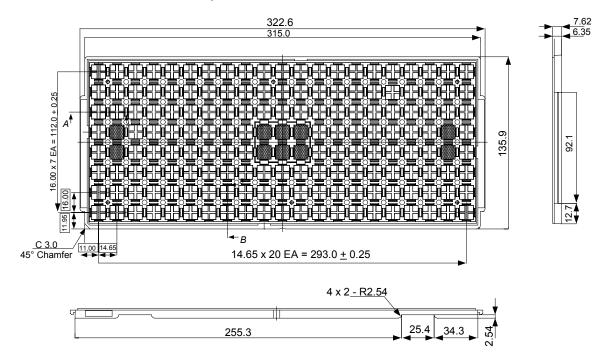


Figure 1. CX805-30 Block Diagram



12 x 12 FPBGA - 160 Balls/ 0.80 mm Ball Pitch



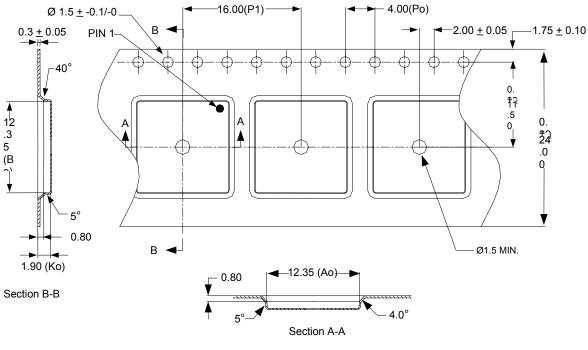


NOTES:

- 1. Trays must meet all requirements of Skyworks GP01-D228 procurement spec for shipping tray.
- 2. Material shall be bakeable carbon fiber/static dissipative w/140° C capability.
- 3. All dimensions and tolerances in accordance with ASME Y14.5M-1994
- ESD-Surface resisitivity shall be >/ = 1 X10⁵ < 1 X 10¹² Ω/Square per EIA, JEDEC, ACH Tray specification.
- 5. All dimensions are in milmeter.

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Figure 3. CX80501-31 and CX80502-33/-35 Shipping Tray



NOTES:

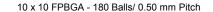
1. Carrier tape material: Black conductive polycarbonate or polystyrene.

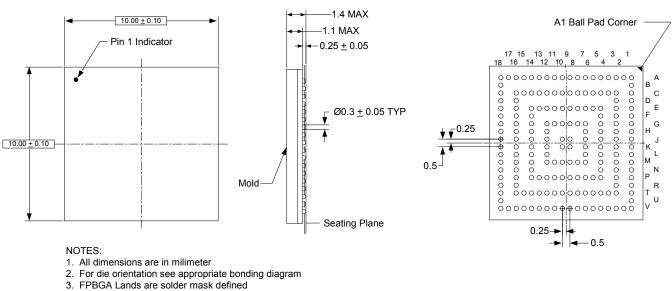
- 2. Cover tape material: Transparent conductive PSA.
- 3. Cover tape size: 21.30 mm width.

4. All dimensions are in milimeter. TR1212

5. Tolerance: .XX = + 0.10

Figure 4. CX80501-31 and CX80502-33/-35 Tape and Reel





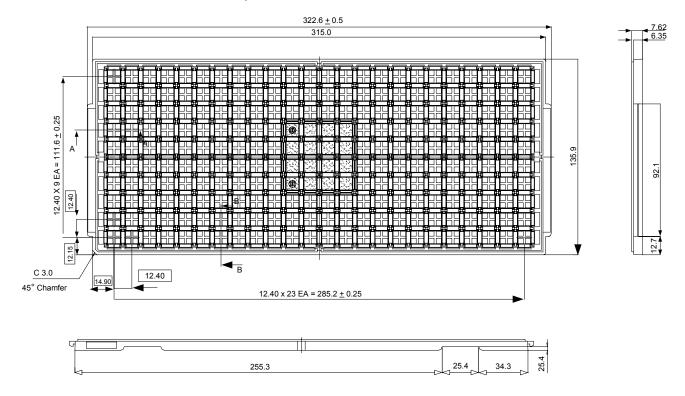
4. Minimum solder pitch is 0.50 mm

5. Dimensioning and tolerancing in accordance with ASME Y14.5 M - 1994

FPBGA 1010

Figure 5. CX80501-32 and CX80502-34/36 Package Description

CX805-30 Baseband Processor Product Summary



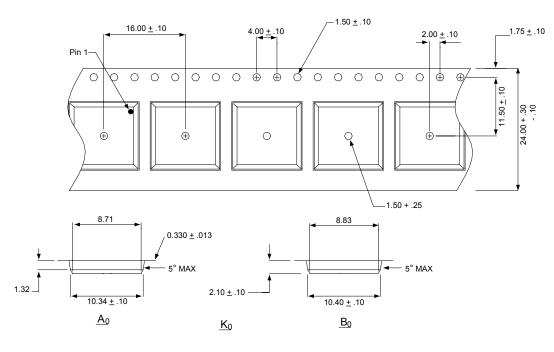
NOTES:

- 1. Trays must meet all requirements of Skyworks GP01-D228 procurement spec for shipping tray.
- 2. Material shall be bakeable carbon fiber/static dissipative w/ 140° C capability.
- 3. All dimensions and tolerances in accordane with ASME Y14.5M-1994.
- 4. ESD-Surface resisitivity shall be >/=1X10⁵ ~ < 1X10¹² Ω /Square per EIA, JEDEC, ACH tray specification.

5. All dimensions are in milimeter

SHP_1010

Figure 6. CX80501-32 and CX80502-34/-36 Shipping Tray



NOTES:

- 1. Carrier tape material: Black conductive polycarbonate or polystyrene.
- 2. Cover tape material: Transparent conductive PSA.
- 3. Cover tape size: 21.30 mm width.
- 4. All dimensions are in milimeter.
- 5. Tolerance: .XX = <u>+</u> 0.10

TR 1010

Figure 7. CX80501-32 and CX80502-34/-36 Tape and Reel

Table 1. Ordering	Information
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Model Name	Part Number	Device Configuration
Baseband Processor	CX80501-31	12 x 12 mm, 160-pin, 0.8 mm pad pitch, FPBGA, GPRS Class 8
	CX80501-32	10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 8
	CX80502-33 ¹	- 12 x 12 mm, 160-pin, 0.8 mm pad pitch, FPBGA, GPRS Class 10
	CX80502-35 ¹	
	CX80502-34 ²	10 v 10 mm 100 sin 0.5 mm red sitek EDBCA CDDC Class 10
	CX80502-36 ²	10 x 10 mm, 180-pin, 0.5 mm pad pitch, FPBGA, GPRS Class 10
<i>Note:</i> ¹ The CX80502-33 and CX80502-35 are interchangeable devices		
² The CX80502-34 and CX80502-36 are interchangeable devices		

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