Multi-Channel Audio CODEC

FEATURES

- Six Channel 24/20-bit DACs.
  - 102 dB SNR
  - 104 dB Dynamic Range.
  - -90 dB THD + N Ratio.
  - 32, 44.1 48 and 96 KHz. Sampling rates.
  - 20-bit and 24-bit Digital Inputs.
  - Containing Digital De-emphasis Filters.
  - Digital Volume Control.
  - I^2S, Left and Right Justified Digital Input Formats.
  - Auto-Mute Control.
  - On -chip Reconstruction Filters.
- Two Channel Stereo ADCs
  - 32, 44.1 and 48 KHz. Sampling Rate.
  - 100 dB SNR and Dynamic Range.
  - -96 dB THD + N Ratio.
  - I^2S and Left Justified Output Formats.
- System clock: 384 fs for 32, 44.1 or 48 KH. Sampling Rates, 194 fs for 96 KHz. Sampling Rate.

General

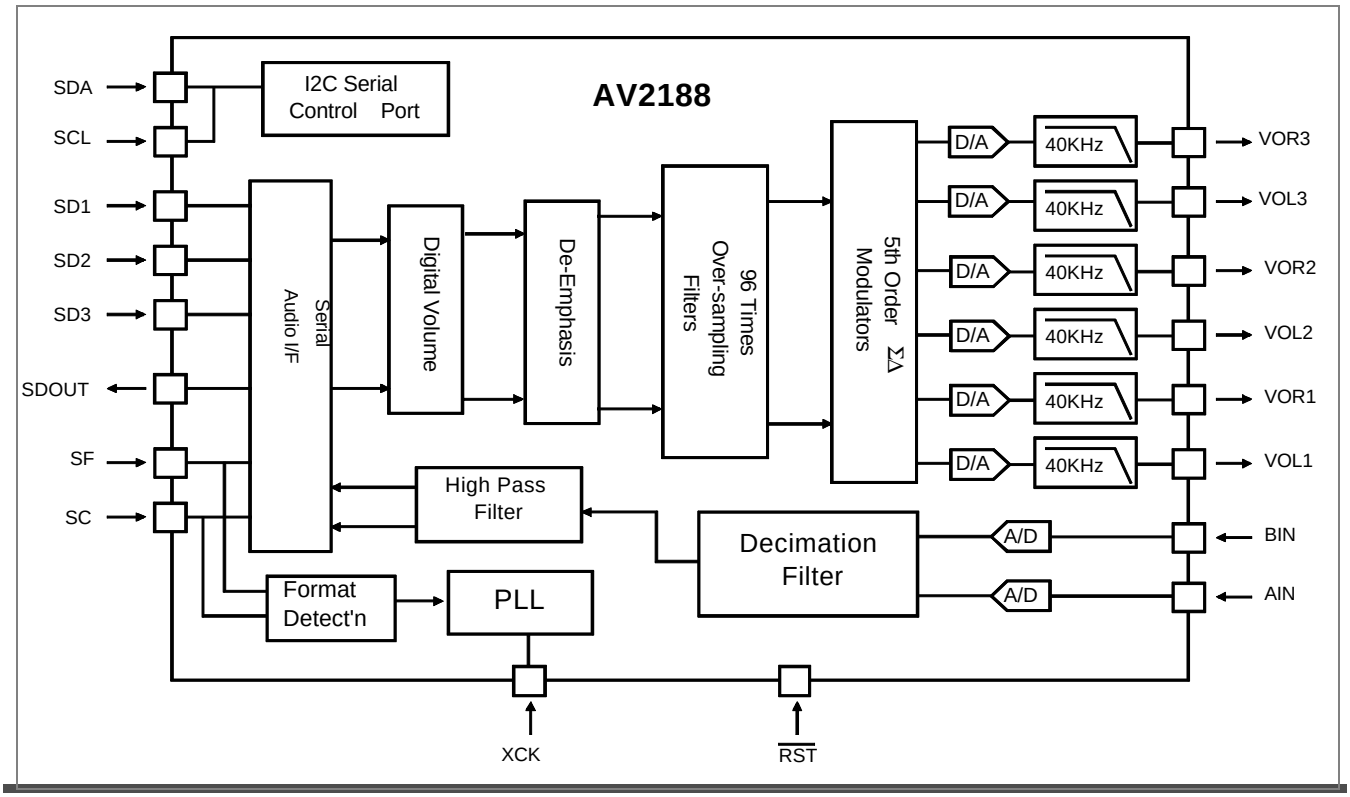
- Automatic input format detection.
- 5-volt Power Supply.
- 3.3 -volt Digital Interface Frindly.
- I^2C Interface for Mode Setting.

Applications

- Digital Surround Sound For Home Theater
- DVD
- Car Audio.

Ordering Information

- 28 pin SOJ package



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Item	PERFORMANCE SPECIFICATIONS	Spec.
	Audio DAC	
1	Audio Output Level	1 Vrms
2	Audio Bandwidth 20Hz - 20 KHz	+/- 0.5 dB
3	SNR (A-weight, Muted)	>102 dB
4	SNR (A-weight, Not Muted)	>96 dB
5	THD + N (A-weight, 0.5 FFS Output)	< -100 dB
6	THD + N (A-weight, FFS Output)	< -92 dB
7	Dynamic Range	104 dB
8	Channel Separation	< -97 dB
9	Nonlinear Distortion	< 0.25 dB
10	Channel Gain Error	< 0.1 dB
	Audio ADC	
1	Full Scale Audio Input Level	1.5 V_{p-p}
2	Maximum Input Level	5.0 V_{p-p}
2	Audio Bandwidth	20 KHz
3	SNR	98 dB
4	THD + N (A-weight, 0.5 FFS Input)	96 dB
4	Dynamic Range	98 dB

All Measurement were taken with only one channel active.

DESCRIPTION

The AV2188 is a mixed signal CMOS monolithic audio CODEC. It consists six channels sigma delta DACs and two channels sigma delta ADCs. The DACs support 20-bit and 24-bit input data, while the ADCs provides 24-bit MSB justified data output.

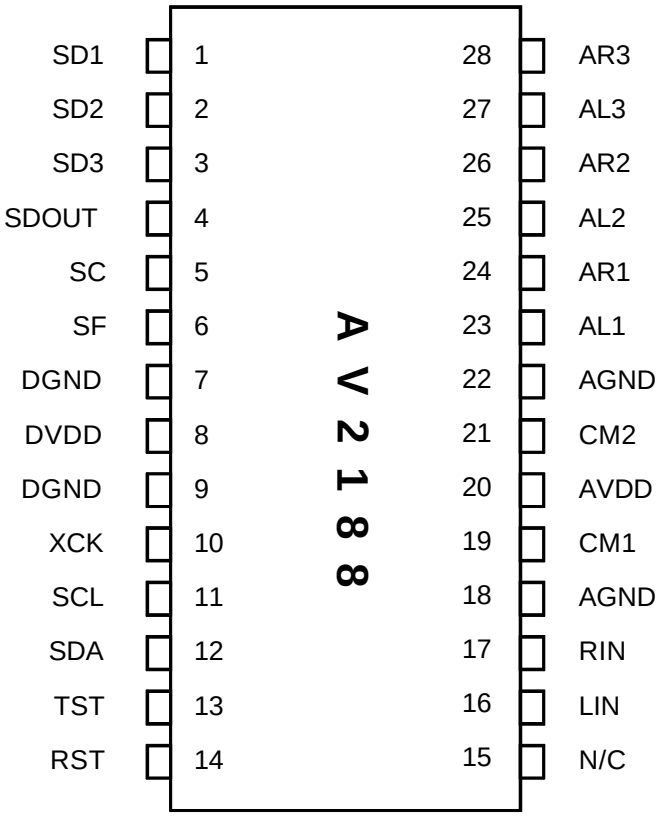
XCK REQUIREMENT

The AV2188 support 384 and 256 times sampling clock for 32, 44.1 and 48 K audio; 192 and 128 times for the 96 K audio.; and 96 and 64 times for the 192K audio. .

XCK Requirement

Sampling Rate	XCK Freq.	
	384*fs	**256*fs**
32 K	12.288 MHz	8.192 MHz
44.1	16.934 Mhz	11.29 Mhz.
48 K	18.432 MHz	12.288 Mhz.
96 K	18.432 MHz	12.288 Mhz.
192 K	18.432 Mhz	12.288 Mhz.

PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	Pin #	Type	Description
DIGITAL			
SD1	1	I	Audio Serial Data Input 1, data can be 20bit/24bit, Right justified, or 24bit Left justified, or 24bit I2S, all in 2's complement format.
SD2	2	I	Audio Serial Data Input 2, data can be 20bit/24bit, Right justified, or 24bit Left justified, or 24bit I2S, all in 2's complement format.
SD3	3	I	Audio Serial Data Input 3, data can be 20bit/24bit, Right justified, or 24bit Left justified, or 24bit I2S, all in 2's complement format.
SDOUT	4	O	Serial Audio Output pin, data can be in 20bit Right justified or 20bit I2S format.
SC	5	I	Audio Serial Data Clock pin.
SF	6	I	Left/Right Channel Clock pin. For Left justified or Right justified mode, a high in SF indicates Left Channel Data, a low in SF indicates Right Channel Data. For I2S mode, a low in SF indicates Left Channel Data, a high in SF indicates Right Channel Data.
DVSS	7	GND	Digital ground
DVDD	8	+5V	Digital power supply.

PIN DESCRIPTION (Continued)

Pin Name	Pin #	Type	Description
DVSS	9	GND	Digital ground
XCK	10	I	External Master Clock Input.
SCL	11	I	I2C clock input.
SDA	12	I/O	I2C DATA bus. Open drain ouput. Externally this pin should tie to a 680 ohm pull up resistor.
TEST	11	O	Test fs reference pin. For test vector verification. For normal operation this pin must be tied to '0'.
$\overline{RST}$	12	I	Active low power down reset. When low, the chip is reset and all programmable registers are reset to default values. Must activate this pin if the P/$\overline{S}$ or ADDR[1:0] change state.

Analog

VOL3	28	O	Analog left channel output 3
VOR3	27	O	Analog right channel output 3.
VOL2	26	O	Analog left channel output 2.
VOR2	25	O	Analog right channel output 2.
VOL1	24	O	Analog left channel output 1.
VOR1	23	O	Analog right channel output 1.
AVSS	22	GND	Analog circuits ground
VCM2	21		Common voltage output pin for the DAC.
AVDD	20	+5V	Analog circuits power supply
VCM1	19		Common voltage output pin for the ADC.
AVSS	18	GND	Analog circuits ground
AINR	17	I	ADC right cahnnel input. 1 volt rms input.
AINL	16	I	ADC left channel input. 1 volt rms input.
N/C	15		No connection, should be tied to AVSS

DIGITAL AUDIO SERIAL INTERFACE

The digital serial interface consists of 3 serial input pins, SD1, SD2, and SD3, one serial output pin, SDOUT, one serial clock input pin, SC, and one left/right indicator input pin, SF. The data are 2's complement MSB first numbers. The AV2188 supports four resolutiont, which are selected either by setting the FMT[1] and FMT[0] pins or by programming the control register CREG0[5:4] via the I^2C serial control port. Table 1 describes these four resolution. .

Table (1): Audio Serial Data Input Format

Format	CREG0[5]	CREG0[4]	SD1, SD2, and SD3	SDOUT
0	0	0	24-bit	24-bit
1	0	1	20-bit	
2	1	0	18-bit	
3	1	1	16-bit	

The SD3, SD2 and SD1 can be either 24-bit or 32-bit per frame as well as left justified, right justified or I2S. The SDOUT only support left justified and I2S format. The AV1488 counts the number of BCK per frame to determine whether the input is 24 or 32 bits format.

Table (1): Audio Serial Data Input Modes

Mode	CREG0[7]	0REG0[6]	SD1, SD2, and SD3	SDOUT
0	0	0	Right Justified	Left Justified
1	0	1	I2S	I2S
2	1	0	Left Justified	Left Justified
3	1	1	Invalid	

Figure 1. Audio Serial Input Data Timing Diagram

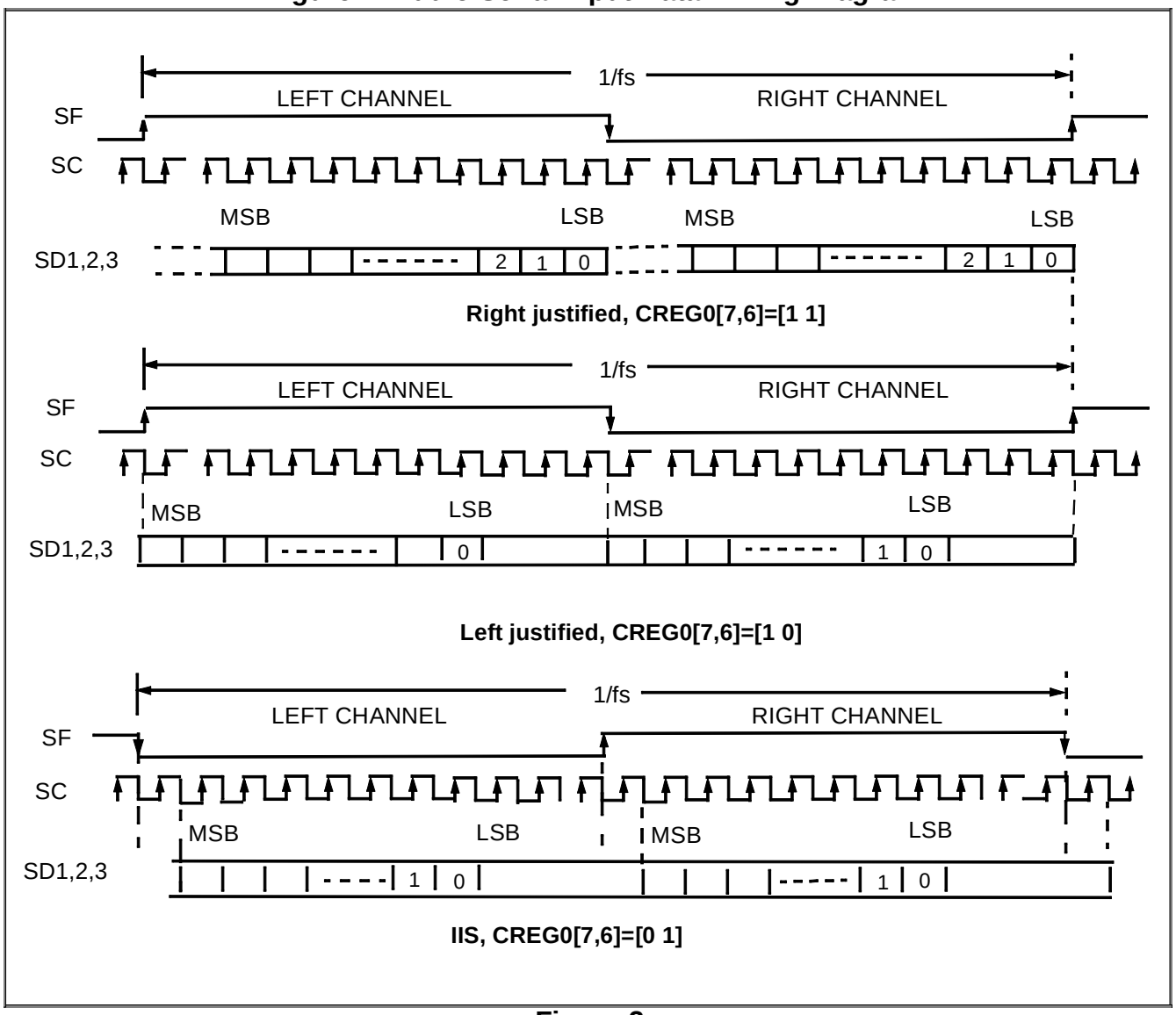
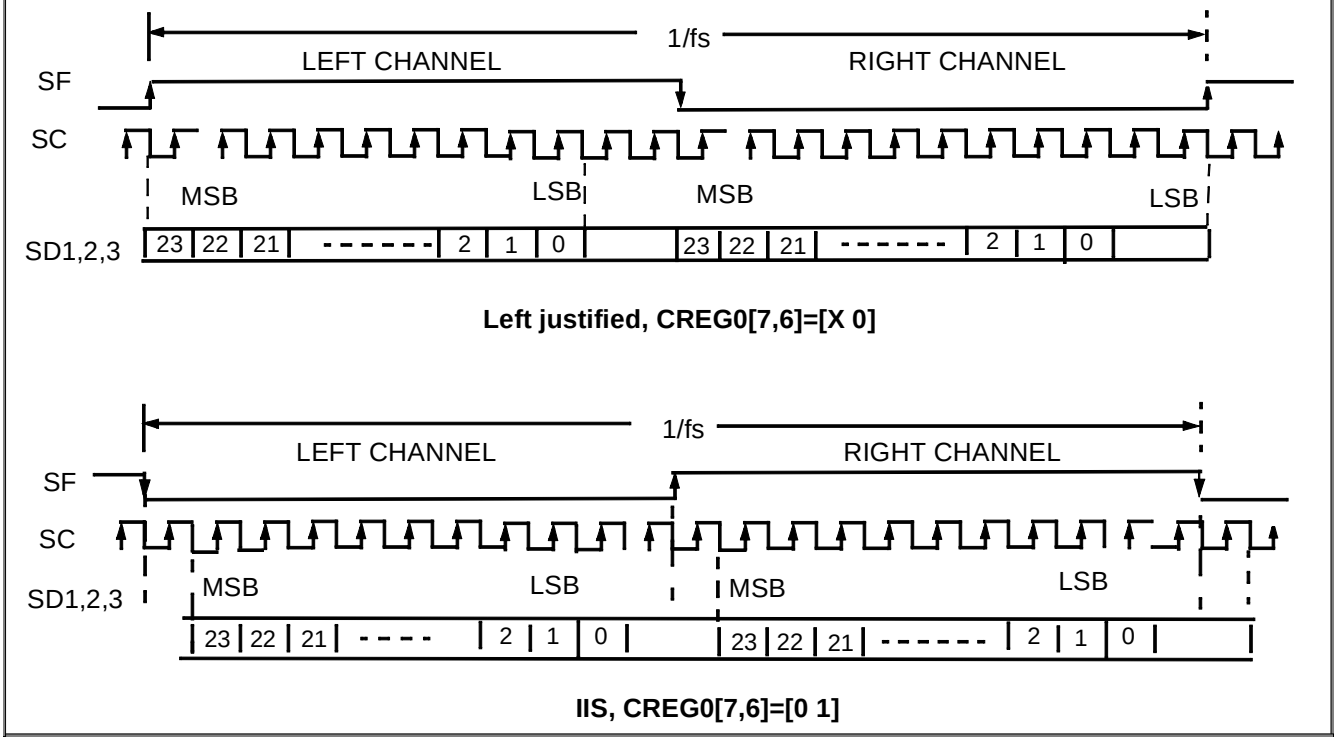


Figure 2.

Figure 3. Audio Serial Output Data Timing Diagram



INFINITE ZERO DETECTION

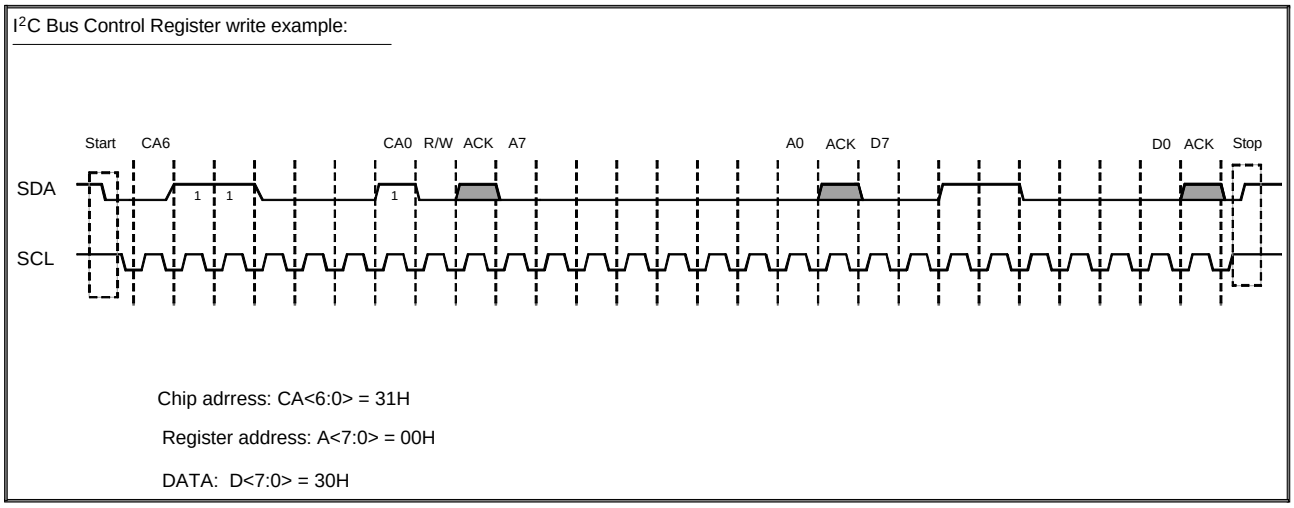
The AV2188 has an Infinite Zero Detection circuit which detects zero in the Audio Serial Port that lasts for approximately 0.5 sec. By default, the zero detection circuit is on. To disable this feature, bit 7 of the programmable register TREG1[7] must be programmed to a “one”.

SERIAL COMMAND PORT

The user can use the pin to select the chip operation or by programming the internal control registers through the 7 bit address I^2C port. The Chip Address for the AV2188 is 31H. The protocal for write operation consists of sending 3 byte data to AV2188, following each byte are the acknowledges generated by AV2188. The first byte is the 7-bit Chip Address followed by the read/write bit (read is high write is low). The second byte is the control register address. The third byte is the control register data.

Upon power up, all programmable registers are set to default values. Figure 4 describes the serial command port timing relationship.

Figure 4. Serial Command Port Timing



SERIAL PORT CONTROL REGISTER ASSIGNMENT

There are 3 registers dedicated to the AV2188 for chip functional programmin,. One register for testinging. The register addresse assignments are

Address (decimal)	Register	Default Value	Register Function
0	CREG0[7:0]	00	Data input format, de-emphasis filter selection
1	CREG1[7:0]	00	DAC and ADC power down control
2	VOLREG[7:0]	80	Volume control
3	TREG1[7:0]	00	Test control

CONTROL REGISTERS DESCRIPTION

Control Register 0(ADDR=hex00, default=hex80)

ADDR[4:0]	CREG0[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 00	LT	IIS	FMT[1:0]		AMUTE		DEM[1:0]	
Default Value	0				0	0	0	0
R/W	R/W				R/W	R/W	R/W	R/W

[LT, IIS] Digital Serial Bus Format Select
- 00: - Normal or Right Justified Format. (default)
- 01: - I2S Format.
- 10: - Left Justified Format.
- 10: - Not allowed.

FMT[1:0]: - These two bits define the seial audio input resolution
- 00: - 24-bit resolution . (default)
- 01: - 20-bit resolution.
- 10: - 18-bit resolution.
- 11: - 16-bit resolution.

AMUTE: - Active low automute detection enable.
- 0: - Automute enabled. (default)
- 1: - No automute.

DEML: - De-emphasis Control
- 00: - No De-emphasis. (default)
- 01: - Select 44.1K de-emphasis filter.
- 10:- Select 48 K de-emphasis filter.

Control Register 1 (ADRS=hex01, default=hex80)

ADDR[4:0]	CREG1[7:0]							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 01	ADCPWD		fs384	px4s	px2s	DACPWD12	DACPWD34	DACPWd56
Default Value	1	0	0	0		0	0	0
R/W	R/W		R/W	R/W		R/W	R/W	R/W

ADCPWD: ADC Control.
- 0 - ADC operational.
- 1 - Power down the ADC.

DACPWD56: DAC5 and DAC6 Control.
0 - DAC5 and DAC 6 operational.
1 - Power down the DAC5 and DAC6.

DACPWD43: DAC3 and DAC4 Control.
0 - DAC3 and DAC4 operational.
1 - Power down the DAC3 and DAC4.

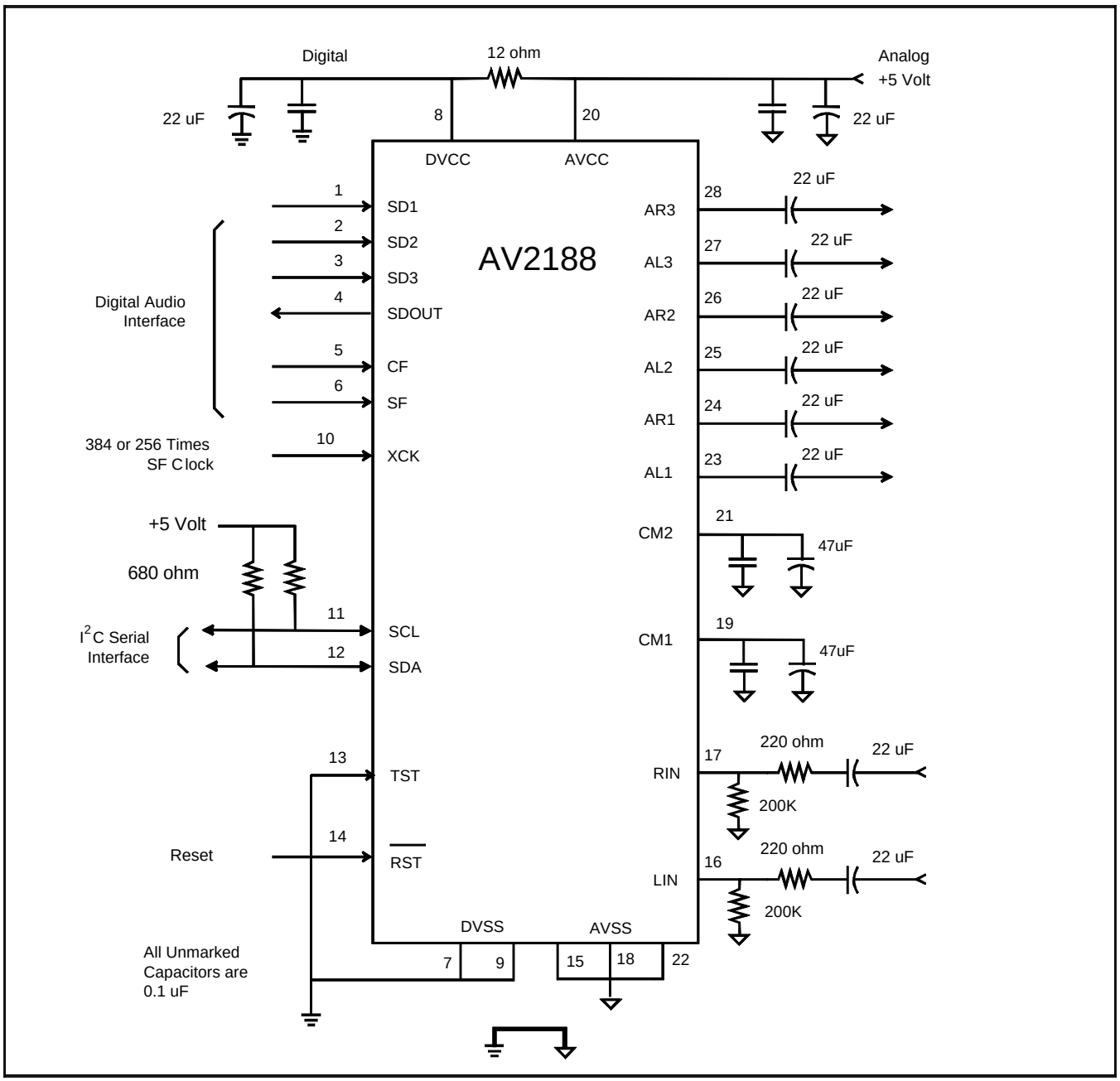
DACPWD21: DAC2 and DAC1 Control.
0 - DAC2 and DAC1 operational.
1 - Power down the DAC2 and DAC1.

Volume Registers, (ADRS=hex02, default=hex80)

ADDR[4:0]	Volume Registers							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Hex 02	VLREG[7:0]							
Default Value	1	0	0	0	0	0	0	0

VOLREG:- Control the volume of the 6 DAC's
80h- corresponds to 0 dB setting.

Application Connection Example:



TIMING DIAGRAM

Figure 5. Audio Serial Interface Timing Requirement

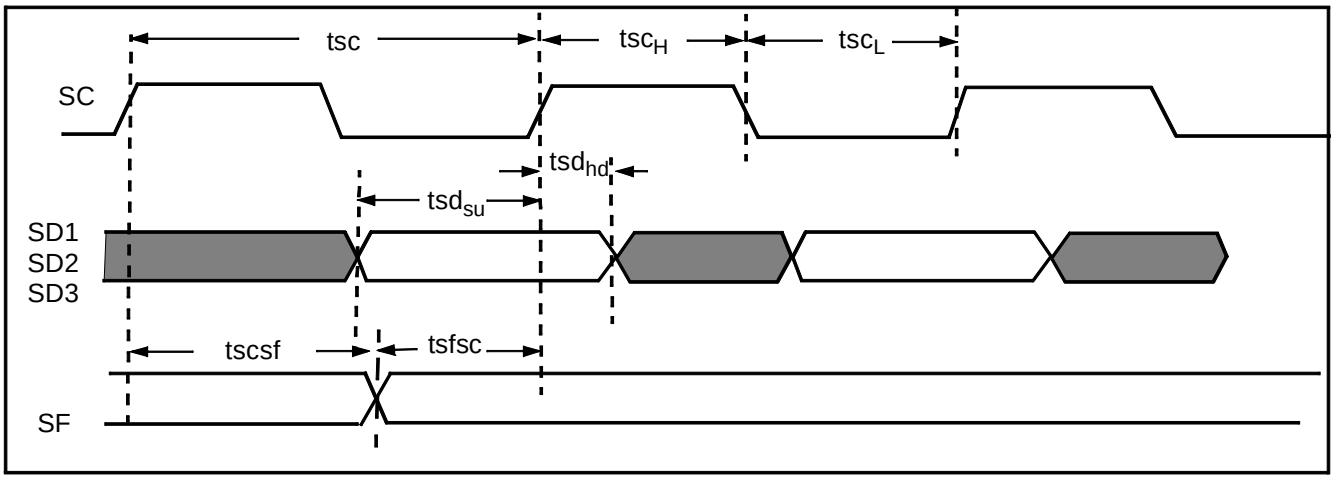


Figure 6. Serial Data Output Timing Requirement

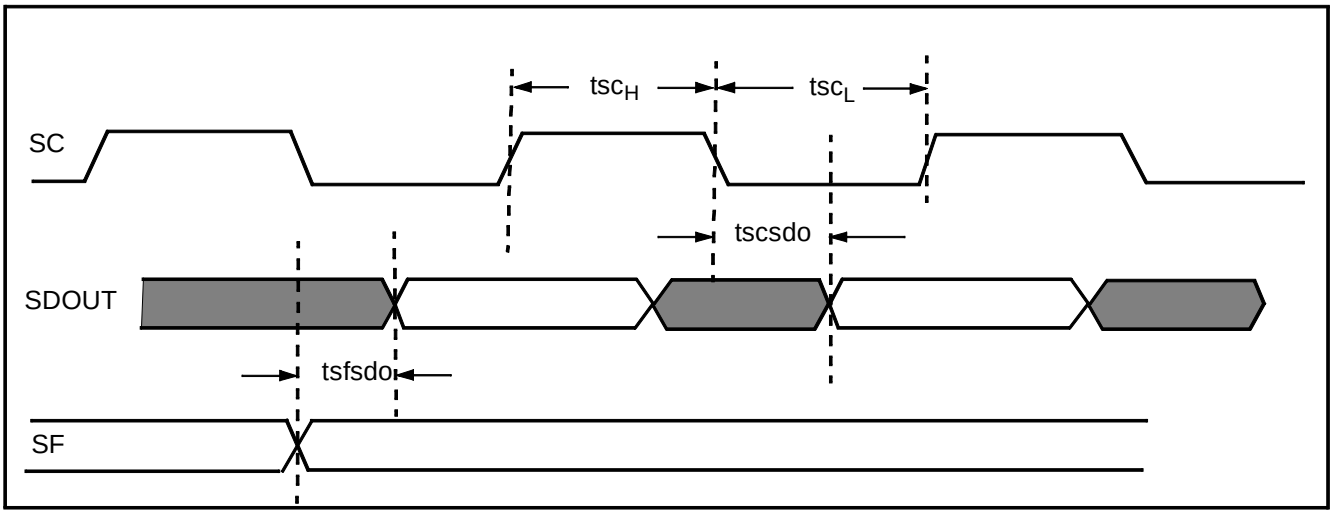


Figure 7. Serial Command Port Write Timing Requirement

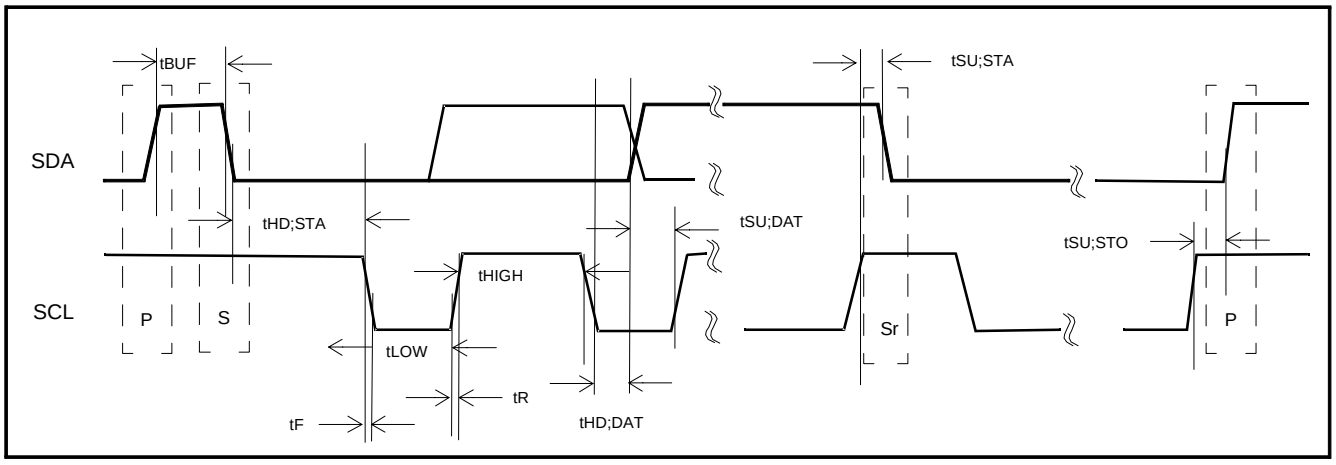
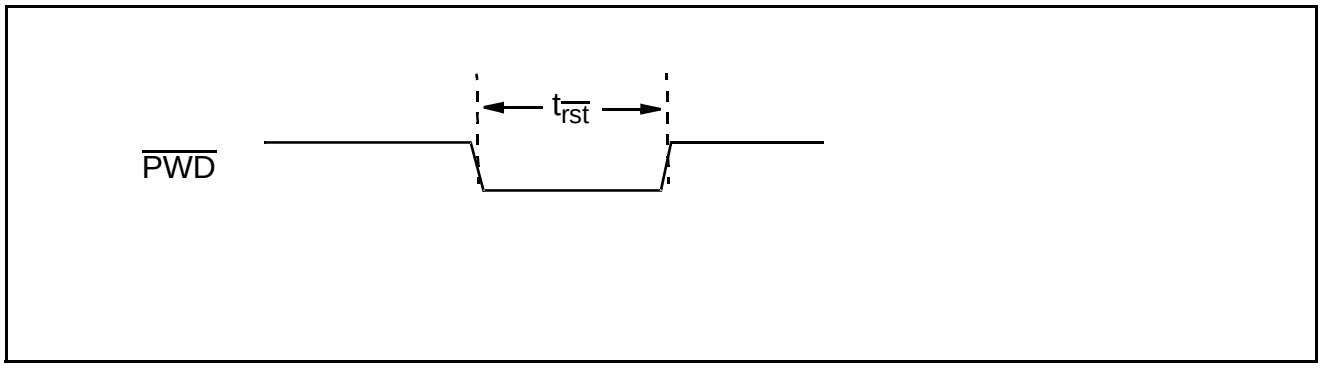


Figure 8. Power Down / Reset Timing



ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min	Max	Units
V_{DD}	Power Supply Voltage (Measured to GND)	-0.5	+7.0	V
V_i	Digital Input Applied Voltage[2]	GND-0.5		V
A_i	Digital Input Forced Current[3,4]	-100	100	mA
V_o	Digital Output Applied Voltage[2]	GND-0.5	V_{DD}+0.5	V
A_o	Digital Output Forced Current[3,4]	-100	100	mA
TDsc	Digital Short Circuit Duration (single output high state to Vss)		1	Sec
TA_{SC}	Analog Short Circuit Duration (single output to VSS1)		infinite	Sec
T_a	Ambient Operating Temperature Range	-25	+125	^oC
Tstg	Storage Temperature Range	-65	+150	^oC
T_j	Junction Temperature (Plastic Package)	-65	+150	^oC
Tsol	Lead Soldering Temperature (10 sec., 1/4” from pin)		300	^oC
Tvsol	Vapor Phase Soldering (1 minute)		220	^oC
T_{stor}	Storage Temperature	-65	+150	^oC

Notes:

1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.

2. Applied voltage must be current limited to specified range, and measured with respect to VSS.

3. Forcing voltage must be limited to specified range.

4. Current is specified as conventional current, flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Typical	Max	Units
V_{DD}	Power supply voltage	4.5	5	5.5	V
V_{VCM}	Reference voltage		2.25	2.41	V
R_L	Analog output load		37.5	70	Ω
T_a	Ambient operating temperature range	0		70	^oC

ELECTRICAL CHRACTERISTICS

Parameter	Characteristics	Min	Typ	Max	Units
Supply					
I_{DD}	Total Power Supply Current, Analog + Digital		135	145	mA
I_{DDQ}	Total Power Supply Current,ADC Power Down		115	120	mA
Digital Characteristics					
V_{IH}	Digital Input Voltage, Logic HIGH, TTL Compatible Inputs.	2.0		V_{DD}	V
V_{IL}	Digital Input Voltage, Logic LOW, TTL Compatible Inputs	V_{SS}		0.8	V
I_{IH}	Digital Input Current, Logic HIGH, (V_{IN}=4.0V)			10	µA
I_{IL}	Digital Input Current, Logic LOW, (V_{IN}=0.4V)			-10	µA
C_{IN}	Digital Input Capacitance (f=1Mhz, V_{IN}=2.4V)			7	pF
V_{OH}	Digital Output Voltage, Logic HIGH, (I_{OH}= -1mA)	3.2	3.4	3.5	V
V_{OL}	Digital Output Voltage, Logic LOW, (I_{OL}=4.0 mA)	V_{SS}		0.4	V
I_{OZH}	Hi-Z Leakage Current, HIGH, V_{DD}=Max, V_{IN}=$V_{DD)}$			10	µA
I_{OZL}	Hi-Z Leakage Current, LOW, V_{DD}=Max, V_{IN}=$V_{SS)}$			-10	µA
C_I	Digital Input Capacitance (T^A=25^{o}C, f=1Mhz)			8	pF
C_O	Digital Output Capacitance (T^A=25^{o}C, f=1Mhz)			10	pF

Parameter	Characteristics	Min	Typ	Max	Units
Audio Serial Interface Timing					
tsc	SC Cycle Time	120			ns
tsc_H	SC Pulse Width, HIGH	50			ns
tsc_L	SC Pulse Width, LOW	50			ns
tsd_{su}	Audio Data Setup Time With Respect To Rising Edge of SC	30			ns
tsd_{hd}	Audio Data Hold Time With Respect to Rising Edge of SC	30			ns
tsfsc	Audio SFSetup Time With Respect To Rising Edge of SC	30			ns
tscsf	Audio SF Hold Time With Respect To Rising Edge of SC	30			ns
tscsdo	SC falling edge to SDOUT			50	ns
tsfsdo	SF transition to SDOUT	30			ns
Reset Signal					
$t_{\overline{rst}}$	Active low reset time		1		µs
Serial Command Port					
fsc	SCL Clock Frequency			100	kHz
tsu;sta	Start condition set up time	4.7			us
thd;sta	Start condition hold time	4.0			us
tsu;sto	Stop condition set up time	4.0			us
tLOW	SCL Low time	4.7			us
tHIGH	SCL High time	4.0			us
tr	SCL & SDA rise time			1.0	us
tf	SCL & SDA fall time			0.3	us
tsu;DAT	Data set-up time	250			ns
thd;DAT	Data hold time	0			ns
tvd;DAT	SCL LOW to data out valid			3.4	us
tBUF	Bus Free time	4.7			us

Parameter	Characteristics	Min	Typ	Max	Units
Audio DAC Characteristics					
SNR	Signal To Noise Ratio	101	103		dB
THD+N	Total Harmonic Distortion + Noise		94		dB
	Dynamic Range	102	104		dB
	Channel Separation	84	97		dB
	Full Scale Output Voltage	.95	1	1.09	Vrms
	Center Voltage	2.15	2.25	2.4	V
	Inter-channel Gain Mismatch		0.1		dB
	Analog Output Load Resistance	5			KΩ
	Analog Output Load Capacitance			100	pF
Audio ADC Characteristic					
SNR	Signal To Noise Ratio		98		dB
THD+N	Total Harmonic Distortion + Noise		94		dB
	Dynamic Range		104		dB
	Channel Separation		96		dB
	Full Scale Input Voltage		1.1		Vrms
	Center Voltage		2.25	2.4	V
	Inter-channel Gain Mismatch		0.1		dB
	Analog Input Load Capacitance			30	pF

PACKAGING INFORMATION

Dimensions

	Mils				Mils		
	min	norm	max		min	norm	max
A	93	100	104	E1	291	295	299
A1	4	8	12	E2	394	406	419
b	14	16	19	e		50	
C	9	10	12	L	20	30	40
D	691	702	713				

28-Pin (SOP)