NEC

MOS INTEGRATED CIRCUIT

μPD75312B, 75316B

4-BIT SINGLE-CHIP MICROCOMPUTER

The μPD75316B is a 75X Series 4-bit single-chip microcomputer capable of the same data processing as an 8-bit microcomputer.

It is a low-voltage operation version of the μPD75316 with an on-chip LCD controller/driver. Operation at an ultra-low voltage of 2.0 V is possible. An ultra small-sized plastic TQFP (12 x 12 mm) is also provided and it is suitable for small-sized sets that use an LCD panel.

A detailed explanation of the functions will be given in the user's manual listed below. It should be read before starting design work.

μPD75308 User's Manual: IEM-1263

FEATURES

- Ultra-low-voltage operation possible: V_{DD} = 2.0 to 6.0 V
  - Can be driven by two 1.5-V manganese batteries.
- On-chip memory
  - Program memory (ROM)
    : 16256 × 8 bits (μPD75316B)
    : 12160 × 8 bits (μPD75312B)
  - Data memory (RAM)
    : 1024 × 4 bits
- Instruction execution time adjustment function convenient in high-speed operation and power saving
  - 0.95 μs, 1.91 μs, 15.3 μs (@ 4.19 MHz)
  - 122 μs (@ 32.768 kHz)
- On-chip programmable LCD controller/driver
  - LCD drive voltage: 2.0 V to V_{DD}
- Ultra small-sized plastic TQFP (12 x 12 mm)
  - Suitable for small-sized set, such as a camera.
- PROM version μPD75P316B also available.

APPLICATIONS

Remote control, camcorder, camera, gas meter, etc.

ORDERING INFORMATION

Part number	Package
μPD75312BGC-×××-3B9	80-pin plastic QFP (14 x 14 mm)
μPD75312BGK-×××-BE9	80-pin plastic TQFP (Fine pitch) (12 x 12 mm)
μPD75316BGC-×××-3B9	80-pin plastic QFP (14 x 14 mm)
μPD75316BGK-×××-BE9	80-pin plastic TQFP (Fine pitch) (12 x 12 mm)

Remark ××× : ROM code suffix

Unless stated otherwise, the explanations in this document will use the μPD75316B as a representative part.

The information in this document is subject to change without notice.

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FUNCTION OUTLINE (1/2)

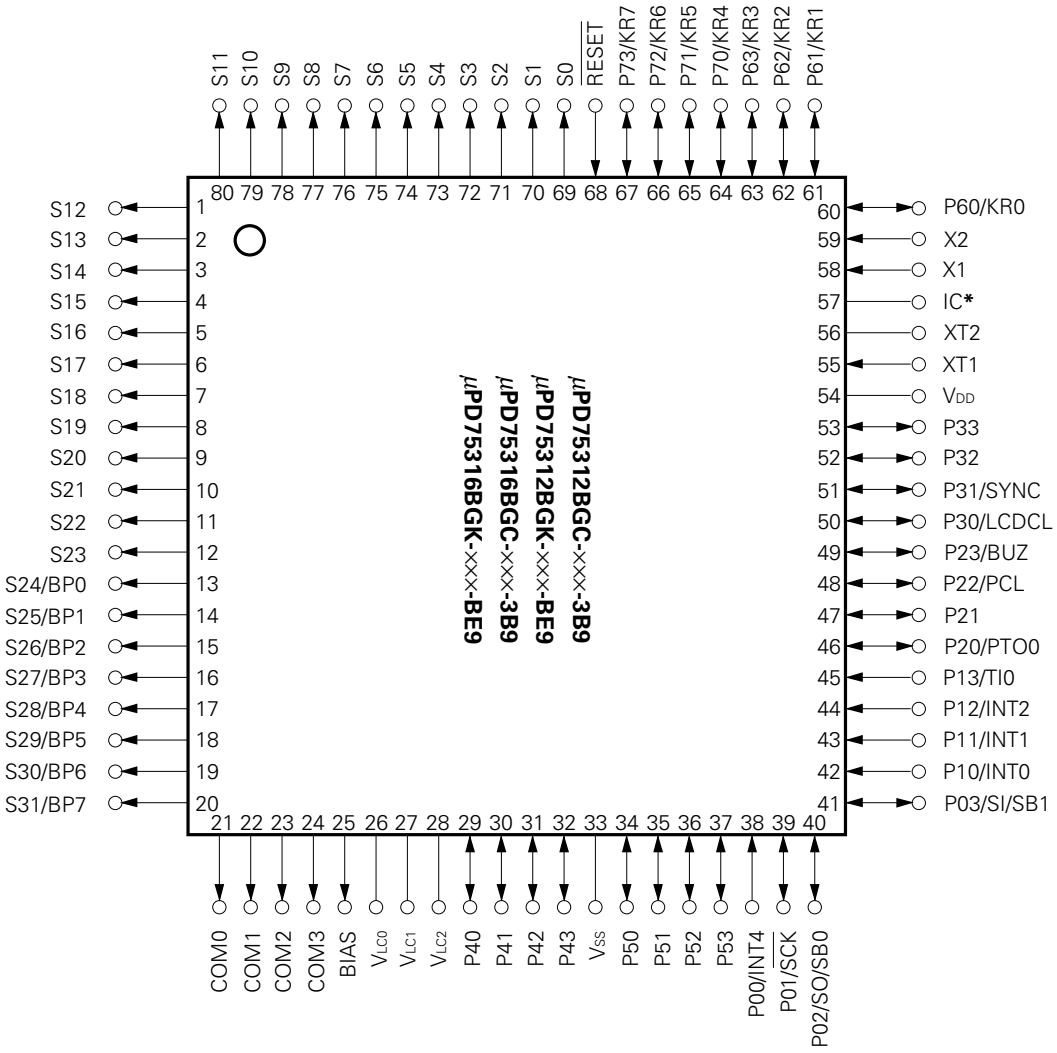
Item		Function			
Number of basic instructions		41			
Instruction cycle		0.95 μs, 1.91 μs, 15.3 μs (main system clock: @ 4.19 MHz) 122 μs (subsystem clock: @ 32.768 kHz)			
On-chip memory	ROM	16256 × 8 bits (μPD75316B), 12160 × 8 bits (μPD75312B)			
	RAM	1024 × 4 bits			
General register		• 4-bit access: 8 (B, C, D, E, H, L, X, A) • 8-bit access: 4 (BC, DE, HL, XA)			
Accumulators		• Bit accumulator (CY) • 4-bit accumulator (A) • 8-bit accumulator (XA)			
Instruction set		• Various bit manipulation instructions • Efficient 4-bit data manipulation instructions • 8-bit data transfer instructions • GETI instruction that can implement 2-byte/3-byte instructions with 1 byte			
I/O lines		40	8	CMOS input	with software-specifiable pull-up resistors : 23
			16	CMOS input/output	
			8	CMOS output	Used with segment pins
			8	N-ch open-drain input/output	10-V withstand voltage, with mask option pull-up resistors: 8
LCD controller/driver		• Number of segments selection: 24/28/32 segments (4/8 can be switched at bit port output.) • Display mode selection: Static, 1/2 duty, 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty • LCD drive split resistor can be incorporated by mask option			
Supply voltage range		V_{DD} = 2.0 to 6.0 V			
Timer		3 channels	• 8-bit timer/event counter • Clock source: 4 stages • Event count possible		
			• 8-bit basic interval timer • Standard clock generation: 1.95 ms, 7.82 ms, 31.3 ms, 250 ms (@ 4.19 MHz) • Watchdog timer application possible		

FUNCTION OUTLINE (2/2)

Item	Function	
Timer	3 channels	• Clock timer • 0.5-second time interval generation • Count clock source: Main system clock and subsystem clock switchable • Clock fast count mode (3.9-ms time interval generation) • Buzzer output possible (2 kHz)
8-bit serial interface	• Three modes application possible • 3-wire serial I/O mode • 2-wire serial I/O mode • SBI mode	
	• LSB first/MSB first switchable	
Bit sequential buffer	Special bit manipulation memory: 16 bits • Perfect for remote control application	
Clock output function	Timer/event counter output (PTO0): square-wave output frequency specifiable	
	Clock output (PCL): Φ, 524, 262, 65.5 kHz (@ 4.19 MHz)	
	Buzzer output (BUZ): 2 kHz (@ 4.19 MHz or 32.768 kHz)	
Vectored interrupt	• External : 3 • Internal : 3	
Test input	• External : 1 • Internal : 1	
System clock oscillator	• Ceramic or crystal oscillator for main system clock oscillation: 4.194304 MHz • Crystal oscillator for subsystem clock oscillation: 32.768 kHz	
Standby	STOP/HALT mode	
Package	• 80-pin plastic QFP (14 x 14 mm) • 80-pin plastic TQFP (Fine pitch) (12 x 12 mm)	

CONTENTS

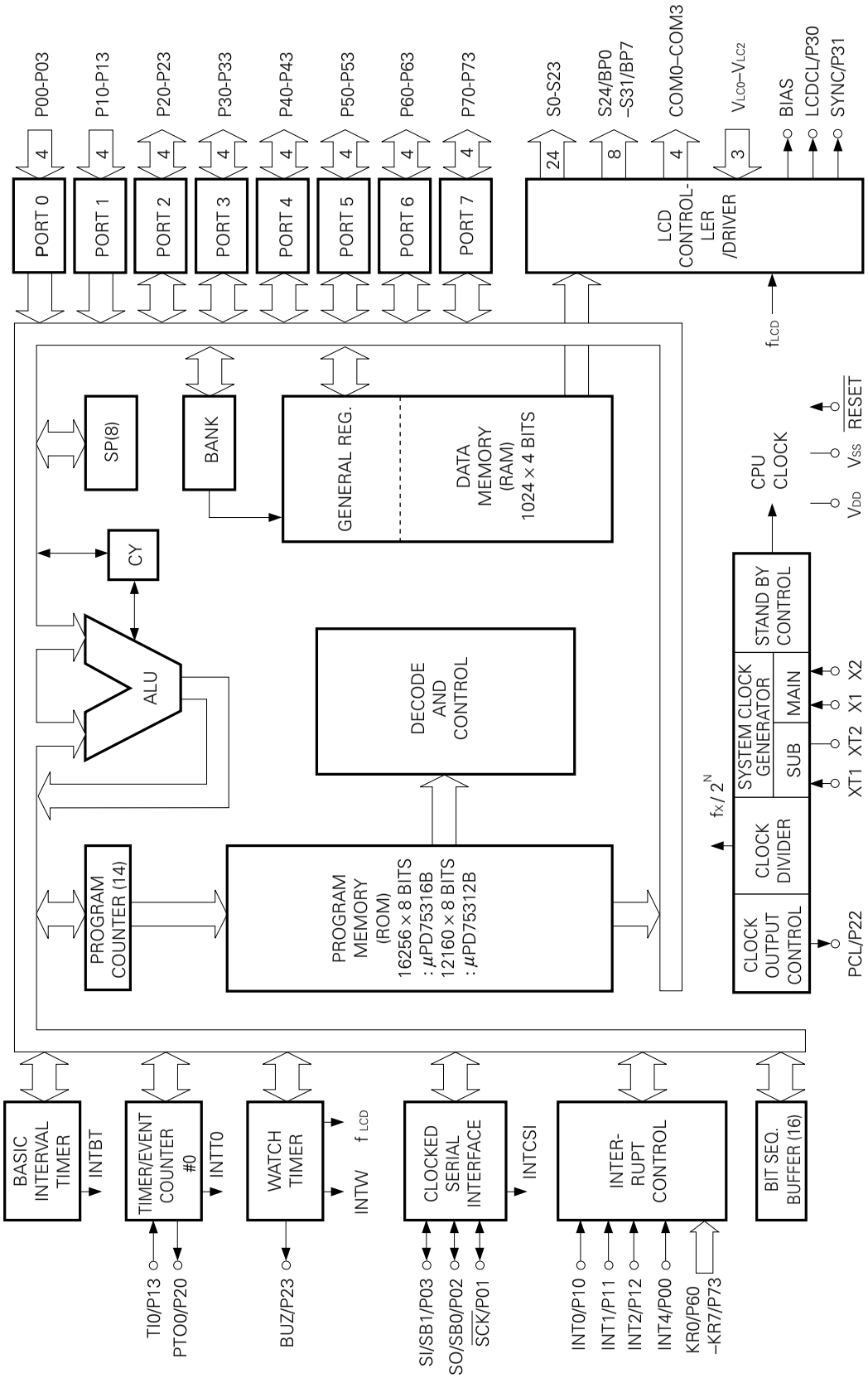
1. PIN CONFIGURATION (TOP VIEW)



***** IC (Internally Connected) pin should be directly connected to V_{DD}.

P00 to 03	: Port 0	S0 to 31	: Segment Output 0 to 31
P10 to 13	: Port 1	COM0 to 3	: Common Output 0 to 3
P20 to 23	: Port 2	V_{LC0-2}	: LCD Power Supply 0 to 2
P30 to 33	: Port 3	BIAS	: LCD Power Supply Bias Control
P40 to 43	: Port 4	LCDCL	: LCD Clock
P50 to 53	: Port 5	SYNC	: LCD Synchronization
P60 to 63	: Port 6	TI0	: Timer Input 0
P70 to 73	: Port 7	PTO0	: Programmable Timer Output 0
BP0 to 7	: Bit Port	BUZ	: Buzzer Clock
KR0 to 7	: Key Return	PCL	: Programmable Clock
$\overline{SCK}$	: Serial Clock	INT0, 1, 4	: External Vectored Interrupt 0, 1, 4
SI	: Serial Input	INT2	: External Test Input 2
SO	: Serial Output	X1, 2	: Main System Clock Oscillation 1, 2
SB0,1	: Serial Bus 0, 1	XT1, 2	: Subsystem Clock Oscillation 1, 2
$\overline{RESET}$	: Reset Input	IC	: Internally Connected

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0) On-chip pull-up resistor can be specified for P01 to P03 as a 3-bit unit by software.	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ - A
P02	Input/output	SO/SB0				Ⓕ - B
P03	Input/output	SI/SB1				Ⓜ - C
P10	Input	INT0	With noise elimination function 4-bit input port (PORT 1) On-chip pull-up resistor can be specified as a 4-bit unit by software.	×	Input	Ⓑ - C
P11		INT1				
P12		INT2				
P13		TI0				
P20	Input/output	PTO0	4-bit input/output port (PORT 2) On-chip pull-up resistor can be specified as a 4-bit unit by software.	×	Input	E - B
P21		—				
P22		PCL				
P23		BUZ				
P30 *2	Input/output	LCDCL	Programmable 4-bit input/output port (PORT 3) Input/output can be specified bit-wise. On-chip pull-up resistor can be specified as a 4-bit unit by software.	×	Input	E - B
P31 *2		SYNC				
P32 *2		—				
P33 *2		—				
P40 to P43 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 4) On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: 10-V withstand voltage	○	High level (on-chip pull-up resistor) or high-impedance	M
P50 to P53 *2	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 5) On-chip pull-up resistor can be specified bit-wise (mask option). Open-drain: 10-V withstand voltage		High level (on-chip pull-up resistor) or high-impedance	M

* **1.** ◯ : Schmitt triggered input
2. LED direct drive possible

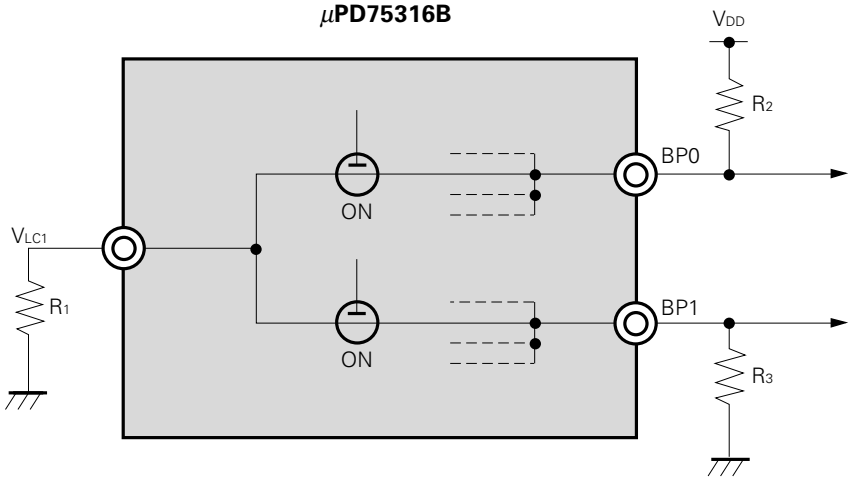
3.1 PORT PINS (2/2)

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	Reset	I/O Circuit Type *1
P60	Input/output	KR0	Programmable 4-bit input/output port (PORT 6) Input/output can be specified bit-wise. On-chip pull-up resistor can be specified as a 4-bit unit by software.	○	Input	Ⓕ - A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/output	KR4	4-bit input/output port (PORT 7) On-chip pull-up resistor can be specified as a 4-bit unit by software.		Input	Ⓕ - A
P71		KR5				
P72		KR6				
P73		KR7				
BP0	Output	S24	1-bit output port (BIT PORT) Also used as segment output pin.	×	* 2	G - C
BP1		S25				
BP2		S26				
BP3		S27				
BP4	Output	S28				
BP5		S29				
BP6		S30				
BP7		S31				

* **1.** ◯ : Schmitt triggered input
2. BP0 to BP7 select V_{LC1} as the input source.
However, the output level depends on BP0 to BP7 and V_{LC1} external circuit.

Example BP0 to BP7 are connected mutually within the μPD75316B. Therefore, the output level of BP0 to BP7 is determined by the value of R1, R2 and R3.

μPD75316B



3.2 NON-PORT PINS

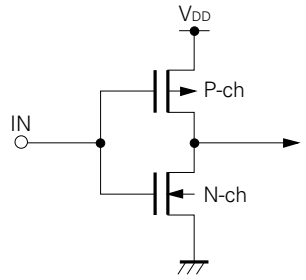
Pin Name	Input/Output	Dual-Function Pin	Function		Reset	I/O Circuit Type *1
TI0	Input	P13	External event pulse input pin to timer/event counter		Input	Ⓑ - C
PTO0	Input/output	P20	Timer/event counter output pin		Input	E - B
PCL	Input/output	P22	Clock output pin		Input	E - B
BUZ	Input/output	P23	Fixed frequency output pin (for buzzer or system clock trimming)		Input	E - B
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin		Input	Ⓕ - A
SO/SB0	Input/output	P02	Serial data output pin Serial bus input/output pin		Input	Ⓕ - B
SI/SB1	Input/output	P03	Serial data input pin Serial bus input/output pin		Input	Ⓜ - C
INT4	Input	P00	Edge detection vectored interrupt input pin (both rising edge and falling edge detection effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input pin (detection edge selectable)	Clocked	Input	Ⓑ - C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input pin (rising edge detection)	Asynchronous	Input	Ⓑ - C
KR0 to KR3	Input/output	P60 to P63	Parallel falling edge detection testable input pin		Input	Ⓕ - A
KR4 to KR7	Input/output	P70 to P73	Parallel falling edge detection testable input pin		Input	Ⓕ - A
S0 to S23	Output	—	Segment signal output pin		*2	G - A
S24 to S31	Output	BP0 to BP7	Segment signal output pin		*2	G - C
COM0 to COM3	Output	—	Common signal output pin		*2	G - B
V_{LC0} to V_{LC2}	—	—	LCD drive power supply pin On-chip split resistor (mask option)		—	—
BIAS	Output	—	External split resistor cut output pin		*3	—
LCDCL *4	Input/output	P30	External expansion driver drive clock output pin		Input	E - B
SYNC *4	Input/output	P31	External expansion driver synchronization clock output pin		Input	E - B
X1, X2	Input	—	Main system clock oscillation crystal/ceramic connection pin. For external clock, the external clock signal is input to X1 and the inverted phase is input to X2.		—	—
XT1	Input	—	Subsystem clock oscillation crystal connection pin. For external clock, the external clock signal is input to XT1 and XT2 is opened. XT1 can be used as a 1-bit input (test) pin.		—	—
XT2	—	—				
$\overline{RESET}$	Input	—	System reset input pin		—	Ⓑ
IC	—	—	Internally Connected. Directly connected to V_{DD}.		—	—
V_{DD}	—	—	Positive power supply pin		—	—
V_{SS}	—	—	GND potential pin		—	—

*** 1.** ○ : Schmitt triggered input
*** 2.** Display outputs are selected with V_{LCX} shown below as the input source.
S0 to S31: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}
However, the level of each display output depends on the display output and VLCX external circuit.
*** 3.** On-chip split resistor.....Low level
No on-chip split resistor... High-impedance
*** 4.** Pins provided for system expansion. Currently, only used as P30 and P31 pins.

3.3 PIN INPUT/OUTPUT CIRCUITS

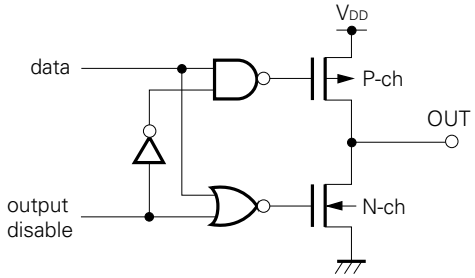
The input/output circuits of each pin of the μPD75316B are shown in schematic form.

TYPE A (For TYPE E-B)



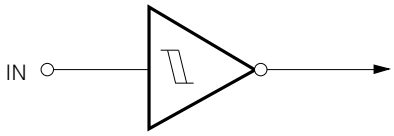
CMOS Standard Input Buffer

TYPE D (For TYPE E-B, F-A)



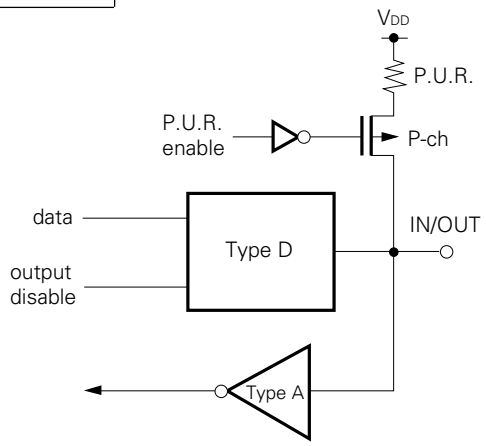
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

TYPE B



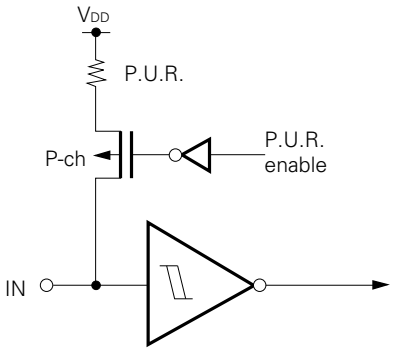
Schmitt-Triggered Input with Hysteresis Characteristic

TYPE E-B



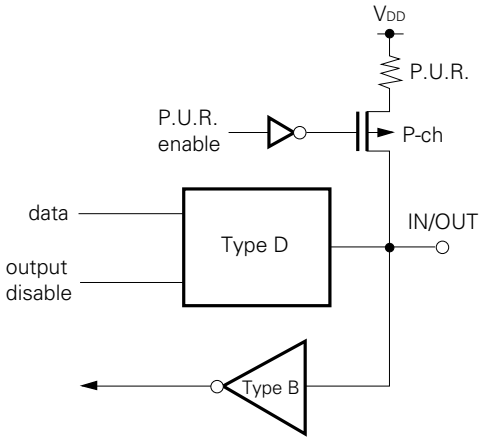
P.U.R.:Pull-Up Resistor

TYPE B-C



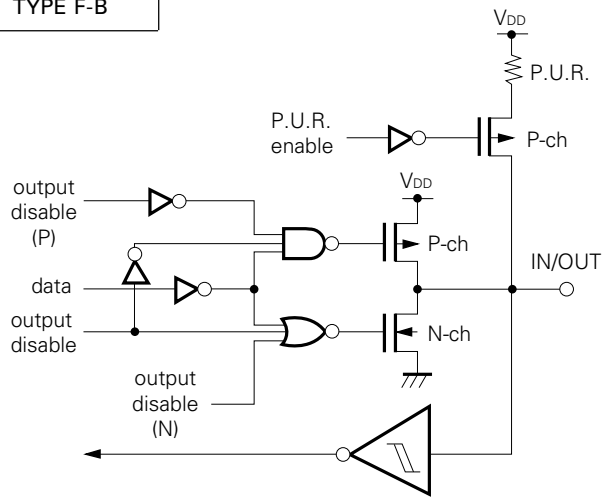
P.U.R. : Pull-Up Resistor

TYPE F-A



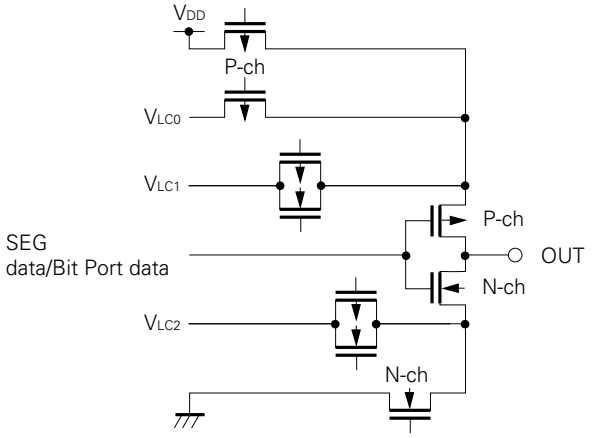
P.U.R.:Pull-Up Resistor

TYPE F-B

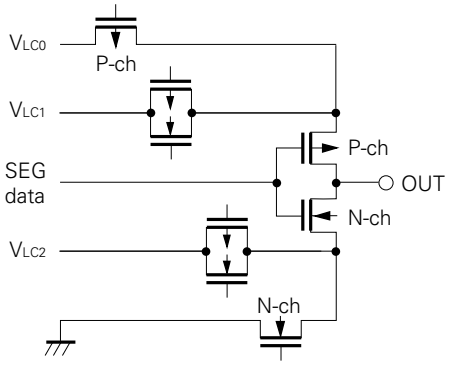


P.U.R.:Pull-Up Resistor

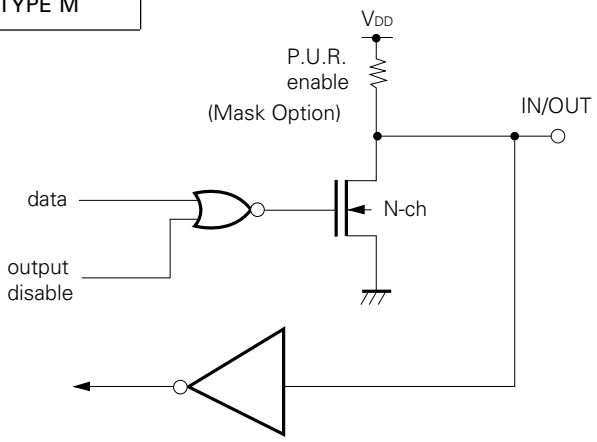
TYPE G-C



TYPE G-A



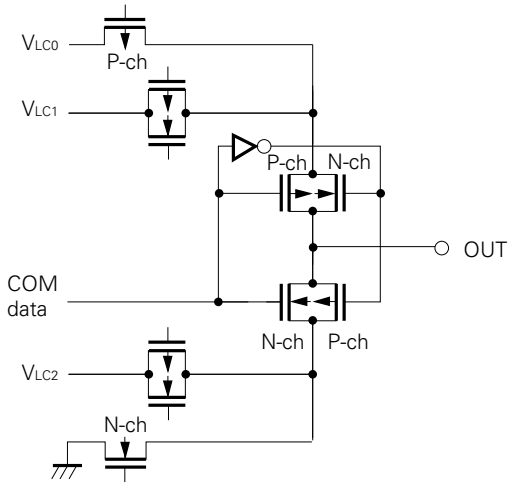
TYPE M



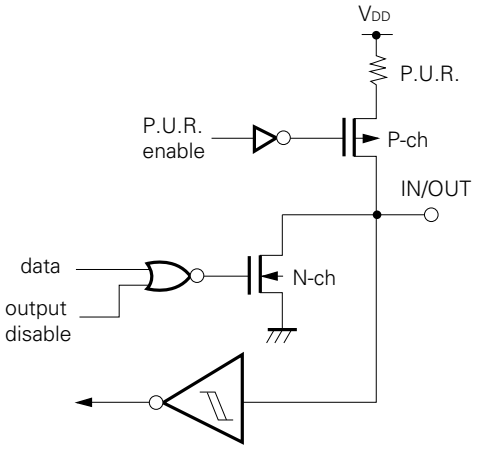
Middle-High Voltage Input Buffer
(+10 V Withstand Voltage)

P.U.R.:Pull-Up Resistor

TYPE G-B



TYPE M-C



P.U.R.:Pull-Up Resistor

3.4 RECOMMENDED CONNECTION OF UNUSED PINS

Table 3-1 List of Recommended Connection of Unused Pins

Pin	Recommended Connection
P00/INT4	Connect to V_{SS}.
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}.
P02/SO/SB0	
P03/SI/SB1	
P10/INT0 to P12/INT2	Connect to V_{SS}.
P13/T10	
P20/TO0	Input state : Connect to V_{SS} or V_{DD}. Output state : Leave open.
P21	
P22/PCL	
P23/BUZ	
P30/LCDCL	
P31/SYNC	
P32	
P33	
P40 to P43	
P50 to P53	
P60/KR0 to P63/KR3	
P70/KR4 to P73/KR7	
S0 to S23	Leave open.
S24/BP0 to S31/BP7	
COM0 to COM3	
V_{LC0} to V_{LC2}	Connect to V_{SS}.
BIAS	Connect to V_{SS} when V_{LC0} to V_{LC2} unused. Otherwise leave open.
XT1	Connect to V_{SS} or V_{DD}.
XT2	Leave open.
IC	Directly connect to V_{DD}.

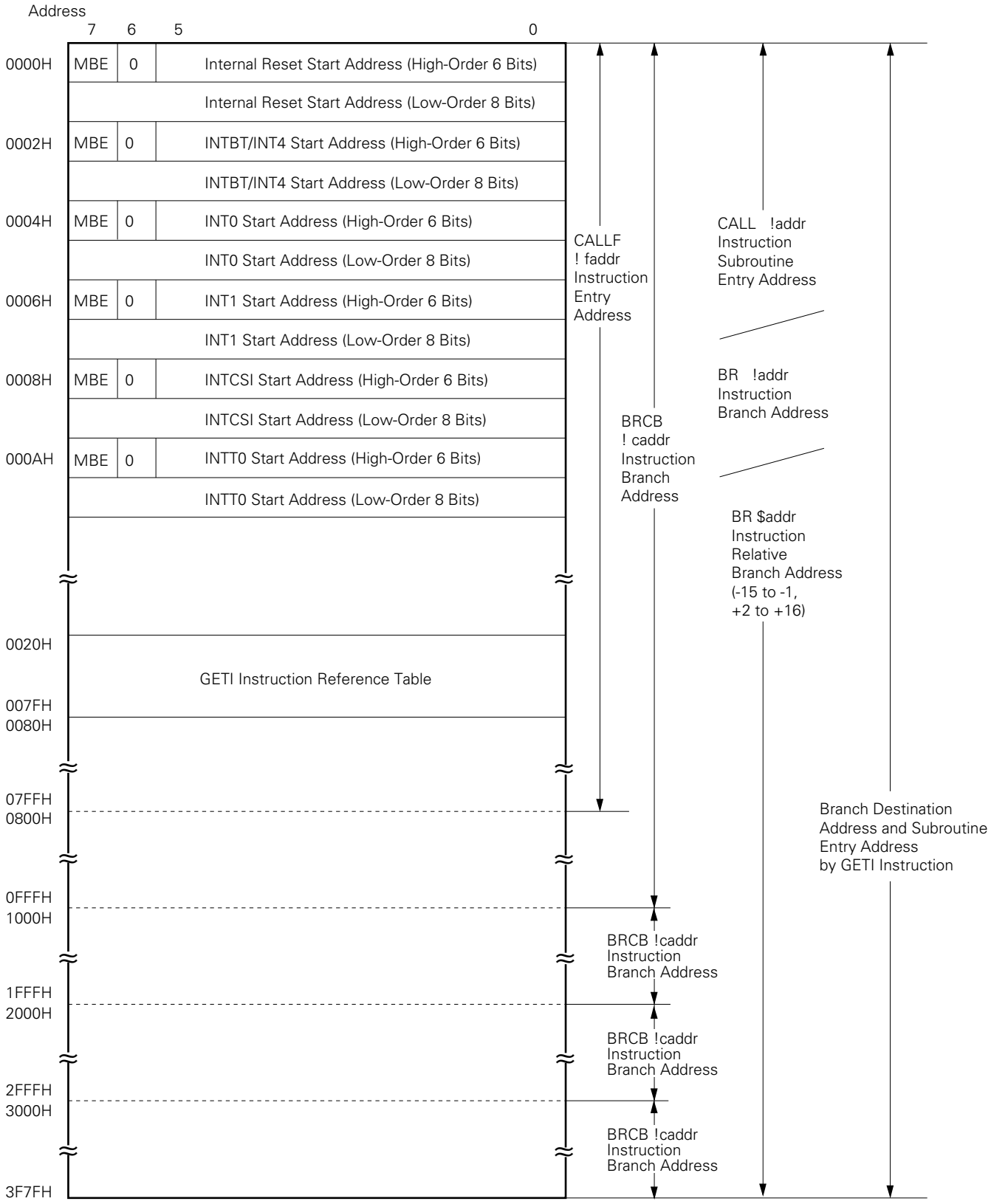
4. MEMORY CONFIGURATION

- Program memory (ROM) ... 16256 × 8 bits (0000H to 3F7FH) : μPD75316B
  ... 12160 × 8 bits (0000H to 2F7FH) : μPD75312B
  - 0000H to 0001H : Vector table in which program start address by reset is written.
  - 0002H to 000BH : Vector table in which program start address by interrupt is written.
  - 0020H to 007FH : Table area that is referred by GETI instruction.

- Data Memory
  - Data area ... 1024 × 4 bits (000H to 3FFH)
  - Peripheral hardware area ... 128 × 4 bits (F80H to FFFH)

Fig. 4-1 Program Memory Map

(a) μPD75316B



(b) μPD75312B

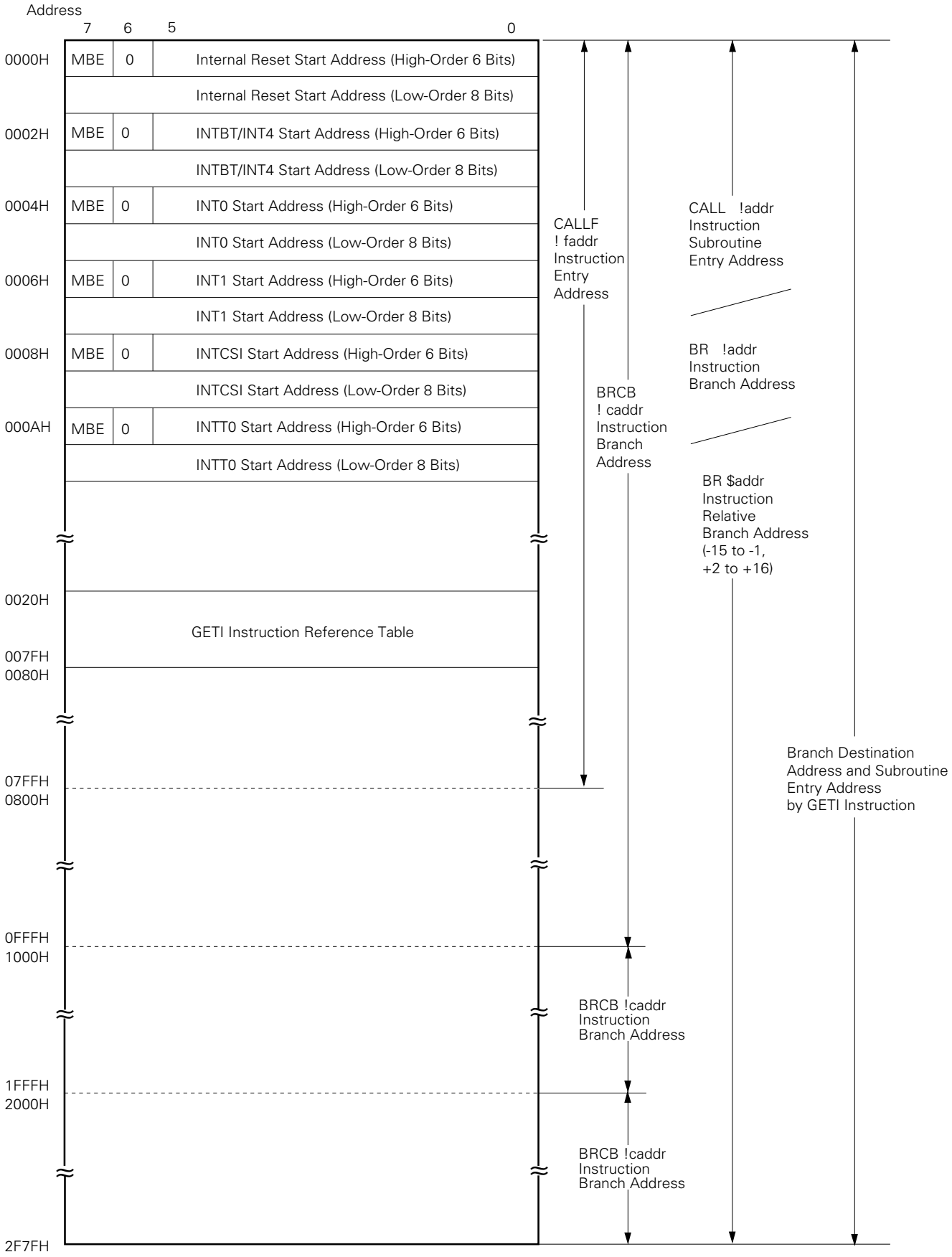
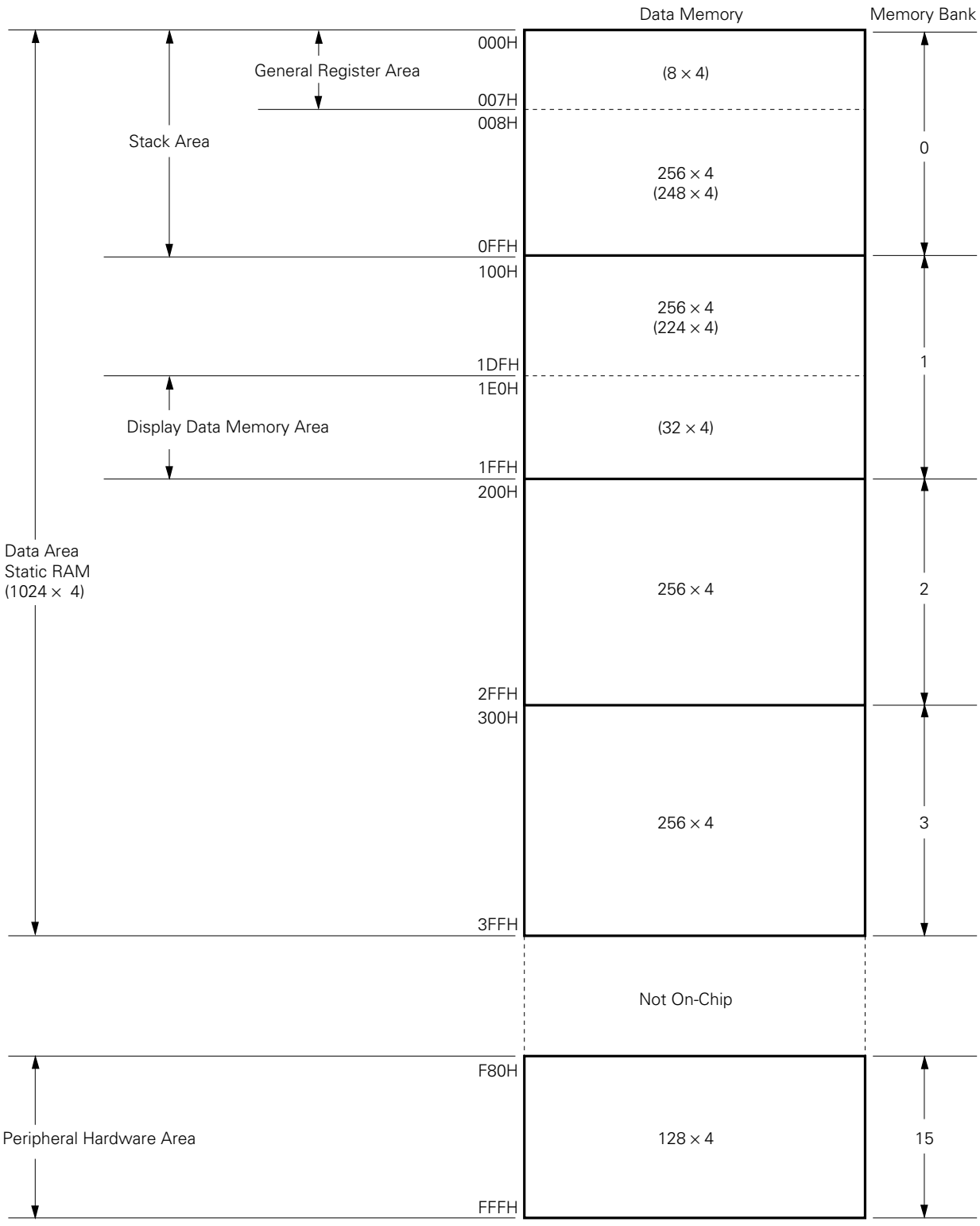

Address
7
6
5
0
0000H
MBE
0
Internal Reset Start Address (High-Order 6 Bits)
Internal Reset Start Address (Low-Order 8 Bits)
0002H
MBE
0
INTBT/INT4 Start Address (High-Order 6 Bits)
INTBT/INT4 Start Address (Low-Order 8 Bits)
0004H
MBE
0
INT0 Start Address (High-Order 6 Bits)
INT0 Start Address (Low-Order 8 Bits)
0006H
MBE
0
INT1 Start Address (High-Order 6 Bits)
INT1 Start Address (Low-Order 8 Bits)
0008H
MBE
0
INTCSI Start Address (High-Order 6 Bits)
INTCSI Start Address (Low-Order 8 Bits)
000AH
MBE
0
INTT0 Start Address (High-Order 6 Bits)
INTT0 Start Address (Low-Order 8 Bits)
0020H
GETI Instruction Reference Table
007FH
0080H
07FFH
0800H
0FFFH
1000H
1FFFH
2000H
2F7FH
CALLF
! faddr
Instruction
Entry
Address
CALL !addr
Instruction
Subroutine
Entry Address
BR !addr
Instruction
Branch Address
BRCB
! caddr
Instruction
Branch
Address
BR $addr
Instruction
Relative
Branch Address
(-15 to -1,
+2 to +16)
Branch Destination
Address and Subroutine
Entry Address
by GETI Instruction
BRCB !caddr
Instruction
Branch Address
BRCB !caddr
Instruction
Branch Address

Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O Ports has 4 types

- CMOS input (PORT0, 1) : 8
- CMOS input/output (PORT2, 3, 6, 7) : 16
- N-ch open-drain (PORT4, 5) : 8
- CMOS output (BP0 to BP7) : 8

Total 40

Table 5-1 Port Function

Port (Symbol)	Function	Operation/Features	Remarks
PORT0	4-bit input	This port can be used for reading or testing regardless of the operating mode of the dual-function pin.	Dual-function as pins INT4, $\overline{SCK}$, SO/B0, SI/B1.
PORT1			Dual-function as pins INT0 to INT2 and TI0.
PORT3*	4-bit input/output	Can be set to 1-bit input or output mode.	Dual-function as pins LCDCL and SYNC.
PORT6			Dual-function as pins KR0 to KR3.
PORT2		Can be set to 4-bit input or output mode. Ports 6 and 7 can be paired for 8-bit data input or output.	Dual-function as pins PTO0, PCL, BUZ.
PORT7			Dual-function as pins KR4 to KR7.
PORT4* PORT5*	4-bit input/output (N-ch open-drain, 10-V withstand voltage)	Can be set to 4-bit input or output mode. Ports 4 and 5 can be paired for 8-bit data input or output.	On-chip pull-up resistor specifiable bit-wise by mask oftion.
BP0 to BP7	1-bit output	Data output in 1-bit units. It is possible to switch the output drive segment output S24 to S31 using the software.	The drive capability is small. For CMOS load drive.

* LED can be driven directly.

5.2 CLOCK GENERATOR

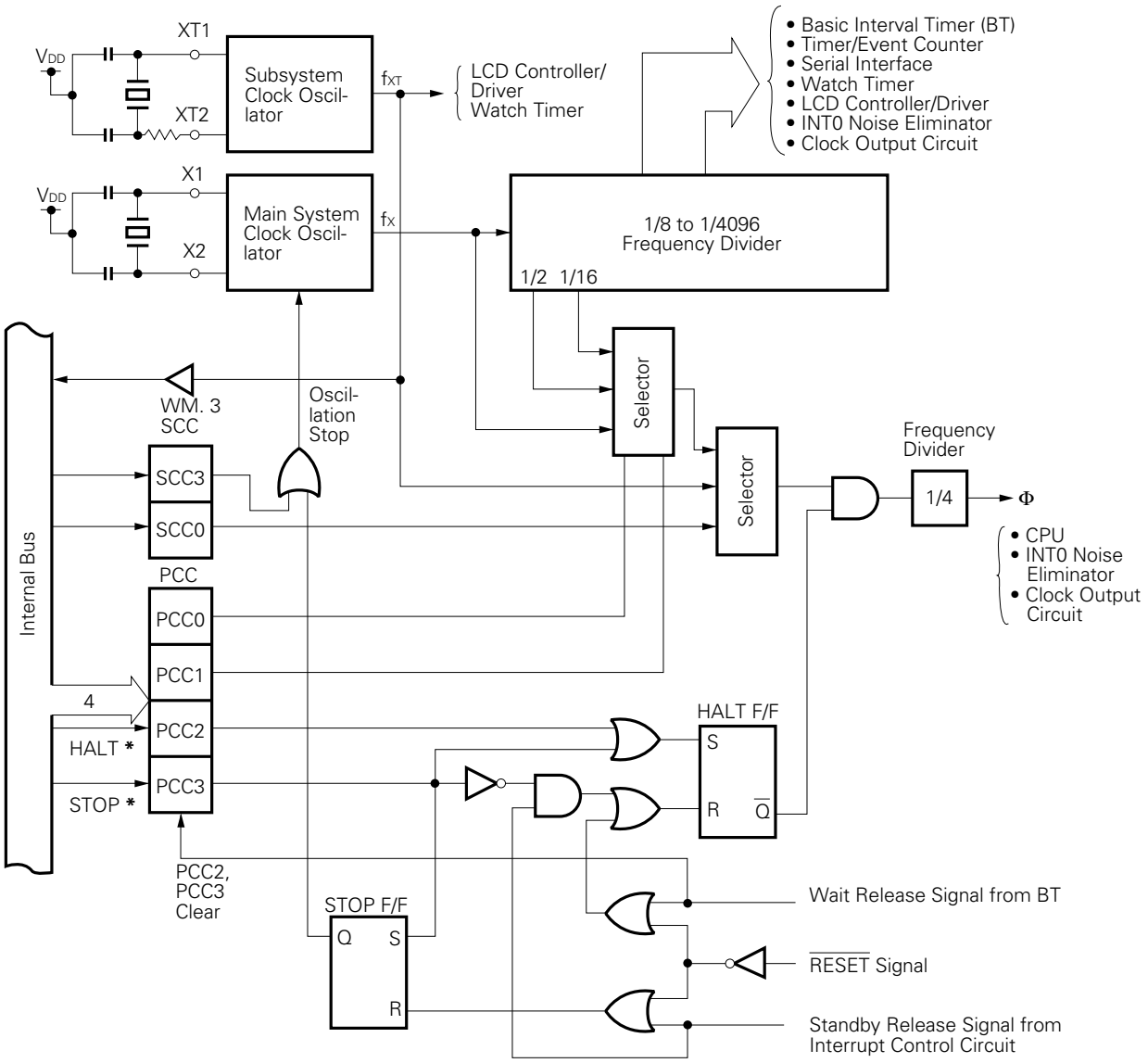
The operation of the clock generator circuit is determined by the processor clock control register (PCC) and the system clock control register (SCC).

There are two kinds of clocks; the main system clock and the subsystem clock.

It is also possible to change the instruction execution time.

- 0.95 μs/1.91 μs/15.3 μs (main system clock: @ 4.19 MHz)
- 122 μs (sub-system clock: @ 32.768 kHz)

Fig. 5-1 Clock Generator Block Diagram



fX: Main system clock frequency

fXT: Subsystem clock frequency

Φ : CPU clock

PCC: Processor clock control register

SCC: System clock control register

Remarks 1. * indicates instruction execution.

2. Φ one clock cycle (t_{CY}) is one machine cycle instruction. For t_{CY}, refer to AC characteristics in "**11 ELECTRICAL SPECIFICATIONS**."

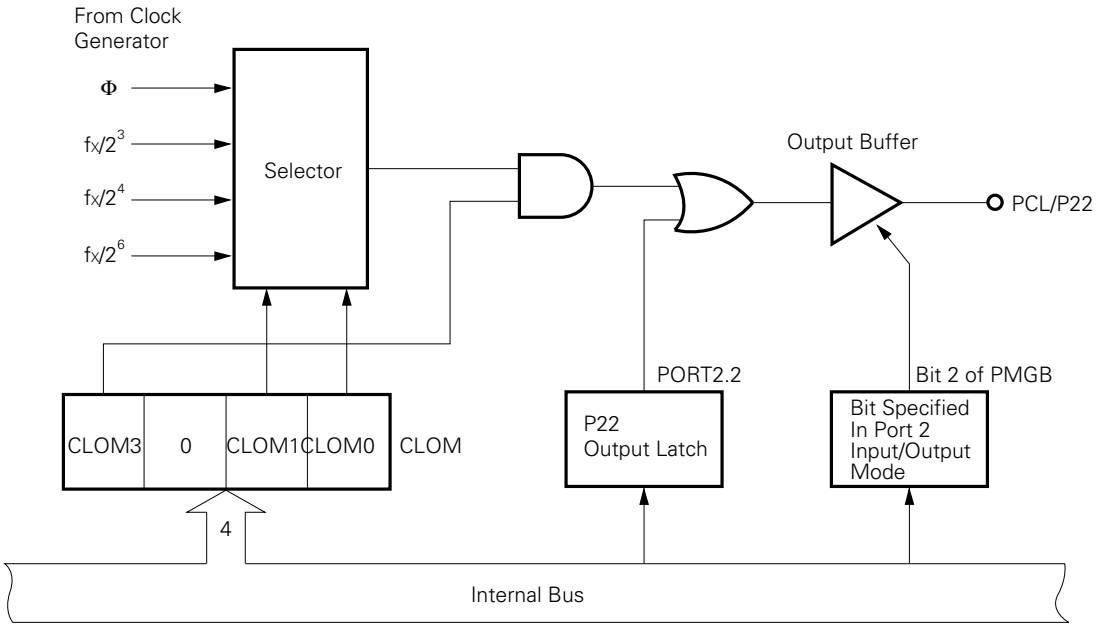
5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit is used for outputting the clock pulse from the P22/PCL pins. It is used, for example, when a clock pulse is to be output to the remote control output, peripheral LSI, etc..

- Clock output (PCL) : Φ , 524, 262, 65.5 kHz (4.19 MHz operation)

The configuration of the clock output circuit is shown below.

Fig. 5-2 Clock Output Circuit Configuration



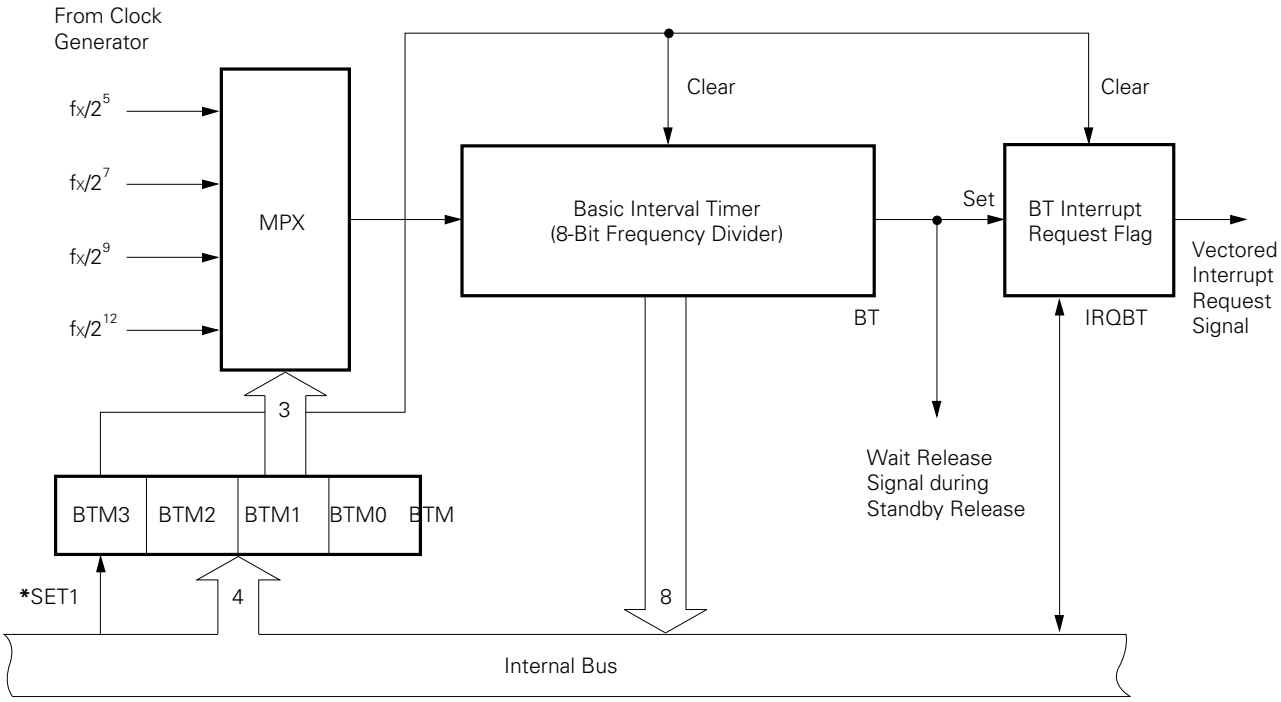
Remark Consideration is given so that a low-amplitude pulse is not output when switching between clocks.

5.4 BASIC INTERVAL TIMER

The basic interval timer includes the following functions.

- It operates as an interval timer which generates reference time interrupts.
- It can be applied as a watchdog timer which detects inadvertent program loop.
- Selects and counts wait times when the standby mode is released.
- It reads count contents.

Fig. 5-3 Basic Interval Timer Configuration



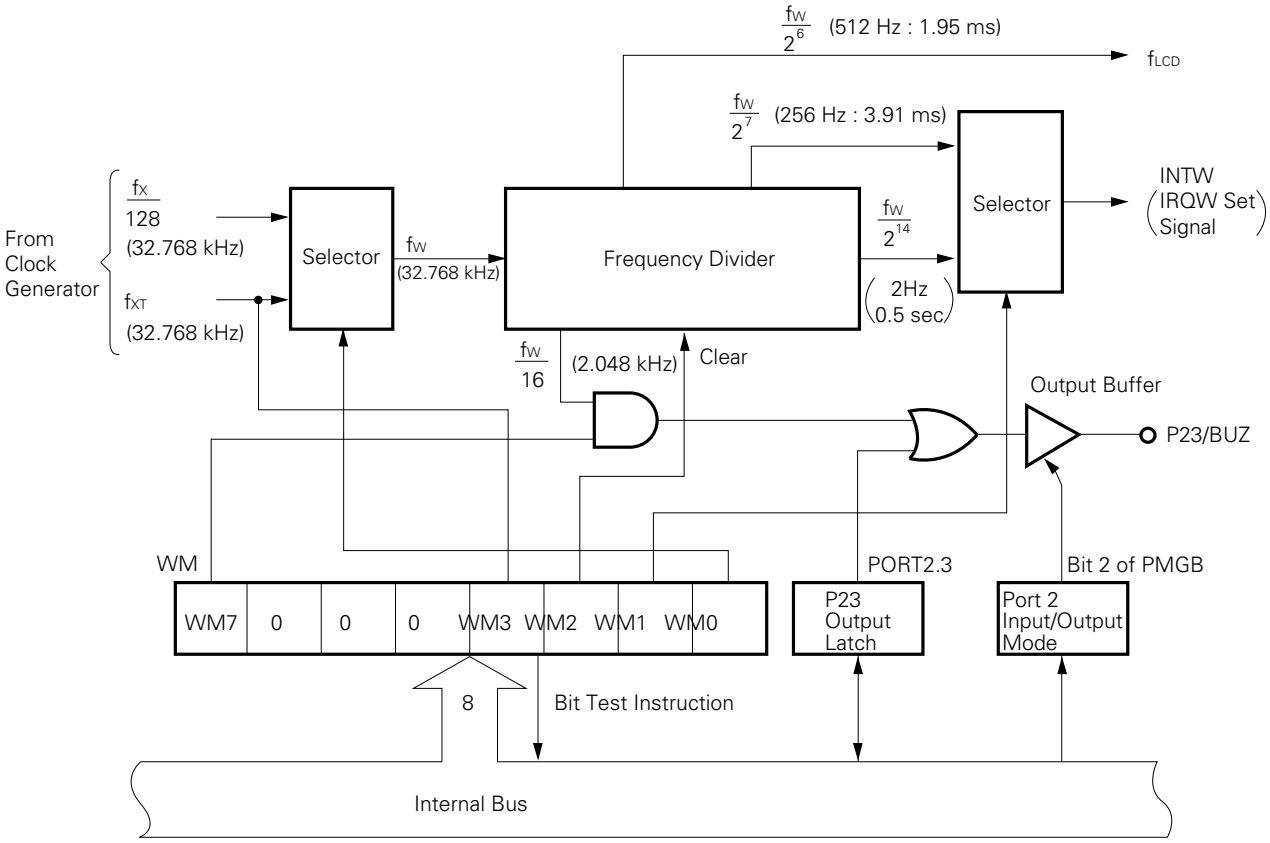
Remark * indicates instruction execution.

5.5 WATCH TIMER

The μPD75316B incorporates a watch timer channel. The watch timer has the following functions.

- Sets test flags (IRQW) at 0.5-second intervals.
  The standby mode can be released with IRQW.
- 0.5-second time intervals can be created in either the main system clock or the subsystem clock.
- In the rapid feed mode, time intervals which are 128 times normal (3.91 ms) can be set, making this function convenient for program debugging and testing.
- A fixed frequency (2.048 kHz) can be output to the P23/BUZ pin for use in generating buzzer sounds and trimming system clock oscillator frequencies.
- The frequency divider can be cleared, enabling creation of watches that can start from 0 second.

Fig. 5-4 Watch Timer Block Diagram



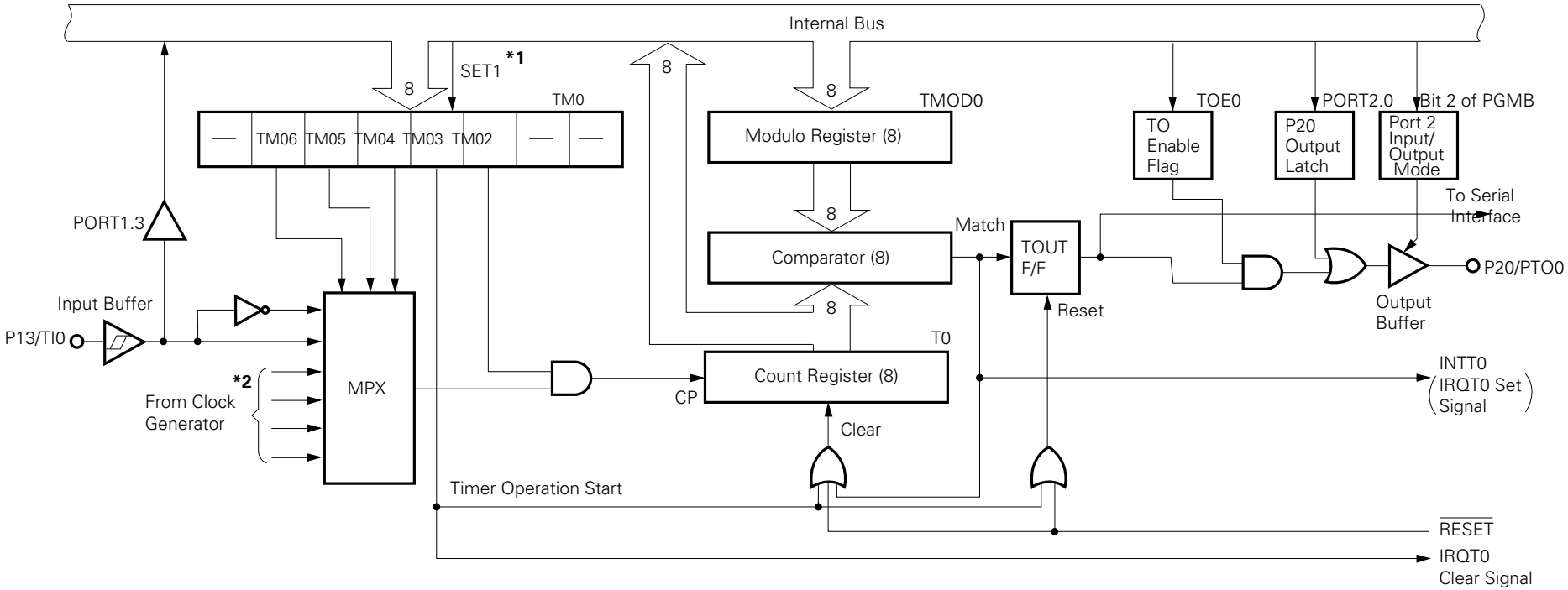
Remark Values in parentheses are when f_X = 4.194304 MHz and f_{XT} = 32.768 kHz.

5.6 TIMER/EVENT COUNTER

The μPD75316B incorporates a timer/event counter channel. The functions of the timer/event counter are as follows.

- Operates as a programmable interval timer.
- Outputs square waves in the desired frequency to the PTO0 pin.
- Operates as an event counter.
- Divides the TI0 pin input into N divisions and outputs it to the PTO0 pin (frequency divider operation).
- Supplies a serial shift clock to the serial interface circuit.
- Count status read function.

Fig. 5-5 Timer/Event Counter Block Diagram



* **1.** SET1: Instruction execution

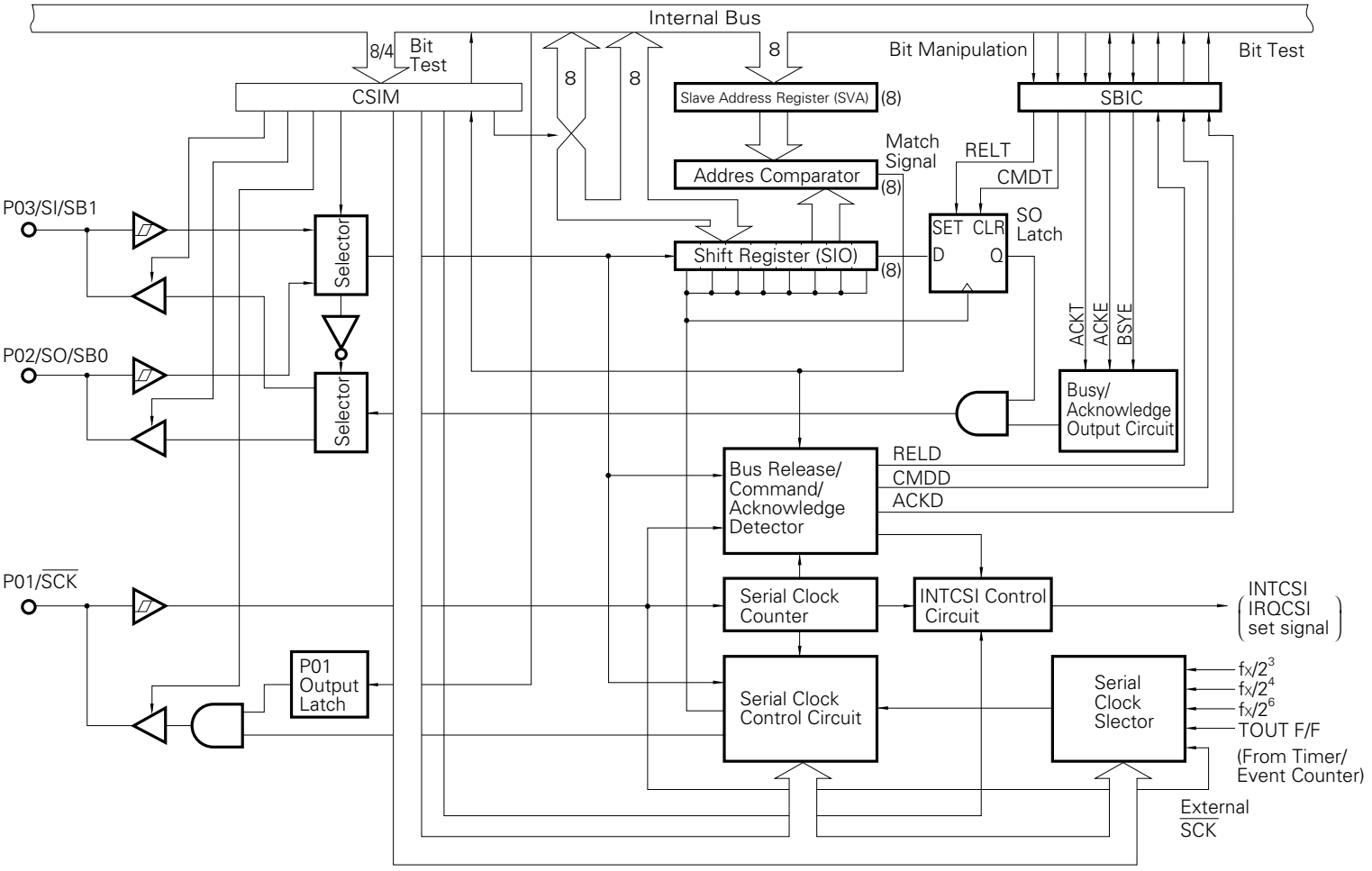
2. For detail, see **Fig. 5-1.**

5.7 SERIAL INTERFACE

The μPD75316B incorporates a clocked 8-bit serial interface which has the following three types of mode.

- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode (serial bus interface mode)

Fig. 5-6 Serial Interface Block Diagram



5.8 LCD CONTROLLER/DRIVER

The μPD75316B has an on-chip display controller which generates segment signals and common signals in accordance with data in display data memory as well as a segment driver and common driver capable of directly driving the LCD panel.

The configuration of the LCD controller/driver is shown in Fig. 5-7.

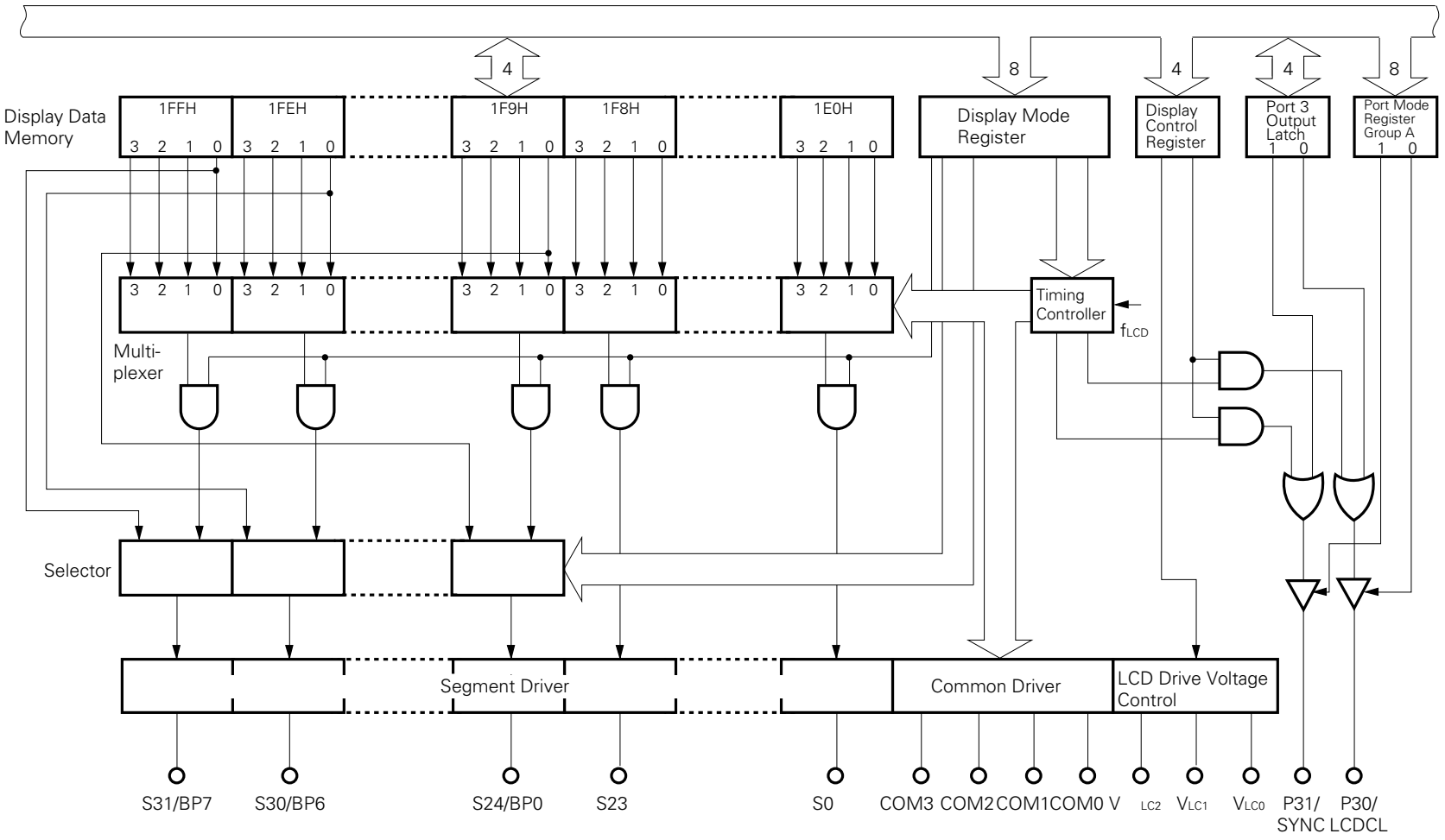
The functions of the LCD controller/driver are as follows.

- Display data memory are read automatically through DMA operations and segment signals and common signals are generated.
- 5 different display modes can be selected.

① Static
② 1/2 duty (1/2 bias)
③ 1/3 duty (1/2 bias)
④ 1/3 duty (1/3 bias)
⑤ 1/4 duty (1/3 bias)

- In each of the display modes, 4 types of frame frequency can be selected.
- The segment signal output is a maximum of 32 segments (S0 to S31) and 4 common outputs (COM0 to COM3).
- Segment signal outputs (S24 to S27, S28 to S31) are in 4-segment units and they can be switched for use as output ports (BP0 to BP3, BP4 to BP7).
- Split resistors can be incorporated for the LCD drive power supply (mask option).
  - Conformity to various bias methods and LCD drive voltages is possible.
  - When the display is OFF, the current flowing to the split resistors is cut.
- Display data memory not used for the display can be used as ordinary data memory.
- Operation by the subsystem clock is also possible.

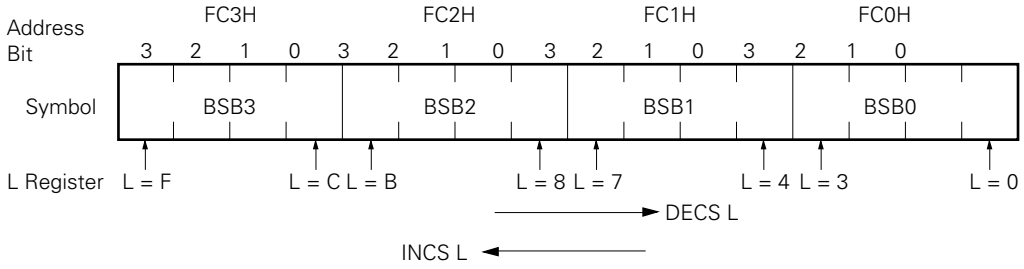
Fig. 5-7 LCD Controller/Driver Block Diagram



5.9 BIT SEQUENTIAL BUFFER ..... 16 BITS

The bit sequential buffer is special data memory for bit manipulations and can be used easily particularly for bit manipulations where addresses and bit specifications are changed sequentially, so it is convenient for processing data with long bit lengths bit-wise.

Fig. 5-8 Bit Sequential Buffer Format



Remark In "pmem.@L" addressing, the specified bit corresponding to the L register is moved.

6. INTERRUPT FUNCTION

The μPD75316B has six interrupt sources which enable multiple interrupt by software control. It also has two test sources, of which the INT2 has two edge detection testable inputs.

Table 6-1. Types of Interrupt Sources

Interrupt sources		Internal/external	Interrupt priority[Note 1]	Vectored interrupt request signal (vector table address)
INTBT	(standard interval signal from basic interval timer)	Internal	1	VRQ1 (0002H)
INT4	(both rising and falling edge detection are valid.)	External		
INT0	(Rising or falling detection edge is selected.)	External	2	VRQ2 (0004H)
INT1		External	3	VRQ3 (0006H)
INTCSI	(serial data transfer end signal)	Internal	4	VRQ4 (0008H)
INTT0	(match signal between the count register and modulo register of programmable timer/counter)	Internal	5	VRQ5 (000AH)
INT2[Note 2]	(rising edge detection of input to INT2 pin or falling edge detection of input to KR0-KR7)	External	Testable input signal (IRQ2 and IRWQ are set.)	
INTW[Note 2]	(signal from clock timer)	Internal		

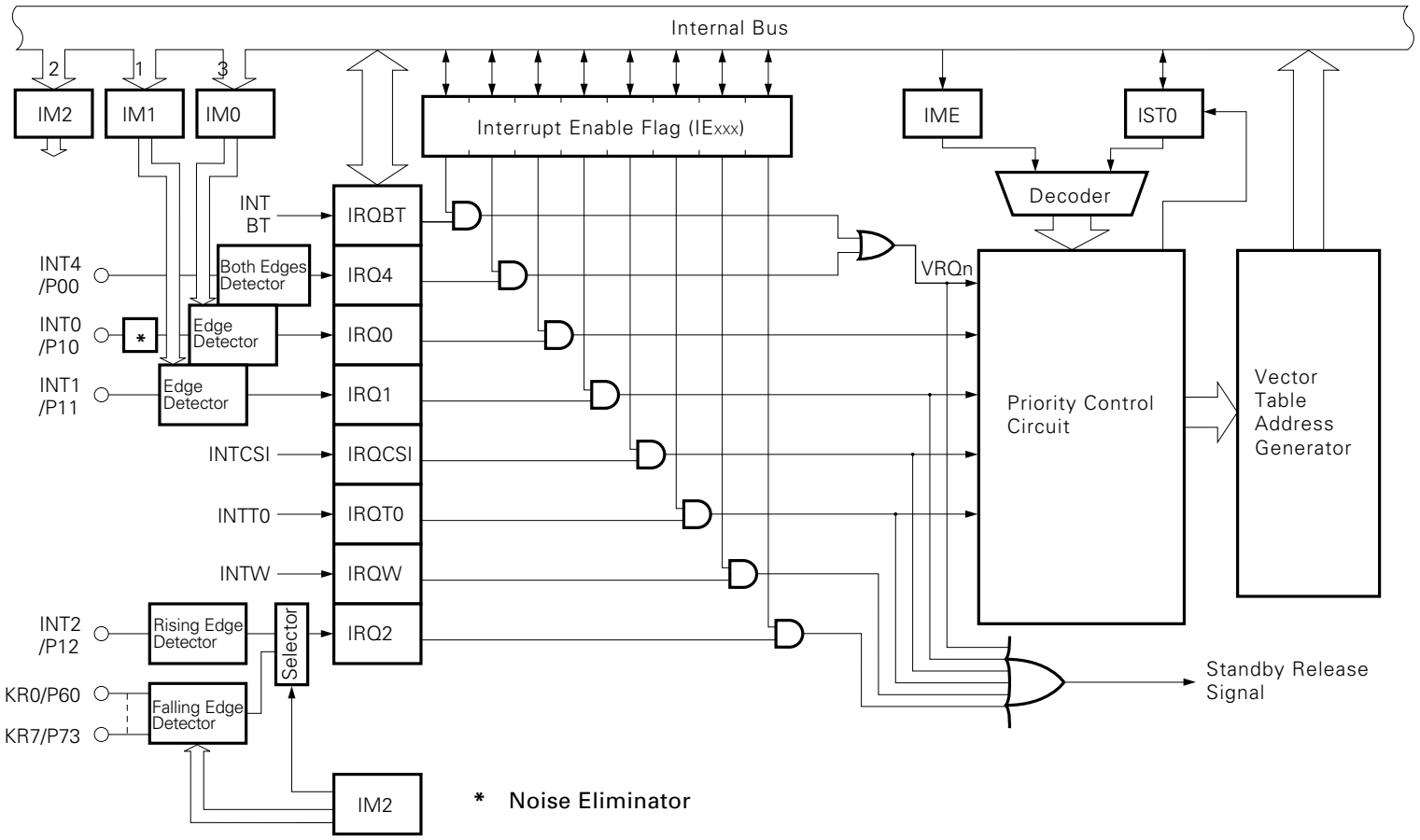
Notes 1. Interrupt priority is serviced according to the order of priority, when several interrupt requests are generated simultaneously.

2. Test source. They are affected by the interrupt enable flag in the same way as the interrupt source, but no vectored interrupt is generated.

The μPD75316B interrupt control circuit has the following functions:

- Hardware control vectored interrupt function that can control interrupt acknowledgement by interrupt flag (IE×××) and interrupt master enable flag (IME).
- Interrupt start address can be set.
- Interrupt request flag (IRQ×××) test function (interrupt generation confirmation by software possible).
- Standby mode release (selection of interrupt that releases the standby mode by interrupt enable flag possible).

Fig.6-1 Interrupt Control Circuit Block Diagram



7. STANDBY FUNCTION

To reduce the power consumption during program wait, the μPD75316B has two standby modes: STOP mode and HALT mode.

Table 7-1 Operation Status at Standby Mode

		STOP Mode	HALT Mode
Setting instruction		STOP instruction	HALT instruction
System clock at setting		Only main system clock settable	Main system clock or subsystem clock settable
Operation Status	Clock generator	Only main system clock oscillation stopped	Only CPU clock Φ stopped (oscillation continued)
	Basic interval timer	Stopped	Operable (IRQBT set at reference time intervals)*
	Serial interface	Operable only when external $\overline{SCK}$ input selected as serial clock	Operable*
	Timer/event counter	Operable only when TI0 pin input specified as count clock	Operable*
	Watch timer	Operable only when f_{XT} selected as count clock	Operable
	LCD controller	Operable only when f_{XT} selected as LCDCL	Operable
	External interrupt	INT1, 2, 4: Operable Only INT0 inoperable	
	CPU	Stopped	
Release signal		Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input	Interrupt request signal from operable hardware enabled by interrupt enable flag, or $\overline{RESET}$ input

* Cannot be operable during main system clock stop.

8. RESET FUNCTION

The μPD75316B is reset and the hardware is initialized as shown in Table 8-1 by $\overline{\text{RESET}}$ input. The reset operation timing is shown in Fig. 8-1.

Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

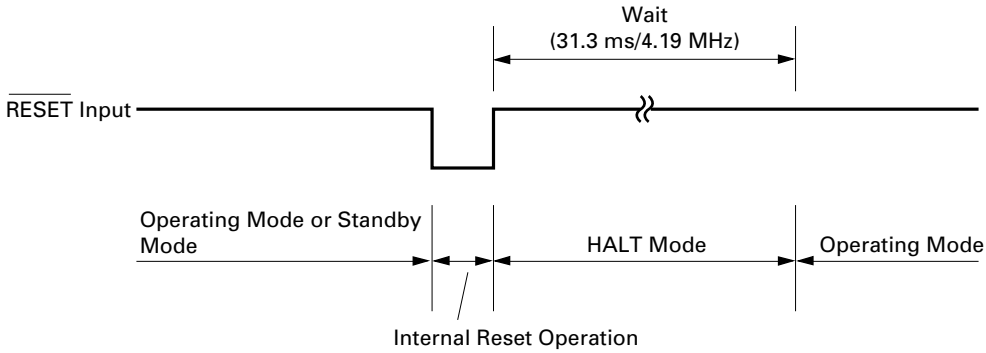


Table 8-1 Status of Each Hardware after Resetting (1/3)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Program counter (PC)		Low-order 6 bits of program memory address 0000H are set in PC13 to 8 and the contents of address 0001H are set in PC7 to 0.	Same as the left
PSW	Carry flag (CY)	Held	Undefined
	Skip flag (SK0 to 2)	0	0
	Interrupt status flag (IST0)	0	0
	Bank enable flag (MBE)	Bit 7 of program memory address 0000H is set in MBE.	Same as the left
Stack pointer (SP)		Undefined	Undefined
Data memory (RAM)		Held*	Undefined
General register (X, A, H, L, D, E, B, C)		Held	Undefined
Bank selection register (MBS)		0	0

* Data of data memory addresses 0F8H to 0FDH becomes undefined by $\overline{\text{RESET}}$ input.

Table 8-1 Status of Each Hardware after Resetting (2/3)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Basic interval timer	Counter (BT)	Undefined	Undefined
	Mode register (BTM)	0	0
Timer/event counter	Counter (T0)	0	0
	Modulo register (TMOD0)	FFH	FFH
	Mode register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch timer	Mode register (WM)	0	0
Serial interface	Shift register (SIO)	Held	Undefined
	Operating mode register (CSIM)	0	0
	SBI control register (SBIC)	0	0
	Slave address register (SVA)	Held	Undefined
Clock generator, clock output circuit	Processor clock control register (PCC)	0	0
	System clock control register (SCC)	0	0
	Clock output mode register (CLOM)	0	0
LCD controller	Display mode register (LCDM)	0	0
	Display control register (LCDC)	0	0
Interrupt function	Interrupt request flag (IRQ×××)	Reset (0)	Reset (0)
	Interrupt enable flag (IE×××)	0	0
	Interrupt master enable flag (IME)	0	0
	INT0, 1, 2 mode registers (IM0, 1, 2)	0, 0, 0	0, 0, 0

Table 8-1 Status of Each Hardware after Resetting (3/3)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Digital port	Output buffer	OFF	OFF
	Output latch	Clear (0)	Clear (0)
	I/O mode register (PMGA, B)	0	0
	Pull-up resistor specification register (POGA)	0	0
Bit sequential buffer (BSB0 to 3)		Held	Undefined

9 INSTRUCTION SET

(1) Operand identifier and description method

The operand is described in the operand field of each instruction in accordance with the description method for the operand identifier of the instruction. For details refer to **RA75X Assembler Package User's Manual Language Volume (EEU-1363)**. When there are multiple elements in the description method, one of the elements is selected. Uppercase letters and symbols (+,–) are keywords and should be described without change as shown.

For immediate data, a suitable value or label is described.

Various register or flag symbols can be used as a label instead of mem, fmem, pmem, bit, etc. (see the **μPD75308 User's Manual (IEM-1263)** for details). However, there are restrictions on the labels for which fmem and pmem can be used.

Identifier	Description	
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L	
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE	
rpa rpa1	HL, DE, DL DE, DL	
n4 n8	4-bit immediate data or label 8-bit immediate data or label	
mem* bit	8-bit immediate data or label 2-bit immediate data or label	
fmem pmem	FB0H to FBFH, FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label	
addr	μPD75312B	0000H to 2F7FH immediate data or label
	μPD75316B	0000H to 3F7FH immediate data or label
caddr	12-bit immediate data or label	
faddr	11-bit immediate data or label	
taddr	20H to 7FH immediate data (however, bit0 = 0) or label	
PORTn IE××× MBn	PORT 0 to PORT 7 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW MB0, MB1, MB2, MB3, MB15	

* For mem, only even addresses can be entered in the case of 8-bit data processing.

(2) Operation description legend

A	:	A register; 4-bit accumulator
B	:	B register;
C	:	C register;
D	:	D register;
E	:	E register;
H	:	H register;
L	:	L register;
X	:	X register;
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
PORTn	:	Portn (n = 0 to 7)
IME	:	Interrupt master enable flag
IE×××	:	Interrupt enable flag
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
.	:	Address, bit delimiter
(××)	:	Contents addressed by ××
××H	:	Hexadecimal data

(3) Description of addressing area field symbols

*1	MB = MBE • MBS (MBS = 0 to 3, 15)		Data Memory Addressing
*2	MB = 0		
*3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 1 : MB = MBS (MBS = 0 to 3, 15)		
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH		
*5	MB = 15, pmem = FC0H to FFFH		
*6	μPD75312B	addr = 0000H to 2F7FH	Program Memory Addressing
	μPD75316B	addr = 0000H to 3F7FH	
*7	addr = (Current PC) –15 to (Current PC) –1, (Current PC) +2 to (Current PC) + 16		
*8	μPD75312B	caddr = 0000H to 0FFFH (PC_{13} = 0, PC_{12} = 0)or 1000H to 1FFFH (PC_{13} = 0, PC_{12} = 1) or 2000H to 2F7FH (PC_{13} = 1, PC_{12} = 0)	
	μPD75316B	caddr = 0000H to 0FFFH (PC_{13} = 0, PC_{12} = 0) or 1000H to 1FFFH (PC_{13} = 0, PC_{12} = 1) or 2000H to 2FFFH (PC_{13} = 1, PC_{12} = 0) or 3000H to 3F7FH (PC_{13} = 1, PC_{12} = 1)	
*9	faddr = 0000H to 07FFH		
*10	taddr = 0020H to 007FH		

Remarks **1.** MB indicates the accessible memory bank.
2. For *2, MB = 0 without regard to MBE and MBS.
3. For *4 and *5, MB = 15 without regard to MBE and MBS.
4. *6 to *10 indicate the addressable area.

(4) Explanation of machine cycle field

S shows the number of machine cycles required when skip is performed by an instruction with skip. The value of S changes as follows:

- No skip ..... S = 0
- When instruction to be skipped is 1-byte or 2-byte instruction ..... S = 1
- When instruction to be skipped is 3-byte instruction (BR !addr, CALL !addr instruction) ..... S = 2

Caution One machine cycle is required to skip a GETI instruction.

One machine cycle is equivalent to one cycle (= t_{CY}) of the CPU clock Φ. Three times can be selected by PCC setting.

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A ← n4		Stack A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		Stack A
		HL, #n8	2	2	HL ← n8		Stack B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A,reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
Note 2	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		
Operation	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ⊻ n4		
		A, @HL	1	1	A ← A ⊻ (HL)	*1	

Notes **1.** Instruction Group

2. Table reference

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Note 2	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Note 3	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
Note 4	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) \leftarrow 1$	*5	
		@H + mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 1$	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) \leftarrow 0$	*5	
		@H + mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 0$	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) = 1$	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) = 0$	*5	(pmem.@L) = 0
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 0$	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit\ (L_{1-0})) = 1$ and clear	*5	(pmem.@L) = 1
		@H + mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$ and clear	*1	(@H + mem.bit) = 1

Notes **1.** Instruction Group
2. Accumulator operation
3. Increment/decrement
4. Carry flag manipulation

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Memory bit manipulation	AND1	CY, fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∧ (H + mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∨ (H + mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ ($pmem_{7-2}$ + L_{3-2}.bit (L_{1-0}))	*5	
		CY, @H + mem.bit	2	2	CY ← CY ∀ (H + mem_{3-0}.bit)	*1	
Branch	BR	addr	—	—	PC_{13-0} ← addr (The assembler selects the optimum instruction from among the BR !addr, BRCB !caddr, and BR $addr instructions.)	*6	
		!addr	3	3	PC_{13-0} ← addr	*6	
		$addr	1	2	PC_{13-0} ← addr	*7	
	BRCB	!caddr	2	2	PC_{13-0} ← $PC_{13, 12}$ + $caddr_{11-0}$	*8	
Subroutine stack control	CALL	!addr	3	3	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← addr, SP ← SP – 4	*6	
	CALLF	!faddr	2	2	(SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← 00, faddr, SP ← SP – 4	*9	
	RET		1	3	MBE, PC_{13}, PC_{12} ← $(SP + 1)_{3, 1, 0}$ PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4		
	RETS		1	3+S	MBE, PC_{13}, PC_{12} ← $(SP + 1)_{3, 1, 0}$ PC_{11-0} ← (SP) (SP + 3) (SP + 2) SP ← SP + 4, then skip unconditionally		Unconditional
	RETI		1	3	PC_{13}, PC_{12} ← $(SP + 1)_{1, 0}$ PC_{11-0} ← (SP) (SP + 3) (SP + 2) PSW ← (SP + 4) (SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1) (SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← 0, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1) (SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), SP ← SP + 2		
Note 2	EI		2	2	IME ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME ← 0		
		IE×××	2	2	IE××× ← 0		

Notes 1. Instruction Group

2. Interrupt control

Note 1	Mnemonic	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Condition
Input/output	IN	A, PORTn	2	2	A ← $PORT_n$ (n = 0–7)		
		XA, PORTn	2	2	XA ← $PORT_{n+1}$, $PORT_n$ (n = 4, 6)		
	OUT	PORTn, A	2	2	$PORT_n$ ← A (n = 2–7)		
		PORTn, XA	2	2	$PORT_{n+1}$, $PORT_n$ ← XA (n =4, 6)		
Note 2	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS ← n (n = 0 to 3, 15)		
	GETI	taddr	1	3	• TBR Instruction PC_{13-0} ← (taddr) $_{5-0}$ + (taddr + 1)	*10	
					• TCALL Instruction (SP – 4) (SP – 1) (SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← (taddr) $_{5-0}$ ← (taddr + 1) SP ← SP – 4		
					• Other than TBR and TCALL Instruction Execution of an instruction addressed at (taddr) and (taddr + 1)		Conforms to referenced instruction.

Caution: At IN/OUT instruction execution, MBE = 0 or MBE = 1, MBS = 15 must be set in advance.

Notes 1. Instruction Group
2. CPU control

Remark The TBR and TCALL instructions are assembler pseudo instructions for GETI instruction table definition.

10. MASK OPTION SELECTION

The following mask options are available at the pins:

Pin Function	Mask Option
P40 to P43, P50 to P53	• Pull-up resistor (specifiable bit-wise) • No pull-up resistor (specifiable bit-wise)
V_{LC0} to V_{LC2}, BIAS	• LCD drive power supply split resistor (specified in units of 4) • No LCD drive power supply split resistor (specified in units of 4)

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Except ports 4, 5		–0.3 to V_{DD} +0.3	V
	V_{I2}	Ports 4, 5	On-chip pull-up resistor	–0.3 to V_{DD} +0.3	V
			Open-drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} +0.3	V
Output current, high	I_{OH}	Per pin		–15	mA
		All output pins		–30	mA
Output current, low	I_{OL}*	Per pin	Peak value	30	mA
			Effective value	15	mA
		Total of ports 0, 2, 3, 5	Peak value	100	mA
			Effective value	60	mA
		Total of ports 4, 6, 7	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

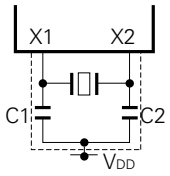
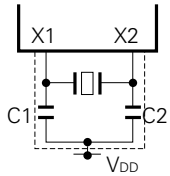
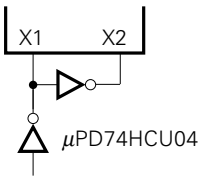
* Calculate the effective value with the formula [Effective value] = [Peak value] × $\sqrt{\text{duty}}$.

Caution: If even one parameter exceeds the absolute maximum rating, even momentarily, the quality of the product may be impaired. The absolute maximum rating is a rated threshold value at which the product can be physically damaged. Be sure to use the product within the absolute maximum ratings.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pin returned to 0 V			15	pF
Output capacitance	C_{OUT}				15	pF
Input /output capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

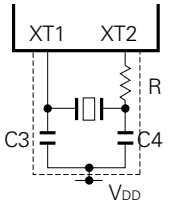
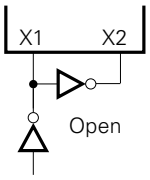
RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_{XX}) ***1**		1.0		5.0***3**	MHz
		Oscillation stabilization time ***2**	After V_{DD} reaches the minimum value in the oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_{XX}) ***1**		1.0	4.19	5.0***3**	MHz
		Oscillation stabilization time ***2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) ***1**		1.0		5.0***3**	MHz
		X1 input high and low level widths (t_{XH}, t_{XL})		100		500	ns

*** 1.** For the oscillator frequency and the X1 input frequency, only the characteristics of the oscillation circuit are shown. For the instruction execution time, refer to the AC characteristics.

2. Time required for oscillation to become stabilized after V_{DD} application or STOP mode release.

3. When the oscillator frequency is 4.19 MHz < f_{XX} ≤ 5.0 MHz, do not select PPC = 0011 as instruction execution time. If PCC = 0011 is selected, 1 machine cycle becomes less than 0.95 μs, with the result that specified MIN. value 0.95 μs cannot be observed.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high and low level widths (t_{XTH}, t_{XTL})		5		15	μs

***** Time required for oscillation to become stabilized after V_{DD} application.

Caution: **When the main system clock oscillator or subsystem clock oscillator is used, the shaded area in the figures should be wired as follows to prevent influence from the wiring capacitance, etc.**

- **Wiring should be as short as possible.**
- **Do not cross signal lines.**
- **Do not place the circuit close to a line in which varying high current flows.**
- **The connecting point of oscillator capacitor should always be the same potential as V_{DD}. Do not connect it to the power supply pattern in which high current flows.**
- **Do not fetch a signal from the oscillator.**

When the subsystem clock is used, special care is needed for the wiring. The subsystem clock oscillator is designed to be low-amplification circuit for low current consumption, thus mulfunction due to noise occurs more often than with the main system clock oscillator.

RECOMMENDED OSCILLATOR CONSTANTS

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (Ta = –40 to +85 °C)

Manufacture	Product Name	Frequency (MHz)	Recommended constants			Oscillator voltage range (V)	
			C1 (pF)	C2 (pF)	R (kΩ)	MIN.	MAX.
MURATA	CSB ××××J	1.000 to 1.250	100	100	5.6	2.0	6.0
	CSA×.×××MK040	1.251 to 1.799			–		
	CSA ×.××MG040	1.800 to 2.440					
	CST ×.××MG040		Internal	Internal			
	CSA ×.××MG	2.450 to 5.000	30	30			
	CST ×.××MGW		Internal	Internal			

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (Ta = –40 to +85 °C)

Manufacture	Product Name	Frequency (MHz)	Recommended constants		Oscillator voltage range (V)	
			C1 (pF)	C2 (pF)	MIN.	MAX.
KYOCERA	KBR-1000Y	1.00	100	100	2.0	6.0
	KBR-1000F					
	KBR-2.0MS	2.00				
	PBRC 2.00A					
	KBR-4.0MSA	4.00	33	33		
	PBRC 4.00A					
	KBR-4.0MKS		Internal	Internal		
	KBR-4.0MWS					
	KBR-5.0MSA	6.00	33	33		
	PBRC 5.00A					
	KBR-5.0MKS		Internal	Internal		
	KBR-5.0MWS					

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (Ta = –40 to +85 °C)

Manufacture	Product Name	Frequency (MHz)	Recommended constants		Oscillator voltage range (V)	
			C1 (pF)	C2 (pF)	MIN.	MAX.
TOKOU	CRHF 2.50	2.5	30	30	2.0	6.0
	CRHF 3.00	3.0				
	CRHF 4.00	4.0				
	CRHF 5.00	5.0				

SUBSYSTEM CLOCK: CRYSTAL RESONATOR (Ta = –15 to +60 °C)

Manufacture	Product Name	Frequency (MHz)	Recommended constants			Oscillator voltage range (V)	
			C3 (pF)	C4 (pF)	R (kΩ)	MIN.	MAX.
KYOCERA	KF-38G	32.768	18	33	220	2.0	6.0

Caution: Make the fine-adjustment of crystal resonator frequency with external capacitor C1 or C3.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage, high	V_{IH1}	Ports 2 and 3		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	On-chip pull-up resistor	0.7 V_{DD}		V_{DD}	V
			Open-drain	0.7 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Ports 2, 3, 4 and 5		0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
Output voltage, high	V_{OH1}	Ports 0, 2, 3, 6, 7, BIAS	V_{DD} = 4.5 to 6.0 V I_{OH} = –1mA	V_{DD} –1.0			V
			I_{OH} = –100 μA	V_{DD} –0.5			V
	V_{0H2}	BP0 to BP7 (with 2 I_{OH} outputs)	V_{DD} = 4.5 to 6.0 V I_{OH} = –100 μA	V_{DD} –2.0			V
			I_{OH} = –30 μA	V_{DD} –1.0			V
Output voltage, low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6 and 7	Ports 3, 4, 5 V_{DD} = 4.5 to 6.0 V I_{OL} = 15 mA		0.5	2.0	V
			V_{DD} = 4.5 to 6.0 V I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
		SB0, 1	Open-drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	V_{DD} = 4.5 to 6.0 V I_{OL} = 100 μA			1.0	V
			I_{OL} = 50 μA			1.0	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5 (when open -drain)			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V) (2/2)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below				3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (when open-drain)				20	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V					–3	μA
On-chip pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6 and 7 (Except P00) V_{IN} = 0 V	V_{DD} = 5.0 V ±10%		15	40	80	kΩ
			V_{DD} = 3.0 V ±10%		30		200	kΩ
	R_{L2}	Ports 4, 5 V_{OUT} = V_{DD} -2.0 V	V_{DD} = 5.0 V ±10%		15	40	70	kΩ
			V_{DD} = 3.0 V ±10%		15	40	70	kΩ
LCD drive voltage	V_{LCD}				2.0		V_{DD}	V
LCD split resistor	R_{LCD}				60	100	150	kΩ
LCD output voltage deviation***1** (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3 2.7 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2	V
LCD output voltage deviation***1** (segment)	V_{ODS}	I_O = ±1μA			0		±0.2	V
Supply current ***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1=C2= 22 pF	V_{DD} = 5 V ±10%***4**			3.0	9	mA
			V_{DD} = 3 V ±10%***5**			0.4	1.2	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10%		1	3	mA
				V_{DD} = 3 V ±10%		300	900	μA
	I_{DD3}	32 kHz ***6** crystal oscillation	V_{DD} = 3 V ±10%			20	60	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10%		7	21	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V±10%			1	25	μA
			V_{DD} = 3 V ±10%			0.5	15	μA
				T_a = 25°C		0.5	5	μA

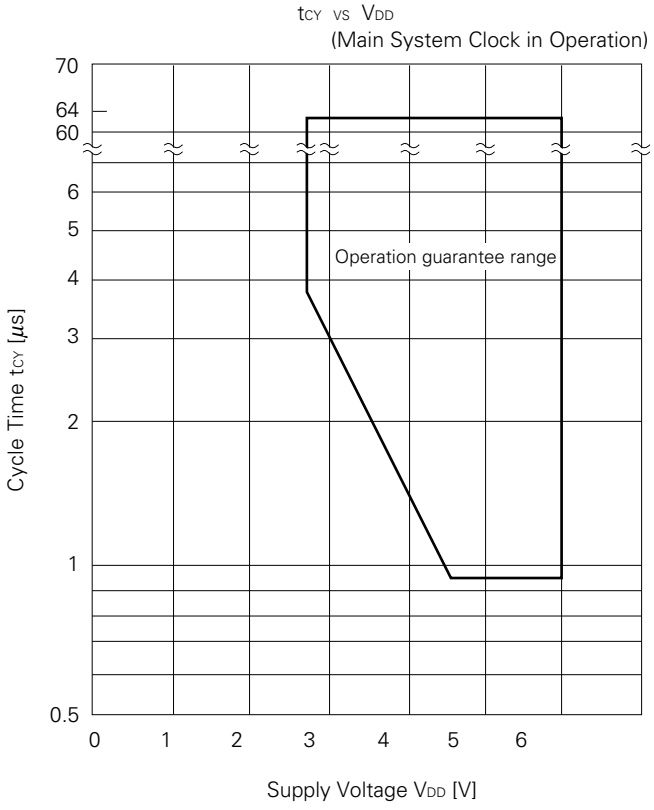
* **1.** The voltage deviation is a difference between the segment and common output ideal value (V_{LCDn}; n = 0, 1, 2) and output voltage.
  2. Current flowing in the internal pull-up resistor and LCD split resistor are not included.
  3. Includes the case when the subsystem clock is oscillated.
  4. When the processor clock control register (PCC) is set to 0011 and operated in high-speed mode.
  5. When the PCC is set to 0000 and operated in low-speed mode.
  6. When operated by the subsystem clock with the system clock control register (SCC) set to 1001 and the main system clock oscillation stopped.

AC CHARACTERISTICS (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = one machine cycle)***1**	t_{CY}	Operation with main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operation with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHZ
				0		275	kHz
TI0 input high- and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high- and low-level widths	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0–7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

*** 1.** CPU clock (Φ) cycle time is determined by oscillation frequency of the connected resonator, system clock control register (SCC) and processor clock control register (PCC).
Characteristics for supply voltage V_{DD} vs. Cycle time t_{CY} in main system clock operation is shown below.

2. It becomes $2t_{CY}$ or $128/f_X$ by interrupt mode register (IM0) setting.



SERIAL TRANSFER OPERATION

2-wire and 3-wire serial I/O mode ($\overline{SCK}$...Internal clock output): (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high- and low-level widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2-50$			ns
	t_{KH1}			$t_{KCY1}/2-150$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}			150			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

2-wire and 3-wire serial I/O mode ($\overline{SCK}$...External clock input): (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$...Internal clock output (master)): (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high- and low-level widths	t_{KL3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2–50			ns
	t_{KH3}			t_{KCY3}/2–150			ns
SB0 and SB1 setup time (to $\overline{SCK}$↑)	t_{SIK3}			150			ns
SB0 and SB1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0 and SB1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY3}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY3}			ns

* R_L and C_L are SB0, SB1 output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$...External clock input (slave)): (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level widths	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0 and SB1 setup time (to $\overline{SCK}$↑)	t_{SIK4}			100			ns
SB0 and SB1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0 and SB1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY4}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY4}			ns

* R_L and C_L are SB0, SB1 output line load resistance and load capacitance, respectively.

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V) (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage, high	V_{IH1}	Ports 2 and 3		0.8 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4 and 5	On-chip pull-up resistor	0.8 V_{DD}		V_{DD}	V
			Open-drain	0.8 V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD} –0.3		V_{DD}	V
Input voltage, low	V_{IL1}	Ports 2, 3, 4 and 5		0		0.2 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.25	V
Output voltage, high	V_{OH1}	Ports 0, 2, 3, 6, 7, BIAS	I_{OH} = –100 μA	V_{DD} –0.5			V
	V_{OH2}	BP0 to BP7 (with 2 I_{OH} outputs)	I_{OH} = –10 μA	V_{DD} –0.4			V
Output voltage, low	V_{OL1}	Ports 0, 2, 3, 4, 5, 6 and 7	I_{OL} = 400 μA			0.5	V
		SB0, 1	Open-drain pull-up resistor ≥ 1 kΩ			0.2 V_{DD}	V
	V_{OL2}	BP0 to BP7 (with 2 I_{OL} outputs)	I_{OL} = 10 μA			0.4	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_{IN} = 10 V	Ports 4 and 5 (when open -drain)			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Other than below			–3	μA
	I_{LIL2}		X1, X2, XT1			–20	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 10 V	Ports 4 and 5 (when open -drain)			20	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V) (2/2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
On-chip pull-up resistor	R_{L1}	Ports 0, 1, 2, 3, 6 and 7 (except P00) V_{IN} = 0 V	V_{DD} = 2.5 V ±10%	50		600	kΩ
	R_{L2}	Ports 4, 5 V_{OUT} = V_{DD} -1.0 V	V_{DD} = 2.5 V ±10%	15	40	70	kΩ
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD split resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation***1** (common)	V_{ODC}	Io = ±5 μA	V_{LCD0} = V_{LCD}, V_{LCD1} = V_{LCD} × 2/3, V_{LCD2} = V_{LCD} × 1/3, 2.0 V ≤ V_{LCD} ≤ V_{DD}	0		±0.2	V
LCD output voltage deviation***1** (segment)	V_{ODS}	Io = ±1μA		0		±0.2	V
Supply current ***2**	I_{DD1}	4.19 MHz***3** crystal oscillation C1=C2=22 pF Low-speed mode	V_{DD} = 3 V ±10%***4**		0.4	1.2	mA
			V_{DD} = 2.5 V ±10%***4**		0.3	0.9	mA
	I_{DD2}		HALT mode, V_{DD} = 3 V ±10%		300	900	μA
			HALT mode, V_{DD} = 2.5 V ±10%		200	600	μA
	I_{DD3}	32 kHz ***5** crystal oscillation	V_{DD} = 3 V ±10%		20	60	μA
			V_{DD} = 2.5 V ±10%		15	45	μA
	I_{DD4}		HALT mode, V_{DD} = 3 V ±10%		7	21	μA
			HALT mode, V_{DD} = 2.5 V ±10%		4	12	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 3 V ±10%		0.5	15	μA
			V_{DD} = 3 V ±10%, T_a = 25°C		0.5	5	μA
			V_{DD} = 2.5 V ±10%		0.4	15	μA
			V_{DD} = 2.5 V ±10%, T_a = 25°C		0.4	5	μA

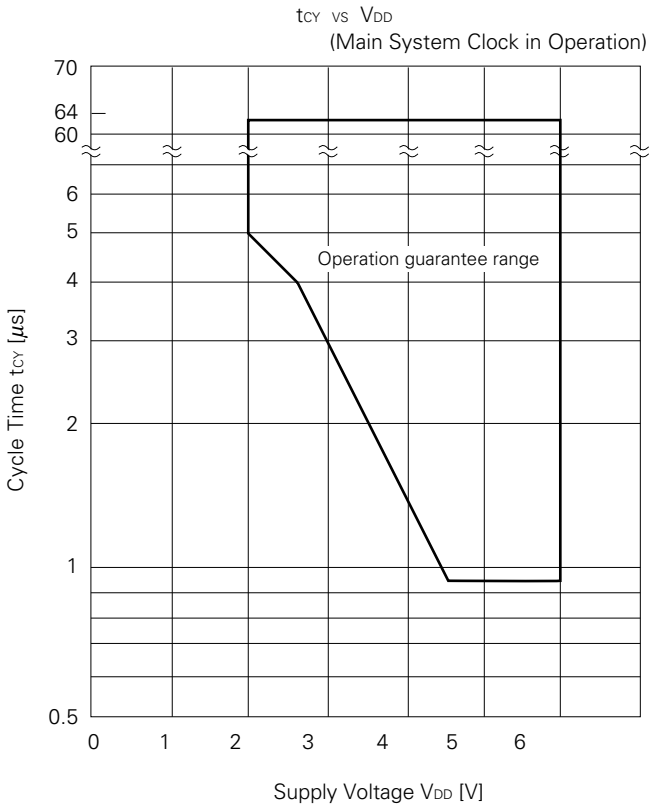
* **1.** The voltage deviation is a difference between the segment and common output ideal value (V_{LCDn}; n = 0, 1, 2) and output voltage.
  2. Current flowing in the on-chip pull-up resistor and LCD split resistor are not included.
  3. Includes the case when the subsystem clock is oscillated.
  4. When the PCC is set to 0000 and operated in low-speed mode.
  5. When operated by the subsystem clock with the system clock control register (SCC) set to 1001 and the main system clock stopped.

AC CHARACTERISTICS (Ta = –40 to +85 °C , V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = one machine cycle)***1**	t_{CY}	Operation with main system clock	V_{DD} = 2.7 to 6.0 V	3.8		64	μs
			V_{DD} = 2.0 to 6.0 V	5		64	μs
			T_a = –4.0 to +6.0 V V_{DD} = 2.2 to 6.0 V	3.4		64	μs
		Operation with subsystem clock		114	122	125	μs
TI0 input frequency	f_{TI}			0		275	kHz
TI0 input high- and low-level widths	t_{TIH}, t_{TIL}			1.8			μs
Interrupt input high- and low-level widths	t_{INTH}, t_{INTL}	INT0		***2**			μs
		INT1, 2, 4		10			μs
		KR0–7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

*** 1.** CPU clock (Φ) cycle time is determined by oscillation frequency of the connected resonator, system clock control register (SCC) and processor clock control register (PCC).
Characteristics for supply voltage V_{DD} vs. Cycle time t_{CY} in main system clock operation is shown below.

2. It becomes $2t_{CY}$ or $128/f_X$ by interrupt mode register (IM0) setting.



SERIAL TRANSFER OPERATION

2-wire and 3-wire serial I/O mode ($\overline{SCK}$...Internal clock output): (Ta = –40 to +85 °C , V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high- and low-level width	t_{KL1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2–50$			ns
	t_{KH1}			$t_{KCY1}/2–150$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}			250			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

2-wire and 3-wire serial I/O mode ($\overline{SCK}$...External clock input): (Ta = –40 to +85 °C , V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* R_L and C_L are SO output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$...Internal clock output (master)): (Ta = –40 to +85 °C , V_{DD} = 2.0 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high- and low-level widths	t_{KL3}	V_{DD} = 4.5 to 6.0 V		$t_{KCY3}/2–50$			ns
	t_{KH3}			$t_{KCY3}/2–150$			ns
SB0 and SB1 setup time (to $\overline{SCK}$↑)	t_{SIK3}			250			ns
SB0 and SB1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0 and SB1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY3}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY3}			ns

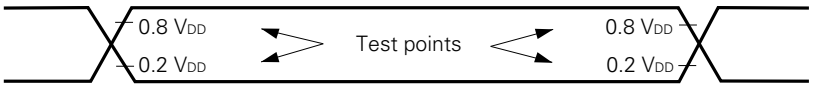
* R_L and C_L are SB0, SB1 output line load resistance and load capacitance, respectively.

SBI mode ($\overline{SCK}$...External clock input (slave)): (Ta = –40 to +85 °C , V_{DD} = 2.0 to 6.0 V)

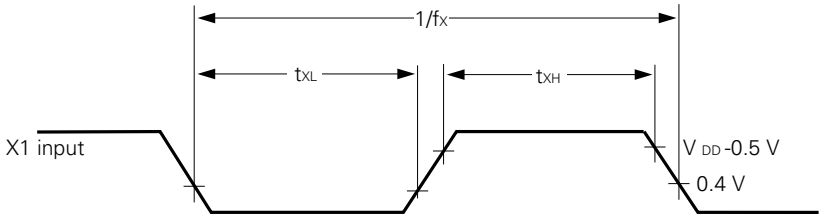
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high- and low-level widths	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0 and SB1 setup time (to $\overline{SCK}$↑)	t_{SIK4}			100			ns
SB0 and SB1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0 and SB1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0 and SB1 low-level widths	t_{SBL}			t_{KCY4}			ns
SB0 and SB1 high-level widths	t_{SBH}			t_{KCY4}			ns

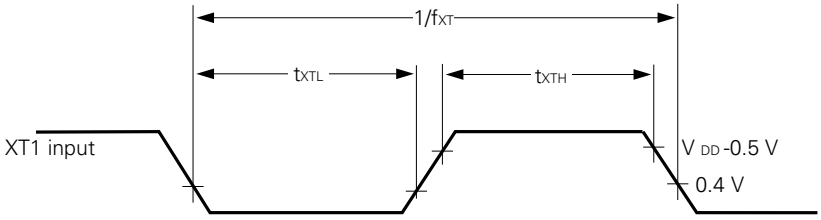
* R_L and C_L are SB0, SB1 output line load resistance and load capacitance, respectively.

AC Timing Test Points (except X1 and XT1 input)

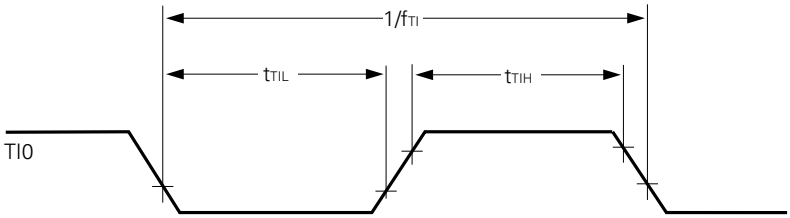


Clock Timing



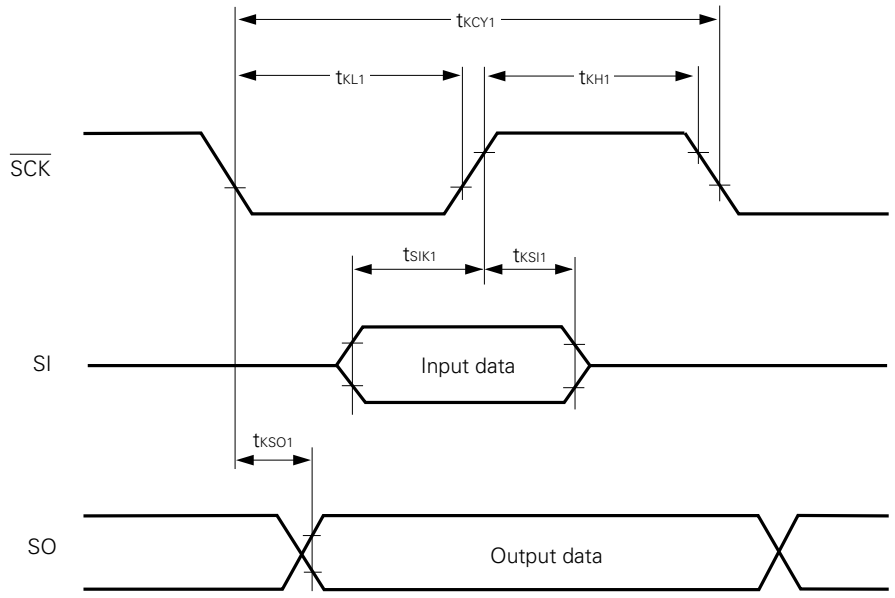


TI0 Timing

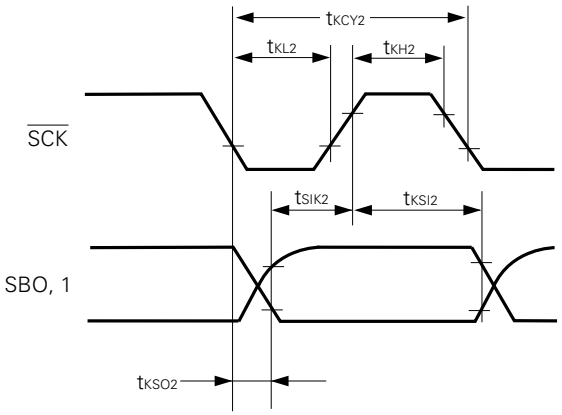


Serial Transfer Timing

3-wire serial I/O mode:

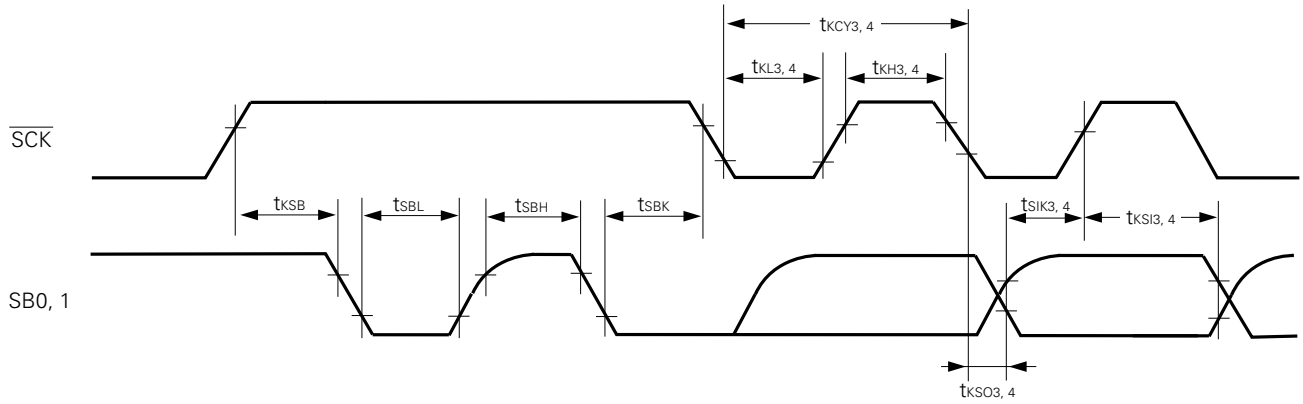


2-wire serial I/O mode:

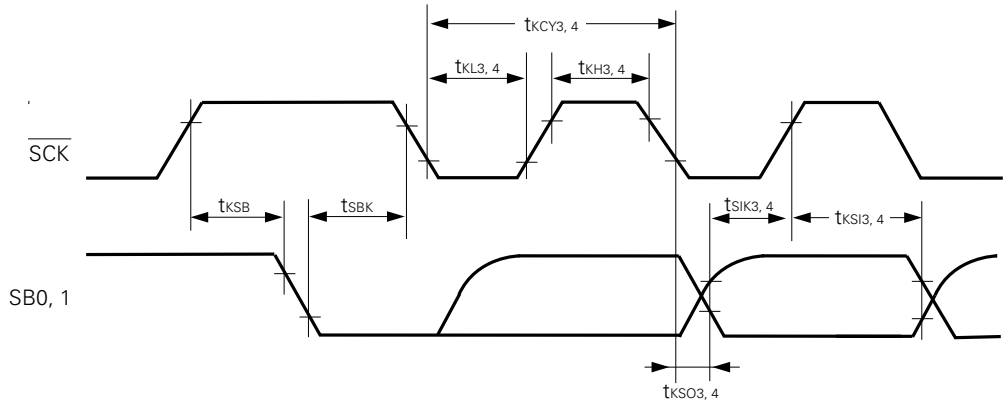


Serial Transfer Timing

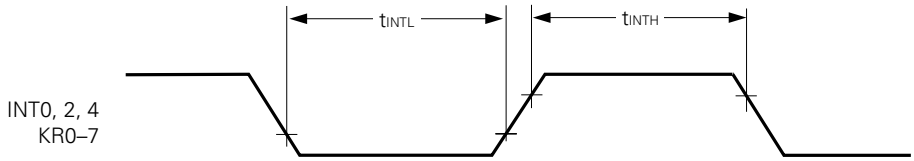
Bus release signal transfer:



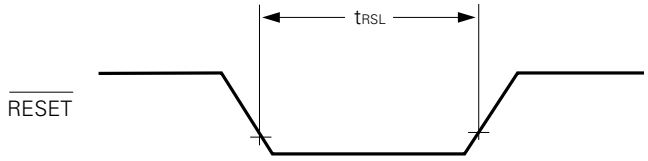
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



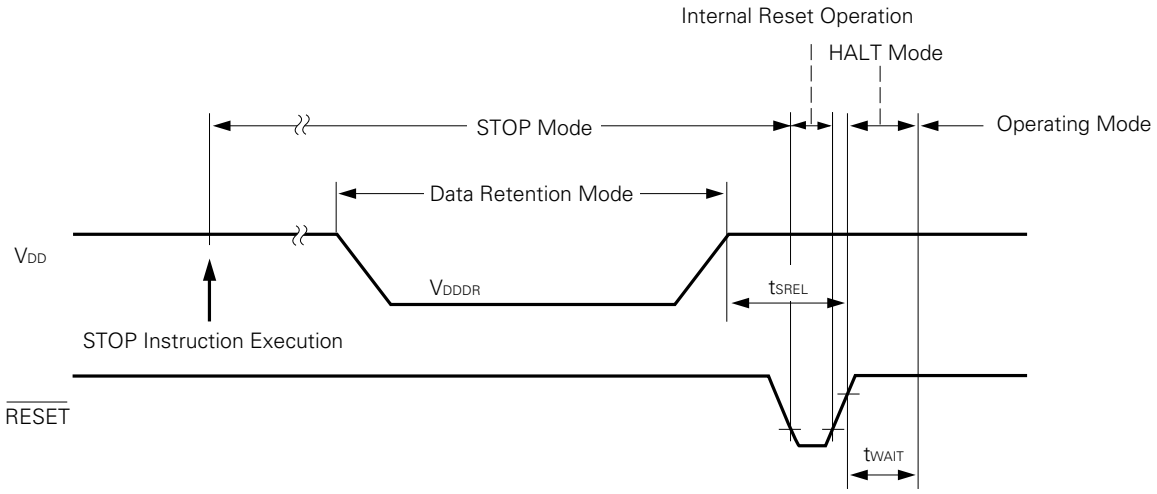
DATA RETENTION CHARACTERISTICS IN DATA MEMORY STOP MODE AND LOW SUPPLY VOLTAGE
(Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current *1	I_{DDDR}	V_{DDDR} = 2.0 V		0.3	15	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time *2	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		*3		ms

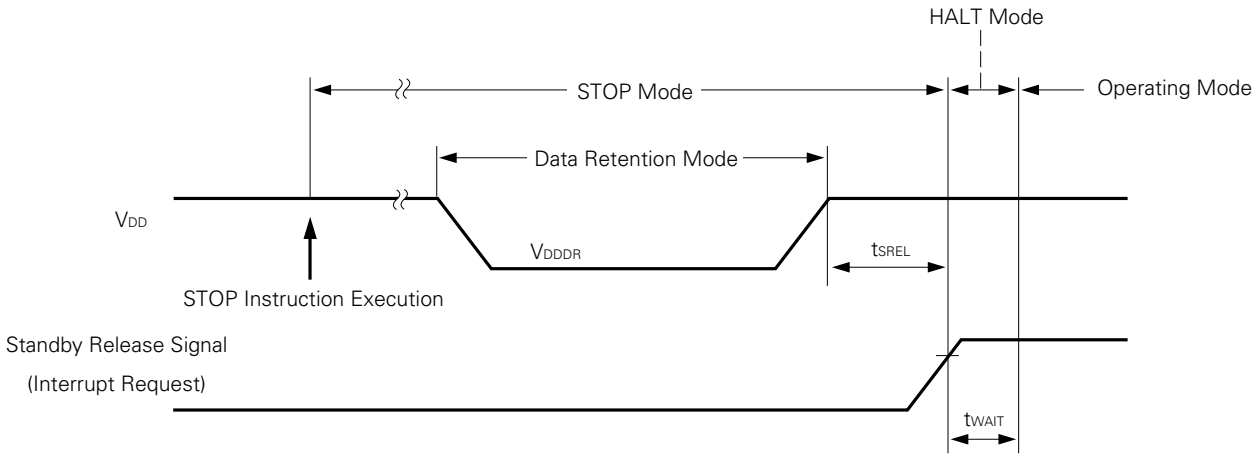
* **1.** Current to the on-chip pull-up resistor is not included.
2. Oscillation stabilization wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.
3. According to the setting of the basic interval timer mode register (BTM) (see below).

BTM3	BTM2	BTM1	BTM0	Wait Time (Values at f_X = 4.19 MHz in parentheses)
—	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



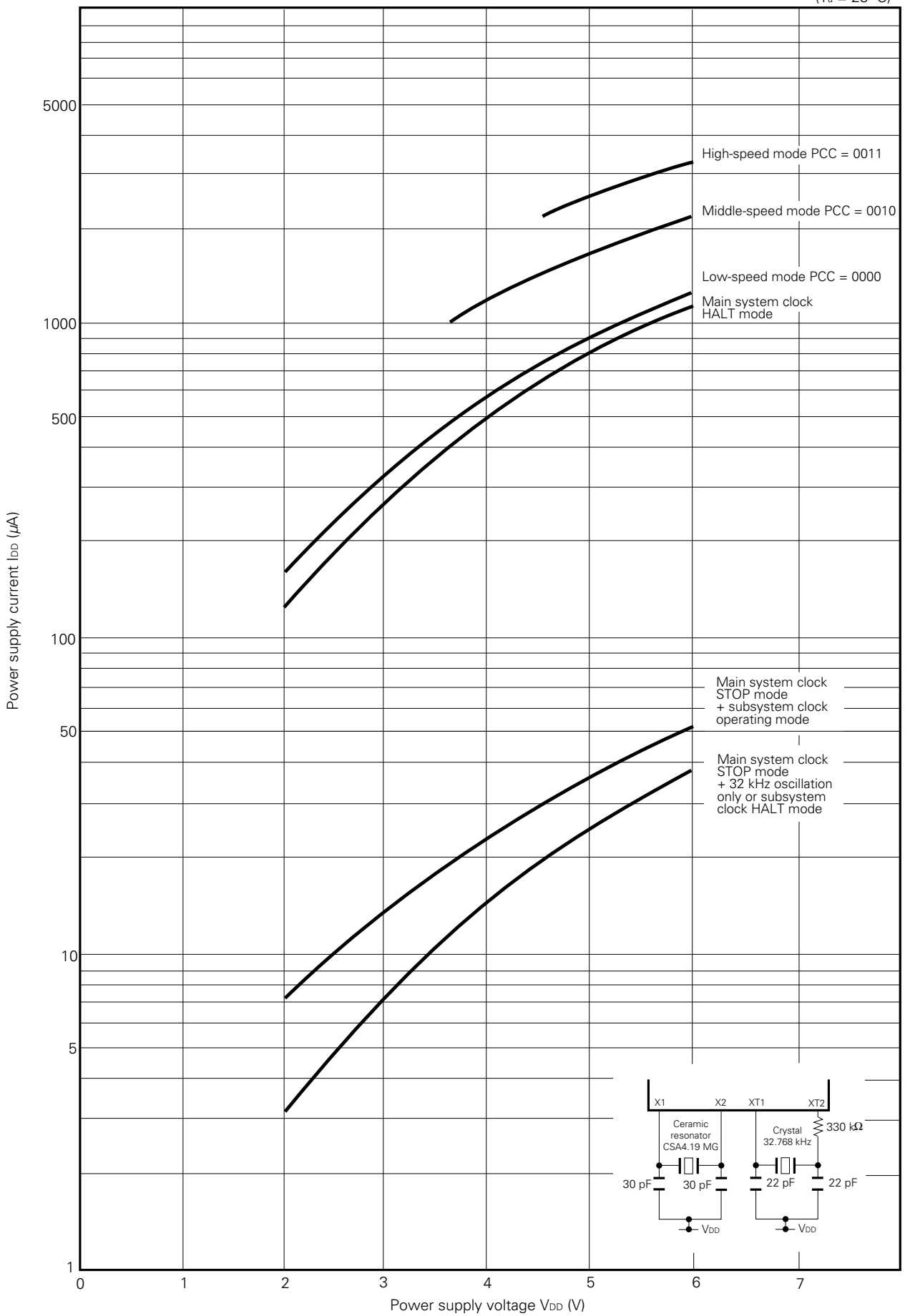
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



12. CHARACTERISTIC CURVES (For Reference Only)

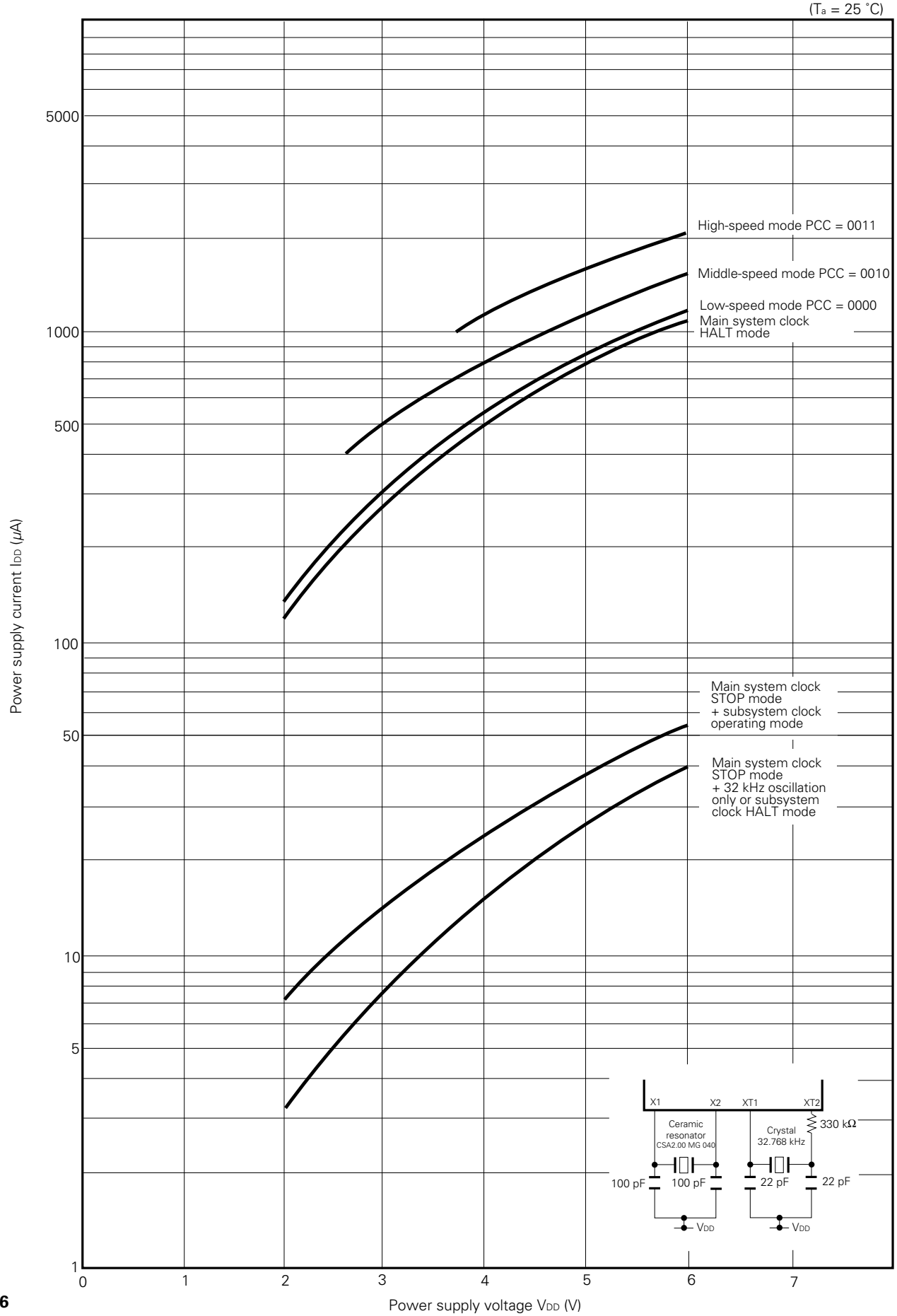
I_{DD} vs V_{DD} (Ceramic Oscillation: 4.19 MHz)

(T_a = 25 °C)

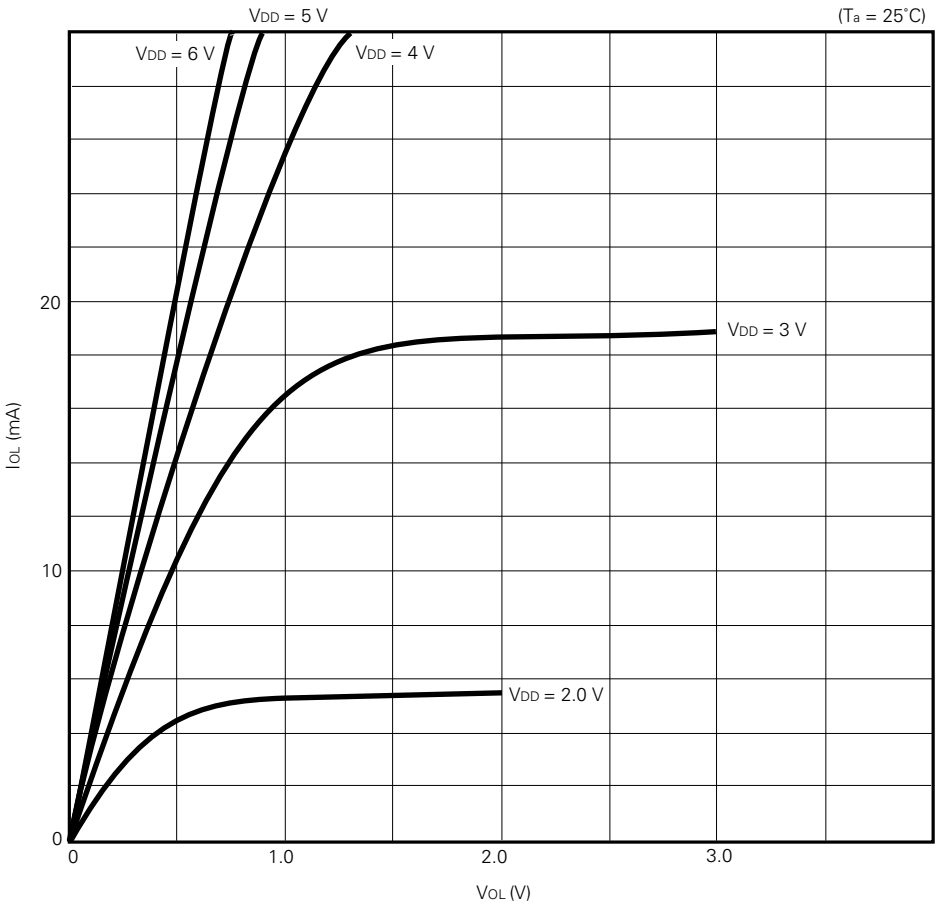


I_{DD} vs V_{DD} (Ceramic Oscillation: 2.00 MHz)

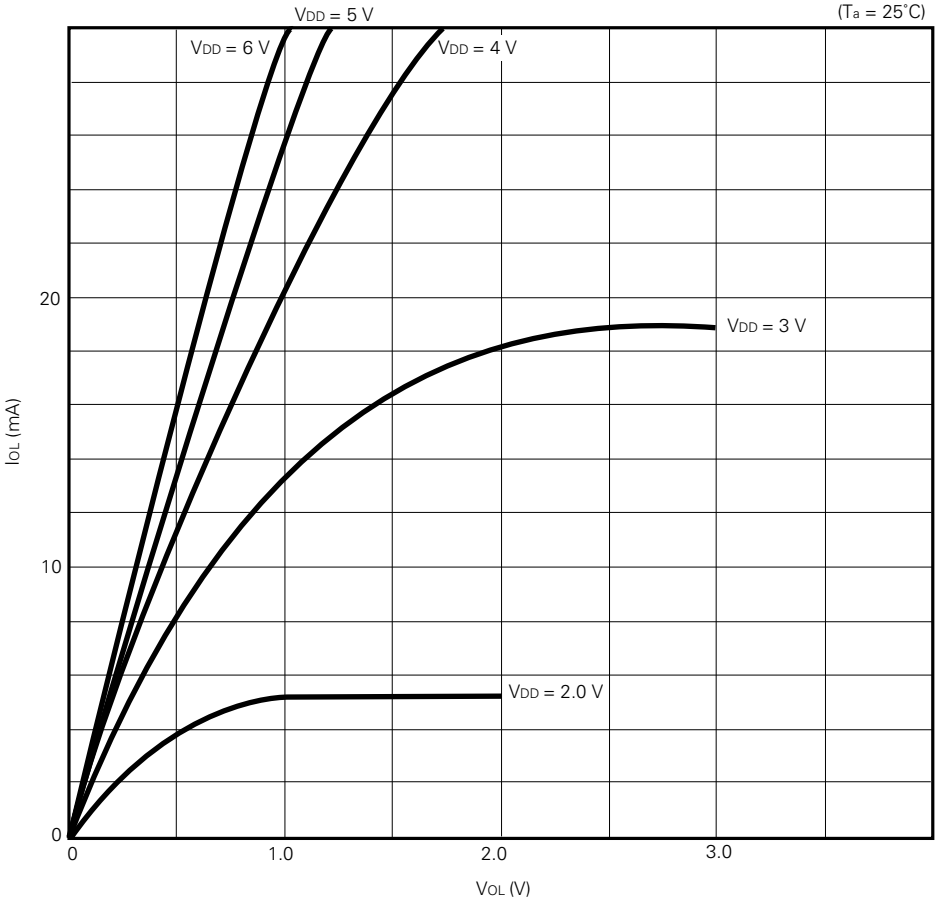
(T_a = 25 °C)



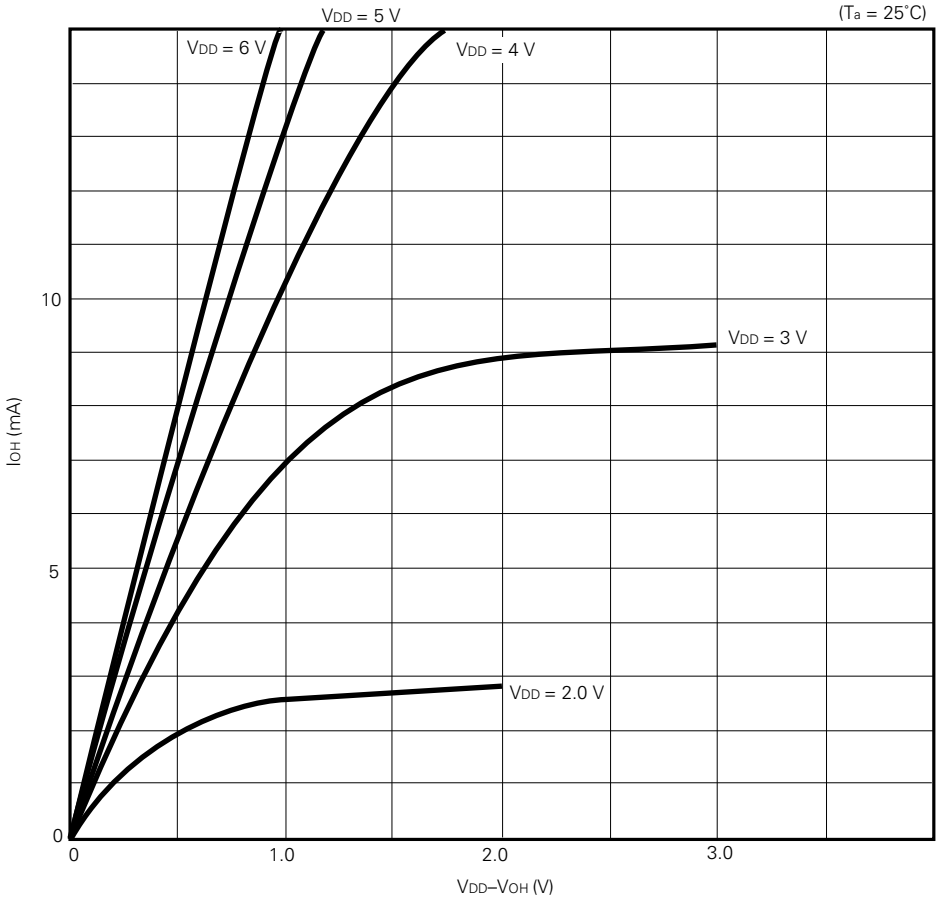
I_{OL} vs V_{OL} (Port 0, 2, 6, and 7)



I_{OL} vs V_{OL} (Port 3, 4, and 5)

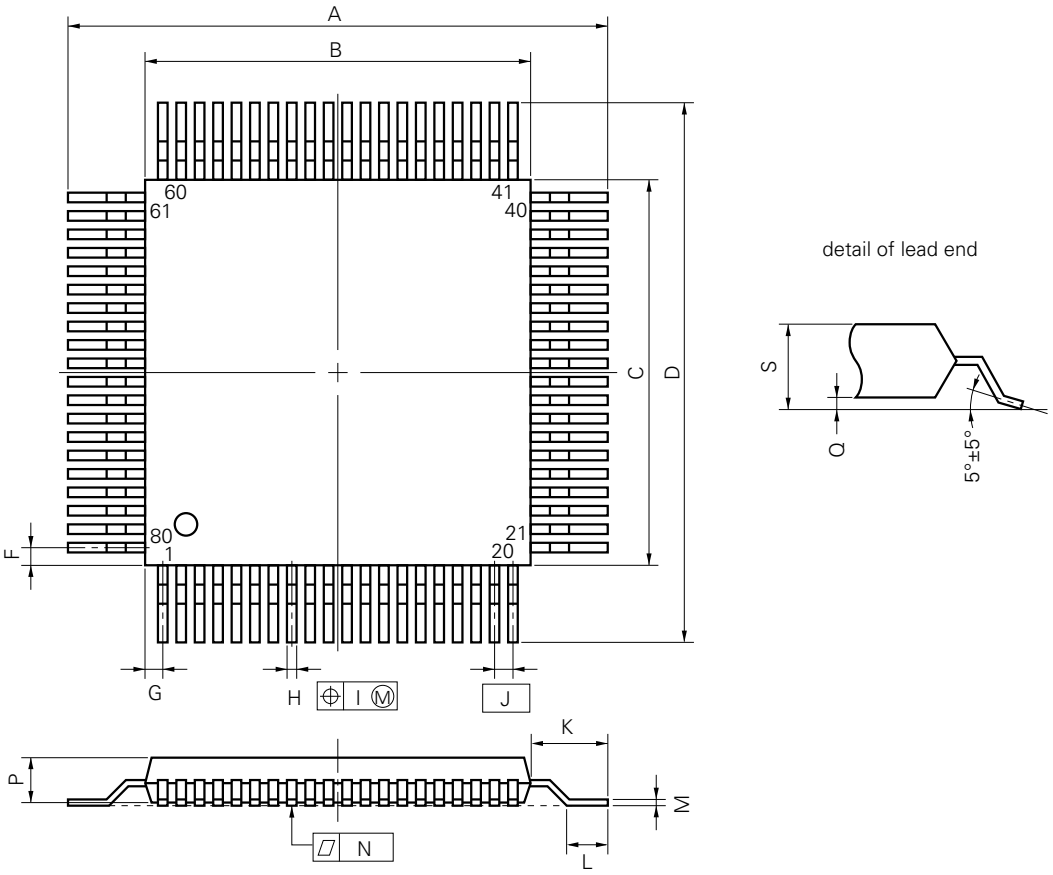


IOH vs VOH


VDD = 5 V
(Ta = 25°C)
VDD = 6 V
VDD = 4 V
VDD = 3 V
VDD = 2.0 V
10
5
0
IOH (mA)
0
1.0
2.0
3.0
VDD–VOH (V)

13. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (□14)



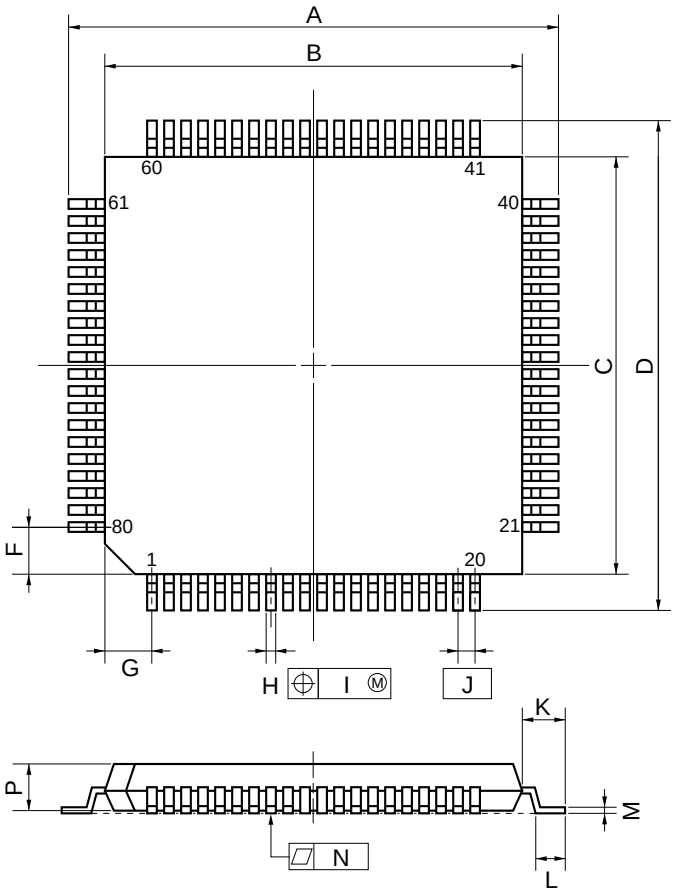
S80GC-65-3B9-3

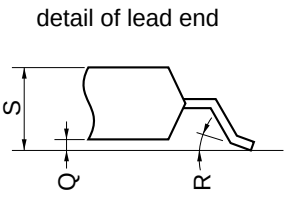
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

80 PIN PLASTIC TQFP (FINE PITCH) (□12)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

14. RECOMMENDED SOLDERING CONDITIONS

The product should be soldered and mounted under the conditions recommended in the table below.

For the details of recommended soldering conditions, refer to the information document "**Semiconductor Device Mounting Technology Manual**" (IEI-1207).

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1 Surface Mounting Type Soldering Conditions

μPD75312BGC-×××-3B9 **: 80-pin plastic QFP (14 x 14 mm)**

μPD75316BGC-×××-3B9 **: 80-pin plastic QFP (14 x 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: Within 30 s (at 210 °C or higher), Count: Twice or less **<Attention>** (1) Perform the second reflow when the device temperature has come down to the room temperature from the heating by the first reflow. (2) Do not wash flux away with water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: Within 40 s (at 200 °C or higher), Count: Twice or less **<Attention>** (1) Perform the second reflow when the device temperature has come down to the room temperature from the heating by the first reflow. (2) Do not wash flux away with water after the first reflow.	VP15-00-2
Wave soldering	Soldering tank temperature: 260 °C or less, Time: Within 10 s, Count: Once, Preheating temperature: 120 °C MAX. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C or less, Time: Within 3 s (per side of device)	——

Caution: Do not use several soldering methods in combination (except partial heating).

μPD75312BGK-×××-3B9 **: 80-pin plastic QFP (12 x 12 mm)**
μPD75316BGK-×××-3B9 **: 80-pin plastic QFP (12 x 12 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: Within 30 s (at 210 °C or higher), Count: Twice or less, Exposure limit : Seven* days (after seven days, prebake at 125 °C is required for 10 hours) **<Attention>** (1) Perform the second reflow when the device temperature has come down to the room temperature from the heating by the first reflow. (2) Do not wash flux away with water after the first reflow.	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: Within 40 s (at 200 °C or higher), Count: Twice or less, Exposure limit : Seven*days (after seven days, prebake at 125 °C is required for 10 hours) **<Attention>** (1) Perform the second reflow at the time the device temperature has come down to the room temperature from the heating by the first reflow. (2) Do not wash flux away with water after the first reflow.	VP15-107-2
Partial heating	Pin temperature: 300 °C or less, Time: Within 3 s (per side of device)	——

***** For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

Caution: Do not use several soldering methods in combination (except partial heating).

APPENDIX A. DIFFERENCES AMONG μPD75308B SERIES PRODUCTS

Item \ Name		μPD75304B/75306B/75308B	μPD75312B	μPD75316B	μPD75P316B	μPD75P316A
Supply voltage range		2.0 to 6.0 V				
ROM configuration		Mask ROM			EPROM/one-time PROM	
Program memory (bytes)		4096/6016/8064	12160	16256		
Data memory (× 4 bits)		512	1024			
Instruction cycle		0.95 μs, 1.91 μs, 15.3 μs (main system clock:@ 4.19 MHz) 122 μs (subsystem clock:@ 32.768 kHz)				
Input/output port	CMOS input	40	8	Pull-up resistor can be incorporated by software: 23		
	CMOS input/output		16			
	CMOS output		8	Used with segment pin		
	N-ch open-drain input/output		8	10-V withstand voltage, pull-up resistor can be incorporated by mask option.	10-V withstand voltage, without pull-up resistor option	
LCD controller/driver		• Common output: Static – 1/4 duty selected • Segment output: Max. 32				
		LCD drive split resistor can be incorporated by mask option.			No LCD drive split resistor	
LCD drive voltage		2.0 V to V_{DD}				
Timer/counter		• 8-bit timer/event counter • 8-bit basic interval timer • Watch timer				
Serial interface		• NEC standard serial bus interface (SBI) • Clocked serial interface				
Vectored interrupts		• External: 3 • Internal: 3				
Test input		• External: 1 • Internal: 1				
Clock output (PCL)		Φ, 524 kHz, 262 kHz, 65.5 kHz (main system clock:@ 4.19 MHz)				
Buzzer output (BUZ)		2 kHz (main system clock:@ 4.19 MHz, or subsystem clock:@ 32.768 KHz)				
Package		80-pin plastic QFP (14 x 20 mm) 80-pin plastic QFP (14 x 14 mm) 80-pin plastic TQFP (Fine pitch) (12 x 12 mm)	80-pin plastic QFP (14 x 14 mm) 80-pin plastic TQFP (Fine pitch) (12 x 12 mm)		80-pin plastic QFP (14 x 14 mm) 80-pin plastic TQFP (Fine pitch) (12 x 12 mm) 80-pin ceramic WQFN*	80-pin plastic QFP (14 x 20 mm) 80-pin ceramic WQFN
On-chip PROM product		GF package : μPD75P316A GC/GK package : μPD75P316B	μPD75P316B		——	——

* Under development

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75312B, 75316B.

Hardware	IE-75000-R***1** IE-75001-R		75X series in-circuit emulator
	IE-75000-R-EM***2**		Emulation board for the IE-75000-R and the IE-75001-R
	EP-75308BGC-R	EV-9200GC-80	Emulation probe for the μPD75312BGC and the 75316BGC. 80-pin conversion socket EV-9200GC-80 is also provided.
	EP-75308BGK-R	EV-9200GK-80	Emulation probe for the μPD75312BGK and the 75316BGK. 80-pin conversion socket EV-9200GK-80 is also provided.
	PG-1500		PROM programmer
	PA-75P316BGC		PROM programmer adapter for the μPD75P316BGC, connect to PG-1500.
	PA-75P316BGK		PROM programmer adapter for the μPD75P316BGK, connect to PG-1500.
Software	IE control program		Host machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A***3**) IBM PC/AT™ (See "**OS for IBM PC**")
	PG-1500 controler		
	RA75X relocatable assembler		

***** **1.** Maintenance products
2. Not incorporated in IE-75001-R.
3. The task-swap function is provided with the Ver.5.00/5.00A and cannot be used with this software.

OS for IBM PC

The following OSs are supported for IBM PC

OS	Version
PC DOS™	Ver.5.0.2 to Ver.6.1 J6.03/V
MS-DOS	Ver.3.30 to Ver.5.00A 5.0/V, J6.2/V
IBM DOS™	J5.02/V

Caution: Ver.5.0 or higher contains a task swap function; however, this function cannot be used by this software.

APPENDIX C. RELATED DOCUMENTATION

List of Device-Related Documents

Document Name	Document No.
User's Manual	IEM-1263
Application Note	IEM-1239
	IEM-1245
75X Series Selection Guide	IF-1027

List of Development Tool-Related Documents

	Document Name		Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75308BGC-R User's Manual		EEU-1406
	EP-75308BGK-R User's Manual		EEU-1408
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1363
	PG-1500 Controller User's Manual		EEU-1291

Others

Document Name	Document No.
Package Manual	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-1207
Quality Grade on NEC Semiconductor Device	IEI-1209
NEC Semiconductor Device Reliability and Quality Control	—
Electrostatic Discharge (ESD) Test	—
Semiconductor Device Quality Guarantee Guide	MEI-1202
Micro Computer-Related Products Guide Other Manufacture Volume	—

Remark The related documents listed above may change without prior notice. The most up-to-date documents should be used for design work.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents indicated in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

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