Useful Voice with Real-Time Clock (RTC)

Features

- Single power supply 2.4V – 5.2V
- 4-bit ADPCM & 8-bit PCM synthesis.
- 7K-22KHz max. of playing speed for ADPCM synthesizer
- 12K-32KHz max. of playing speed for PCM synthesizer
- Provides 3~340 seconds voice@ S.R.= 6kHz & 4-bit ADPCM
- Max. of two current type DAC audio outputs
- One PWM output to direct driving a speaker
- Programmable 2-channel tone melody generator
- 16 levels of digital volume control
- Powerful and easy instructions are provided
- Built in a high quality speech synthesizer
- On-chip RC oscillator
- Power saving STOP & HALT modes
- I/O State Change wake-up option for all of I/O port
- Support 32K crystal oscillator share with two pins of PA

General Description

JA21000 is a series of 3 to 340 seconds single chip voice synthesizer IC with RTC which contains a PWM direct drive circuit or AUD output for transistor application. In addition, this chip also provides high sink current port pins, multi external interrupt pins function, and multi oscillator options. JA21000 series offers one of the best cost/performance ratios in the toy or industry for controller.
It also supplies high-sink current port pins, multi-external wake-up pins function and multi-oscillator options. The JA21000 series can support 32K crystal oscillator for timer with low operating current. In addition, this JA21000 series family IC leads users into an easy-to use development environment that shorten developer's period and fasten time-to-market. Moreover, fantastic sound effects can be generated by users easily without writing complex programs. This JA21000 series family offers the best cost/performance ratios for toy, consumer, and industry use.

Selection Table

Part No.	JA21003	JA21007	JA21014	JA21018	JA21032	JA21043
Voice Cap. (second)	3	7	14	18	32	43
Max. of key numbers	16	16	16	16	32	32
Max. of PWM outputs	1	1	1	1	1	1
Max. of DAC outputs				1	1	1

Part No.	JA21064	JA21085	JA21128	JA21170	JA21256	JA21340
Voice Cap. (second)	64	85	128	170	256	340
Max. of key number	32	32	64	64	64	64
Max. of PWM outputs	1	1	1	1	1	1
Max. of DAC outputs	2	2	2	2	2	2

Note：The voice capacity is based on sampling rate of 6KHz and 4-bit ADPCM

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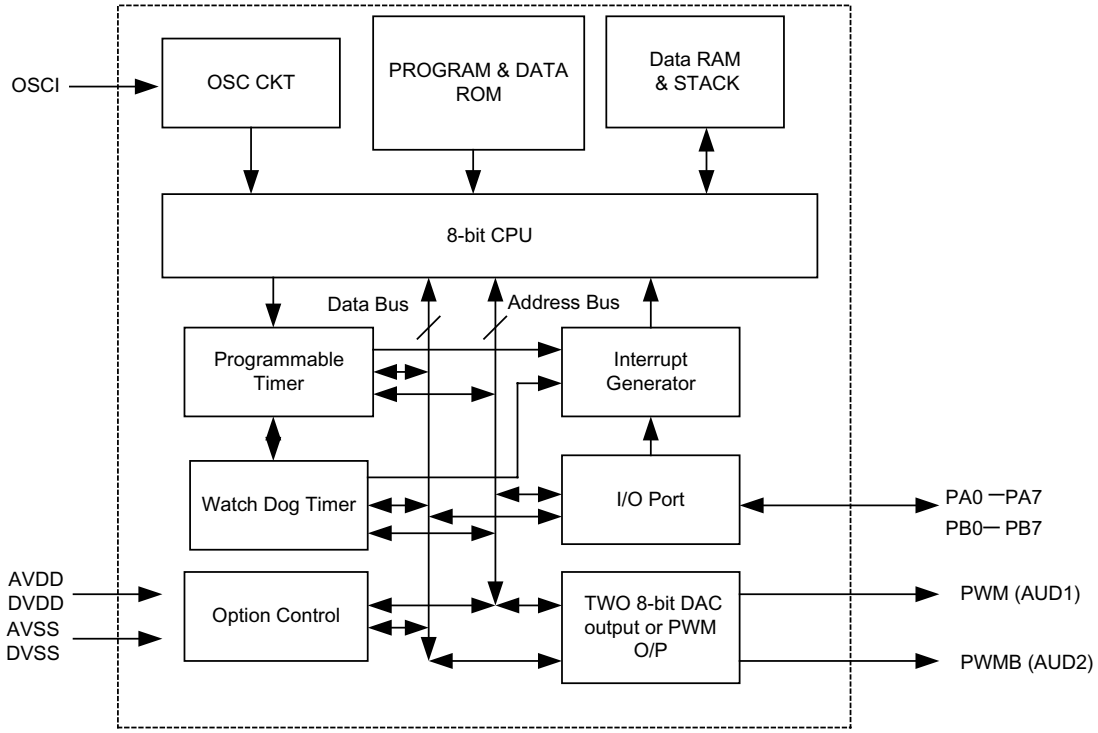
Block Diagram



Pad Assignment

Pin Name	I/O	Internal	Description
DVSS	—	—	Digital negative power supply
AVSS	—	—	Analog negative power supply
PA0 – PA3	I/O	NMOS Open Drain	Keyboards scan output in matrix mode. Normal I/O pins in direct mode. For output mode, they are open drain output; For input mode, they are without pull-high resistor.
PA4 – PA7	I/O	CMOS with pull-high	Keyboards scan output in matrix mode. Normal I/O pins in direct mode. For output mode, they are CMOS output; For input mode, they are with pull-high resistor.
PB0 – PB7	I	CMOS with pull-high	Keyboards scan input in direct/matrix mode. PB0 – PB3 pins are for all series. PB4 – PB7 pins are for JA21128 — JA21340 only.
AVDD, DVDD	—	—	Positive power supply.
OSCI	I	—	In RC mode, it connects an external oscillator resistor between OSCI and VDD. As well, the pin can be used as an external clock input.
PWM (AUD1) PWMB (AUD2)	O	CMOS or Open Drain	Current type output or PWM type output by mask option. For current type output, it must drive an external transistor and only for JA21018 — JA21340. For PWM type output, it can drive a speaker directly. (8 ohm – 32 ohm) The AUD1 output is provided to JA21018 — JA21340, and the AUD2 output is provided to JA21064 — JA21340 only.

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I/O pins and AUD output selection table

Part No	JA21003	JA21007	JA21014	JA21018	JA21032	JA21043
PA port	PA0 — PA3	PA0 — PA3	PA0 — PA3	PA0 — PA3	PA0 — PA7	PA0 — PA7
PB port	PB0 — PB3	PB0 — PB3	PB0 — PB3	PB0 — PB3	PB0 — PB3	PB0 — PB3
AUD output	X	X	X	AUD1	AUD1	AUD1
PWM output	V	V	V	V	V	V
Register (*)	R0 — R6	R0 — R6	R0 — R6	R0 — R6	R0 — R14	R0 — R14

Part No	JA21064	JA21085	JA21128	JA21170	JA21256	JA21340
PA port	PA0 — PA7	PA0 — PA7	PA0 — PA7	PA0 — PA7	PA0 — PA7	PA0 — PA7
PB port	PB0 — PB3	PB0 — PB3	PB0 — PB7	PB0 — PB7	PB0 — PB7	PB0 — PB7
AUD output	AUD1, AUD2	AUD1, AUD2	AUD1, AUD2	AUD1, AUD2	AUD1, AUD2	AUD1, AUD2
PWM output	V	V	V	V	V	V
Register (*)	R0 — R14	R0 — R14	R0 — R14	R0 — R14	R0 — R14	R0 — R14

(*) Note：Register Available

	JA21003 ~ JA21018	JA21032 ~ JA21340	Note
General	R0 ~ R6	R0 ~ R12	For JazEASY v2.5
Using Timer Function	R0 ~ R2	R0 ~ R8	
Playing PCM Melody	R0, R3 ~ R6	R0 ~ R12	
Using Timer Function & Playing PCM Melody	R0	R0 ~ R8	
Using “FR=MTn”	R1 ~ R6	R0 ~ R12	
General	R0 ~ R6	R0 ~ R14	For JazEASY v2.6
Using Timer Function	R0, R5, R6	R0 ~ R10	
Playing PCM Melody	R0 ~ R4	R0 ~ R14	
Using Timer Function & Playing PCM Melody	R0	R0 ~ R10	

Port A Initial Status

	JA21003 ~ JA21018	JA21032 ~ JA21340	Note
PA0 ~ PA3	Input-floating	Input-floating	For JazEASY v2.5
PA4 ~ PA7 (*)	Input-high	Input-high	
PA0 ~ PA3	Output-low	Output-low	For JazEASY v2.6
PA4 ~ PA7 (*)	Output-low	Input-high	

(*) Note： The PA port of JA21003-JA21018 real body, there is only PA0-PA3.

Absolute Maximum Rating

Symbol	Rating	Unit
V_{DD}~V_{SS}	V_{SS} -0.5 ~ V_{DD} +0.5	V
VIN (for input)	V_{SS}-0.3 < VIN < V_{DD}+0.3	V
VOUT (for all outputs)	V_{SS} < V_{OUT} < V_{DD}	V
T (operating)	-10 ~ +60	℃
T (storage)	-55 ~ +125	℃

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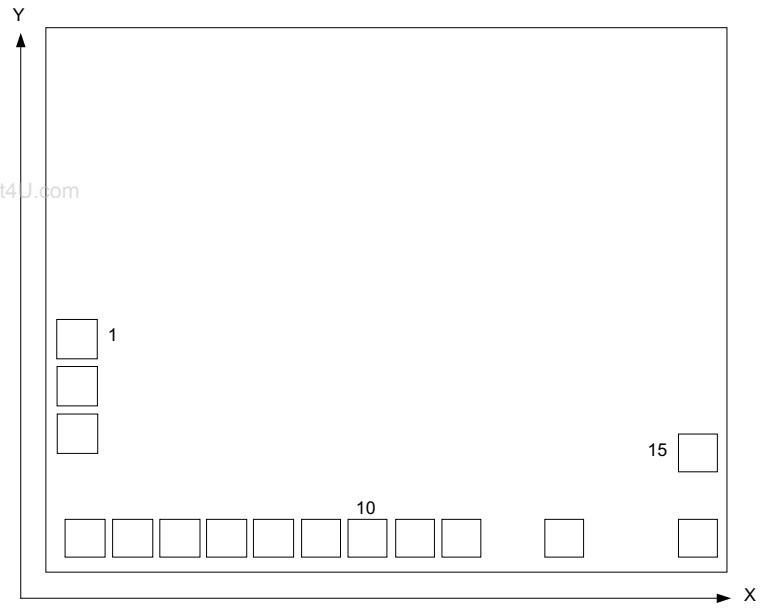
Pad Diagram & Pad Location

1. JA21003



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
01	PA3	70	535.5	09	VSS	638.1	70
02	PA2	70	425.7	10	OSCI	747.9	70
03	PA1	70	315.9	11	VDD	857.7	70
04	PA0	89.1	70	12	VDD	967.5	70
05	PB0	198.9	70	13	PWM	1207.9	70
06	PB1	308.7	70	14	VSS	1521.2	69.3
07	PB2	418.5	70	15	PWMB	1521.2	268.0
08	PB3	528.3	70				
Chip size : 1592 x 1263 $(\mu m)^2$							

Note：The IC substrate should be connect to VSS

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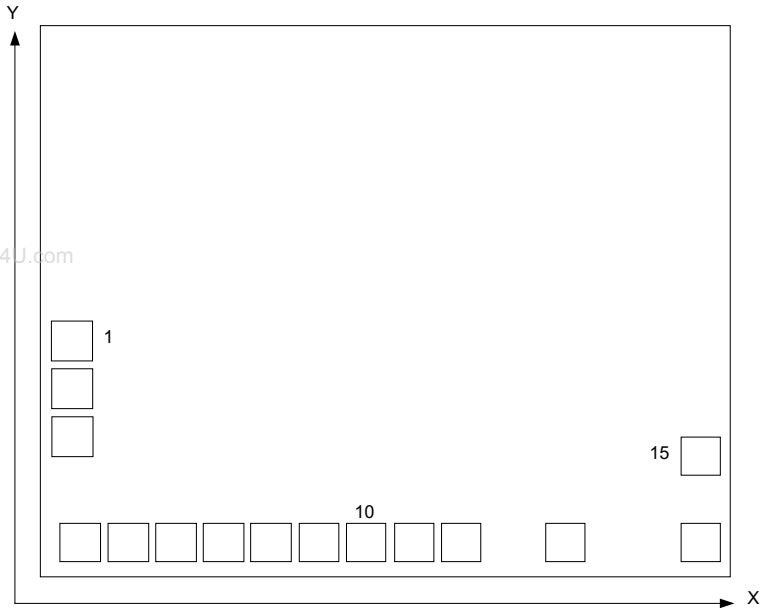
2. JA21007



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
01	PA3	70	535.5	09	VSS	638.1	70
02	PA2	70	425.7	10	OSCI	747.9	70
03	PA1	70	315.9	11	VDD	857.7	70
04	PA0	89.1	70	12	VDD	967.5	70
05	PB0	198.9	70	13	PWM	1207.9	70
06	PB1	308.7	70	14	VSS	1521.2	69.3
07	PB2	418.5	70	15	PWMB	1521.2	268.0
08	PB3	528.3	70				
Chip size : 1592 x 1263 (μm)^2							

Note：The IC substrate should be connect to VSS

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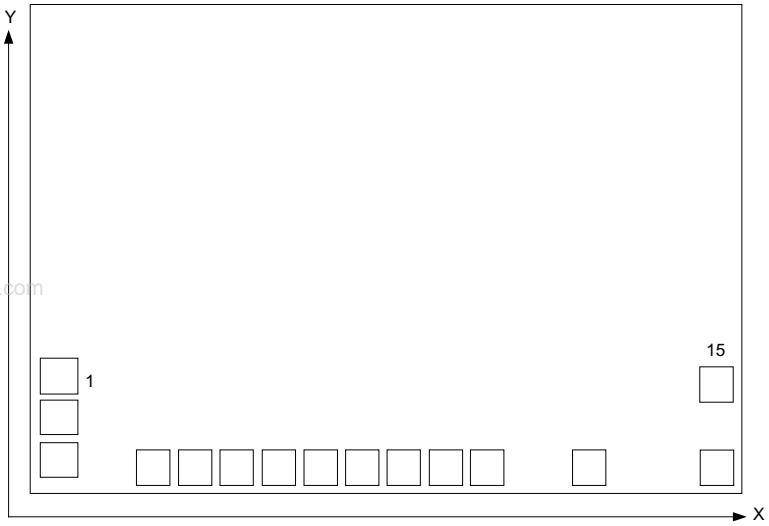
3. JA21014



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
01	PA3	70	308.7	09	VSS	864.9	70
02	PA2	70	198.9	10	OSCI	974.7	70
03	PA1	70	89.1	11	VDD	1084.5	70
04	PA0	315.9	70	12	VDD	1194.3	70
05	PB0	425.7	70	13	PWM	1462.4	70
06	PB1	535.5	70	14	VSS	1794.8	69.3
07	PB2	645.3	70	15	PWMB	1794.8	287.2
08	PB3	755.1	70				
Chip size : 1865 x 1283 (μm)^2							

Note：The IC substrate should be connect to VSS

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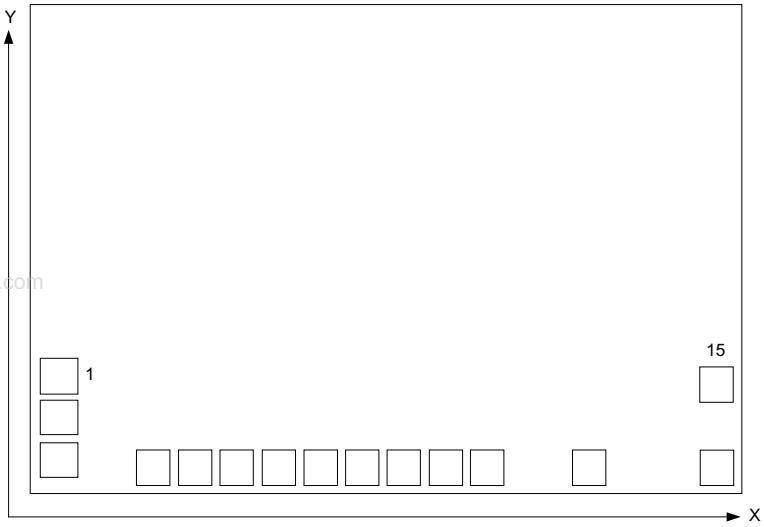
4. JA21018



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
01	PA3	70	308.7	09	VSS	864.9	70
02	PA2	70	198.9	10	OSCI	974.7	70
03	PA1	70	89.1	11	VDD	1084.5	70
04	PA0	315.9	70	12	VDD	1194.3	70
05	PB0	425.7	70	13	PWM	1462.4	70
06	PB1	535.5	70	14	VSS	1794.8	69.3
07	PB2	645.3	70	15	PWMB	1794.8	287.2
08	PB3	755.1	70				
Chip size : 1865 x 1283 $(\mu m)^2$							

Note：The IC substrate should be connect to VSS

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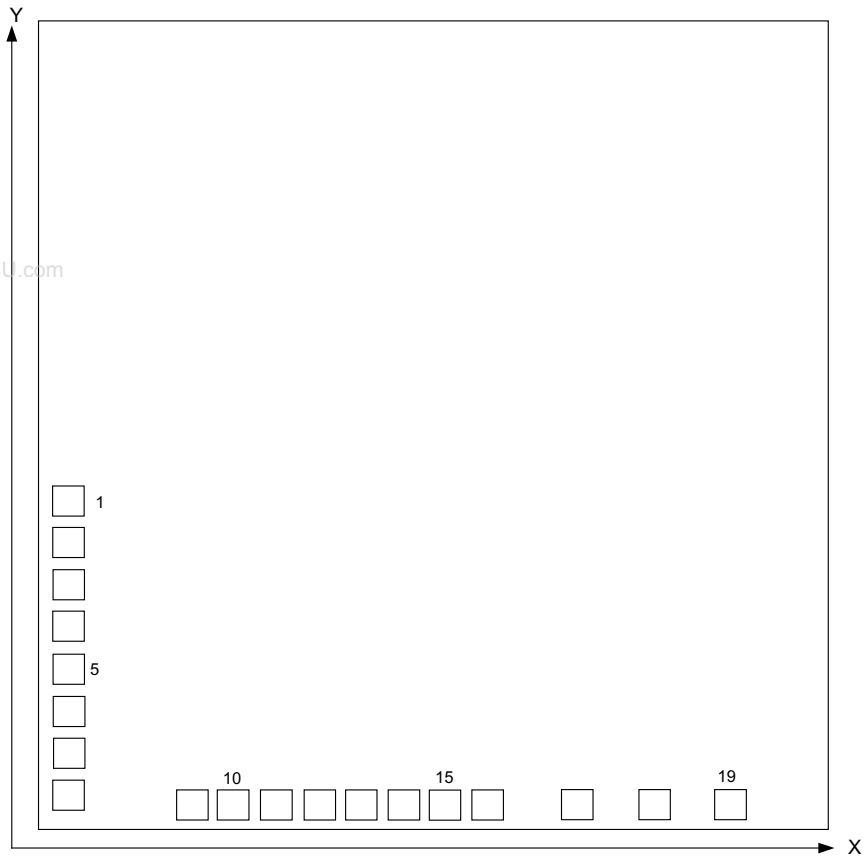
5. JA21032



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	869.3	11	PB2	612.6	70.2
2	PA6	70	759.1	12	PB3	722.8	70.2
3	PA5	70	648.9	13	VSS	833	70.2
4	PA4	70	538.7	14	OSCI	943.2	70.2
5	PA3	70	428.5	15	VDD	1053.4	70.2
6	PA2	70	318.3	16	VDD	1163.6	70.2
7	PA1	70	208.1	17	PWM	1403.8	70.2
8	PA0	70	97.9	18	VSS	1602.5	70.2
9	PB0	392.2	70.2	19	PWMB	1801.2	70.2
10	PB1	502.4	70.2				
Chip size : 2063 x 2118 $(\mu m)^2$							

Note：The IC substrate should be connect to VSS

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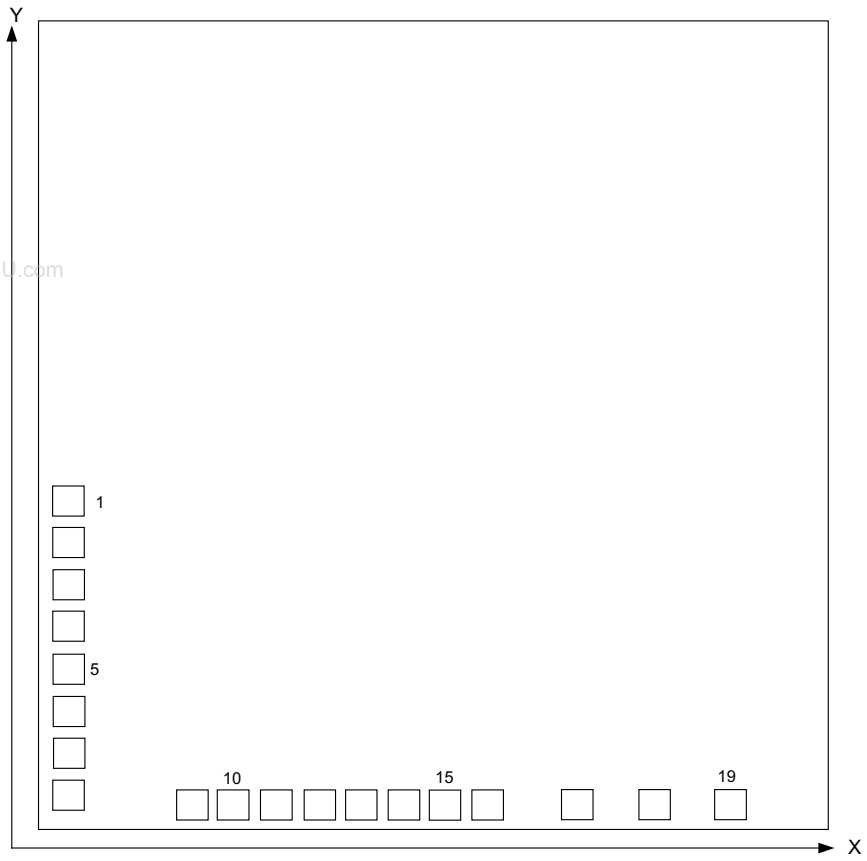
6. JA21043



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	869.3	11	PB2	612.6	70.2
2	PA6	70	759.1	12	PB3	722.8	70.2
3	PA5	70	648.9	13	VSS	833	70.2
4	PA4	70	538.7	14	OSCI	943.2	70.2
5	PA3	70	428.5	15	VDD	1053.4	70.2
6	PA2	70	318.3	16	VDD	1163.6	70.2
7	PA1	70	208.1	17	PWM	1403.8	70.2
8	PA0	70	97.9	18	VSS	1602.5	70.2
9	PB0	392.2	70.2	19	PWMB	1801.2	70.2
10	PB1	502.4	70.2				
Chip size : 2063 x 2118 $(\mu m)^2$							

Note：The IC substrate should be connect to VSS

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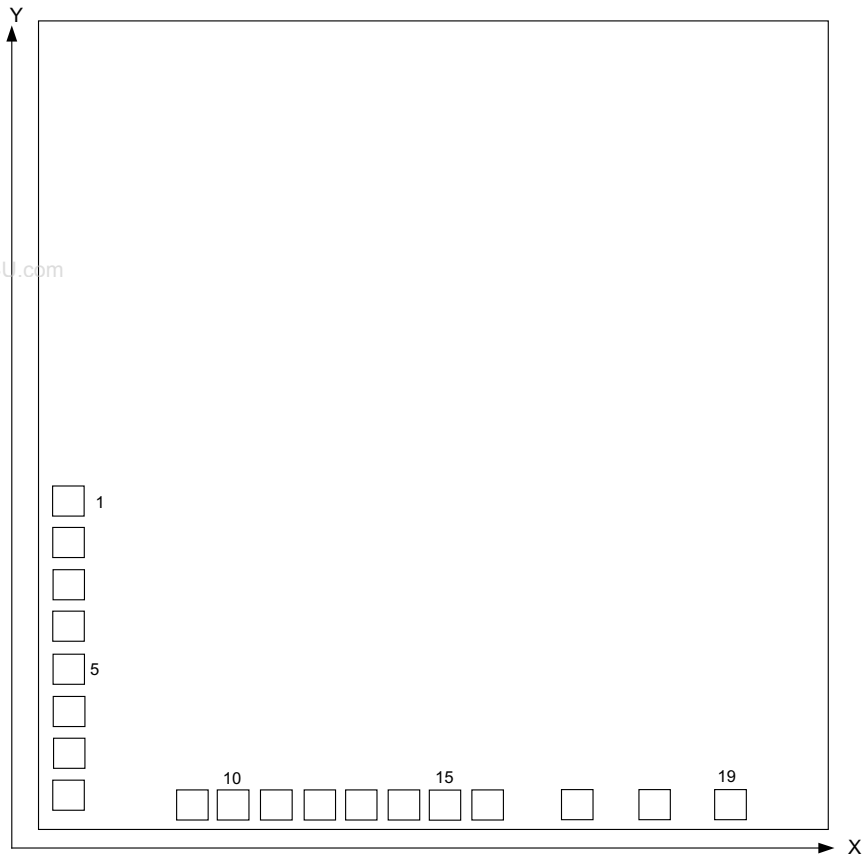
7. JA21064



Pad No.	Pad Name	X(um)	Y(um)	Pad No.	Pad Name	X(um)	Y(um)
1	PA7	70	869.3	11	PB2	612.6	70.2
2	PA6	70	759.1	12	PB3	722.8	70.2
3	PA5	70	648.9	13	VSS	833	70.2
4	PA4	70	538.7	14	OSCI	943.2	70.2
5	PA3	70	428.5	15	VDD	1053.4	70.2
6	PA2	70	318.3	16	VDD	1163.6	70.2
7	PA1	70	208.1	17	PWM	1403.8	70.2
8	PA0	70	97.9	18	VSS	1602.5	70.2
9	PB0	392.2	70.2	19	PWMB	1801.2	70.2
10	PB1	502.4	70.2				
Chip size : 2063 x 2118 $(\mu m)^2$							

Note：The IC substrate should be connect to VSS

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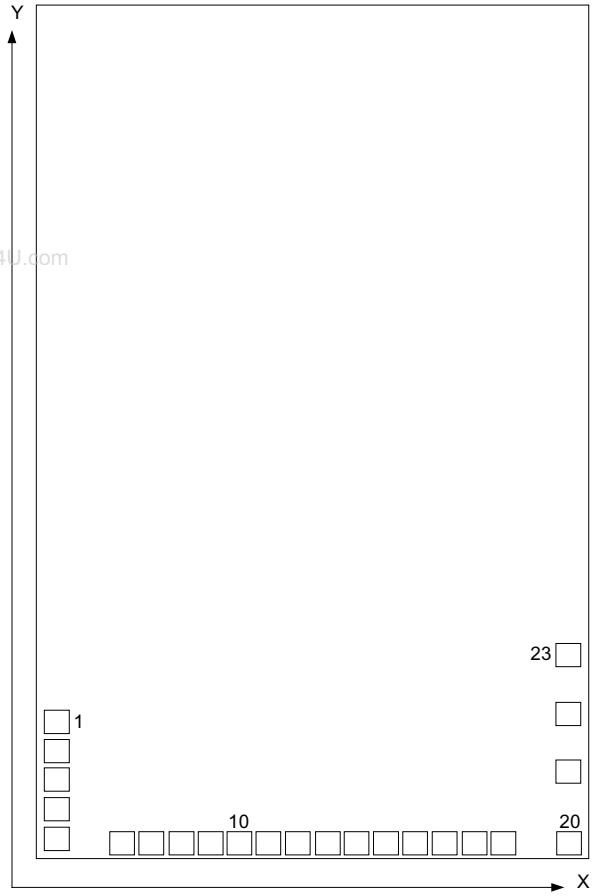
8. JA21085



Note : The IC substrate should be connect to V_{SS}

JA21085			
Pad No.	**Pad Name**	**X(um)**	**Y(um)**
1	PA7	70	528.3
2	PA6	70	418.5
3	PA5	70	308.7
4	PA4	70	198.9
5	PA3	70	89.1
6	PA2	315.9	70
7	PA1	425.7	70
8	PA0	535.5	70
9	PB0	645.3	70
10	PB1	755.1	70
11	PB2	864.9	70
12	PB3	974.7	70
13	PB4	1084.5	70
14	PB5	1194.3	70
15	PB6	1304.1	70
16	PB7	1413.9	70
17	VSS	1523.7	70
18	OSCI	1633.5	70
19	VDD	1743.3	70
20	VDD	1983.8	71.1
21	PWM	1983.8	339.2
22	VSS	1983.8	557.1
23	PWMB	1983.8	775
Chip size : 2054 x 3211 $(\mu m)^2$			

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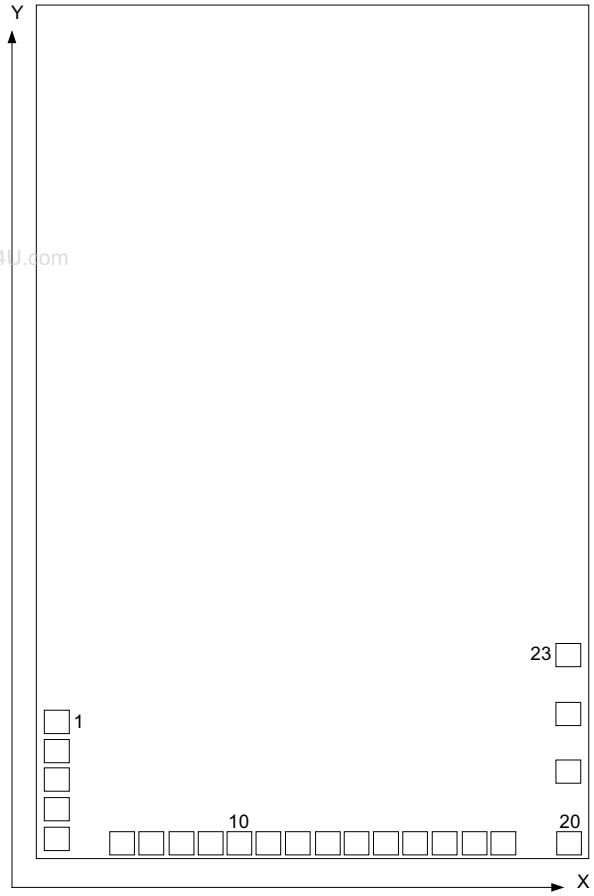
9. JA21128



Note : The IC substrate should be connect to V_{SS}

JA21128			
Pad No.	**Pad Name**	**X(um)**	**Y(um)**
1	PA7	70	528.3
2	PA6	70	418.5
3	PA5	70	308.7
4	PA4	70	198.9
5	PA3	70	89.1
6	PA2	315.9	70
7	PA1	425.7	70
8	PA0	535.5	70
9	PB0	645.3	70
10	PB1	755.1	70
11	PB2	864.9	70
12	PB3	974.7	70
13	PB4	1084.5	70
14	PB5	1194.3	70
15	PB6	1304.1	70
16	PB7	1413.9	70
17	VSS	1523.7	70
18	OSCI	1633.5	70
19	VDD	1743.3	70
20	VDD	1983.8	71.1
21	PWM	1983.8	339.2
22	VSS	1983.8	557.1
23	PWMB	1983.8	775
Chip size : 2054 x 3211 $(\mu m)^2$			

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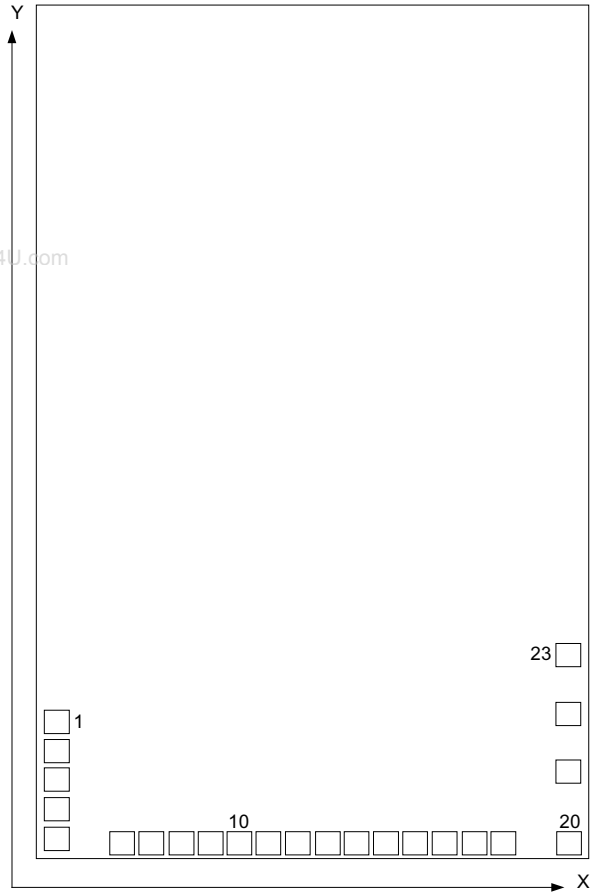
10. JA21170



Note : The IC substrate should be connect to V_{SS}

JA21170			
Pad No.	**Pad Name**	**X(um)**	**Y(um)**
1	PA7	70	528.3
2	PA6	70	418.5
3	PA5	70	308.7
4	PA4	70	198.9
5	PA3	70	89.1
6	PA2	315.9	70
7	PA1	425.7	70
8	PA0	535.5	70
9	PB0	645.3	70
10	PB1	755.1	70
11	PB2	864.9	70
12	PB3	974.7	70
13	PB4	1084.5	70
14	PB5	1194.3	70
15	PB6	1304.1	70
16	PB7	1413.9	70
17	VSS	1523.7	70
18	OSCI	1633.5	70
19	VDD	1743.3	70
20	VDD	1983.8	71.1
21	PWM	1983.8	339.2
22	VSS	1983.8	557.1
23	PWMB	1983.8	775
Chip size : 2054 x 3211 $(\mu m)^2$			

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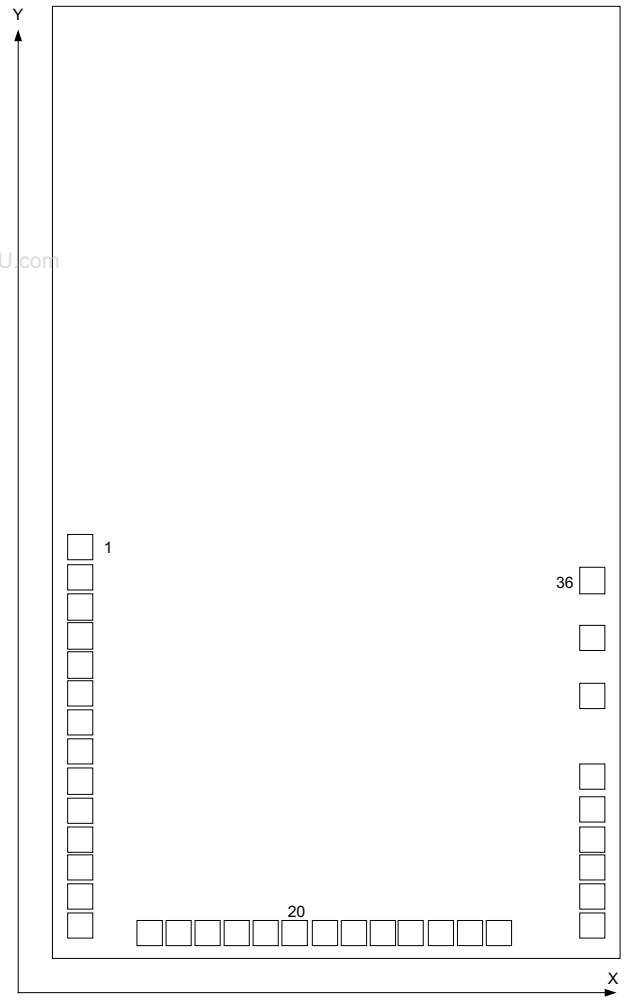
11. JA21256



JA21256			
Pad No.	**Pad Name**	**X(um)**	**Y(um)**
1	PA7	70	1530.3
2	PA6	70	1420.1
3	PA5	70	1309.9
4	PA4	70	1199.7
5	PA3	70	1089.5
6	PA2	70	979.3
7	PA1	70	869.1
8	PA0	70	758.9
9	PB0	70	648.7
10	PB1	70	538.5
11	PB2	70	428.3
12	PB3	70	318.1
13	PB4	70	207.9
14	PB5	70	97.7
15	PB6	335.2	70
16	PB7	445.4	70
17	PC0	555.6	70
18	PC1	665.8	70
19	PC2	776	70
20	PC3	886.2	70
21	PC4	996.4	70
22	PC5	1106.6	70
23	PC6	1216.8	70
24	PC7	1327	70
25	VDD	1437.2	70
26	VSS	1547.4	70
27	LVDET	1657.6	70
28	INTB	2015.9	97.7
29	TMR	2015.9	207.9
30	RESB	2015.9	318.1
31	OSCO	2015.9	428.3
32	OSCI	2015.9	538.5
33	VDD	2015.9	667.7
34	PWM	2015.9	972.9
35	VSS	2015.9	1190.2
36	PWMB	2015.9	1407.5
Chip size :2086.1 x5810.15 (μm)^2			

Note：
1. The IC substrate should be connect to VSS
2. The “RESB” pin should be connected to VDD
3. The “TMR” pin should be connected to VDD or VSS

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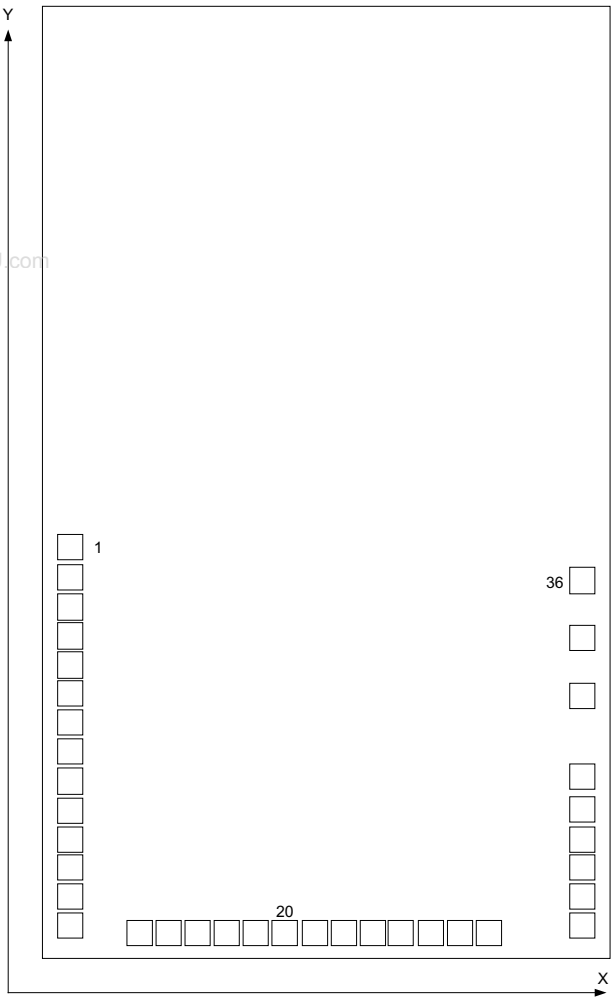
12. JA21340



JA21340			
Pad No.	**Pad Name**	**X(um)**	**Y(um)**
1	PA7	70	1530.3
2	PA6	70	1420.1
3	PA5	70	1309.9
4	PA4	70	1199.7
5	PA3	70	1089.5
6	PA2	70	979.3
7	PA1	70	869.1
8	PA0	70	758.9
9	PB0	70	648.7
10	PB1	70	538.5
11	PB2	70	428.3
12	PB3	70	318.1
13	PB4	70	207.9
14	PB5	70	97.7
15	PB6	335.2	70
16	PB7	445.4	70
17	PC0	555.6	70
18	PC1	665.8	70
19	PC2	776	70
20	PC3	886.2	70
21	PC4	996.4	70
22	PC5	1106.6	70
23	PC6	1216.8	70
24	PC7	1327	70
25	VDD	1437.2	70
26	VSS	1547.4	70
27	LVDET	1657.6	70
28	INTB	2015.9	97.7
29	TMR	2015.9	207.9
30	RESB	2015.9	318.1
31	OSCO	2015.9	428.3
32	OSCI	2015.9	538.5
33	VDD	2015.9	667.7
34	PWM	2015.9	972.9
35	VSS	2015.9	1190.2
36	PWMB	2015.9	1407.5
Chip size : 2086.1 x 5810.15 (μm)^2			

Note：
1. The IC substrate should be connect to VSS
2. The “RESB” pin should be connected to VDD
3. The “TMR” pin should be connected to VDD or VSS

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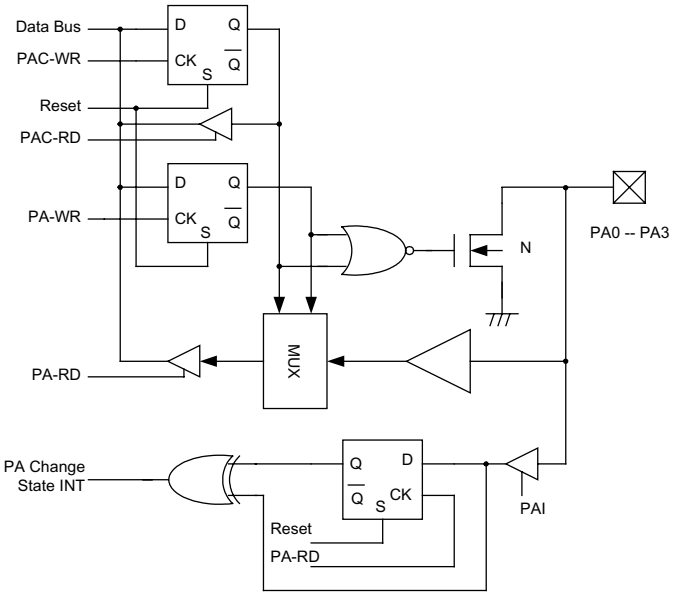
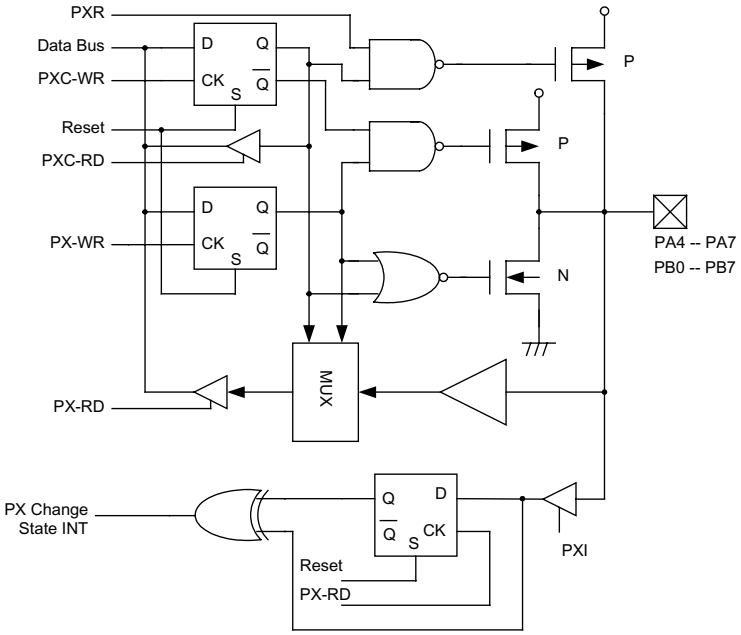
I/O Port structure

For the PA0~PA3, they are defined as NMOS open drain output only when PAC is set as output mode.



For the others of the Port A, they can be configured as follows：



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Electrical Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operating Voltage	—	—	2.4	—	5.2	V
ISTB1	Standby Current	3.0V	System HALT, 32768 Crystal Off	—	—	2	uA
ISTB2	Standby Current	3.0V	System HALT, 32768 Crystal On	—	—	10	uA
IDD1	Operating Current (RC OSC)	3.0V	Fsys=4MHz	—	1	2	mA
VIL1	Input Low Voltage for I/O	3.0V	—	0	—	0.3VDD	V
VIH1	Input High Voltage for I/O	3.0V	—	0.7VDD	—	VDD	V
VRES	Power reset voltage	—	VDD ≤ VRES, System re-start	1.6	1.8	2.0	V
IOL	I/O Sink Current	3.0V	VOL=0.1VDD	4	8	—	mA
IOH	I/O source Current	3.0V	VOH=0.9VDD	–2	–4	—	mA
RPH	Pull-High Resistance	3.0V	VIL=0V	50	100	150	KΩ
FSYS1	System Clock (RC OSC)	3.0V	Rosc=160KΩ	3.6M	4M	4.4M	Hz

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Functional Description

The JA21000 series is 2CH programmable voice synthesizer and melody generator. They provide very powerful functions for the toy applications. By way of Jaztek's tools, the users can program the series chips easily.

The spec. of voice & melody of JA21000 series are shown as below @VDD=3V

8 bits PCM		
Fosc	**Max. of sampling rate**	**Notes**
2MHz	12KHz	R=380KΩ
4MHz	22KHz	R=160KΩ
6MHz	32KHz	R=96KΩ
4 bits ADPCM		
Fosc	**Max. of sampling rate**	**Notes**
2MHz	7KHz	
4MHz	14KHz	
6MHz	22KHz	
Melody		
Item	**Spec.**	**Notes**
Tempo	68~310 beats/min.	
Beats	1/24~63/24	
Octaves	C1~B1--- C5~B5	

Output Definition

There are 4 states can be used in output states declaration. They are "X", "H", "L", and "F".
The definitions of states are list as follows.

State	Definition
X	Don't care, the output pin is set as "input mode"
H	Output High, the output pin is set as logical "Hi" level.
L	Output Low, the output pin is set in logical "Low" level.
F	Output Flash, the output pin is set as "flash" output. It can define as sequential or synchronous mode.

For the "F" state, two output modes can be defined by " FR=Seq/n" and "FR=Syn/n" commands.
The " Seq " and " Syn " mean "Sequential" and "Synchronous" modes, respectively. The n represent to flash rate of output is n times/sec(Hz), it can be 1, 2, 4, or 16 Hz. The flash rate also can be defined as " FR=VV1 or VV2" and "FR=MT1 or MT2". For VVx and MTx commands, the output is synchronous mode only.
VV1, VV2: The output level follows with the volume output of channel 1 (VV1) or channel 2 (VV2).
MT1, MT2: The output level follows with the melody tempo output of channel1 (MT1) or channel2 (MT2).

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Instruction Set

Path commands	Description
Poweron	To set the power on initial
Input state name	To active input state
Out state name	To active output state
Path name	To execute the specifies path
Tempo=n	Define the tempo value (n=68-310)
Vol=n or Vol_1=n	Define the AUD1 output volume (n=0-15)
Vol_2=n	Define the AUD2 output volume (n=0-15)
SR=n or SR_1=n	Define the channel 1 sample rate (3K-24KHz)
SR_2=n	Define the channel 2 sample rate (3K-24KHz)
DELAY(N ms or N s)	To delay N*1 ms or N*1 s (1 ms ~ 65 s)
TRn?H:pathname	If TRn is logic High, then pathname is executed.
TRn?L:pathname	If TRn is logic Low, then pathname is executed.
FR=Seq/n, Syn/n, VV1, VV2, MT1 or MT2	Set the output pulse rate to “n” pulses per second sequentially or synchronously. n=1, 2, 4, 16
END	Enter power down mode.
n*Sound file	Play the sound file n times.
[n*Sound file]	Play the sound file n times. But is continuing execute next path concurrent.
Ri=PA	Read Port A to Ri
STOP1	Stop the playback of channel 1 sound.
STOP2	Stop the playback of channel 2 sound.
Ri=data	Set the content of Ri to be data
Ri=Rj	Set the content of Ri to be Rj
Ri(bn)=1 or 0	Set bit (bn) to be 1 or 0, bn=0-7
Ri=Ri+Rj	Add Ri with Rj to Ri.
Ri=Rj+data	Add immediate data with Ri to Ri.
Ri=Rj.AND.data	And immediate data with Rj to Ri.
Ri=Rj.OR.data	OR immediate data with Rj to Ri.
Ri=Rj.XOR.data	XOR immediate data with Rj to Ri.
Ri=SHL(n)	Shift left of the Ri content n bits; n=1, 2, …, 7.
Ri=SHR(n)	Shift right of the Ri content n bits; n=1, 2, …, 7.
Ri?data:PathName	If Ri=data then PathName is executed.
Ri?Rj:PathName	If Ri=Rj then PathName is executed.
Ri(bn)?1:PathName	If Ri.bn is “1” then PathName is executed.
Ri(bn)?0:PathName	If Ri. bn is “0” then Path Name is executed.
Ri:[Path1, Path2, Path3,…,Pathn]	Path1 is executed when Ri=1; Path2 is executed when Ri=2; : : pathn is executed when Ri=n.
Ri=Rand(N)	Get a random code & put it to Ri. The max of random counter is N. (N≤255)
Timer(n): PathName	Initial the timer. If timer is time-up, then Path is executed. n = 1s — 32768s or n = 0.1s — 3276.8s
TimerON	Turn on the timer count.
TimerOFF	Turn off the timer count.

“Vol_1=15” is equal “Vol=15”.
“SR_1=4KHz” is equal “SR=4KHz”
The VV represents voice volume.
MT means melody tempo.
Ri, Rj are working Registers.

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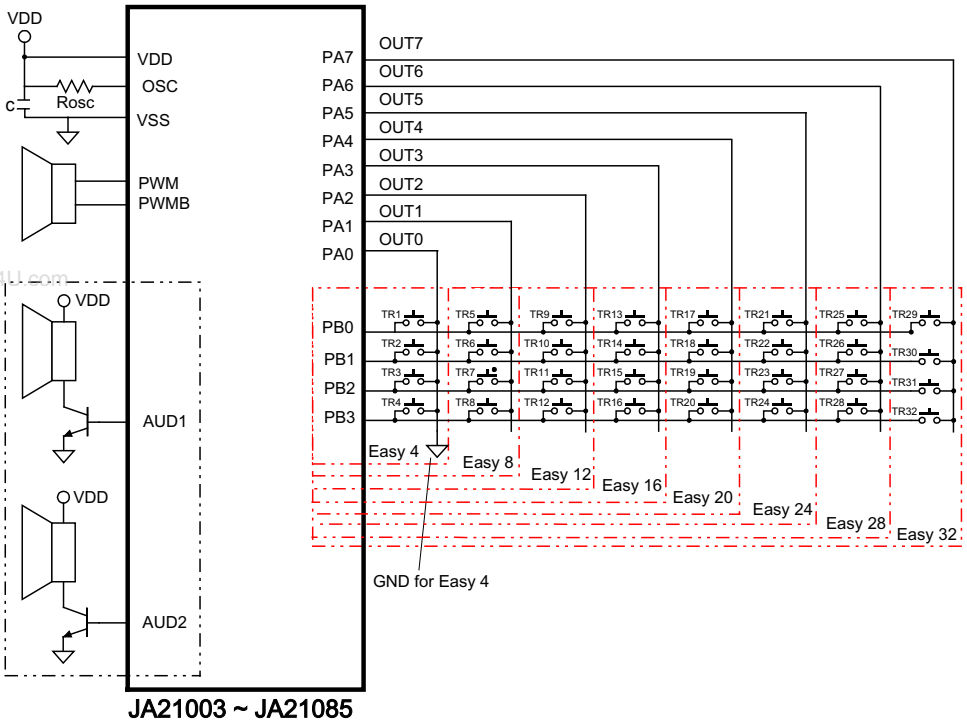
Application Circuit 1 (JA21003~JA21085)



EasyN (N=4, 8, 12, … ,32) for JA21003 — JA21085

Key No	Key Name	Scan Input	Scan Output	Output State(I/O pins)
Easy 4	TR1 — TR4	PB0 — PB3	VSS	PA0(OUT0) — PA7(OUT7)
Easy 8	TR1 — TR8	PB0 — PB3	PA0 — PA1	PA2(OUT2) — PA7(OUT7)
Easy12	TR1 — TR12	PB0 — PB3	PA0 — PA2	PA3(OUT3) — PA7(OUT7)
Easy 16	TR1 — TR16	PB0 — PB3	PA0 — PA3	PA4(OUT4) — PA7(OUT7)
Easy 20	TR1 — TR20	PB0 — PB3	PA0 — PA4	PA5(OUT5) — PA7(OUT7)
Easy 24	TR1 — TR24	PB0 — PB3	PA0 — PA5	PA6(OUT6) — PA7(OUT7)
Easy 28	TR1 — TR28	PB0 — PB3	PA0 — PA6	PA7(OUT7)
Easy 32	TR1 — TR32	PB0 — PB3	PA0 — PA7	X

Note: For JA21003—JA21018 bodies, the max. of Easy N is Easy 16.
For JA21032—JA21085 bodies, the max. of Easy N is Easy 32.
The AUD1 and AUD2 is shared with PWM and PWMB.

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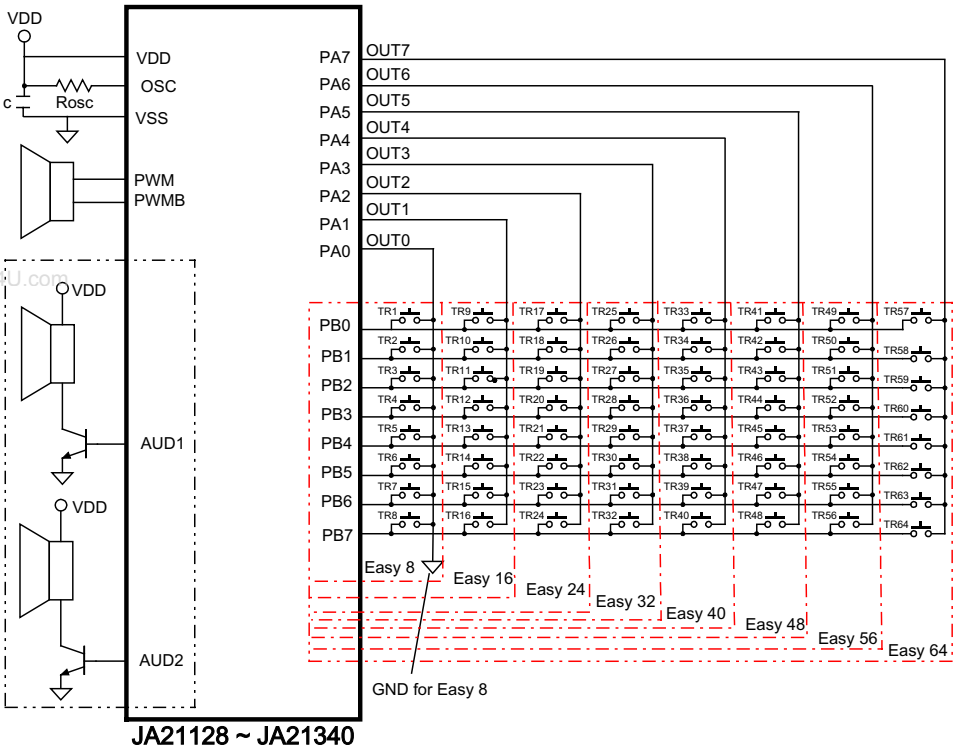
Application Circuit 2 (JA21128~JA21340)



EasyN (N=8, 16, 24, … ,64) for JA21128 — JA21340

Key No	Key Name	Scan Input	Scan Output	Output State
Easy 8	TR1 — TR8	PB0 — PB7	VSS	PA0(OUT0) — PA7(OUT7)
Easy 16	TR1 — TR16	PB0 — PB7	PA0 — PA1	PA2(OUT2) — PA7(OUT7)
Easy 24	TR1 — TR24	PB0 — PB7	PA0 — PA2	PA3(OUT3) — PA7(OUT7)
Easy 32	TR1 — TR32	PB0 — PB7	PA0 — PA3	PA4(OUT4) — PA7(OUT7)
Easy 40	TR1 — TR40	PB0 — PB7	PA0 — PA4	PA5(OUT5) — PA7(OUT7)
Easy 48	TR1 — TR48	PB0 — PB7	PA0 — PA5	PA6(OUT6) — PA7(OUT7)
Easy 56	TR1 — TR56	PB0 — PB7	PA0 — PA6	PA7(OUT7)
Easy 64	TR1 — TR64	PB0 — PB7	PA0 — PA7	X

Note: The AUD1 and AUD2 is shared with PWM and PWMB.

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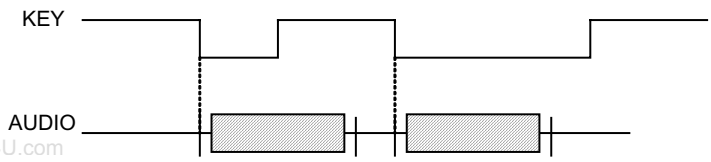
Application Notes

I. Common key definition v.s. programming

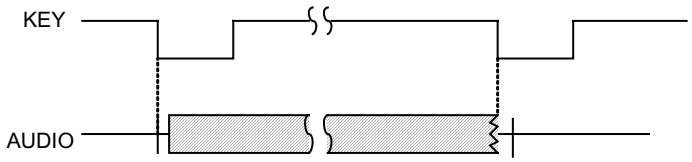
One shot



Example:

easy 4
one.wav/ad4 ; #0
input states
; TG1 TG2 TG3 TG4 ……..
state0: /KEY1 X X X
state1: X X X X
paths
poweron: state0 end
KEY1: state1 1*#0 state0 end

Toggle Active



Example:

easy 4
one.wav/ad4 ; #0
input states
; TG1 TG2 TG3 TG4 ……..
state0: /KEY1 X X X
state1: /KEY2 X X X
paths
poweron: state0 end
KEY1: state1 1*#0 state0 end
KEY2:stop1 end

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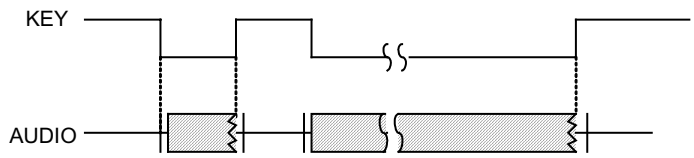
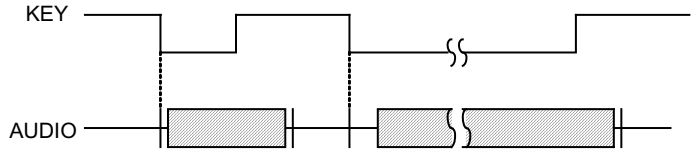
Level Hold



Example:

easy 4
one.wav/ad4 ; #0
input states
; TG1 TG2 TG3 TG4 ……..
state0: /KEY1 X X X
state1: KEY2/ X X X
paths
poweron: state0 end
KEY1: state1 1*#0 KEY1 end
KEY2:stop1 end

Level Trigger (Level Hold Complete Cycle)



Example:

easy 4
one.wav/ad4 ; #0
input states
; TG1 TG2 TG3 TG4 ……..
state0: /KEY1 X X X
state1: X X X X
paths
poweron: state0 end
KEY1: state1 1*#0 TR1?L:KEY1 state0 end

II. 32K Crystal Oscillator Application

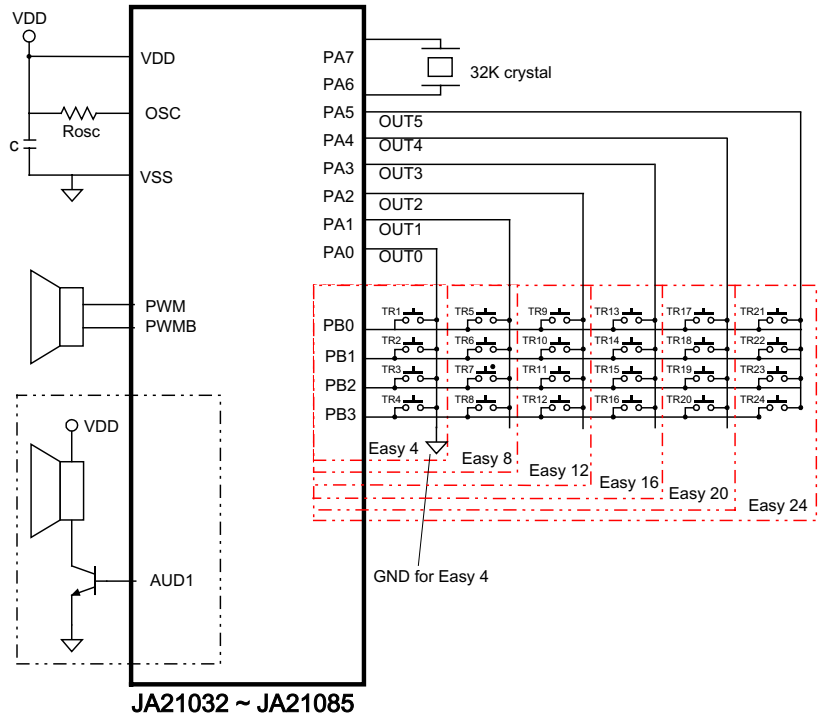
JA21000 series provide two power saving modes, one is **HALT** and the other is **STOP** mode. In HALT mode, the 32K crystal is on and system clock is off. Timer overflow and PX change state can wakeup the system. In HALT mode, 32K crystal offers the Timer count source and the power consumption only takes few uA. This is very useful in long-term timer count application.

32768Hz Crystal oscillator shares with PA table

Part No.	Description
JA21340	PA 6~7
JA21256	PA 6~7
JA21170	PA 6~7
JA21128	PA 6~7
JA21085	PA 6~7
JA21064	PA 6~7
JA21043	PA 6~7
JA21032	PA 6~7
JA21018	PA 2~3
JA21014	PA 2~3
JA21007	PA 2~3
JA21003	PA 2~3

Note：The PA n & PA n+1 or 32K crystal mode is selected by code option.

For example, if using JA21032 the application circuit would be：



JA21032 ~ JA21085

Note：The PWM, PWMB and AUD1, AUD2 is shared with the same pins.

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