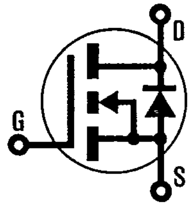
HEXFET® TRANSISTORS IRFP040 IRFP042

N-CHANNEL POWER MOSFETs TO-247AC PACKAGE



50 Volt, 0.028 Ohm, HEXFET TO-247AC (TO-3P) Plastic Package

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and great device ruggedness.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, and high energy pulse circuits.

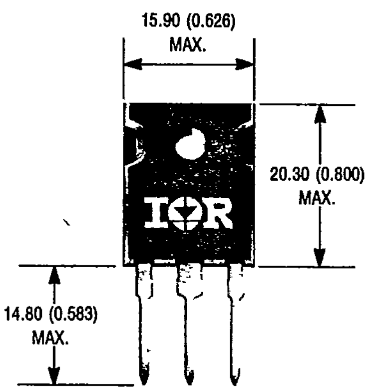
Product Summary

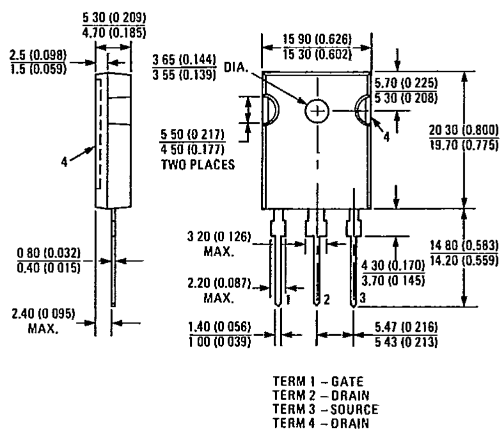
Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFP040	50V	0.028Ω	40A*
IRFP042	50V	0.035Ω	40A*

Features:

- Isolated Central Mounting Hole
- Rugged Package Design
- Ideal for Switch Mode Power Supplies
- Low Thermal Resistance
- Fast Switching

CASE STYLE AND DIMENSIONS





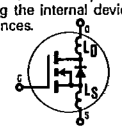
Conforms to JEDEC Outline TO-247AC (TO-3P)
Dimensions in Millimeters and (Inches)

*I_D Current limited by pin diameter

Absolute Maximum Ratings

	Parameter	IRFP040	IRFP042	Units
V_{DS}	Drain - Source Voltage ①	40	40	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	40	40	V
I_D @ T_C = 25°C	Continuous Drain Current ⑤	40	40	A
I_D @ T_C = 100°C	Continuous Drain Current	35	32	A
I_{DM}	Pulsed Drain Current ②	220	200	A
V_{GS}	Gate - Source Voltage	±20		V
P_D @ T_C = 25°C	Max. Power Dissipation	150		W
	Linear Derating Factor	1.2		W/K ⑥
I_{LM}	Inductive Current, Clamped	220 (See Fig. 14), L = 100μH	200	A
I_L	Unclamped Inductive Current (Avalanche Current) ③	(See Fig. 15) 4.3		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

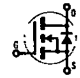
Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFP040	50	—	—	—	V_{GS} = 0V
		IRFP042	50	—	—	—	I_D = 250 μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
I_{GSS}	Gate-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	—	—	−500	nA	V_{GS} = −20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000	μA	V_{DS} = Max. Rating × 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ④ ⑤	IRFP040	40	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)max.}$, V_{GS} = 10V
		IRFP042	40	—	—	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ④	IRFP040	—	0.024	0.028	Ω	V_{GS} = 10V, I_D = 32A
		IRFP042	—	0.030	0.035	Ω	
g_{fs}	Forward Transconductance ④	ALL	14	21	—	S (℧)	V_{DS} = 2 × V_{GS}, I_{DS} = 26A
C_{iss}	Input Capacitance	ALL	—	2000	—	pF	V_{GS} = 0V, V_{DS} = +25V, f = 1.0 MHz
C_{oss}	Output Capacitance	ALL	—	1200	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	ALL	—	290	—	pF	
$t_{d(on)}$	Turn On Delay Time	ALL	—	17	26	ns	V_{DD} = 25V, I_D ≈ 51A, R_G = 9.1Ω, R_D = 0.47Ω
t_r	Rise Time	ALL	—	130	200	ns	See Fig. 16
$t_{d(off)}$	Turn Off Delay Time	ALL	—	39	59	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	—	89	130	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	46	69	nC	V_{GS} = 10V, I_D = 51A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	—	14	21	nC	
Q_{gd}	Gate Drain ("Miller") Charge	ALL	—	18	27	nC	
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. / Modified MOSFET symbol showing the internal device inductances. 
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	—	—	0.83	K/W ⑥	
R_{thCS}	Case-to-Sink	ALL	—	0.10	—	K/W ⑥	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	—	—	40	K/W ⑥	Typical socket mount.
	Mounting Torque	ALL	—	—	10	in.•lbs.	Standard 6-32 screw

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFP040	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		IRFP042	—	—	40	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFP040	—	—	220	A	
		IRFP042	—	—	200	A	
V_{SD}	Diode Forward Voltage ②	ALL	—	—	2.5	V	$T_C = 25°C$, $I_S = 56A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time	ALL	80	181	414	ns	$T_J = 25°C$, $I_F = 51A$, $dI_F/dt = 100A/\mu s$
Q_{RR}	Reverse Recovered Charge	ALL	0.31	0.72	1.75	μC	$T_J = 25°C$, $I_F = 51A$, $dI_F/dt = 100A/\mu s$
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25°C$ to $150°C$

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ @ $V_{dd} = 25V$, $T_j = 25°C$, $L = 100\ \mu H$, $R_G = 25\Omega$

④ Pulse Test: Pulse width ≤ 300 μs, Duty Cycle ≤ 2%

⑤ I_D current limited by pin diameter

⑥ K/W = °C/W
W/K = W/°C

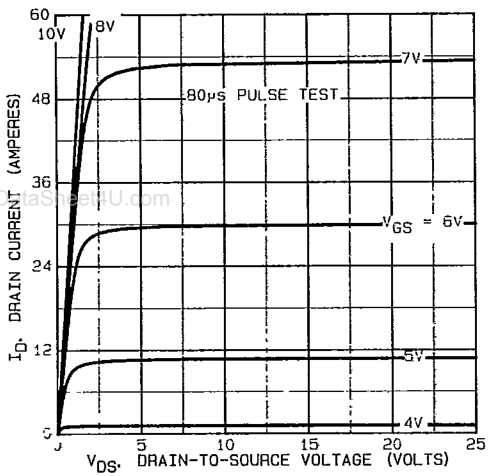


Fig. 1 — Typical Output Characteristics

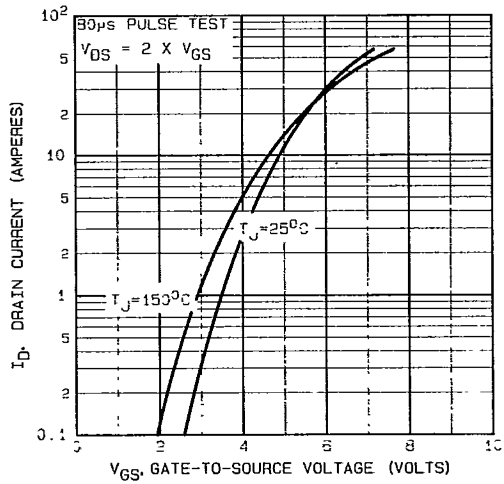


Fig. 2 — Typical Transfer Characteristics

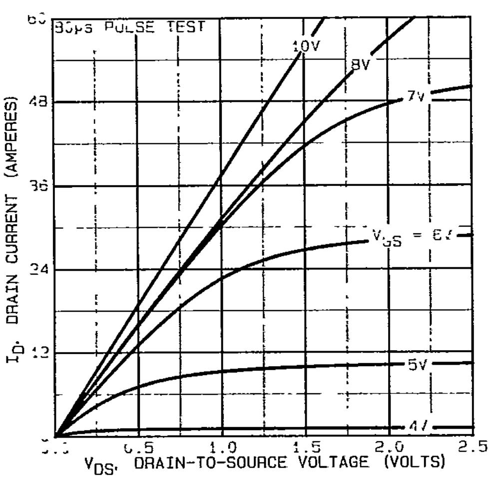


Fig. 3 — Typical Saturation Characteristics

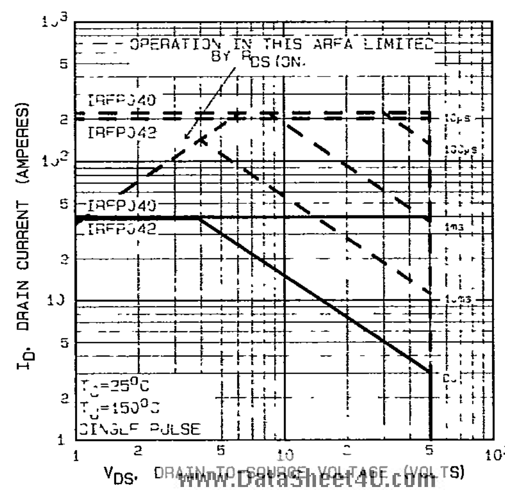


Fig. 4 — Maximum Safe Operating Area

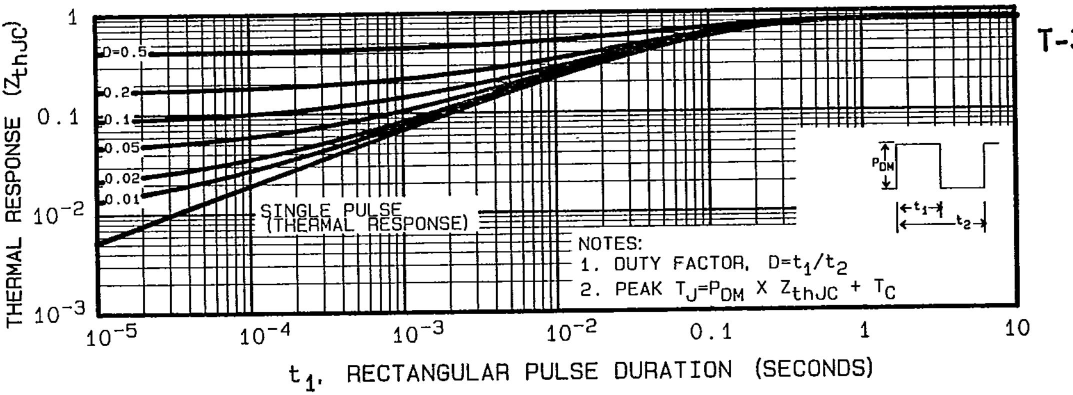


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

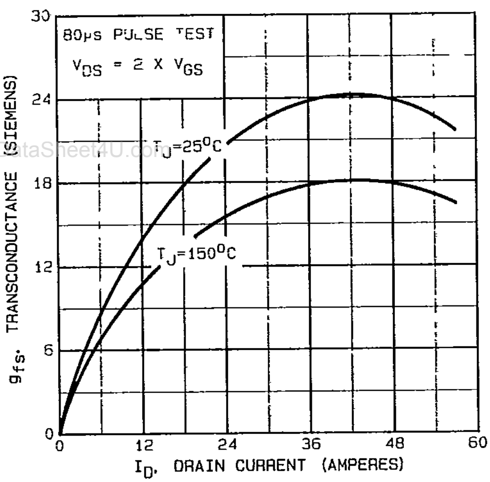


Fig. 6 – Typical Transconductance Vs. Drain Current

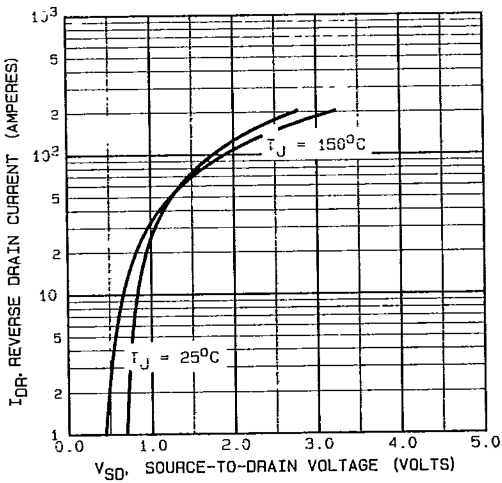


Fig. 7 – Typical Source-Drain Diode Forward Voltage

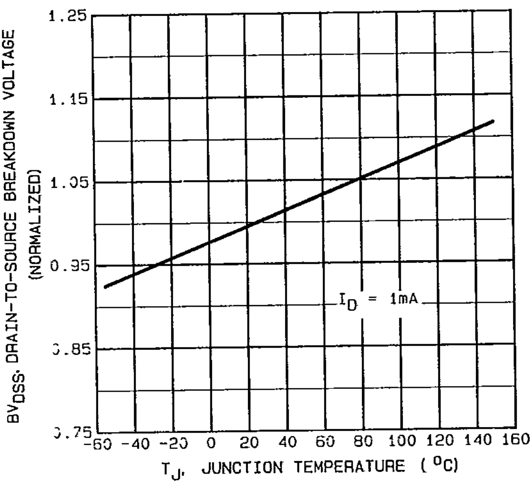


Fig. 8 – Breakdown Voltage Vs. Temperature

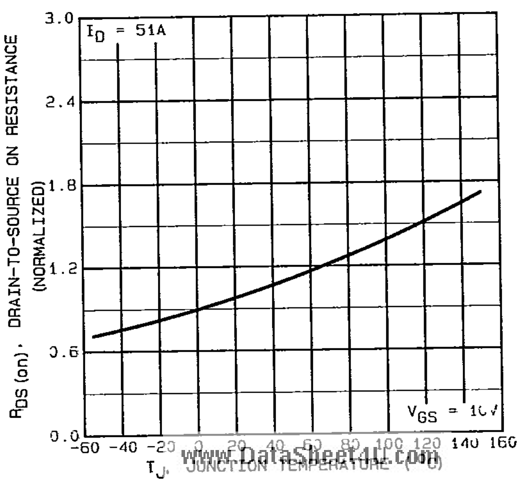


Fig. 9 – Normalized On-Resistance Vs. Temperature

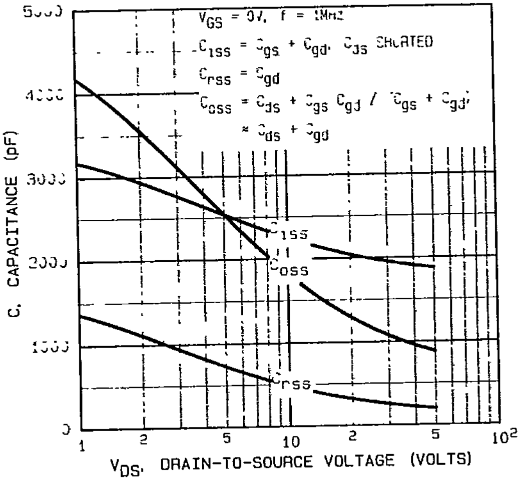


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

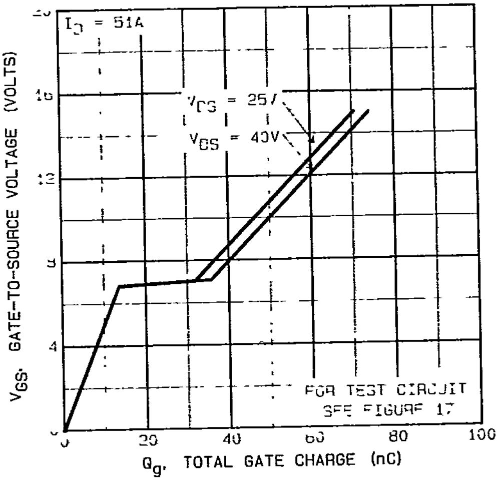


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

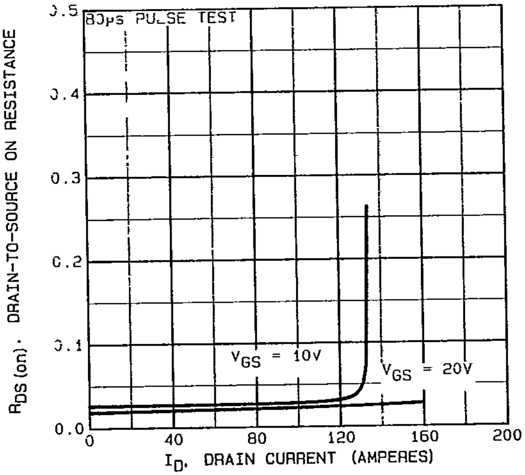


Fig. 12 — Typical On-Resistance Vs. Drain Current

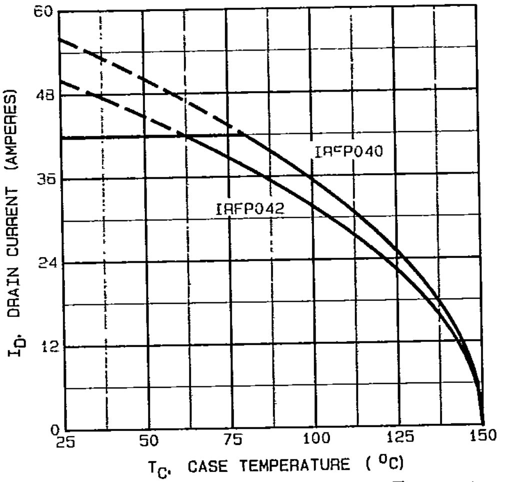


Fig. 13 — Maximum Drain Current Vs. Case Temperature

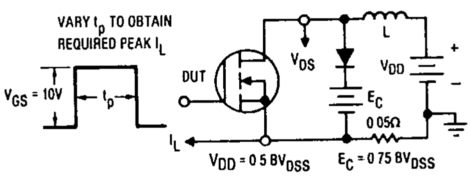


Fig. 14a — Clamped Inductive Test Circuit

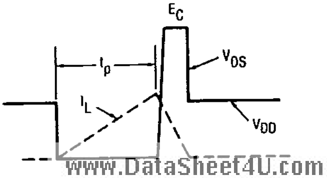


Fig. 14b — Clamped Inductive Waveforms

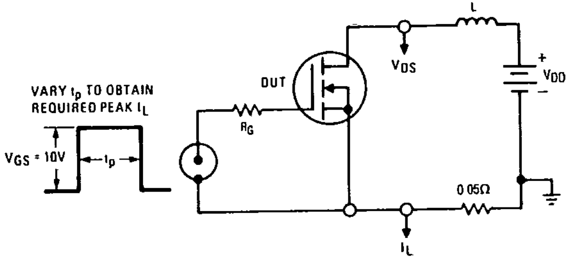


Fig. 15a — Unclamped Inductive Test Circuit

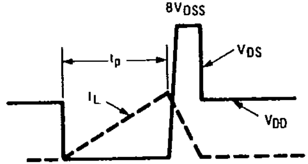


Fig 15b. — Unclamped Inductive Load Test Waveforms

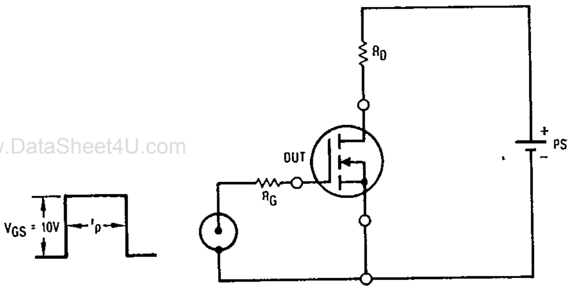


Fig. 16 — Switching Time Test Circuit

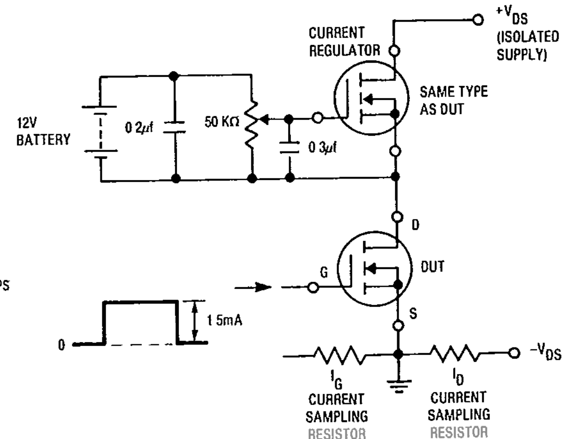


Fig. 17 — Gate Charge Test Circuit