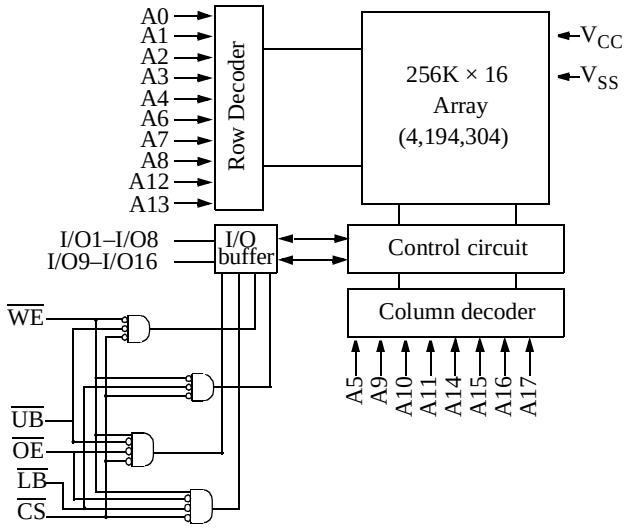
2.3V to 3.6V 256K×16 Intelliwatt™ low-power CMOS SRAM with one chip enable

‘Features

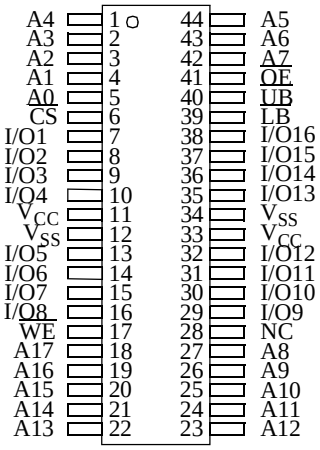
- AS6UA25616
- Intelliwatt™ active power circuitry
- Industrial and commercial temperature ranges available
- Organization: 262,144 words x 16 bits
- 2.7V to 3.6V at 55 ns
- 2.3V to 2.7V at 70 ns
- Low power consumption: ACTIVE
  - 114 mW at 3.6V and 55 ns
  - 68 mW at 2.7V and 70 ns
- Low power consumption: STANDBY
  - 72 µW max at 3.6V
  - 41 µW max at 2.7V
- 1.2V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CS}$, $\overline{OE}$ inputs
- Smallest footprint packages
  - 48-ball FBGA
  - 400-mil 44-pin TSOP II
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement (top view)

44-pin 400-mil TSOP II



48-CSP Ball-Grid-Array Package

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	NC
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CS}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	V_{SS}	I/O12	A17	A7	I/O4	V_{CC}
E	V_{CC}	I/O13	NC	A16	I/O5	V_{SS}
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	$\overline{WE}$	I/O8
H	NC	A8	A9	A10	A11	NC

Selection guide

Product	V_{CC} Range Min (V)	V_{CC} Range Typ[2] (V)	V_{CC} Range Max (V)	Speed (ns)	Power Dissipation Operating (I_{CC}) Max (mA)	Power Dissipation Standby (I_{SB1}) Max (µA)
AS6UA25616	2.7	3.0	3.6	55	2	20
AS6UA25616	2.3	2.5	2.7	70	1	15

Functional description

The AS6UA25616 is a low-power CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words x 16 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 55/70 ns are ideal for low-power applications. Active high and low chip enables ($\overline{CS}$) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CS}$ is high, or $\overline{UB}$ and $\overline{LB}$ are high, the device enters standby mode: the AS6UA25616 is guaranteed not to exceed 72 µW power consumption at 3.6V and 55 ns; 41µW at 2.7V and 70 ns. The device also returns data when V_{CC} is reduced to 1.5V for even lower power consumption.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CS}$) low, and $\overline{UB}$ and/or $\overline{LB}$ low. Data on the input pins I/O1–O16 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CS}$ (write cycle 2).To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$), chip enable ($\overline{CS}$), $\overline{UB}$ and $\overline{LB}$ low, with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, or ($\overline{UB}$) and ($\overline{LB}$), output drivers stay in high-impedance mode.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to bewritten and read. $\overline{LB}$ controls the lower bits, I/O1–I/O8, and $\overline{UB}$ controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are CMOS-compatible, and operation is from a single 2.3V to 3.6V supply. Device is available in the JEDEC standard 400-mm, TSOP II, and 48-ball FBGA packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to V_{SS}		V_{tIN}	–0.5	V_{CC} + 0.5	V
Voltage on any I/O pin relative to GND		$V_{tI/O}$	–0.5		V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	–65	+150	°C
Temperature with V_{CC} applied		T_{bias}	–55	+125	°C
DC output current (low)		I_{OUT}	–	20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Supply Current	I/O1–I/O8	I/O9–I/O16	Mode
H	X	X	X	X	I_{SB}	High Z	High Z	Standby (I_{SB})
L	X	X	H	H				
L	H	H	X	X	I_{CC}	High Z	High Z	Output disable (I_{CC})
L	H	L	L	H	I_{CC}	D_{OUT}	High Z	Read (I_{CC})
			H	L		High Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	I_{CC}	D_{IN}	High Z	Write (I_{CC})
			H	L		High Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

Key: X = Don’t care, L = Low, H = High.

Recommended operating condition (over the operating range)

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –2.1mA	V_{CC} = 2.7V	2.4		V
		I_{OH} = –0.5mA	V_{CC} = 2.3V	2.0		
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA	V_{CC} = 2.7V		0.4	V
		I_{OL} = 0.5mA	V_{CC} = 2.3V		0.4	
V_{IH}	Input HIGH Voltage		V_{CC} = 2.7V	2.2	V_{CC} + 0.5	V
			V_{CC} = 2.3V	2.0	V_{CC} + 0.3	
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V	–0.5	0.8	V
			V_{CC} = 2.3V	–0.3	0.6	
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Load Current	GND ≤ V_O ≤ $V_{CC;}$ Outputs High Z		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CS}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 0mA, f = 0	V_{CC} = 3.6V		2	mA
			V_{CC} = 2.7V		1	
I_{CC1} @ 1 MHz	Average V_{CC} Operating Supply Current at 1 MHz	$\overline{CS}$ ≤ 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} – 0.2V, f = 1 mS	V_{CC} = 3.6V		5	mA
			V_{CC} = 2.7V		4	
I_{CC2}	Average V_{CC} Operating Supply Current	$\overline{CS}$ ≠ V_{IL}, V_{IN} = V_{IL} or V_{IH}, f = f_{Max}	V_{CC} = 3.6V (55/70 ns)		40/30	mA
			V_{CC} = 2.7V (70 ns)		25	
I_{SB}	$\overline{CS}$ Power Down Current; TTL Inputs	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ = $\overline{LB}$ ≥ V_{IH}, other inputs = V_{IL} or V_{IH}, f = 0	V_{CC} = 3.6V		100	µA
			V_{CC} = 2.7V		100	
I_{SB1}	$\overline{CS}$ Power Down Current; CMOS Inputs	$\overline{CS}$ ≥ V_{CC} – 0.2V or $\overline{UB}$ = $\overline{LB}$ ≥ V_{CC} – 0.2V, other inputs = 0V – V_{CC}, f = f_{Max}	V_{CC} = 3.6V		20	µA
			V_{CC} = 2.7V		15	
I_{SBDR}	Data Retention	$\overline{CS}$ ≥ V_{CC} – 0.1V, $\overline{UB}$ = $\overline{LB}$ = V_{CC} – 0.1V f = 0	V_{CC} = 1.2V		2	µA

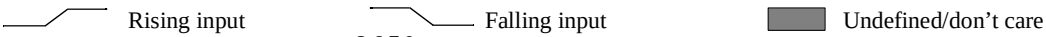
Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

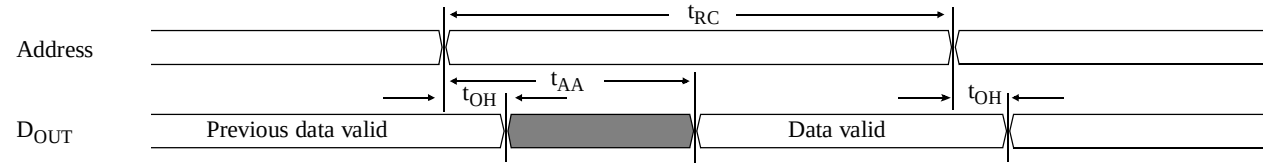
Read cycle (over the operating range)[3,9]

Parameter	Symbol	–55		–70		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	t_{RC}	55	–	70	–	ns	
Address access time	t_{AA}	–	55	–	70	ns	3
Chip enable ($\overline{CS}$) access time	t_{ACS}	–	55	–	70	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	25	–	35	ns	
Output hold from address change	t_{OH}	10	–	10	–	ns	5
$\overline{CS}$ low to output in low Z	t_{CLZ}	10	–	10	–	ns	4, 5
$\overline{CS}$ high to output in high Z	t_{CHZ}	0	20	0	20	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	5	–	5	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ access time	t_{BA}	–	55	–	70	ns	
$\overline{UB}$/$\overline{LB}$ low to low Z	t_{BLZ}	10	–	10	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ high to high Z	t_{BHZ}	0	20	0	20	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	0	20	0	20	ns	4, 5
Power up time	t_{PU}	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	55	–	70	ns	4, 5

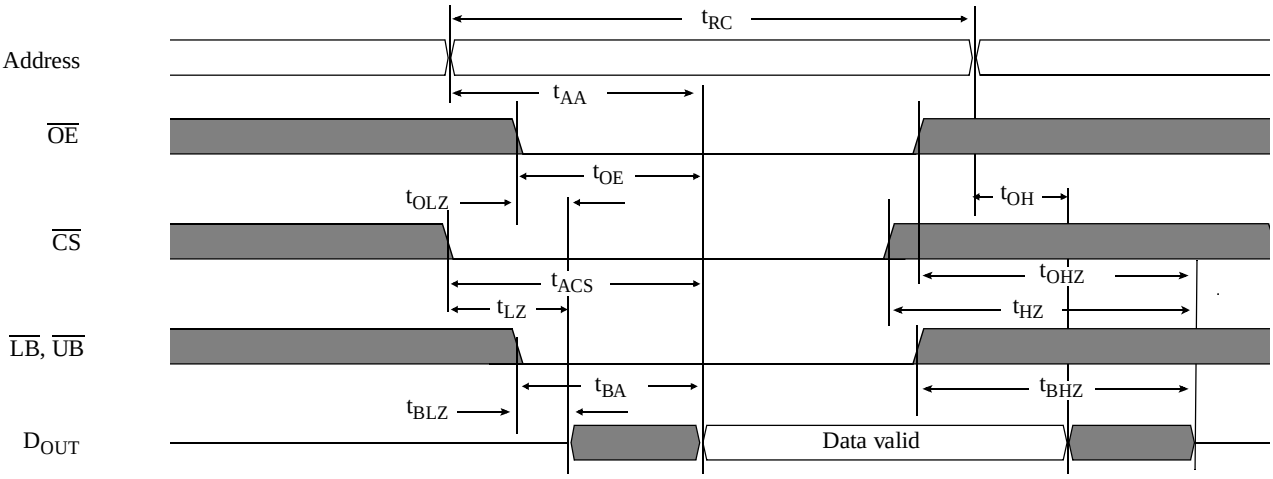
Key to switching waveforms



Read waveform 1 (address controlled)[3,6,7,9]



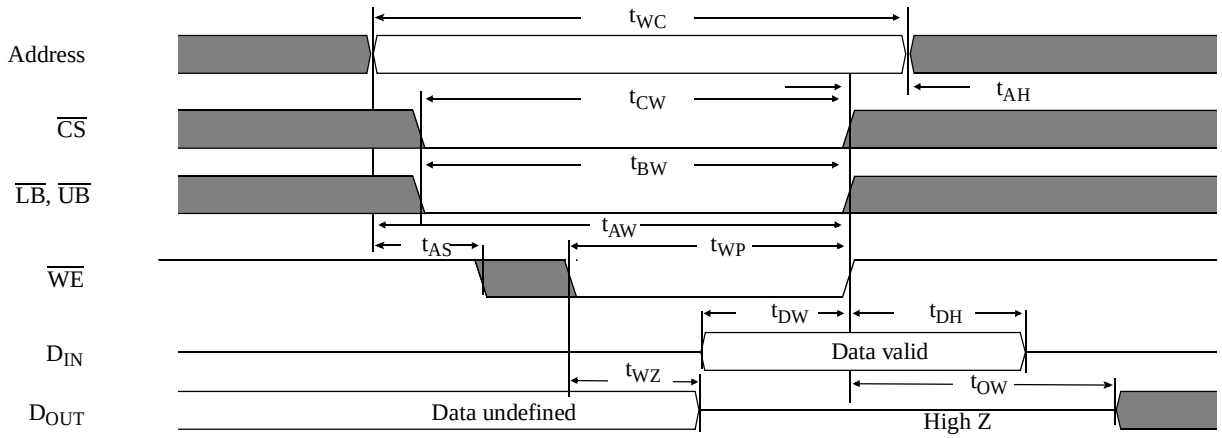
Read waveform 2 ($\overline{CS}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)[3,6,8,9]



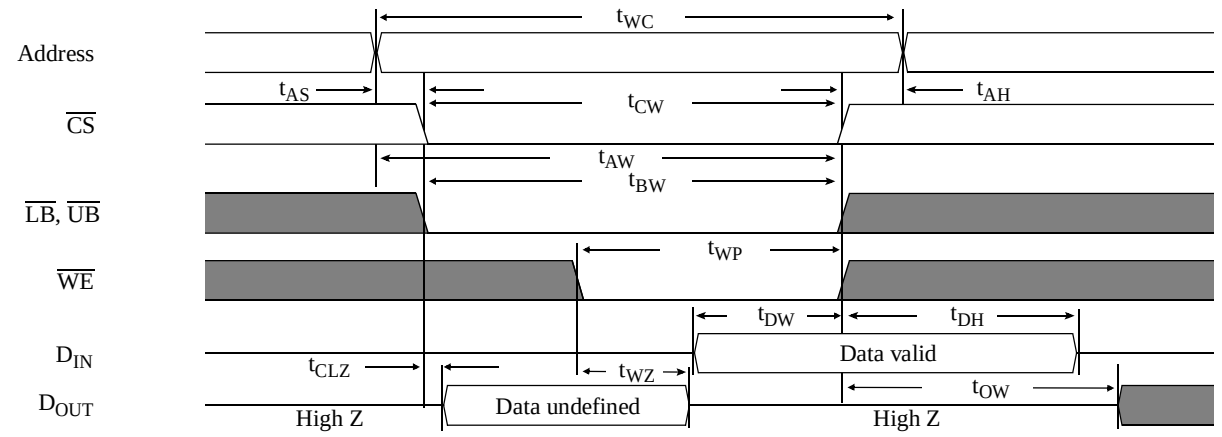
Write cycle (over the operating range)[11]

Parameter	Symbol	–55		–70		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	55	–	70	–	ns	
Chip enable to write end	t_{CW}	40	–	60	–	ns	12
Address setup to write end	t_{AW}	40	–	60	–	ns	
Address setup time	t_{AS}	0	–	0	–	ns	12
Write pulse width	t_{WP}	35	–	55	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	ns	
Data valid to write end	t_{DW}	25	–	30	–	ns	
Data hold time	t_{DH}	0	–	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	0	20	0	20	ns	4, 5
Output active from write end	t_{OW}	5	–	5	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ low to end of write	t_{BW}	35	–	55	–	ns	

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



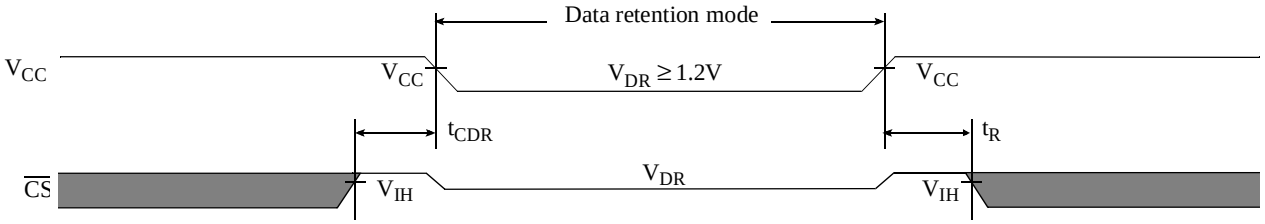
Write waveform 2 ($\overline{CS}$ controlled)[10,11]



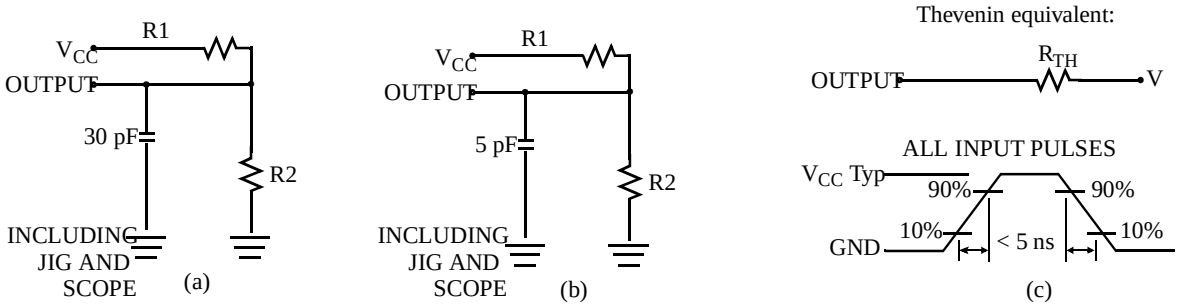
Data retention characteristics (over the operating range)[13,5]

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 1.2V $\overline{CS} \geq V_{CC} - 0.1V$ or $\overline{UB} = \overline{LB} = \geq V_{CC} - 0.1V$ $V_{IN} \geq V_{CC} - 0.1V$ *or* $V_{IN} \leq 0.1V$	1.2V	3.6	V
Data retention current	I_{CCDR}		–	4	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns

Data retention waveform



AC test loads and waveforms



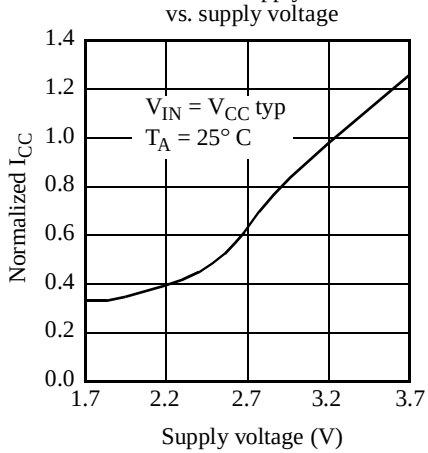
Parameters	V_{CC} = 3.0V	V_{CC} = 2.5V	V_{CC} = 2.0V	Unit
R1	1105	16670	15294	Ohms
R2	1550	15380	11300	Ohms
R_{TH}	645	8000	6500	Ohms
V_{TH}	1.75V	1.2V	0.85V	Volts

Notes

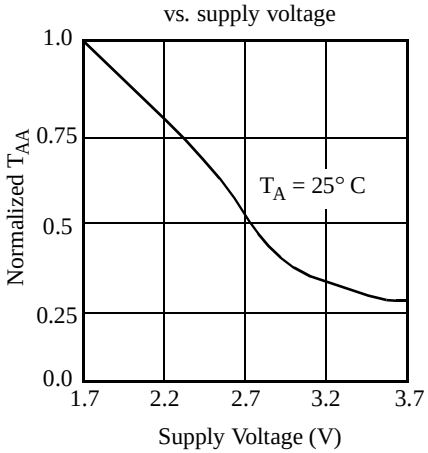
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CS}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ±500 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CS}$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CS}$ or $\overline{WE}$ must be HIGH during address transitions. Either $\overline{CS}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A.
13 1.2V data retention applies to commercial and industrial temperature range operations.
14 C = 30pF, except at high Z and low Z parameters, where C = 5pF.

Typical DC and AC characteristics

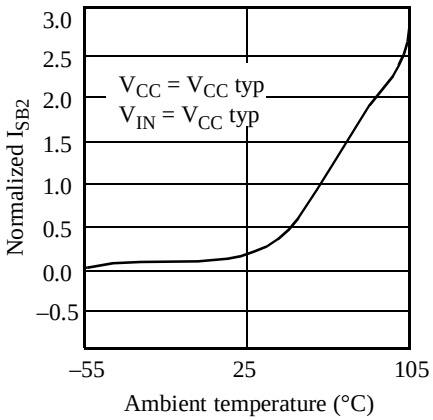
Normalized supply current vs. supply voltage



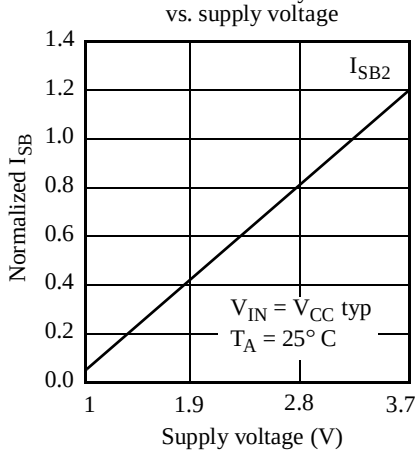
Normalized access time vs. supply voltage



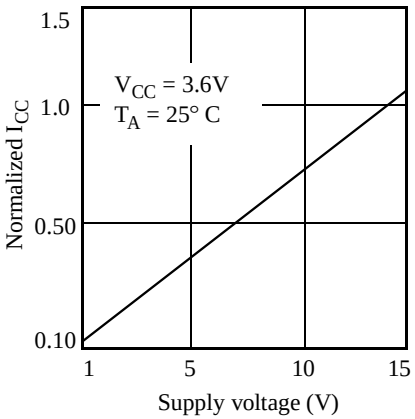
Normalized standby current vs. ambient temperature



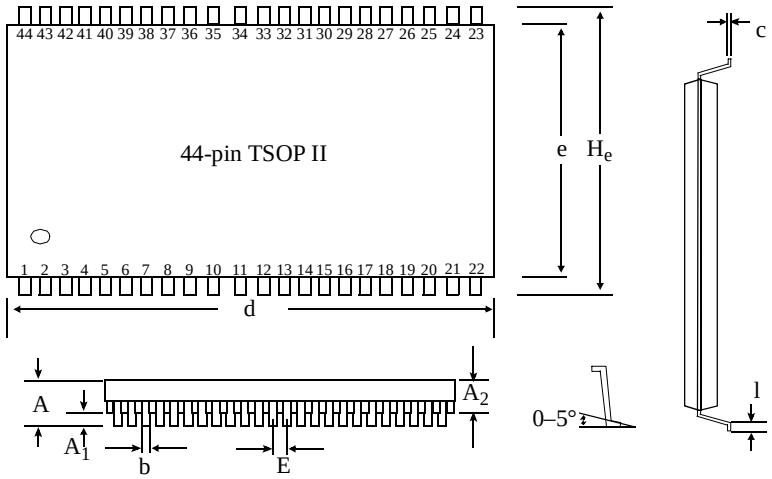
Normalized standby current vs. supply voltage



Normalized I_{CC} vs. Cycle Time

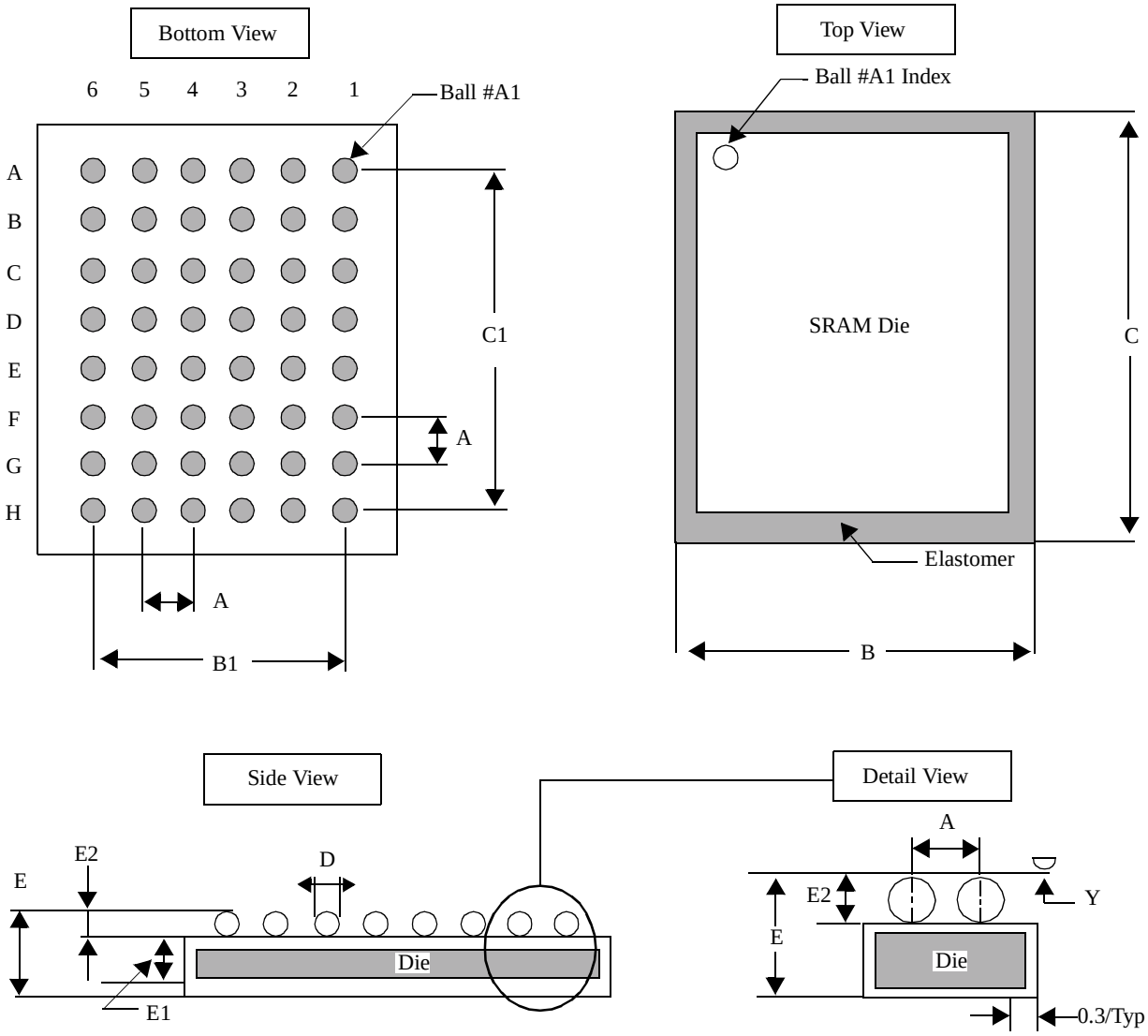


Package diagrams and dimensions



	44-pin TSOP II	
	Min (mm)	Max (mm)
A		1.2
A_1	0.05	
A_2	0.95	1.05
b	0.25	0.45
c	0.15 (typical)	
d	20.85	21.05
e	10.06	10.26
H_e	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60

48-ball FBGA



	Minimum	Typical	Maximum
A	–	0.75	–
B	6.90	7.00	7.10
B1	–	3.75	–
C	10.90	11.00	11.10
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	–	1.20
E1	–	0.68	–
E2	0.22	0.25	0.27
Y	–	–	0.08

Notes

1. Bump counts: 48 (8 row × 6 column).
2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).
3. Units: millimeters.
4. All tolerance are ±0.050 unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.08 (max).

Ordering codes

Speed (ns)	Ordering Code	Package Type	Operating Range
55/70	AS6UA25616-TC	44-pin TSOP II	Commercial
	AS6UA25616-BC	48-ball fine pitch BGA	
55/70	AS6UA25616-TI	44-pin TSOP II	Industrial
	AS6UA25616-BI	48-ball fine pitch BGA	

Part numbering system

AS6UA	25616	T, B	C, I
SRAM Intelliwatt™ prefix	Device number	Package: T: TSOP II B: CSP BGA	Temperature range: C: Commercial: 0° C to 70° C IL Industrial: –40° C to 85° C