iT3012E

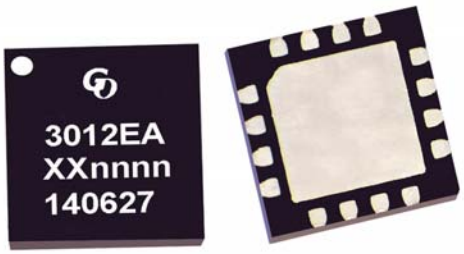
8 GHz Differential-to-Single-Ended Amplifier

Description

The iT3012E is a RoHS-6-compliant packaged differential-to-single-ended amplifier designed for use as an optical modulator predriver with limiting functionality in 10.7 Gb/s and 12.5 Gb/s (OC-192) optical transmitters and receivers. It allows single-ended input signals of 350 mVpp to 900 mVpp or differential signals of 250 mVpp to 1800 mVpp to be limited at a constant single-ended output voltage of 1.9 Vpp. It provides output voltage control and allows external offset correction. iT3012E also provides excellent linear performance when operating at lower output voltages. Both AC and DC input coupling are allowed. DC-coupled SCFL differential input (input "high" voltage = 0 V, input "low" voltage = -900 mV) is allowed.

Features

- Limiting function with 1.9 Vpp single-ended output
- 3 dB bandwidth: 8 GHz
- Single-ended Gain: 17.5 dB
- Standard bias supply levels: -5 V or -5.2 V, +5 V
- Power consumption: 665 mW
- Low group delay and jitter
- Output voltage control
- AC and DC input coupling (SCFL compatible)
- AC and DC output coupling
- RoHS-6-compliant 4x4 mm QFN (MO-220) pac



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
Vee	Power supply voltage	-8	0	V
Vcc	Power supply voltage	0	8	V
Vd	Applied voltage at data input (differential)		3	V
Vm	Applied voltage at data input (single ended)		1.5	V
I_{DCin} (+),(-)	Offset control current		5	mA
Tch	Maximum channel temperature		150	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tc	Operating temperature range (Tcase)	0		85	°C
Vee	Negative power supply voltage	-5.45	-5	-4.75	V
Vcc	Positive power supply voltage	4.75	5	5.25	V
Vcb2	First internal bias control voltage		0		V
Iee	Negative supply current	86	101	116	mA
Icc	Positive supply current	30	35	40	mA
V_{DCin}	Offset control voltage	-5		5	V
Vctrl	Voltage control pin	-2.7		0	V
Vm	Applied peak-peak voltage at data input (single ended)	350		900	mV
Vd	Applied peak-peak voltage at data input (differential)	250		1800	mV
Vindc	DC input voltage (with DC-coupled input)	-0.5		0	V
R	Data bit rate			12.5	Gb/s

iT3012E

8 GHz Differential-to-Single-Ended Amplifier

Electrical Characteristics

At ambient temperature

Vee =- 5 V
Vcc = +5 V

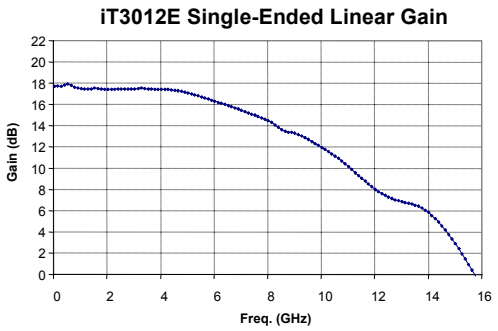
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
P	Pow er consumption	565	665	765	mW
Z DCin	Input impedance at DCin, /DCin	900	1000	1100	Ohm
G	Single-ended small signal gain	16.5	17.5		dB
B3dB	3 dB bandw idth	7	8		GHz
RLin	Input return loss (up to10 GHz)	15	20		dB
RLout	Output return loss (up to 10 GHz)	8	10		dB
Vout	Output peak-peak voltage (single ended) (Vctrl =-2.7V for max. output voltage)	1.75	1.9		V
ΔVout	Vout sensitiviy vs bias (Vee=-5 V +/-5%, Vcc=5 V +/-5%)			+/-11	%
Voutdc	DC output voltage (DC coupled to 50 ohm load)	200	300	400	mV
Trse	Output rise time (single ended at maximum output voltage)		28	35	psec
Tfse	Output fall time (single ended at maximum output voltage)		22	28	psec
JRMS	RMS jitter degradation (*)		1	1.7	psec

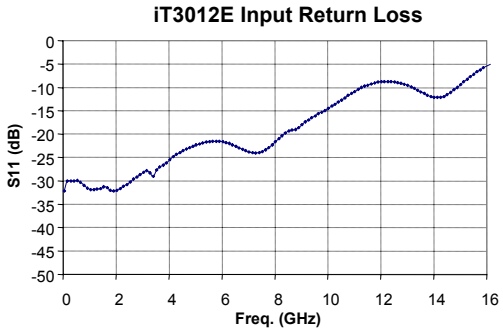
(*) JRMS=sqrt($(J_{RMS\_dut})^2$-$(J_{MRS\_thru})^2$)

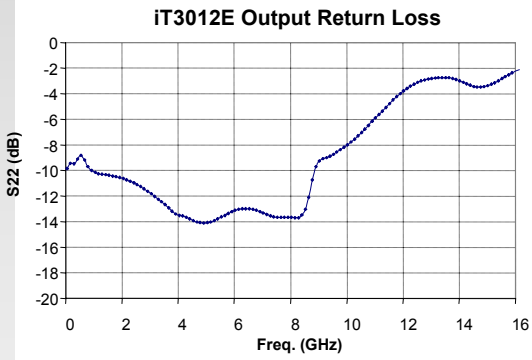
S-Parameter Data

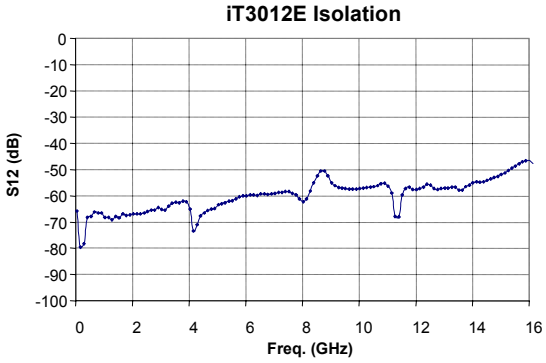
Measured on connectorized evaluation board

Vee = -5 V, Vcc = +5 V



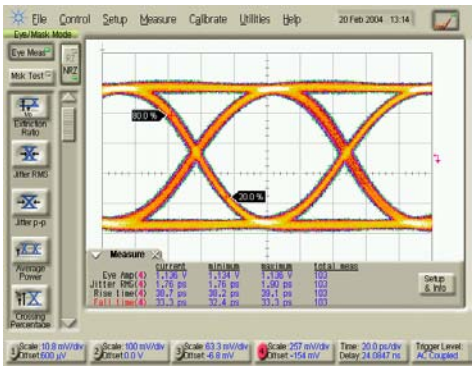




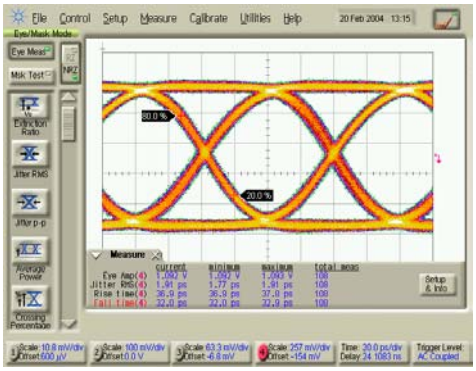


Eye Diagram Performance

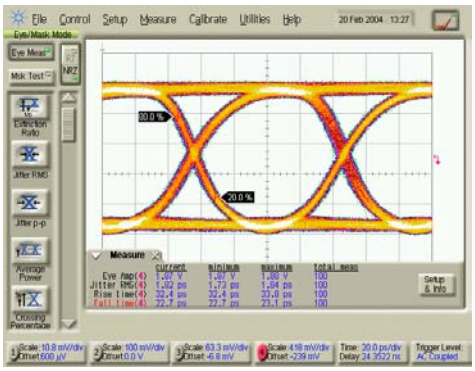
Vee = -5 V
Vcc = +5 V



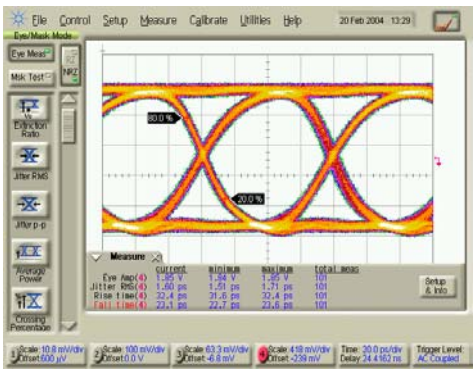
Linear performance
Bit rate: 10.7 Gb/s
Vin = +/-75 mVpp, Vout = +/-1.1 Vpp



Linear performance
Bit Rate: 12.5 Gb/s
Vin = +/-75 mVpp, Vout = +/-1.1 Vpp

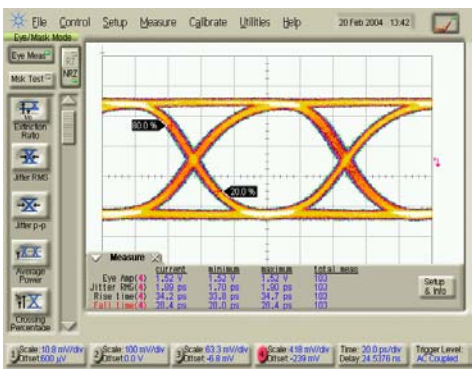


. Saturated performance
Bit rate: 10.7 Gb/s
Vin = +/-400 mVpp, Vout = +/-1.9 Vpp

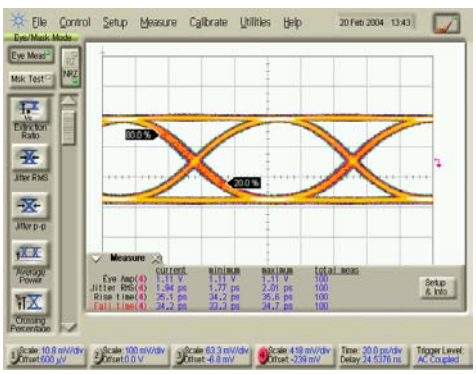


Saturated performance
Bit rate: 12.5 Gb/s
Vin = +/-400 mVpp, Vout = +/-1.9 Vpp

Voltage Control

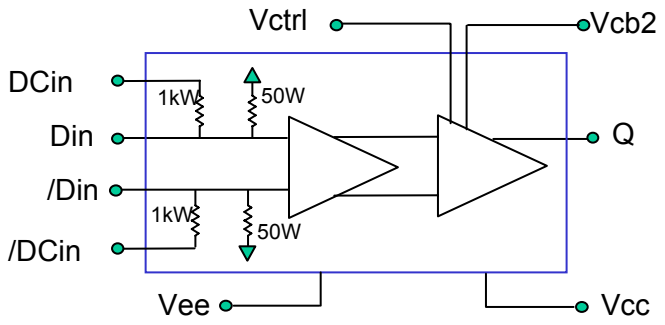


Bit rate: 10.7 Gb/s
Vctrl =-1.5 V, Vout =1.7 Vpp



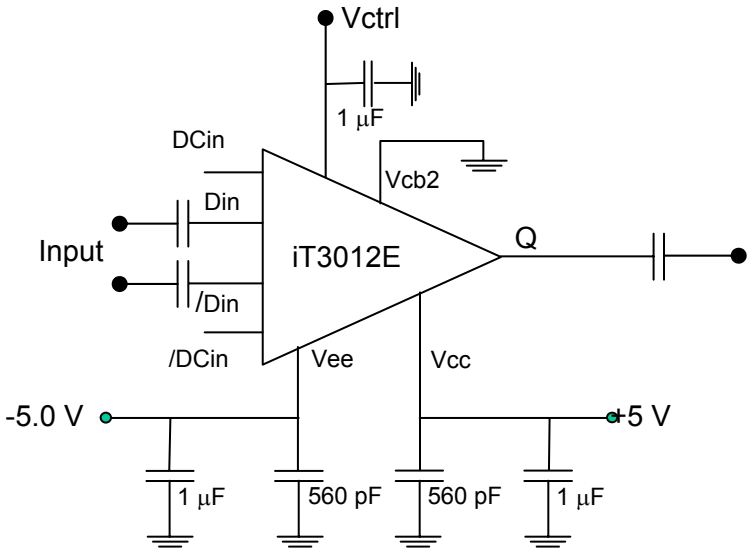
Bit rate: 10.7 Gb/s
Vctrl =-1.1 V, Vout =1.0 Vpp

Device Diagram



Recommended Operational Setup

DC blocking capacitors optional



Bias Conditions

For Vee = -5 V Bias Condition
- Apply +5.0 V at Vcc
- Apply -5 V at Vee
- Vcb2 = 0 V
- Vctrl=-2.7 V or open for maximum output voltage
- Vctrl from –2.7 V to –1 V for output voltage control

For Vee = -5.2 V Bias Conditions
- Apply +5 V at Vcc
- Apply -5.2 V at Vee
- Vcb2 = 0V
- Vctrl = -1.8V for maximum output voltage
- Vctrl from –1.8 V to –1 V for output voltage control

"E" Package Drawings, Pinouts, Marking

Notes:
Dimensions in inches (mm)

Tolerances are ±0.0039 in. (0.100 mm)

Package drawing encompasses JEDEC MO-220 Version VGGC-2.

See iTerra Application Note 10 for recommended pad Layout. RoHS parts are backward compatible if application note pad layout is followed.

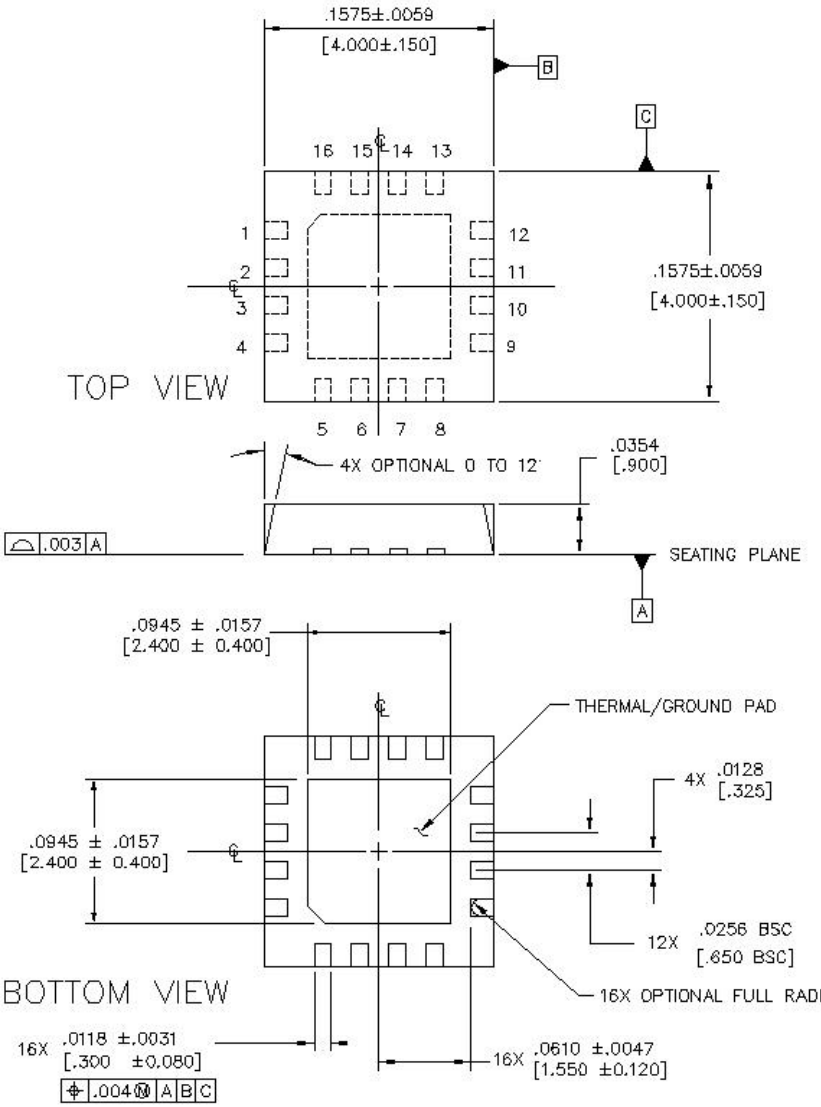
Lead frame material is copper alloy.

Mold compound is UL94V0 compliant.

Lead finish is NiPdAu.

Marking Information
iTerra
MMMMEA
XXNNNN
LLYYWW

Where,
MMMM = part no.
E = Package Type
A =Temp. Range
XX = Wafer Lot
NNNN = Ser. No.
LLYYWW =MFG D/C



Pinouts

P1: GND	P9: GND
P2: Din (RF input)	P10: N/C
P3: /Din (/RF input)	P11: Q (RF Out)
P4: GND	P12: GND
P5: /DCin	P13: Vcb2
P6: Vee	P14: Vctrl (voltage control)
P7: N/C	P15: Vcc
P8: N/C	P16: DCin