

## Section 20 Electrical Characteristics

### 20.1 Absolute Maximum Ratings

Table 20-1 lists the absolute maximum ratings.

**Table 20-1 Absolute Maximum Ratings**

—Preliminary—

Item	Symbol	Value	Unit
Power supply voltage	$V_{CC}$	-0.3 to +7.0	V
Programming voltage	$V_{PP}$	-0.3 to +13.5	V
Input voltage (except port 7)	$V_{IN}$	-0.3 to $V_{CC} + 0.3$	V
Input voltage (port 7)	$V_{IN}$	-0.3 to $AV_{CC} + 0.3$	V
Reference voltage	$V_{REF}$	-0.3 to $AV_{CC} + 0.3$	V
Analog power supply voltage	$AV_{CC}$	-0.3 to +7.0	V
Analog input voltage	$V_{AN}$	-0.3 to $AV_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	Regular specifications: -20 to +75	°C
		Wide-range specifications: -40 to +85	°C
Storage temperature	$T_{stg}$	-55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

## 20.2 Electrical Characteristics

### 20.2.1 DC Characteristics

Table 20-2 lists the DC characteristics. Table 20-3 lists the permissible output currents.

**Table 20-2 DC Characteristics**

Conditions:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}^*$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Schmitt trigger input voltages	Port A,	$V_T^-$	1.0	—	—	V	
	PB <sub>0</sub> to PB <sub>2</sub> ,	$V_T^+$	—	—	$V_{CC} \times 0.7$	V	
	PB <sub>0</sub> to PB <sub>3</sub>	$V_T^+ - V_T^-$	0.4	—	—	V	
Input high voltage	RES, STBY, NMI, MD <sub>2</sub> to MD <sub>0</sub>	$V_{IH}$	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		2.0	—	$AV_{CC} + 0.3\text{ V}$		
	Ports 1, 2, 3, 4, 5, 6, 9, PB <sub>3</sub> , PB <sub>4</sub> , PB <sub>4</sub> to PB <sub>7</sub>		2.0	—	$V_{CC} + 0.3\text{ V}$		
Input low voltage	RES, STBY, MD <sub>2</sub> to MD <sub>0</sub>	$V_{IL}$	-0.3	—	0.5	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, PB <sub>3</sub> , PB <sub>4</sub> , PB <sub>4</sub> to PB <sub>7</sub>		-0.3	—	0.8	V	
Output high voltage	All output pins	$V_{OH}$	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu\text{A}$
			3.5	—	—	V	$I_{OH} = -1\ \text{mA}$

Note: \* If the A/D and D/A converters are not used, do not leave the  $AV_{CC}$ ,  $AV_{SS}$ , and  $V_{REF}$  pins open. Connect  $AV_{CC}$  and  $V_{REF}$  to  $V_{CC}$ , and connect  $AV_{SS}$  to  $V_{SS}$ .

**Table 20-2 DC Characteristics (cont)**

Conditions:  $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $V_{REF} = 4.5 \text{ V to } AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0 \text{ V}^*1$ ,  $T_a = -20^\circ\text{C to } +75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Output low voltage	All output pins (except RESO)	$V_{OL}$	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$	
	Ports 1, 2, 5, and B		—	1.0	V	$I_{OL} = 10 \text{ mA}$	
	RESO		—	0.4	V	$I_{OL} = 2.6 \text{ mA}$	
Input leakage current	STBY, NMI, RES, MD <sub>2</sub> to MD <sub>0</sub>	$ I_{IN} $	—	1.0	$\mu\text{A}$	$V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$	
	Port 7		—	1.0	$\mu\text{A}$	$V_{IN} = 0.5 \text{ to } AV_{CC} - 0.5 \text{ V}$	
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$ I_{TS1} $	—	1.0	$\mu\text{A}$	$V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$	
	RESO		—	10.0	$\mu\text{A}$	$V_{IN} = 0.5 \text{ to } V_{CC} - 0.5 \text{ V}$	
Input pull-up current	Ports 2, 4, and 5	$-I_p$	50	300	$\mu\text{A}$	$V_{IN} = 0 \text{ V}$	
Input capacitance	NMI	$C_{IN}$	—	50	pF	$V_{IN} = 0 \text{ V}$ $f = 1 \text{ MHz}$ $T_a = 25^\circ\text{C}$	
	All input pins except NMI		—	15			
Current dissipation*2	Normal operation	$I_{CC}$	—	35	55	mA	$f = 10 \text{ MHz}$
			—	40	65	mA	$f = 12 \text{ MHz}$
			—	50	80	mA	$f = 16 \text{ MHz}$
	Sleep mode		—	25	40	mA	$f = 10 \text{ MHz}$
			—	30	45	mA	$f = 12 \text{ MHz}$
			—	35	60	mA	$f = 16 \text{ MHz}$
	Standby mode*3		—	0.01	5.0	$\mu\text{A}$	$T_a \leq 50^\circ\text{C}$
			—	—	20.0	$\mu\text{A}$	$50^\circ\text{C} < T_a$

- Notes: 1. If the A/D and D/A converters are not used, do not leave the  $AV_{CC}$ ,  $AV_{SS}$ , and  $V_{REF}$  pins open. Connect  $AV_{CC}$  and  $V_{REF}$  to  $V_{CC}$ , and connect  $AV_{SS}$  to  $V_{SS}$ .  
 2. Current dissipation values are for  $V_{IHmin} = V_{CC} - 0.5 \text{ V}$  and  $V_{ILmax} = 0.5 \text{ V}$  with all output pins unloaded and the on-chip pull-up transistors in the off state.  
 3. The values are for  $V_{RAM} \leq V_{CC} < 4.5 \text{ V}$ ,  $V_{IHmin} = V_{CC} \times 0.9$ , and  $V_{ILmax} = 0.3 \text{ V}$ .

**Table 20-2 DC Characteristics (cont)**

Conditions:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}^*1$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Analog power supply current	During A/D conversion	$AI_{CC}$	—	1.2	2.0	mA	
	During A/D and D/A conversion		—	2.0	5.0	mA	
	Idle		—	0.01	5.0	$\mu\text{A}$	
Reference current	During A/D conversion	$AI_{CC}$	—	0.2	0.5	mA	$V_{REF} = 5.0\text{ V}$
	During A/D and D/A conversion		—	0.5	1.0	mA	
	Idle		—	0.01	5.0	$\mu\text{A}$	
RAM standby voltage		$V_{RAM}$	2.0	—	—	V	

- Notes: 1. If the A/D and D/A converters are not used, do not leave the  $AV_{CC}$ ,  $AV_{SS}$ , and  $V_{REF}$  pins open. Connect  $AV_{CC}$  and  $V_{REF}$  to  $V_{CC}$ , and connect  $AV_{SS}$  to  $V_{SS}$ .
2. Current dissipation values are for  $V_{IHmin} = V_{CC} - 0.5\text{ V}$  and  $V_{ILmax} = 0.5\text{ V}$  with all output pins unloaded and the on-chip pull-up transistors in the off state.
3. The values are for  $V_{RAM} < V_{CC} < 4.5\text{ V}$ ,  $V_{IHmin} = V_{CC} \times 0.9$ , and  $V_{ILmax} = 0.3\text{ V}$ .

**Table 20-2 DC Characteristics (cont)**

Conditions:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}^*$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Schmitt trigger input voltages	Port A,	$V_T^-$	$V_{CC} \times 0.2$	—	—	V	
	PB <sub>0</sub> to PB <sub>2</sub> ,	$V_T^+$	—	—	$V_{CC} \times 0.7$	V	
	PB <sub>0</sub> to PB <sub>3</sub>	$V_T^+ - V_T^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	RES, STBY, NMI, MD <sub>2</sub> to MD <sub>0</sub>	$V_{IH}$	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port 7		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Ports 1, 2, 3, 4, 5, 6, 9, P8 <sub>3</sub> , P8 <sub>4</sub> , PB <sub>4</sub> to PB <sub>7</sub>		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low voltage	RES, STBY, MD <sub>2</sub> to MD <sub>0</sub>	$V_{IL}$	-0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL, ports 1, 2, 3, 4, 5, 6, 7, 9, P8 <sub>3</sub> , P8 <sub>4</sub> , PB <sub>4</sub> to PB <sub>7</sub>		-0.3	—	$V_{CC} \times 0.2$	V	$V_{CC} < 4.0\text{ V}$
					0.8	V	$V_{CC} = 4.0\text{ V to }5.5\text{ V}$
Output high voltage	All output pins	$V_{OH}$	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu\text{A}$
			$V_{CC} - 1.0$	—	—	V	$I_{OH} = -1\ \text{mA}$
Output low voltage	All output pins (except RES <sub>0</sub> )	$V_{OL}$	—	—	0.4	V	$I_{OL} = 1.6\ \text{mA}$
			Ports 1, 2, 5, and B	—	—	1.0	V
	RES <sub>0</sub>	—	—	0.4	V	$I_{OL} = 2.6\ \text{mA}$	
Input leakage current	STBY, NMI, RES, MD <sub>2</sub> to MD <sub>0</sub>	$I_{IN}$	—	—	1.0	$\mu\text{A}$	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\ \text{V}$
	Port 7		—	—	1.0	$\mu\text{A}$	$V_{IN} = 0.5\text{ to }AV_{CC} - 0.5\ \text{V}$

Note: \* If the A/D and D/A converters are not used, do not leave the  $AV_{CC}$ ,  $AV_{SS}$ , and  $V_{REF}$  pins open. Connect  $AV_{CC}$  and  $V_{REF}$  to  $V_{CC}$ , and connect  $AV_{SS}$  to  $V_{SS}$ .

**Table 20-2 DC Characteristics (cont)**

Conditions:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}^1$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Three-state leakage current (off state)	Ports 1, 2, 3, 4, 5, 6, 8 to B	$ I_{TS1} $	—	—	1.0	$\mu\text{A}$ $V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$	
	$\overline{RES0}$	—	—	10.0	$\mu\text{A}$	$V_{IN} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$	
Input pull-up current	Ports 2, 4, and 5	$-I_p$	10	—	300	$\mu\text{A}$ $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ , $V_{IN} = 0\text{ V}$	
Input capacitance	NMI	$C_{IN}$	—	—	50	$\text{pF}$ $V_{IN} = 0\text{ V}$	
	All input pins except NMI	—	—	—	15	$f = 1\text{ MHz}$ $T_a = 25^\circ\text{C}$	
Current dissipation*2	Normal operation	$I_{CC}^{*4}$	—	30 (5.0 V)	36.2 (5.5 V)	$\text{mA}$ $f = 8\text{ MHz}$	
	Sleep mode	—	—	20 (5.0 V)	27.4 (5.5 V)	$\text{mA}$ $f = 8\text{ MHz}$	
	Standby mode*3	—	—	0.01	5.0	$\mu\text{A}$	$T_a \leq 50^\circ\text{C}$
		—	—	—	20.0	$\mu\text{A}$	$50^\circ\text{C} < T_a$
Analog power supply current	During A/D conversion	$AI_{CC}$	—	1.0	2.0	$\text{mA}$	$AV_{CC} = 3.0\text{ V}$
			—	1.2	—	$\text{mA}$	$AV_{CC} = 5.0\text{ V}$
	During A/D and D/A conversion	—	—	1.8	4.0	$\text{mA}$	$AV_{CC} = 3.0\text{ V}$
			—	2.0	—	$\text{mA}$	$AV_{CC} = 5.0\text{ V}$
	Idle	—	—	0.01	5.0	$\mu\text{A}$	

- Notes: 1. If the A/D and D/A converters are not used, do not leave the  $AV_{CC}$ ,  $AV_{SS}$ , and  $V_{REF}$  pins open. Connect  $AV_{CC}$  and  $V_{REF}$  to  $V_{CC}$ , and connect  $AV_{SS}$  to  $V_{SS}$ .  
2. Current dissipation values are for  $V_{IHmin} = V_{CC} - 0.5\text{ V}$  and  $V_{ILmax} = 0.5\text{ V}$  with all output pins unloaded and the on-chip pull-up transistors in the off state.  
3. The values are for  $V_{RAM} \leq V_{CC} < 2.7\text{ V}$ ,  $V_{IHmin} = V_{CC} \times 0.9$ , and  $V_{ILmax} = 0.3\text{ V}$ .  
4.  $I_{CC}$  depends on  $V_{CC}$  and  $f$  as follows:  
 $I_{CCmax} = 1.0\text{ (mA)} + 0.8\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$  [normal mode]  
 $I_{CCmax} = 1.0\text{ (mA)} + 0.6\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$  [sleep mode]

**Table 20-2 DC Characteristics (cont)**

Conditions:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}^*$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Reference current	During A/D conversion	$AI_{CC}$	—	0.1	0.2	mA	$V_{REF} = 3.0\text{ V}$
		—	0.2	—	—	mA	$V_{REF} = 5.0\text{ V}$
	During A/D and D/A conversion	—	0.2	0.4	—	mA	$V_{REF} = 3.0\text{ V}$
		—	0.5	—	—	mA	$V_{REF} = 5.0\text{ V}$
Idle	—	—	0.01	5.0	$\mu\text{A}$		
RAM standby voltage	$V_{RAM}$	2.0	—	—	V		

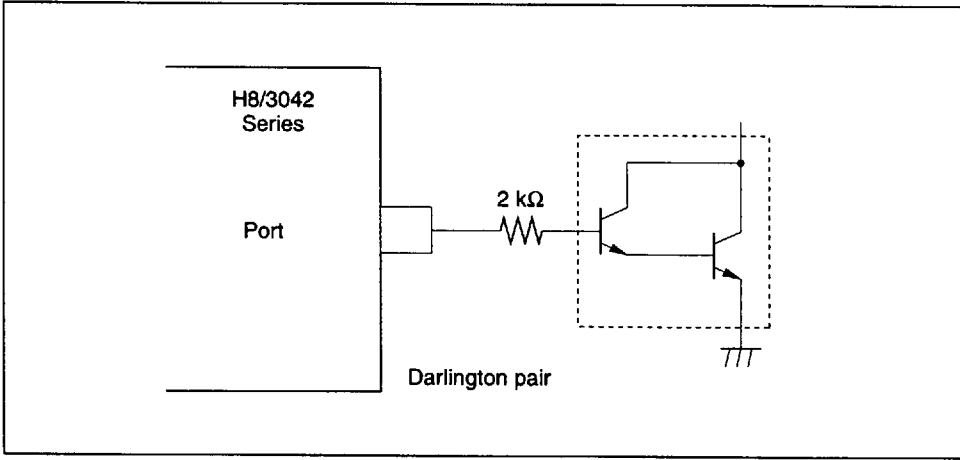
Note: \* If the A/D and D/A converters are not used, do not leave the  $AV_{CC}$ ,  $AV_{SS}$ , and  $V_{REF}$  pins open. Connect  $AV_{CC}$  and  $V_{REF}$  to  $V_{CC}$ , and connect  $AV_{SS}$  to  $V_{SS}$ .

**Table 20-3 Permissible Output Currents**

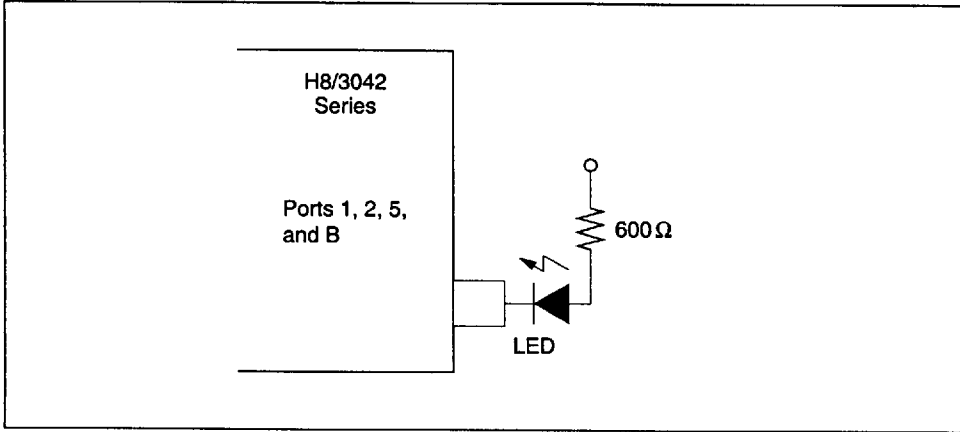
Conditions:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  
 $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	
Permissible output low current (per pin)	Ports 1, 2, 5, and B	$I_{OL}$	—	—	10	mA
	Other output pins	—	—	—	2.0	mA
Permissible output low current (total)	Total of 28 pins in ports 1, 2, 5, and B	$\Sigma I_{OL}$	—	—	80	mA
	Total of all output pins, including the above	—	—	—	120	mA
Permissible output high current (per pin)	All output pins	$I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma I_{OH}$	—	—	40	mA

Notes: 1. To protect chip reliability, do not exceed the output current values in table 20-3.  
2. When driving a darlington pair or LED, always insert a current-limiting resistor in the output line, as shown in figures 20-1 and 20-2.



**Figure 20-1 Darlington Pair Drive Circuit (Example)**



**Figure 20-2 LED Drive Circuit (Example)**



## 20.2.2 AC Characteristics

Bus timing parameters are listed in table 20-4. Refresh controller bus timing parameters are listed in table 20-5. Control signal timing parameters are listed in table 20-6. Timing parameters of the on-chip supporting modules are listed in table 20-7.

**Table 20-4 Bus Timing (1)**

- Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)
- Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Condition A		Condition B				Unit	Test Conditions		
		8 MHz		10 MHz		12 MHz				16 MHz	
		Min	Max	Min	Max	Min	Max			Min	Max
Clock cycle time	$t_{CYC}$	125	500	100	500	83.3	500	62.5	500	ns	Figure 20-4, Figure 20-5
Clock rise time	$t_{CR}$	—	20	—	10	—	10	—	10		
Clock fall time	$t_{CF}$	—	20	—	10	—	10	—	10		
Address delay time	$t_{AD}$	—	60	—	40	—	35	—	30		
Address hold time	$t_{AH}$	25	—	20	—	15	—	10	—		
Address strobe delay time	$t_{ASD}$	—	60	—	40	—	35	—	30		
Write strobe delay time	$t_{WSD}$	—	60	—	40	—	35	—	30		
Strobe delay time	$t_{SD}$	—	60	—	40	—	35	—	30		
Write data strobe pulse width 1	$t_{WSW1}^*$	85	—	70	—	55	—	35	—		
Write data strobe pulse width 2	$t_{WSW2}^*$	150	—	120	—	95	—	65	—		
Address setup time 1	$t_{AS1}$	20	—	15	—	10	—	10	—		
Address setup time 2	$t_{AS2}$	80	—	65	—	50	—	40	—		
Read data setup time	$t_{RDS}$	50	—	20	—	20	—	20	—		
Read data hold time	$t_{RDH}$	0	—	0	—	0	—	0	—		

**Table 20-4 Bus Timing (cont)**

Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular  
specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular  
specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Condition A		Condition B				Unit	Test Conditions		
		8 MHz	10 MHz	12 MHz	16 MHz	Min	Max				
Write data delay time	$t_{WDD}$	—	75	—	65	—	60	—	60	ns	Figure 20-4, Figure 20-5
Write data setup time 1	$t_{WDS1}$	90	—	75	—	60	—	35	—		
Write data setup time 2	$t_{WDS2}$	15	—	10	—	10	—	5	—		
Write data hold time	$t_{WDH}$	25	—	20	—	20	—	20	—		
Read data access time 1	$t_{ACC1*}$	—	110	—	100	—	80	—	55		
Read data access time 2	$t_{ACC2*}$	—	230	—	200	—	160	—	115		
Read data access time 3	$t_{ACC3*}$	—	55	—	50	—	40	—	25		
Read data access time 4	$t_{ACC4*}$	—	160	—	150	—	120	—	85		
Precharge time	$t_{PCH*}$	85	—	70	—	55	—	40	—		
Wait setup time	$t_{WTS}$	40	—	35	—	25	—	25	—	ns	Figure 20-6
Wait hold time	$t_{WTH}$	10	—	10	—	5	—	5	—		
Bus request setup time	$t_{BRQS}$	40	—	40	—	40	—	40	—	ns	Figure 20-18
Bus acknowledge delay time 1	$t_{BACD1}$	—	60	—	50	—	40	—	30		
Bus acknowledge delay time 2	$t_{BACD2}$	—	60	—	50	—	40	—	30		
Bus-floating time	$t_{BZD}$	—	70	—	60	—	50	—	40		

Note is on next page.

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 78 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 83 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 38 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 70 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 40 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 90 \text{ (ns)}\end{aligned}$$

At 10 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 50 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 30 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 50 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 30 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 50 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 30 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 50 \text{ (ns)}\end{aligned}$$

At 12 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 45 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 28 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 48 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 30 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 43 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 28 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 47 \text{ (ns)}\end{aligned}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$\begin{aligned}t_{ACC1} &= 1.5 \times t_{cyc} - 39 \text{ (ns)} & t_{WSW1} &= 1.0 \times t_{cyc} - 28 \text{ (ns)} \\t_{ACC2} &= 2.5 \times t_{cyc} - 41 \text{ (ns)} & t_{WSW2} &= 1.5 \times t_{cyc} - 28 \text{ (ns)} \\t_{ACC3} &= 1.0 \times t_{cyc} - 38 \text{ (ns)} & t_{PCH} &= 1.0 \times t_{cyc} - 23 \text{ (ns)} \\t_{ACC4} &= 2.0 \times t_{cyc} - 40 \text{ (ns)}\end{aligned}$$

**Table 20-5 Refresh Controller Bus Timing**

Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Condition A		Condition B				Unit	Test Conditions	
		8 MHz	10 MHz	12 MHz	16 MHz	Min	Max			
RAS delay time 1	$t_{RAD1}$	—	60	—	30	—	30	—	30	ns Figure 20-7 to Figure 20-13
RAS delay time 2	$t_{RAD2}$	—	60	—	30	—	30	—	30	
RAS delay time 3	$t_{RAD3}$	—	60	—	30	—	30	—	30	
Row address hold time*	$t_{RAH}$	25	—	20	—	15	—	15	—	
RAS precharge time*	$t_{RP}$	85	—	70	—	55	—	40	—	
CAS to RAS precharge time*	$t_{CRP}$	85	—	70	—	55	—	40	—	
CAS pulse width	$t_{CAS}$	110	—	40	—	40	—	40	—	
RAS access time*	$t_{RAC}$	—	160	—	150	—	120	—	85	
Address access time	$t_{AA}$	—	105	—	55	—	55	—	55	
CAS access time*	$t_{CAC}$	—	50	—	50	—	40	—	25	
Write data setup time 3	$t_{WDS3}$	75	—	40	—	40	—	40	—	
CAS setup time*	$t_{CSR}$	20	—	15	—	15	—	15	—	
Read strobe delay time	$t_{RSD}$	—	60	—	30	—	30	—	30	

Note: At 8 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{cyc} - 38 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{cyc} - 75 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{cyc} - 90 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{cyc} - 43 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 40 \text{ (ns)}$$

At 10 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{cyc} - 30 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{cyc} - 50 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{cyc} - 50 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{cyc} - 35 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 30 \text{ (ns)}$$

At 12 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{cyc} - 27 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{cyc} - 43 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{cyc} - 47 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{cyc} - 27 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 28 \text{ (ns)}$$

At 16 MHz, the times below depend as indicated on the clock cycle time.

$$t_{RAH} = 0.5 \times t_{cyc} - 16 \text{ (ns)} \quad t_{CAC} = 1.0 \times t_{cyc} - 38 \text{ (ns)}$$

$$t_{RAC} = 2.0 \times t_{cyc} - 40 \text{ (ns)} \quad t_{CSR} = 0.5 \times t_{cyc} - 16 \text{ (ns)}$$

$$t_{RP} = t_{CRP} = 1.0 \times t_{cyc} - 23 \text{ (ns)}$$

**Table 20-6 Control Signal Timing**

Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular  
specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular  
specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Condition A		Condition B				Unit	Test Conditions		
		8 MHz	10 MHz	12 MHz	16 MHz	Min	Max				
RES setup time	$t_{RESS}$	200	—	200	—	200	—	200	—	ns	Figure 20-15
RES pulse width	$t_{RESW}$	10	—	10	—	10	—	10	—	$t_{CYC}$	
RESO output delay time	$t_{RESO}$	—	100	—	100	—	100	—	100	ns	Figure 20-16
RESO output pulse width	$t_{RESOW}$	132	—	132	—	132	—	132	—	$t_{CYC}$	
NMI setup time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$ )	$t_{NMIS}$	150	—	150	—	150	—	150	—	ns	Figure 20-17
NMI hold time (NMI, $\overline{IRQ_5}$ to $\overline{IRQ_0}$ )	$t_{NMIH}$	10	—	10	—	10	—	10	—		
Interrupt pulse width (NMI, $\overline{IRQ_2}$ to $\overline{IRQ_0}$ when exiting software standby mode)	$t_{NMIW}$	200	—	200	—	200	—	200	—		
Clock oscillator settling time at reset (crystal)	$t_{OSC1}$	20	—	20	—	20	—	20	—	ms	Figure 20-19
Clock oscillator settling time in software standby (crystal)	$t_{OSC2}$	8	—	8	—	8	—	8	—	ms	Figure 19-1

**Table 20-7 Timing of On-Chip Supporting Modules**

Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

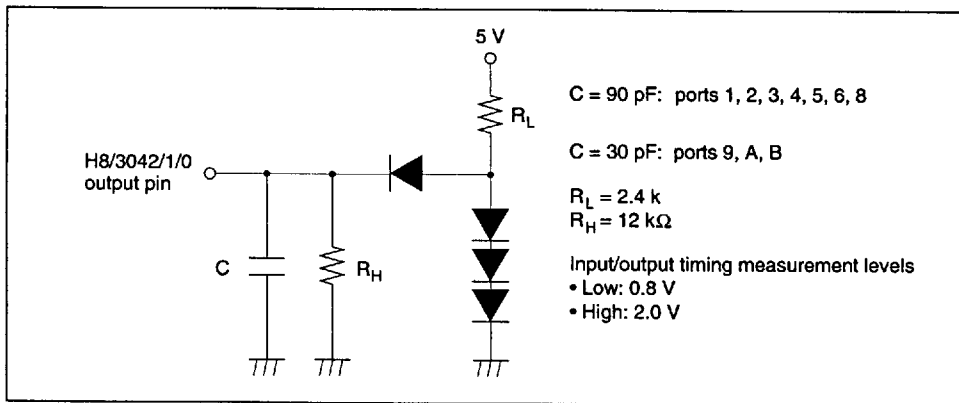
Item	Symbol	Condition A		Condition B				Unit	Test Conditions				
		8 MHz	10 MHz	12 MHz	16 MHz	Min	Max						
DMAC	DREQ setup time	$t_{DRQS}$	40	—	30	—	30	—	30	—	ns	Figure 20-27	
	DREQ hold time	$t_{DRQH}$	10	—	10	—	10	—	10	—			
	TEND delay time 1	$t_{TED1}$	—	100	—	50	—	50	—	50			Figure 20-25, Figure 20-26
	TEND delay time 2	$t_{TED2}$	—	100	—	50	—	50	—	50			
ITU	Timer output delay time	$t_{TOCD}$	—	100	—	100	—	100	—	100	ns	Figure 20-21	
	Timer input setup time	$t_{TICS}$	50	—	50	—	50	—	50	—			
	Timer clock input setup time	$t_{TCKS}$	50	—	50	—	50	—	50	—		Figure 20-22	
	Timer clock pulse width	Single edge	$t_{TCKWH}$	1.5	—	1.5	—	1.5	—	1.5	—		$t_{cyc}$
		Both edges	$t_{TCKWL}$	2.5	—	2.5	—	2.5	—	2.5	—		
SCI	Input clock cycle	Asynchronous	$t_{SCYC}$	4	—	4	—	4	—	4	—	$t_{cyc}$	Figure 20-23
		Synchronous	$t_{SCYC}$	6	—	6	—	6	—	6	—		
	Input clock rise time	$t_{SCKr}$	—	1.5	—	1.5	—	1.5	—	1.5	$t_{scyc}$		
	Input clock fall time	$t_{SCKf}$	—	1.5	—	1.5	—	1.5	—	1.5			
	Input clock pulse width	$t_{SCKw}$	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6			

**Table 20-7 Timing of On-Chip Supporting Modules (cont)**

Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Symbol	Condition A				Condition B				Test Conditions		
		8 MHz		10 MHz		12 MHz		16 MHz				
		Min	Max	Min	Max	Min	Max	Min	Max			
SCI	Transmit data delay time	$t_{TXD}$	—	100	—	100	—	100	—	100	ns	Figure 20-24
	Receive data setup time (synchronous)	$t_{RXS}$	100	—	100	—	100	—	100	—		
	Receive data hold time (synchronous)	$t_{RXH}$	100	—	100	—	100	—	100	—		
Ports and TPC	Output data delay time	$t_{PWD}$	—	100	—	100	—	100	—	100	ns	Figure 20-20
TPC	Input data setup time	$t_{PRS}$	50	—	50	—	50	—	50	—		
	Input data hold time	$t_{PRH}$	50	—	50	—	50	—	50	—		



**Figure 20-3 Output Load Circuit**

### 20.2.3 A/D Conversion Characteristics

Table 20-8 lists the A/D conversion characteristics.

**Table 20-8 A/D Converter Characteristics**

Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular  
specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$  (regular  
specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Condition A			Condition B				Unit					
	8 MHz			10 MHz		12 MHz			16 MHz				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	10	10	10	bits
Conversion time	—	—	16.8	—	—	13.4	—	—	11.2	—	—	8.4	$\mu\text{s}$
Analog input capacitance	—	—	20	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	$10^1$	—	—	10	—	—	10	—	—	$10^3$	k $\Omega$
	—	—	$5^2$	—	—	—	—	—	—	—	—	$5^4$	
Nonlinearity error	—	—	$\pm 6.0$	—	—	$\pm 3.0$	—	—	$\pm 3.0$	—	—	$\pm 3.0$	LSB
Offset error	—	—	$\pm 4.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Full-scale error	—	—	$\pm 4.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	—	—	$\pm 2.0$	LSB
Quantization error	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	—	—	$\pm 0.5$	LSB
Absolute accuracy	—	—	$\pm 8.0$	—	—	$\pm 4.0$	—	—	$\pm 4.0$	—	—	$\pm 4.0$	LSB

- Notes: 1. The value is for  $4.0 \leq AV_{CC} \leq 5.5$ .  
2. The value is for  $2.7 \leq AV_{CC} \leq 4.0$ .  
3. The value is for  $\phi \leq 12\text{ MHz}$ .  
4. The value is for  $\phi > 12\text{ MHz}$ .



### 20.2.4 D/A Conversion Characteristics

Table 20-9 lists the D/A conversion characteristics.

**Table 20-9 D/A Converter Characteristics**

- Condition A:  $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 2.7\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }8\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$   
 (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)
- Condition B:  $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $AV_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{REF} = 4.5\text{ V to }AV_{CC}$ ,  
 $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $\phi = 2\text{ MHz to }16\text{ MHz}$ ,  $T_a = -20^\circ\text{C to }+75^\circ\text{C}$   
 (regular specifications),  $T_a = -40^\circ\text{C to }+85^\circ\text{C}$  (wide-range specifications)

Item	Condition A			Condition B								Unit	Test Conditions	
	8 MHz			10 MHz			12 MHz			16 MHz				
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ			Max
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits	
Conversion time	—	—	10	—	—	10	—	—	10	—	—	10	$\mu\text{S}$	20-pF capacitive load
Absolute accuracy	—	$\pm 2.0$	$\pm 3.0$	—	$\pm 1.0$	$\pm 1.5$	—	$\pm 1.0$	$\pm 1.5$	—	$\pm 1.0$	$\pm 1.5$	LSB	2-M $\Omega$ resistive load
	—	—	$\pm 2.0$	—	—	$\pm 1.0$	—	—	$\pm 1.0$	—	—	$\pm 1.0$	LSB	4-M $\Omega$ resistive load

## 20.3 Operational Timing

This section shows timing diagrams.

### 20.3.1 Bus Timing

Bus timing is shown as follows:

- **Basic bus cycle: two-state access**

Figure 20-4 shows the timing of the external two-state access cycle.

- **Basic bus cycle: three-state access**

Figure 20-5 shows the timing of the external three-state access cycle.

- **Basic bus cycle: three-state access with one wait state**

Figure 20-6 shows the timing of the external three-state access cycle with one wait state inserted.

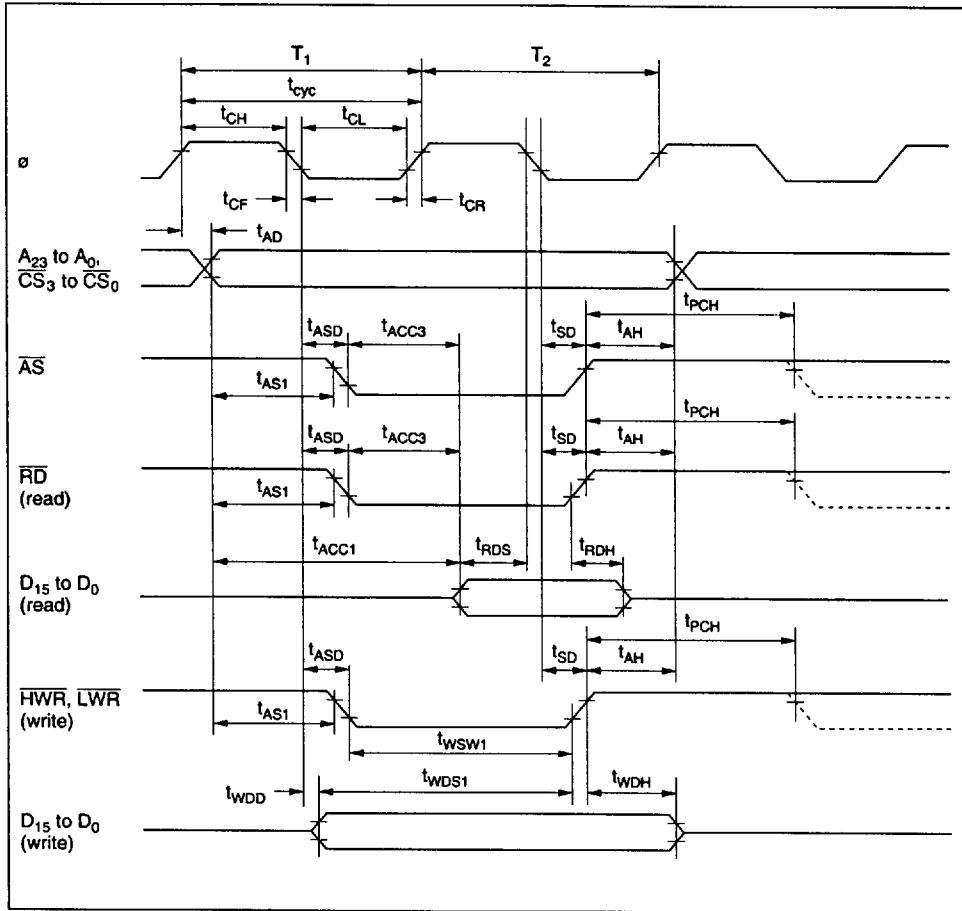


Figure 20-4 Basic Bus Cycle: Two-State Access

to D

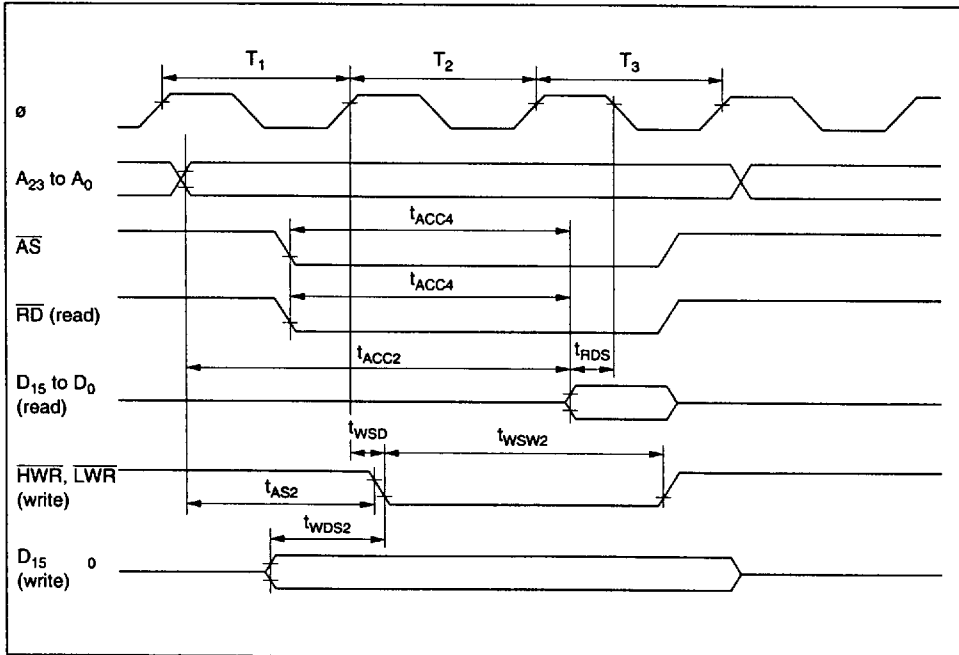


Figure 20-5 Basic Bus Cycle: Three-State Access

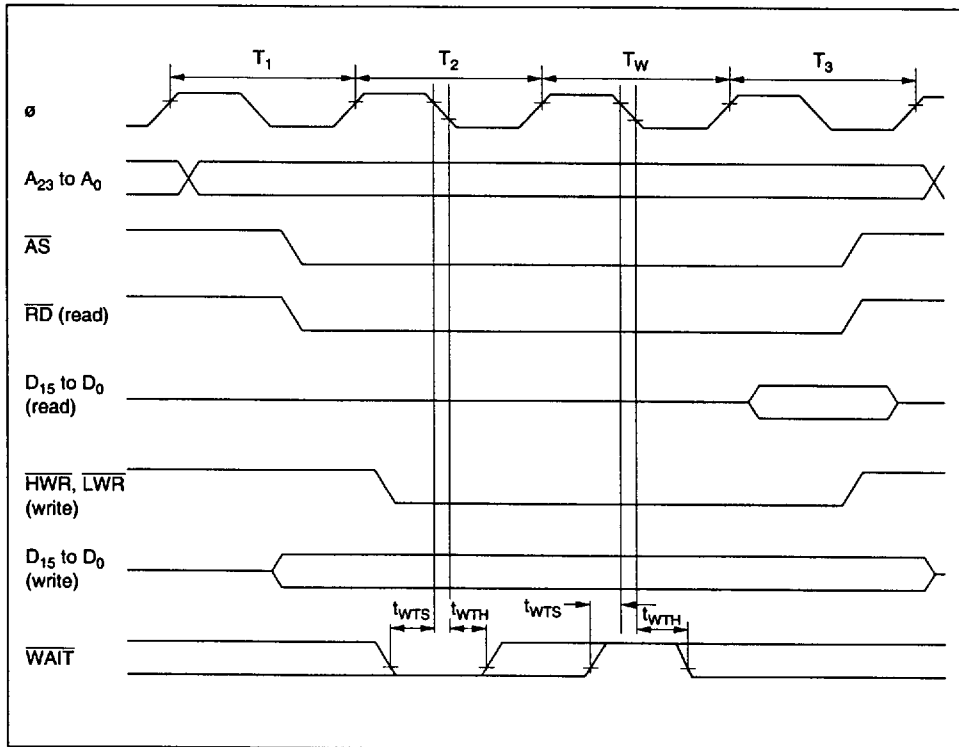


Figure 20-6 Basic Bus Cycle: Three-State Access with One Wait State

### 20.3.2 Refresh Controller Bus Timing

Refresh controller bus timing is shown as follows:

- DRAM bus timing

Figures 20-7 to 20-12 show the DRAM bus timing in each operating mode.

- PSRAM bus timing

Figures 20-13 and 20-14 show the pseudo-static RAM bus timing in each operating mode.

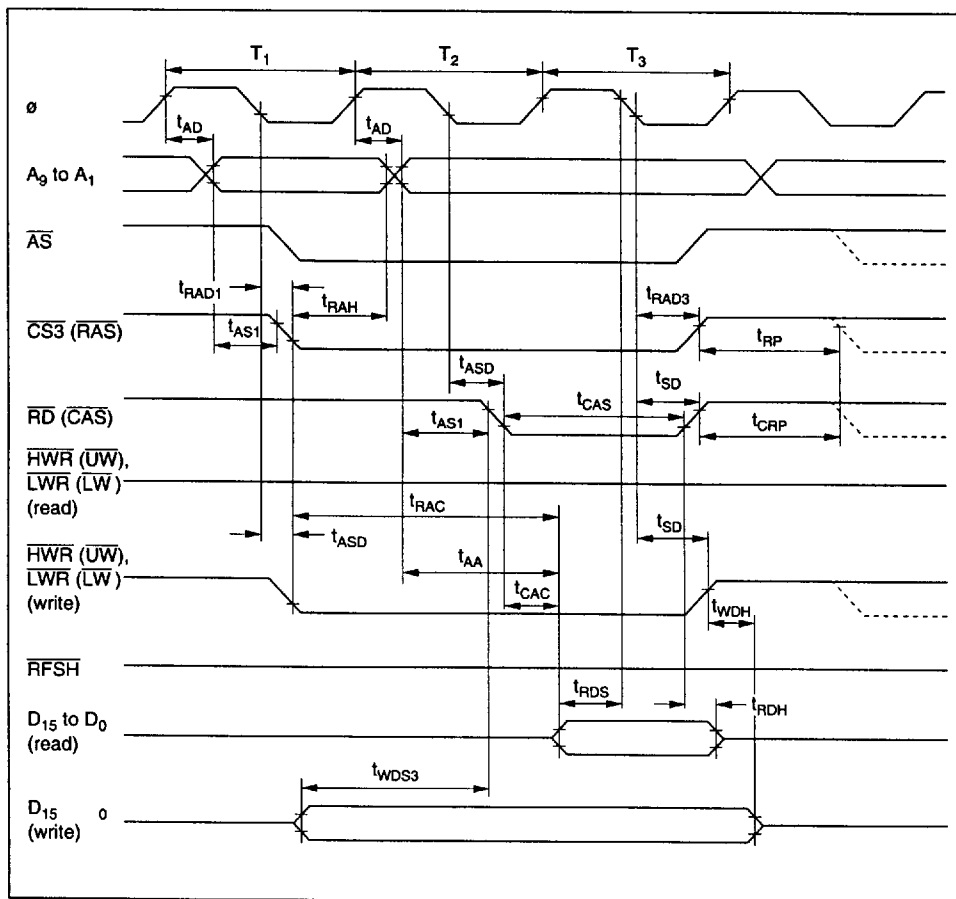


Figure 20-7 DRAM Bus Timing (Read/Write): Three-State Access  
— 2WE Mode —

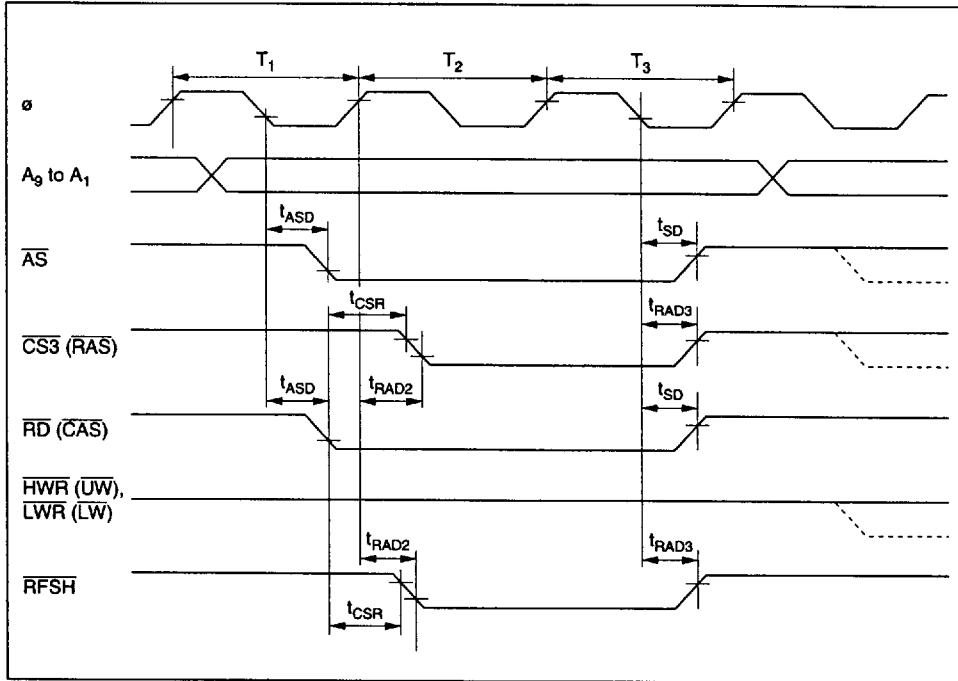


Figure 20-8 DRAM Bus Timing (Refresh Cycle): Three-State Access  
— 2WE Mode —

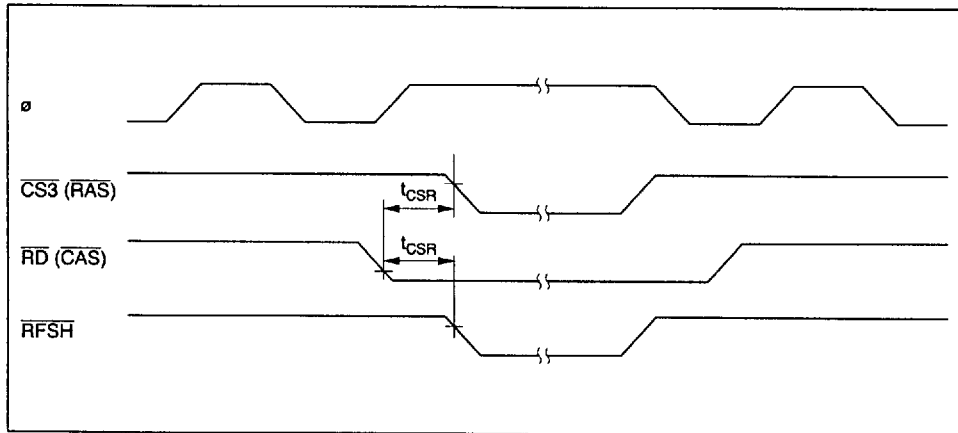


Figure 20-9 DRAM Bus Timing (Self-Refresh Mode)  
— 2WE Mode —

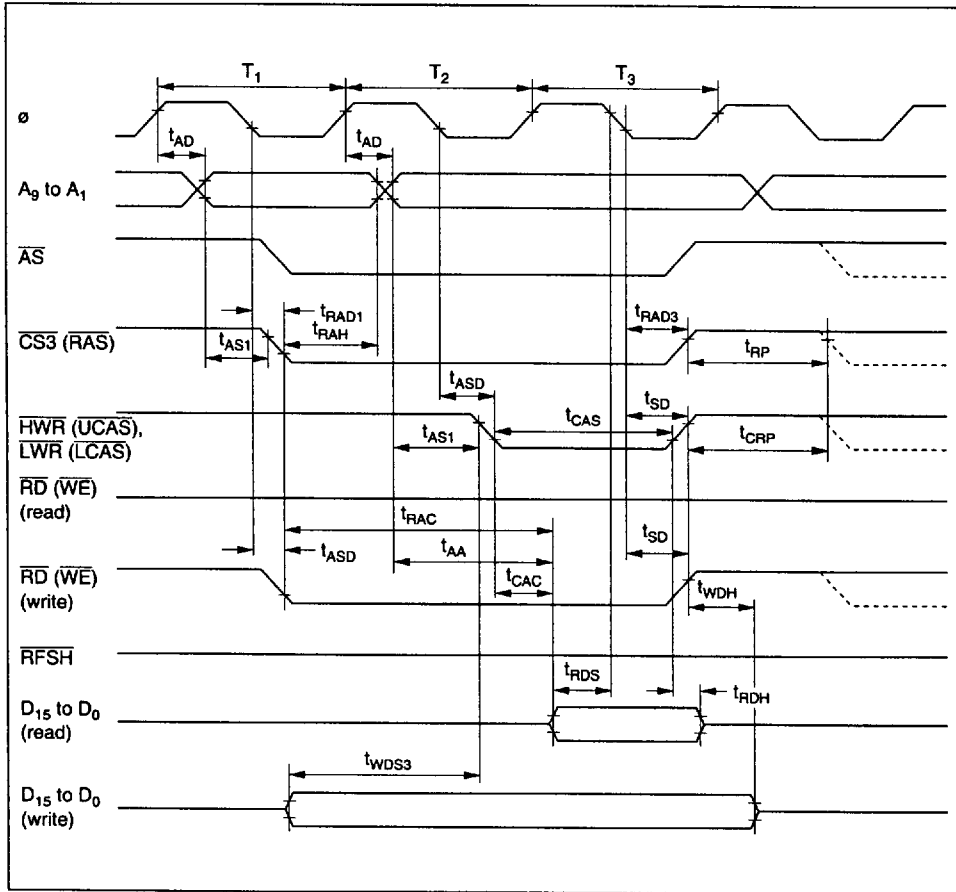


Figure 20-10 DRAM Bus Timing (Read/Write): Three-State Access  
— 2CAS Mode —



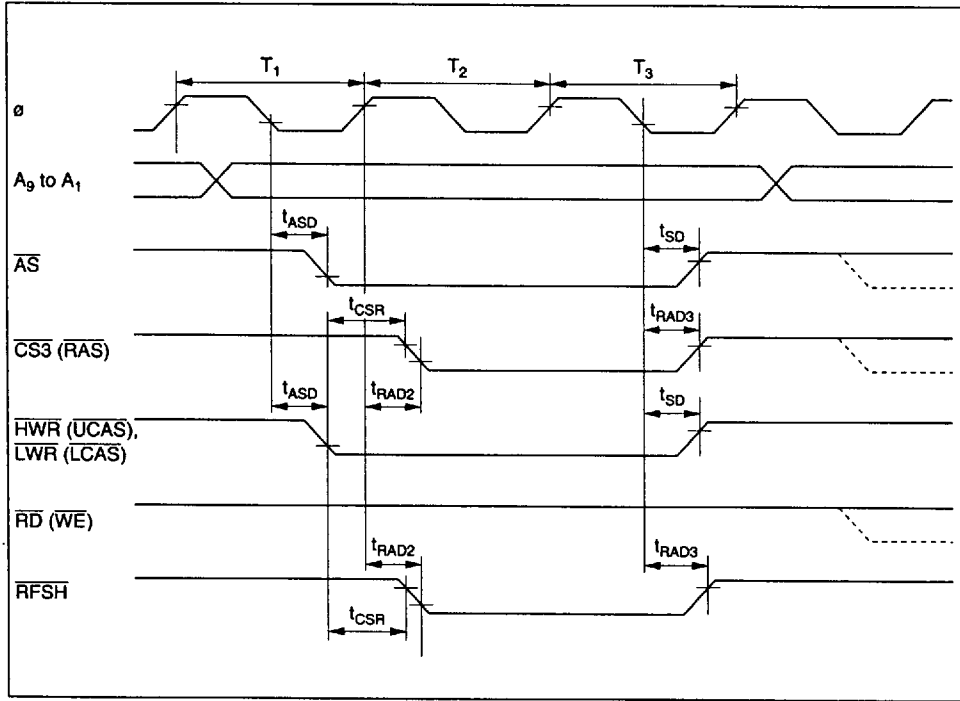


Figure 20-11 DRAM Bus Timing (Refresh Cycle): Three-State Access  
— 2CAS Mode —

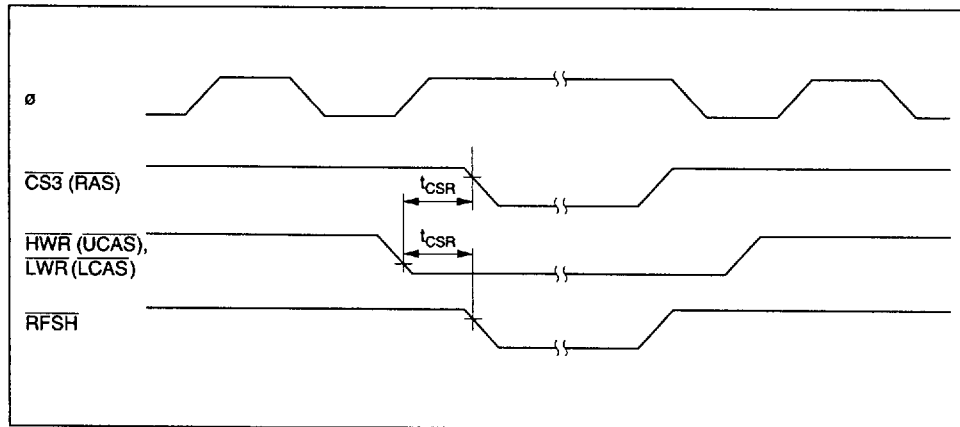


Figure 20-12 DRAM Bus Timing (Self-Refresh Mode)  
— 2CAS Mode —

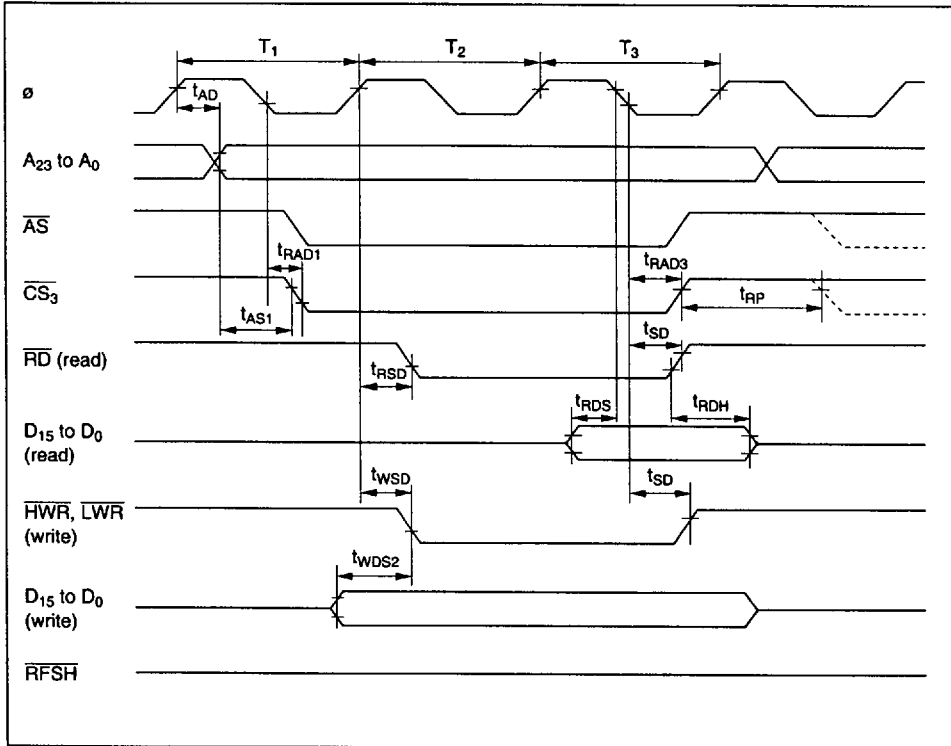


Figure 20-13 PSRAM Bus Timing (Read/Write): Three-State Access

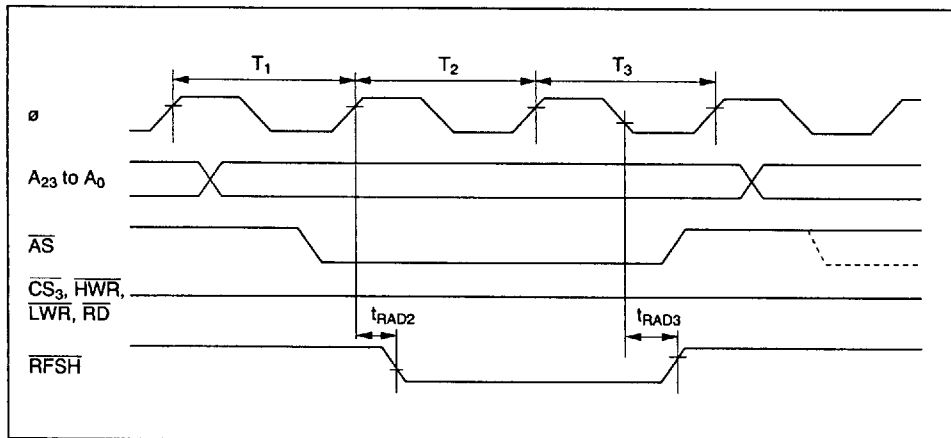


Figure 20-14 PSRAM Bus Timing (Refresh Cycle): Three-State Access

### 20.3.3 Control Signal Timing

Control signal timing is shown as follows:

- Reset input timing

Figure 20-15 shows the reset input timing.

- Reset output timing

Figure 20-16 shows the reset output timing.

- Interrupt input timing

Figure 20-17 shows the input timing for NMI and  $\overline{IRQ}_5$  to  $\overline{IRQ}_0$ .

- Bus-release mode timing

Figure 20-18 shows the bus-release mode timing.

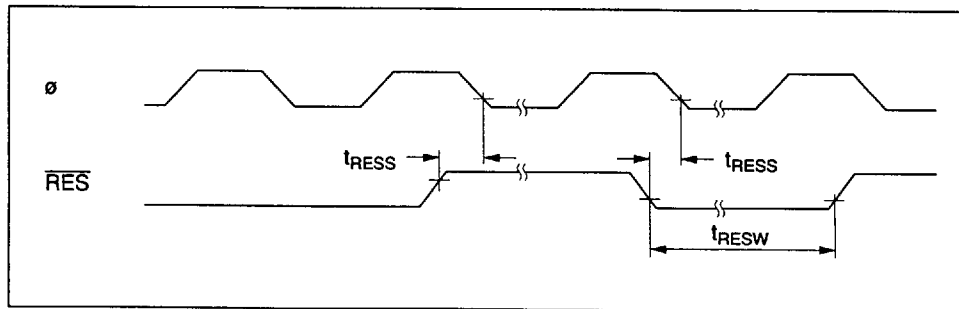


Figure 20-15 Reset Input Timing

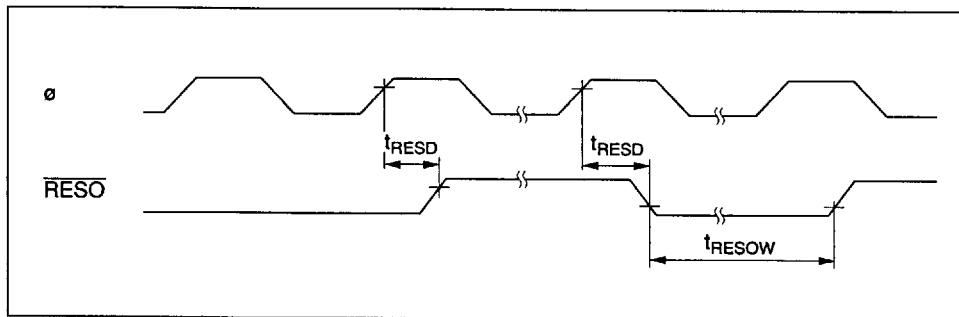


Figure 20-16 Reset Output Timing

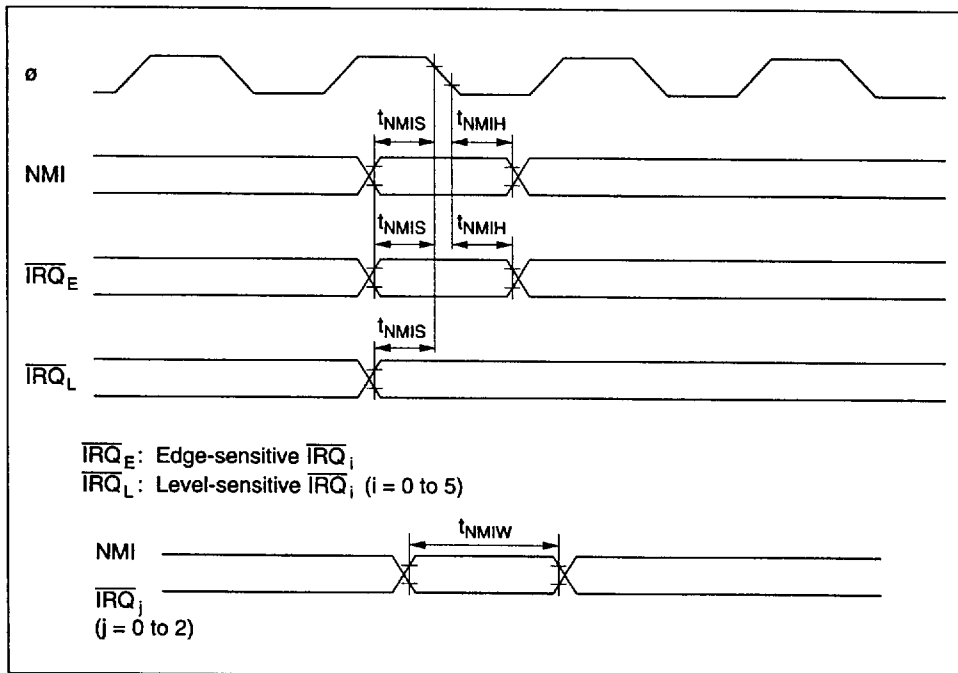


Figure 20-17 Interrupt Input Timing

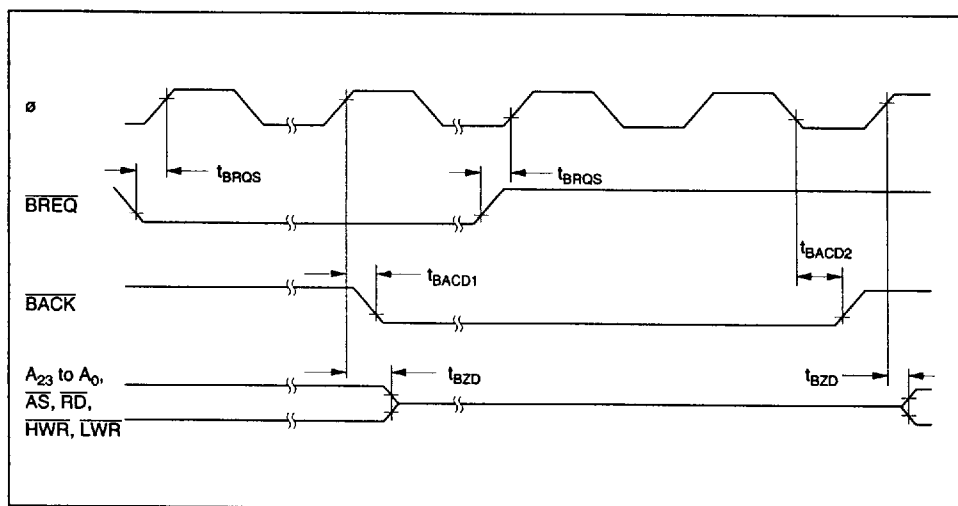


Figure 20-18 Bus-Release Mode Timing

### 20.3.4 Clock Timing

Clock timing is shown as follows:

- Oscillator settling timing

Figure 20-19 shows the oscillator settling timing.

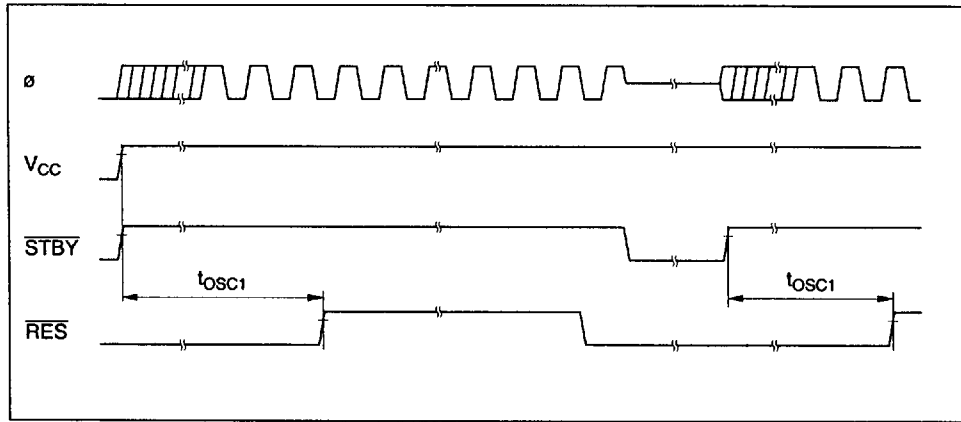


Figure 20-19 Oscillator Settling Timing

### 20.3.5 TPC and I/O Port Timing

TPC and I/O port timing is shown as follows.

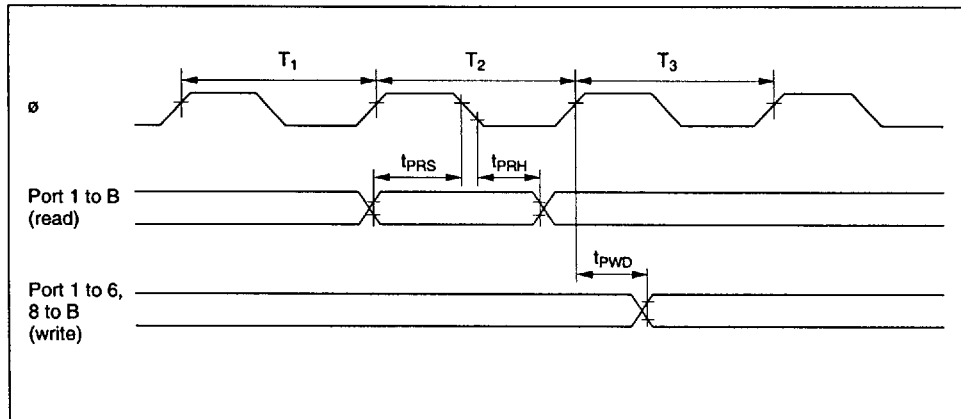


Figure 20-20 TPC and I/O Port Input/Output Timing

### 20.3.6 ITU Timing

ITU timing is shown as follows:

- ITU input/output timing

Figure 20-21 shows the ITU input/output timing.

- ITU external clock input timing

Figure 20-22 shows the ITU external clock input timing.

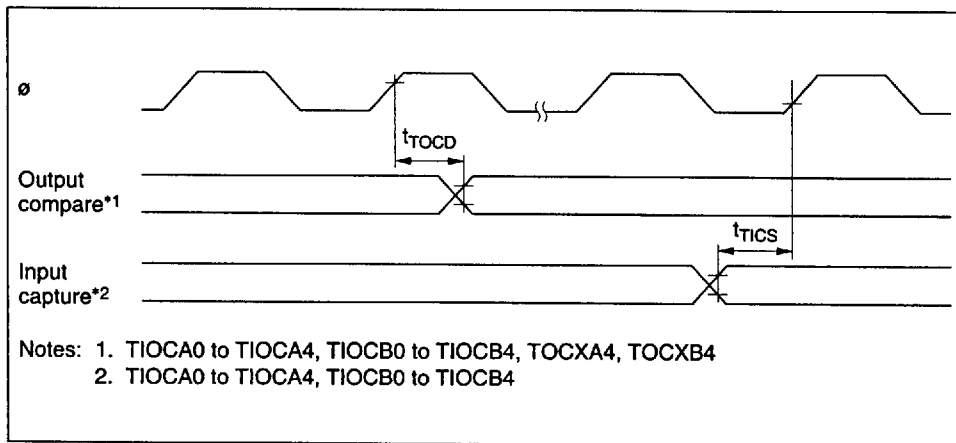


Figure 20-21 ITU Input/Output Timing

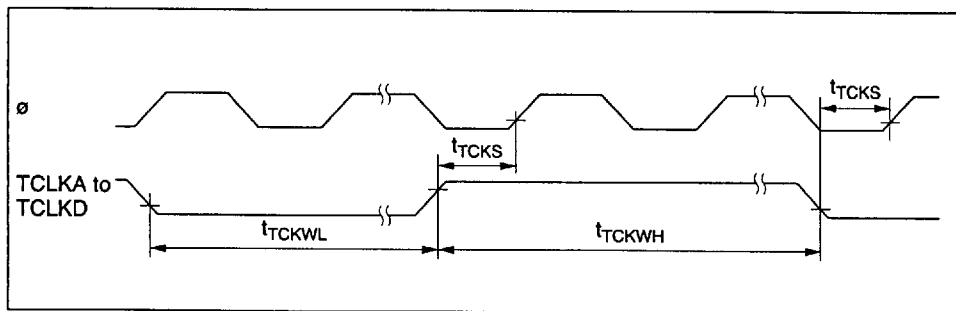


Figure 20-22 ITU Clock Input Timing

### 20.3.7 SCI Input/Output Timing

SCI timing is shown as follows:

- SCI input clock timing

Figure 20-23 shows the SCI input clock timing.

- SCI input/output timing (synchronous mode)

Figure 20-24 shows the SCI input/output timing in synchronous mode.

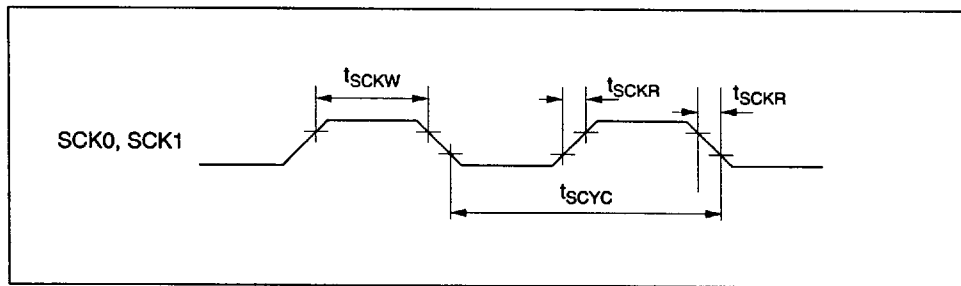


Figure 20-23 SCK Input Clock Timing

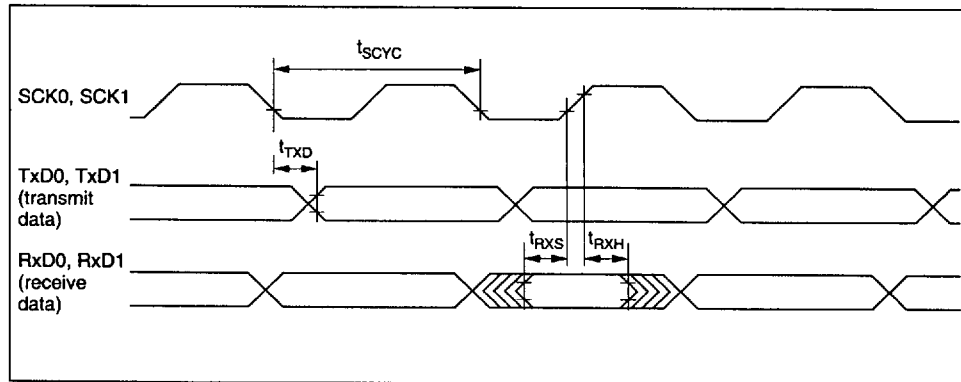


Figure 20-24 SCI Input/Output Timing in Synchronous Mode

### 20.3.8 DMAC Timing

DMAC timing is shown as follows.

- DMAC  $\overline{TEND}$  output timing for 2 state access

Figure 20-25 shows the DMAC  $\overline{TEND}$  output timing for 2 state access.

- DMAC  $\overline{TEND}$  output timing for 3 state access

Figure 20-26 shows the DMAC  $\overline{TEND}$  output timing for 3 state access.

- DMAC  $\overline{DREQ}$  input timing

Figure 20-27 shows DMAC  $\overline{DREQ}$  input timing.

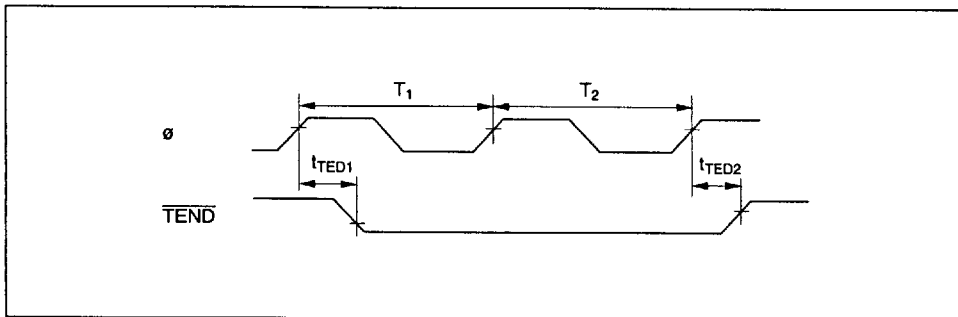


Figure 20-25 DMAC  $\overline{TEND}$  Output Timing for 2 State Access

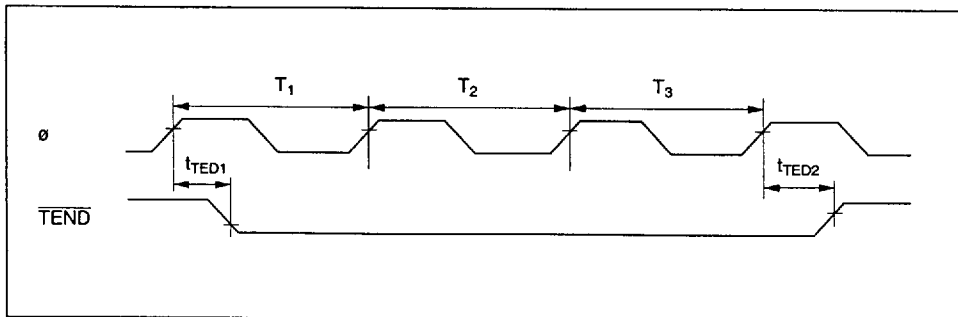


Figure 20-26 DMAC  $\overline{TEND}$  Output Timing for 3 State Access



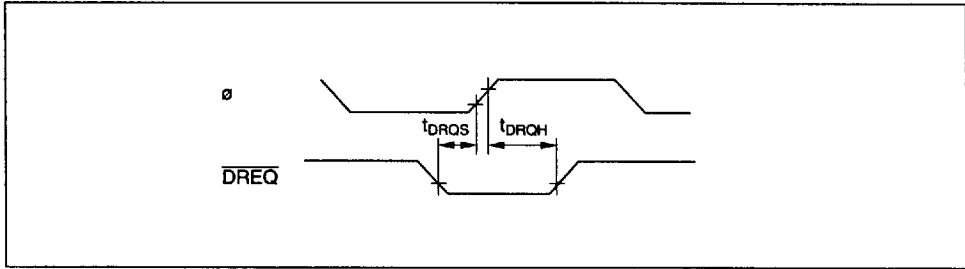


Figure 20-27 DMAC  $\overline{\text{DREQ}}$  Input Timing