GD4029B
SYNCHRONOUS UP/DOWN COUNTER

DESCRIPTION – The 4029B is a Synchronous Edge-Triggered Up/Down 4-Bit Binary/BCD Decade Counter with a Clock Input (CP), an active LOW Count Enable Input ($\overline{CE}$), an Up/Down Control Input (UP/$\overline{DN}$), a Binary/Decade Control Input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH Parallel Load Input (PL), four Parallel Data Inputs (P_0–P_3), four Parallel Buffered Outputs (Q_0–Q_3) and an active LOW Terminal Count Output ($\overline{TC}$).

Information on the Parallel Inputs (P_0–P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions. With the Parallel Load Input (PL) LOW, operation is synchronous and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). Operation is determined by the three synchronous Mode Control Inputs; UP/$\overline{DN}$, BIN/$\overline{DEC}$ and $\overline{CE}$ (see the Mode Selection Table). These inputs must be stable only during the set-up time prior to the LOW-to-HIGH transition of the Clock Input (CP) and the hold time after this clock transition. The Terminal Count Output ($\overline{TC}$) is LOW when the counter is at its terminal count, as determined by the counting mode, and the Count Enable Input ($\overline{CE}$) is LOW (see Logic Equation for $\overline{TC}$).

- **BINARY OR DECADE UP/DOWN COUNTER**
- **ASYNCHRONOUS PARALLEL LOAD**
- **ACTIVE LOW COUNT ENABLE**
- **CLOCK EDGE-TRIGGERED ON THE LOW-TO-HIGH TRANSITION**
- **ACTIVE LOW TERMINAL COUNT FOR CASCADING**
- **TYPICAL COUNT FREQUENCY OF 12 MHz AT V_{DD} = 10 V**

PIN NAMES

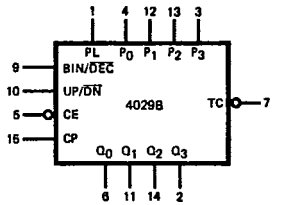
PL	Parallel Load Input
P_0–P_3	Parallel Data Inputs
BIN/$\overline{DEC}$	Binary/Decade Control Input
UP/$\overline{DN}$	Up/Down Control Input
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
Q_0–Q_3	Buffered Parallel Outputs
$\overline{TC}$	Terminal Count Output (Active LOW)

MODE SELECTION TABLE

PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	X	H	X	No Change
L	L	L	L	⎍	Count Down, Decade
L	L	H	L	⎍	Count Up, Decade
L	H	L	L	⎍	Count Down, Binary
L	H	H	L	⎍	Count Up, Binary

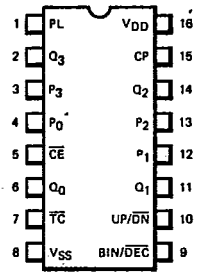
H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = Positive-Going Transition

LOGIC SYMBOL



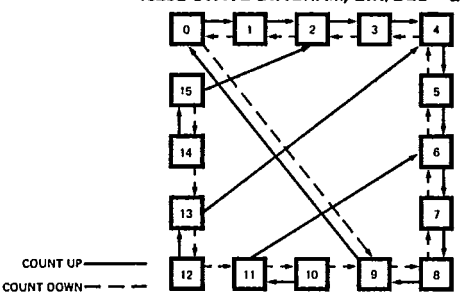
V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)

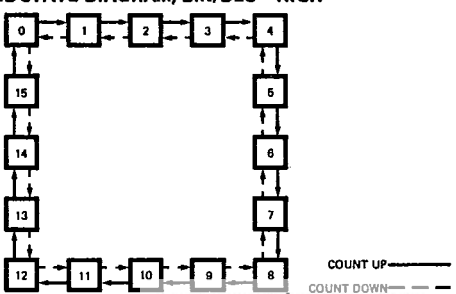


NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

4029B STATE DIAGRAM, BIN/$\overline{DEC}$ = LOW



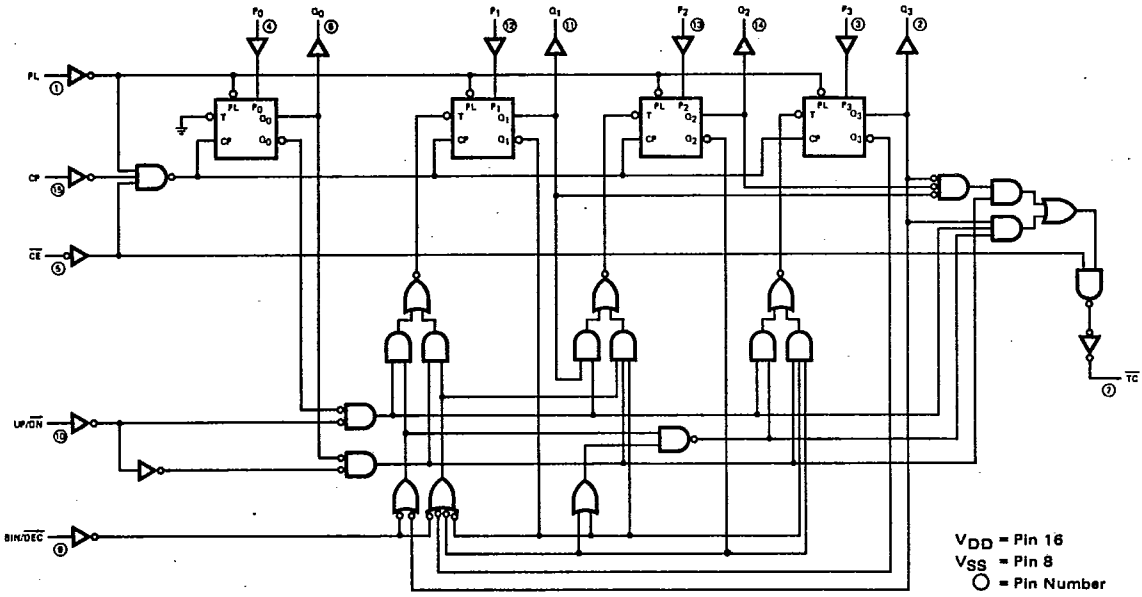
4029B STATE DIAGRAM, BIN/$\overline{DEC}$ = HIGH

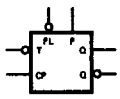


LOGIC EQUATION FOR TERMINAL COUNT

$$TC = CE \bullet [UP \bullet Q_0 \bullet Q_3 \bullet (\overline{BIN} + (Q_1 \bullet Q_2)) + (\overline{UP} \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)]$$

LOGIC DIAGRAM





$\overline{PL}$ (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when $\overline{PL}$ is LOW Overriding all Other Inputs
$\overline{T}$ (Toggle Input) — Forces the Q Output to Synchronously Toggle when a LOW is Placed on this Input.
CP (Clock Pulse Input)
Q, $\overline{Q}$ (True and Complimentary Outputs)

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	µA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	µA	MIN, 25°C	
					150			300			600		MAX	

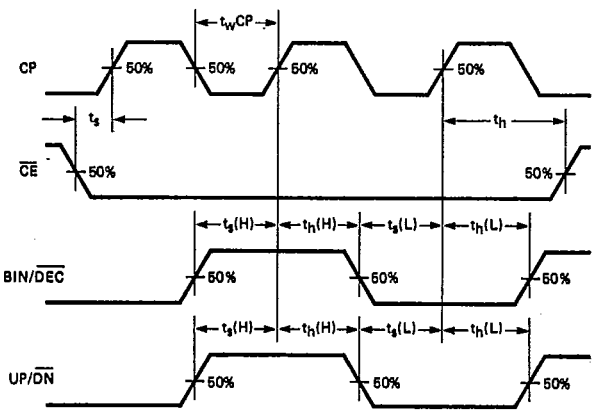
. Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 3)

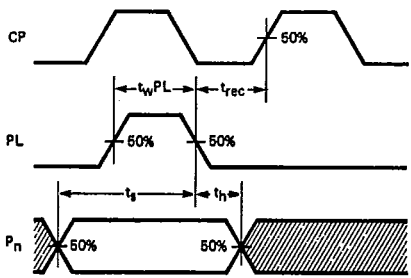
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		150	350		62	160		41	128	ns	
t_{PHL}			150	350		59	160		39	128	ns	
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167	450		71	180		48	144	ns	
t_{PHL}			252	650		100	245		66	196	ns	
t_{PLH}	Propagation Delay, PL to Q_n		170	325		70	150		45	120	ns	
t_{PHL}			220	450		90	195		62	156	ns	
t_{TLH}	Output Transition Time		60	135		31	75		23	45	ns	
t_{THL}			65	135		25	75		18	45	ns	
t_wCP	CP Minimum Pulse Width	125	50		60	21		48	14		ns	C_L = 50 pF,
t_wPL	PL Minumum Pulse Width	150	60		55	21		44	16		ns	R_L = 200 kΩ
t_{rec}	PL Recovery Time	150	62		60	24		48	17		ns	Input Transition
t_s	Set-Up Time, BIN/$\overline{DEC}$ to CP	250	106		100	41		80	29		ns	Times ≤ 20 ns
t_h	Hold Time, BIN/$\overline{DEC}$ to CP	0	-90		0	-35		0	-25		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP	325	145		130	55		104	38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP	0	-90		0	-35		0	-25		ns	
t_s	Set-Up Time, $\overline{CE}$ to CP	275	118		120	49		96	23		ns	
t_h	Hold Time, $\overline{CE}$ to CP	0	-40		0	-15		0	-10		ns	
t_s	Set-Up Time, P_n to PL	70	29		30	11		24	8		ns	
t_h	Hold Time, P_n to PL	0	-40		0	-20		0	-20		ns	
f_{MAX}	Input Clock Frequency (Note 2)	2	5		5	12		6	14		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. For f_{MAX} input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

SWITCHING WAVEFORMS



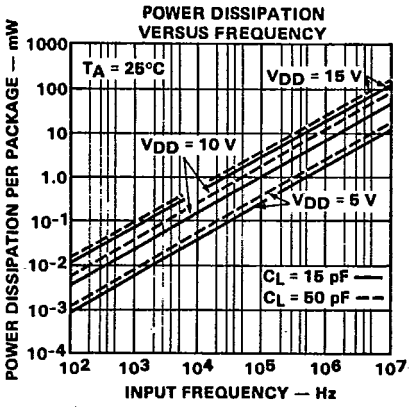
MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP, BIN/$\overline{DEC}$ TO CP AND UP/$\overline{DN}$ TO CP

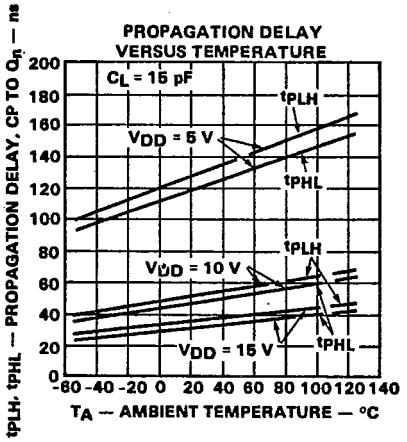


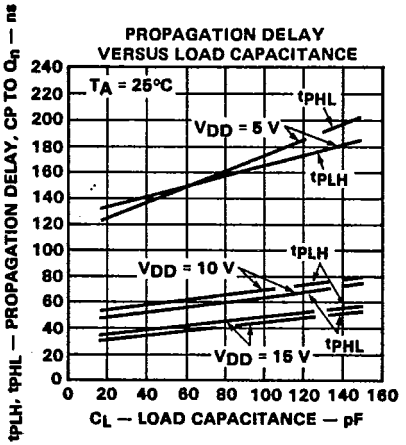
MINIMUM PL PULSE WIDTH, RECOVERY TIME FOR PL, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS







APPLICATIONS

Interconnection techniques for multistage counting are shown in Figures 1 through 4. When using the schemes shown in Figures 1, 3 and 4, the BIN/$\overline{\text{DEC}}$ and UP/$\overline{\text{DN}}$ Inputs may be changed only when the Clock Input to the first stage is HIGH. However, when using the scheme shown in Figure 2, UP/$\overline{\text{DN}}$, BIN/$\overline{\text{DEC}}$ and $\overline{\text{CE}}$ may be changed independent of the state of the Clock Input. The methods illustrated in Figures 1 and 3 will operate with long transition times at the Clock Input to the first counter; whereas, the other schemes require a fast transition at the Clock Input.

Figure 1 is a ripple clock expansion scheme in which the maximum counting frequency is limited only by the frequency capability of the first counter. The disadvantage of this technique is that the Outputs of the most significant stage do not change until the clock has rippled through all the preceding stages.

A fully synchronous expansion method is shown in Figure 2. Since the Clock Input is applied simultaneously to all stages, the Outputs of all stages change simultaneously. The maximum counting frequency is limited by the time required for the Count Enable to ripple through all the stages before the next Clock Input is applied.

The semi-synchronous technique illustrated in Figure 3 allows a higher counting frequency than the method shown in Figure 2 by allowing $\overline{\text{TC}}$ to take either 10 or 16 clock periods to ripple from the second stage to the most significant stage (10 clock periods when BIN/$\overline{\text{DEC}}$ = L, 16 clock periods when BIN/$\overline{\text{DEC}}$ = H). The Outputs of all stages, except the first, change simultaneously. The Outputs of the first stage change before the other stages.

The speed advantage of this scheme is lost if the count direction or count modulus is rapidly changed.

The method shown in Figure 4 is the same as in Figure 3 except an external gate is added to reduce the delay between the Clock Input to the first stage and the Clock Input to the following stages.

APPLICATIONS (Cont'd)

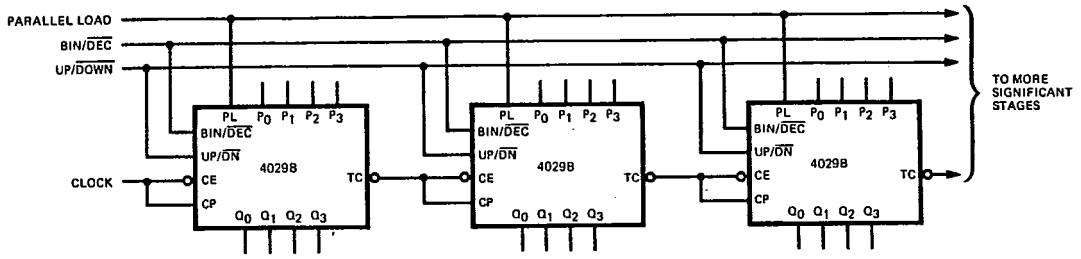


Fig. 1 RIPPLE CLOCK EXPANSION

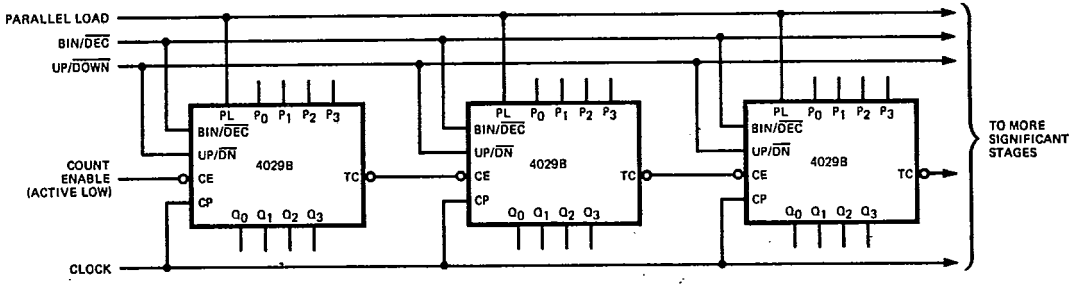


Fig. 2 PARALLEL CLOCK EXPANSION (FULLY SYNCHRONOUS)

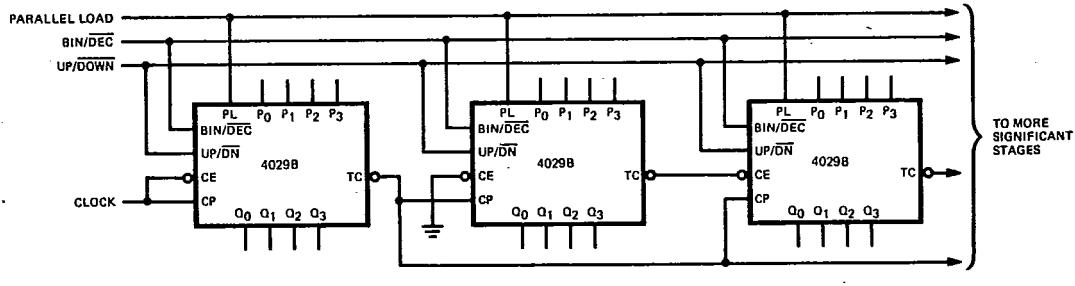


Fig. 3 SEMI-SYNCHRONOUS EXPANSION

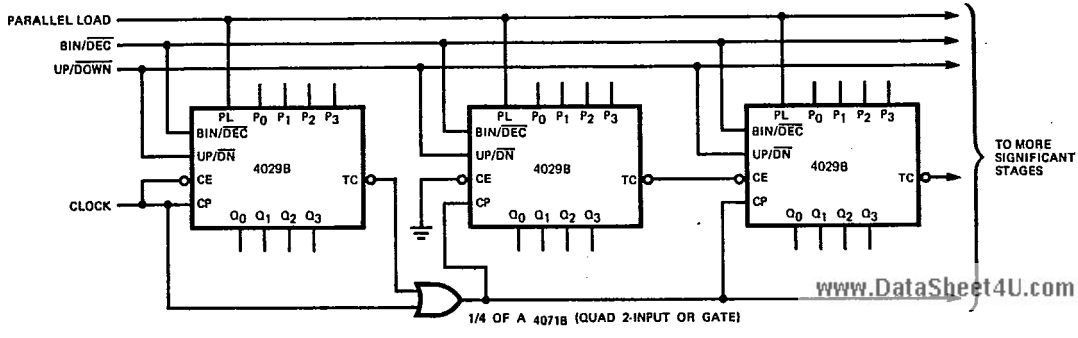


Fig. 4 HIGH SPEED SEMI-SYNCHRONOUS EXPANSION