



EMIF02-MIC03F1

2 LINES EMI FILTER AND ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS:

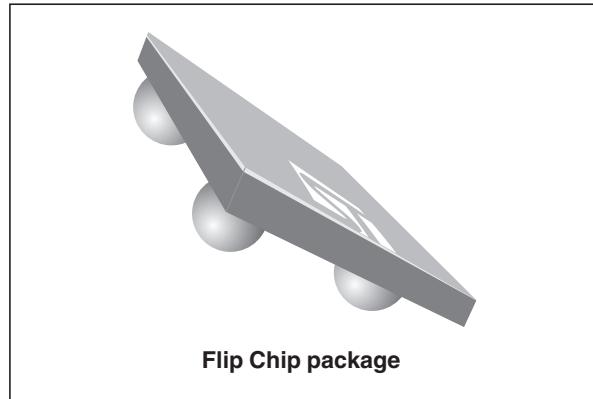
Where EMI filtering in ESD sensitive equipment is required :

- Mobile phones and communication systems
- Computers, printers and MCU Boards

DESCRIPTION

The EMIF02-MIC03 is a highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF02 flip chip packaging means the package size is equal to the die size.

This filter includes an ESD protection circuitry which prevents the device from destruction when subjected to ESD surges up to 15kV.



Flip Chip package

BENEFITS

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.07mm x 1.47mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

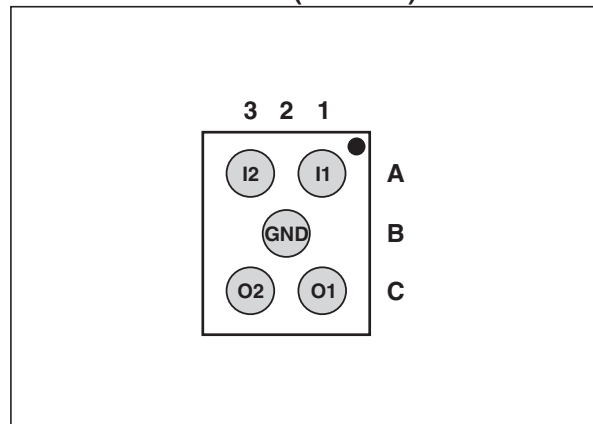
COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2

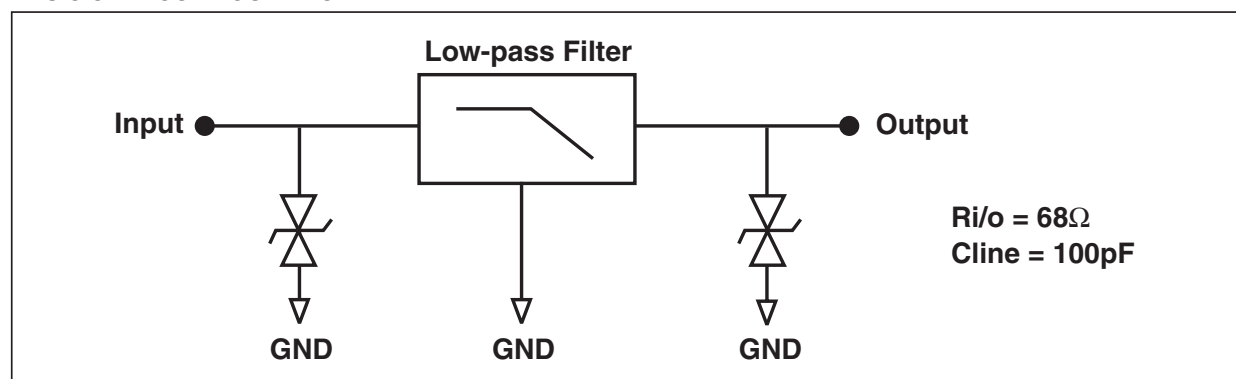
Level 4	on input pins	15kV (air discharge)
		8 kV (contact discharge)
Level 1	on output pins	2kV (air discharge)
		2kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3

PIN CONFIGURATION (ball side)



BASIC CELL CONFIGURATION



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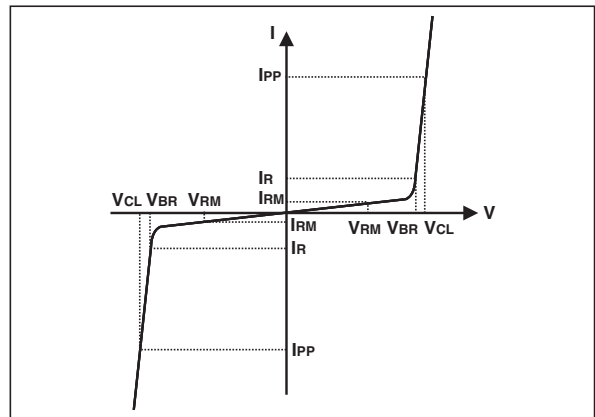
EMIF02-MIC03F1

ABSOLUTE RATINGS (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^\circ\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	8		V
I_{RM}	$V_{RM} = 3\text{ V per line}$			500	nA
$R_{I/O}$	Tolerance $\pm 20\%$		68		Ω
C_{line}	$V_R = 0\text{ V}$		100		pF

Fig. 1: S21(dB) attenuation measurement and Aplac simulation.

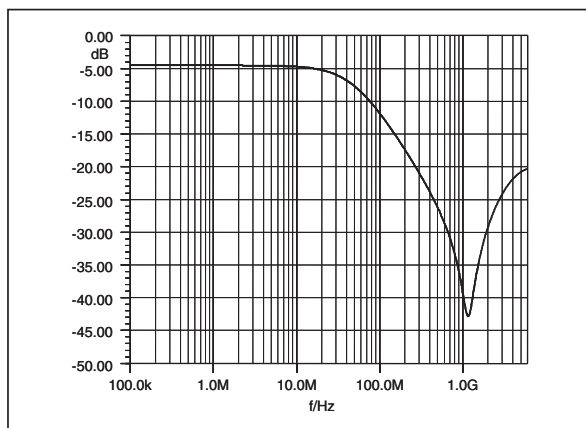


Fig. 2: Analog crosstalk measurements.

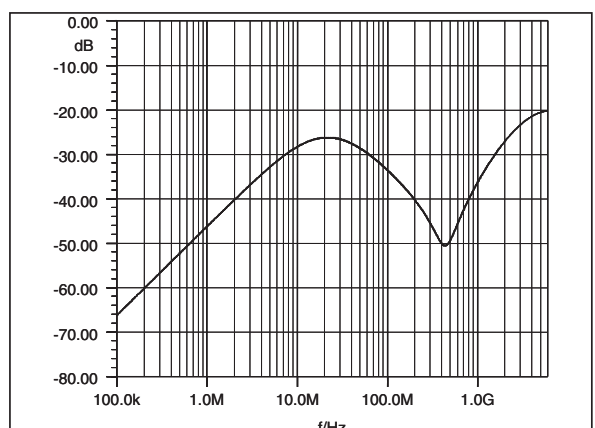


Fig. 3: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout).

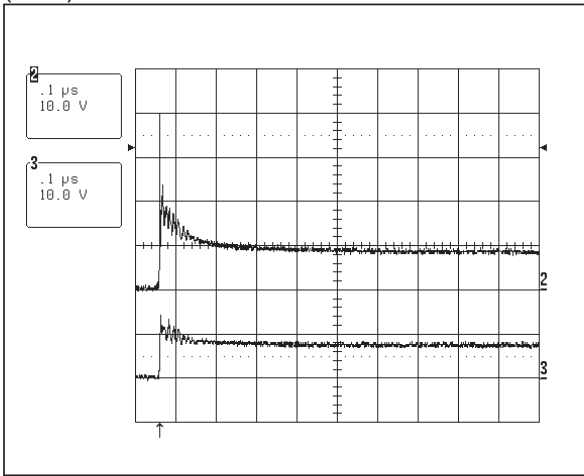


Fig. 4: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout).

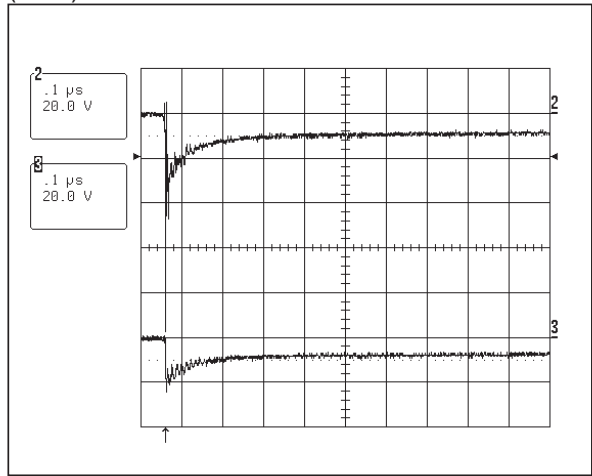
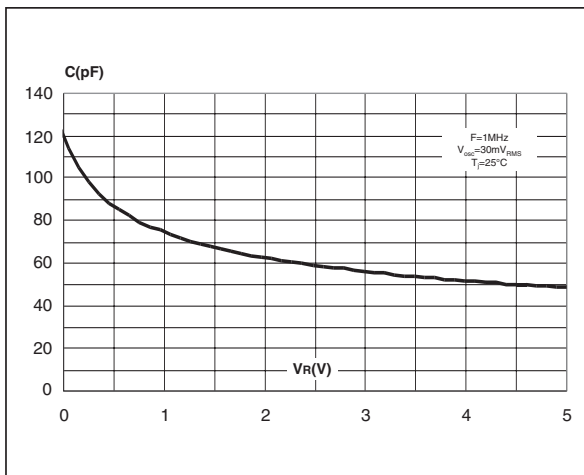
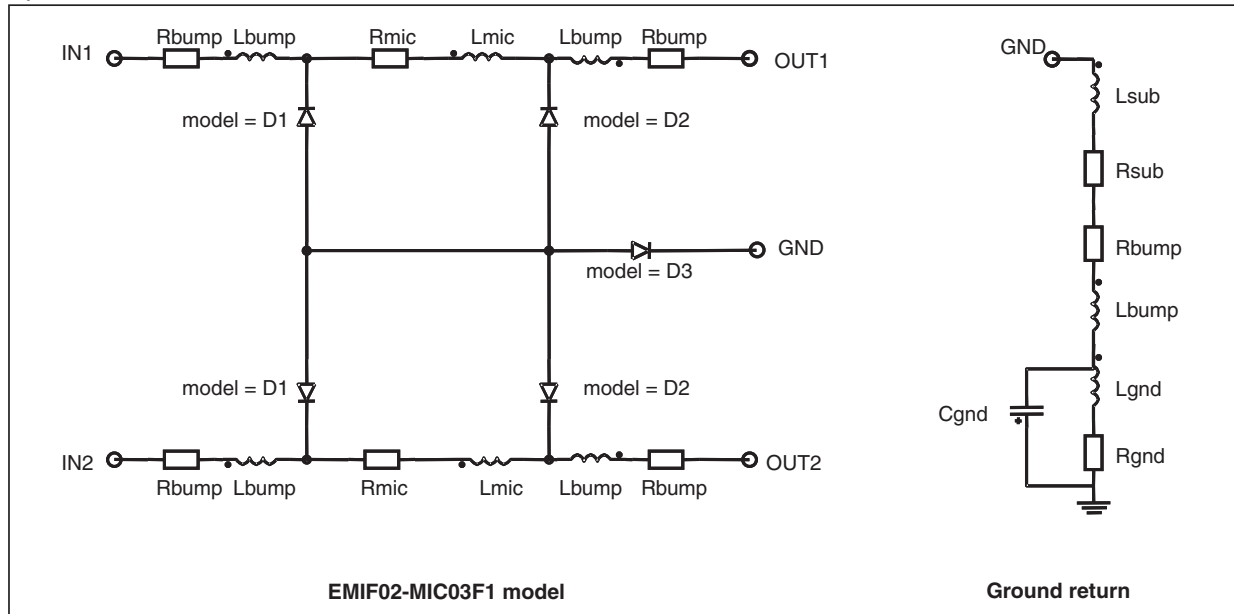


Fig. 5: Line capacitance versus applied voltage.



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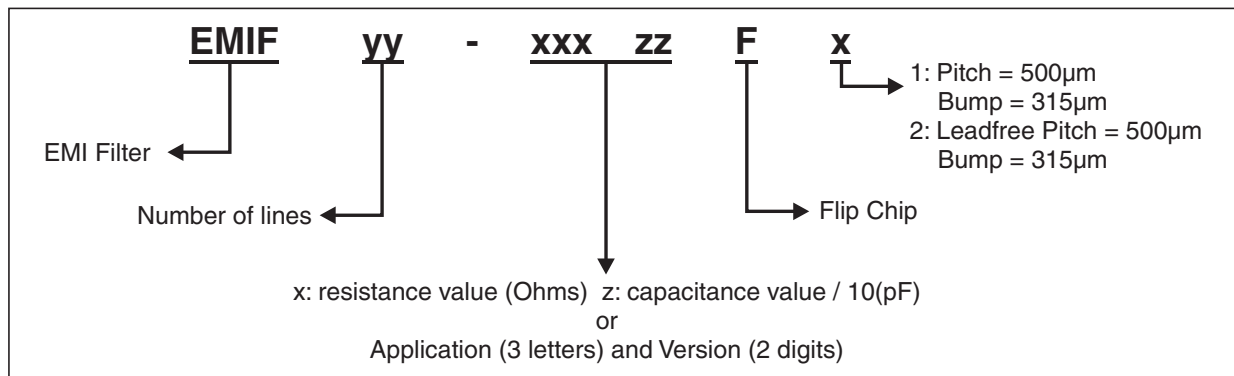
Aplac model.



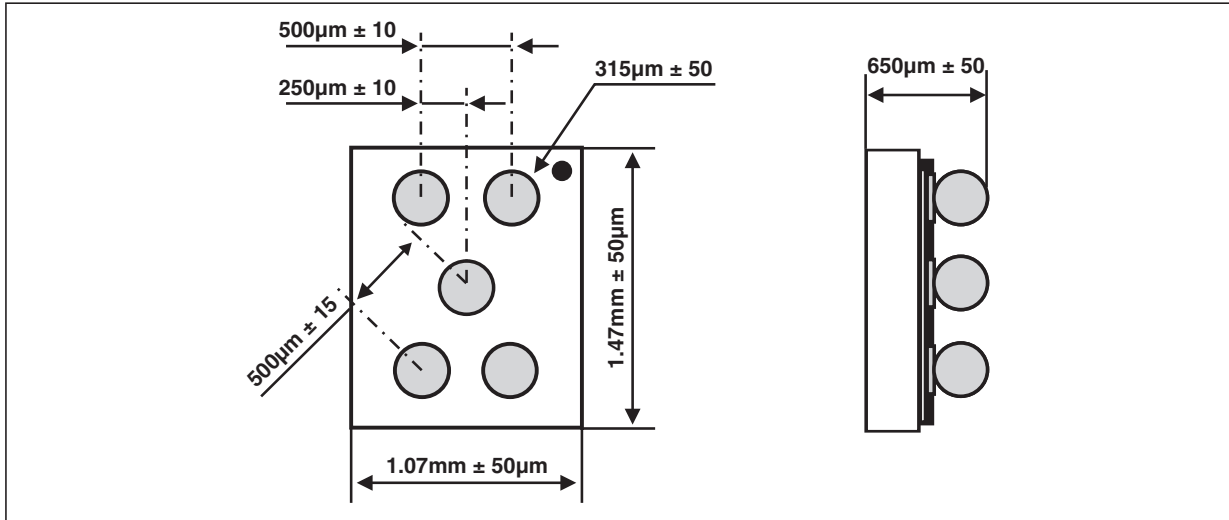
Aplac parameters.

Model D1	Model D3	Model D2	aplacvar Rmic 68
CJO=Cdiode1	CJO=Cdiode3	CJO=Cdiode2	aplacvar Lmic 10p
BV=7	BV=7	BV=7	aplacvar Cdiode1 100pF
IBV=1u	IBV=1u	IBV=1u	aplacvar Cdiode2 3.6pF
IKF=1000	IKF=1000	IKF=1000	aplacvar Cdiode3 1.17nF
IS=10f	IS=10f	IS=10f	aplacvar Lbump 50pH
ISR=100p	ISR=100p	ISR=100p	aplacvar Rbump 20m
N=1	N=1	N=1	aplacvar Rsub 0.5m
M=0.3333	M=0.3333	M=0.3333	aplacvar Rgnd 10m
RS=0.7	RS=0.12	RS=0.3	aplacvar Lgnd 50pH
VJ=0.6	VJ=0.6	VJ=0.6	aplacvar Cgnd 0.15pF
TT=50n	TT=50n	TT=50n	aplacvar Lsub 10pH

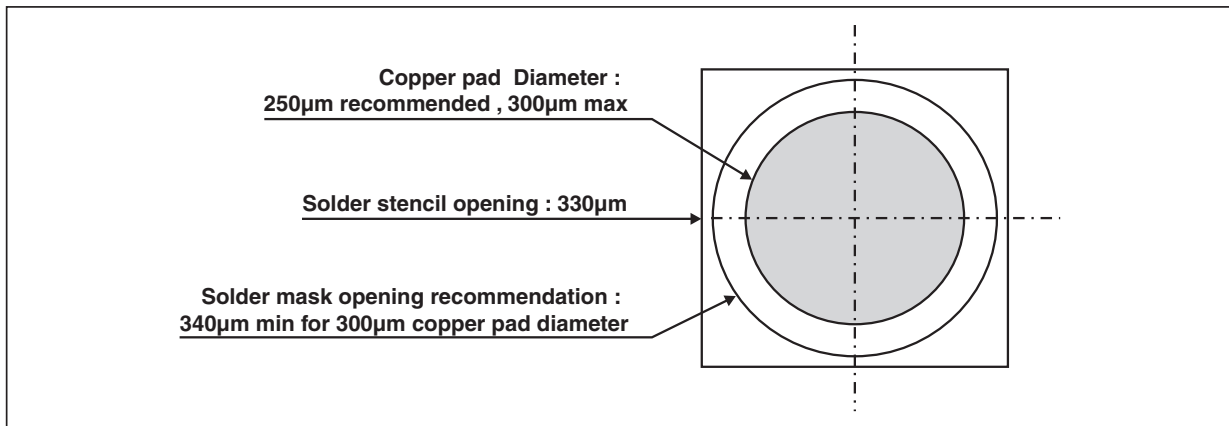
ORDER CODE



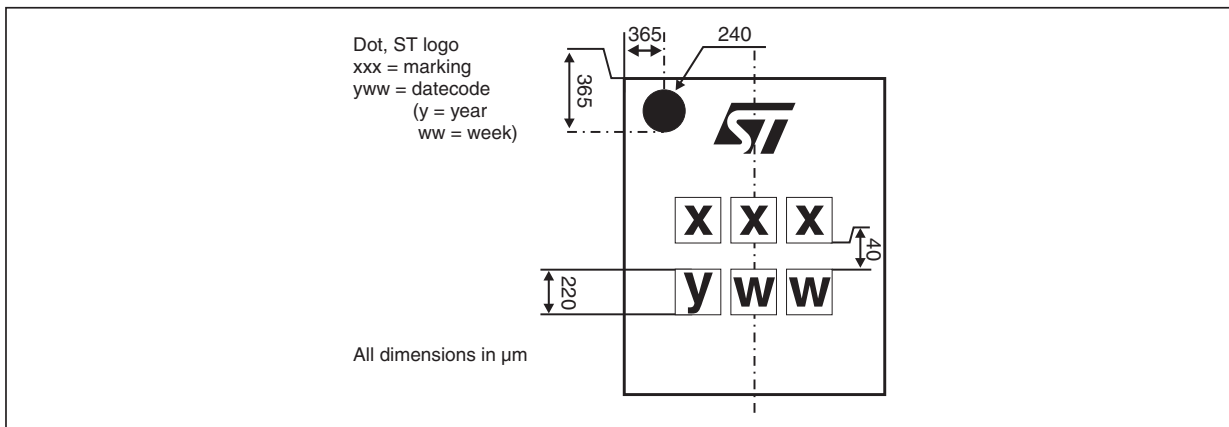
**PACKAGE MECHANICAL DATA
FLIP CHIP**



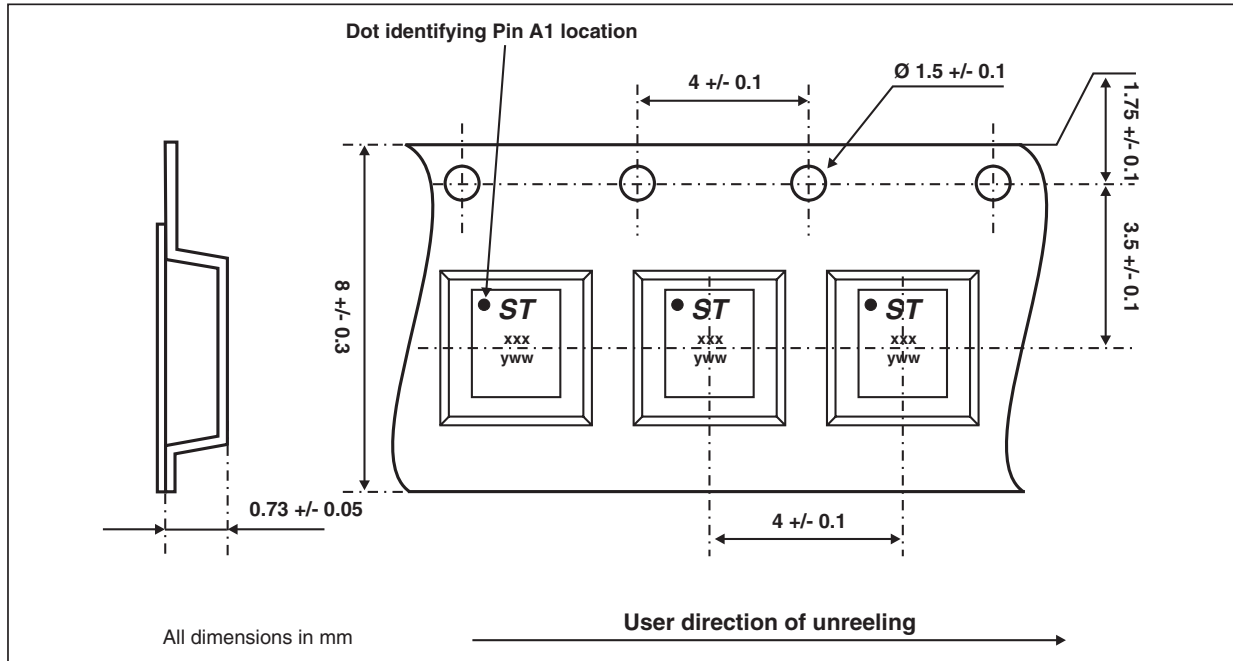
FOOT PRINT RECOMMENDATIONS



MARKING



PACKING



OTHER INFORMATION

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC03F1	FWT	Flip Chip	2.1 mg	5000	Tape & reel (7")

Note: More packing informations are available in the application notes
 AN1235: "Flip-Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

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