AN-6858
Applying SG6858 to Control a Flyback Power Supply

Summary

This application note describes a detailed design strategy for a high-efficiency, compact flyback converter. Design considerations, mathematical equations, and guidelines for printed circuit board layout are presented.

Features

- Green-mode PWM
- Supports the “Blue Angel” standard
- Low start-up current (10µA)
- Low operating current (2.5mA)
- Leading-edge blanking
- Constant output power limit
- Universal input
- Built-in synchronized slope compensation
- Current-mode operation
- Cycle-by-cycle current limiting
- Under voltage lockout (UVLO)
- Programmable PWM frequency
- V_{DD} over-voltage protection (auto restart)
- Gate output voltage clamped at 17V
- Low cost
- Few external components required
- Small SOT-26 and DIP-8 packages

Description

This highly integrated PWM controller provides several special enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to meet power conservation requirements.

The BiCMOS fabrication process enables reducing the start-up current to 10µA and the operating current to 2.5mA. To further improve power conservation, a large start-up resistance can be used. Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation provides a constant output power limit over a universal line input range ($90V_{AC}$ to $264V_{AC}$). Pulse-by-pulse current limiting ensures safe operation even during short circuits.

To protect the external power MOSFET from being damaged by excessive supply voltage, the SG6858’s output driver is clamped at 17V. SG6858 controllers can be used to improve the performance and reduce the production cost of power supplies. The SG6858 replaces linear and RCC-mode power adapters. It is available in 8-pin DIP and 6-pin SOT-26 packages.

Pin Configuration

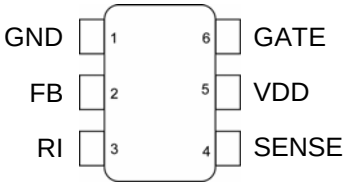

Figure 1. SOT-26 Pin Configuration

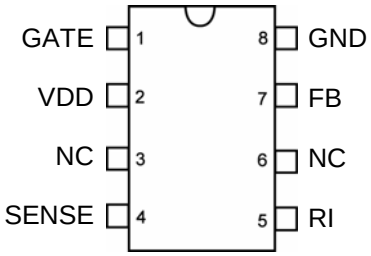

Figure 2. 8-Lead DIP Pin Configuration

Block Diagram

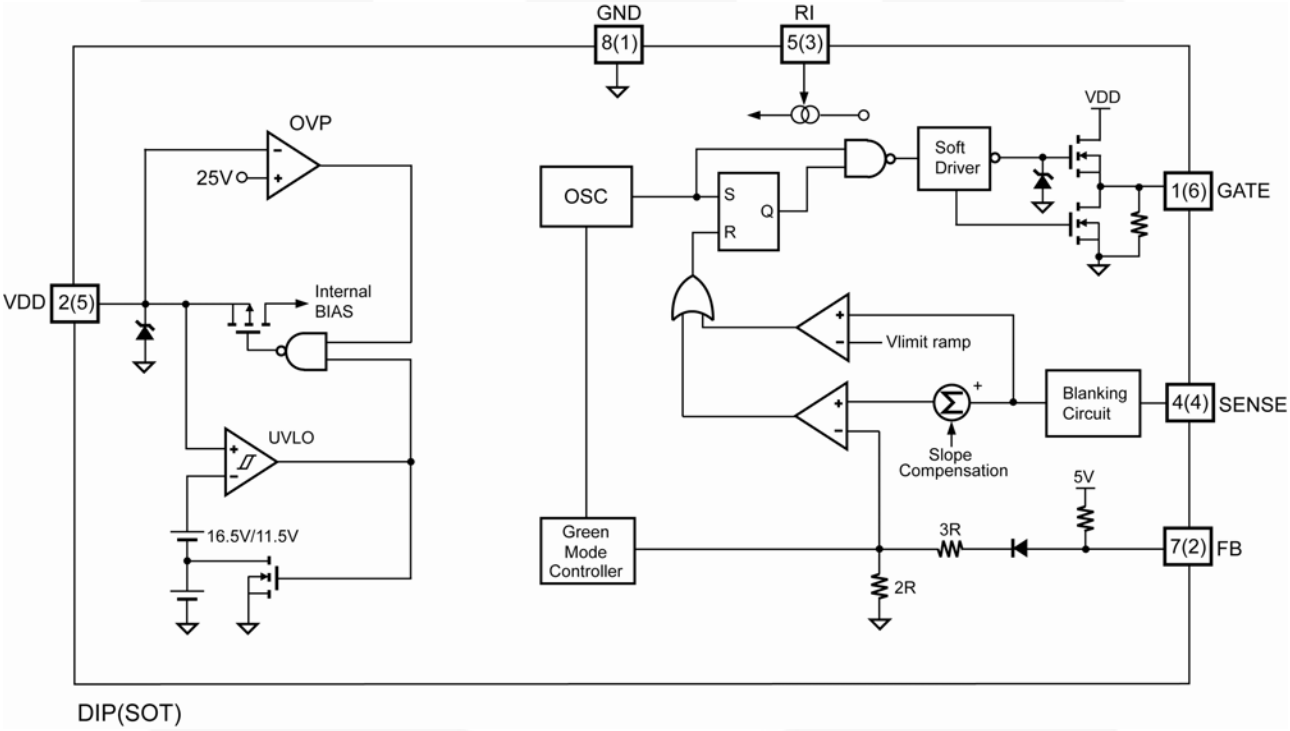

Figure 3. DIP-8 Pin Assignment (Numbers in Parenthesis are SOT-26 Pin Assignment)

Startup Circuitry

When the power is turned on, the input rectified voltage, V_{DC}, charges the hold-up capacitor C1 via startup resistor R_{IN}. As the voltage of the VDD pin reaches the start threshold voltage V_{DD-ON}, SG6858 activates the entire power supply.

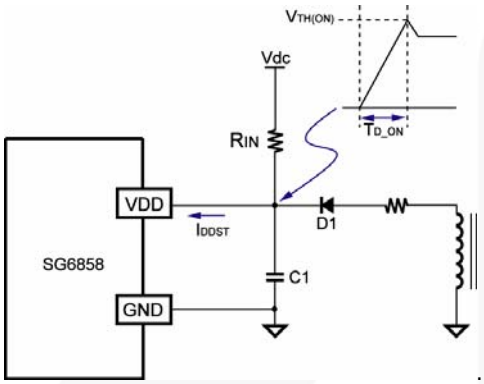

Figure 4. Circuit Providing Power

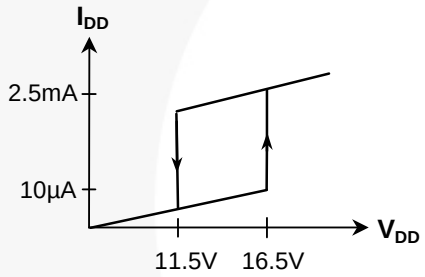

Figure 5. UVLO Specification

The maximum power-on delay time is determined as:

$$V_{DD-ON} = \left(V_{DC} - I_{DD-ST} \times R_{IN}\right)\left[1 - e^{-\frac{t_{D\_ON}}{R_{IN} \times C1}}\right] \quad (1)$$

where:

I_{DDST} is the startup current and

t_{D_ON} is the power-on delay of the power supply.

Due to the low start-up current, a large $R_{IN,}$ such as 1.5MΩ, can be used. With a hold-up capacitor of 10μF/50V, the power-on delay t_{D_ON} is less than 2.8s for $90V_{AC}$ input.

FB Input

This pin is designed for feedback control and to activate green mode. Figure 6 is a typical feedback circuit mainly consisting of a shunt regulator and an opto-coupler. R1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. RFB= 47Ω, C_{FB} = 1nF) placed from the FB pin to GND can increase stability. The maximum source current on the FB pin is 2mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor R_b is determined as:

$$\frac{V_O - V_D - V_Z}{R_b} \times K \geq 2mA \quad (2)$$

where:
V_D is the drop voltage of a photodiode, about 1.2V;

V_Z is the minimum operating voltage of the shunt regulator (typical 2.5V); and

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_O = 5V with CTR = 100%, the maximum value of R_b is 650Ω.

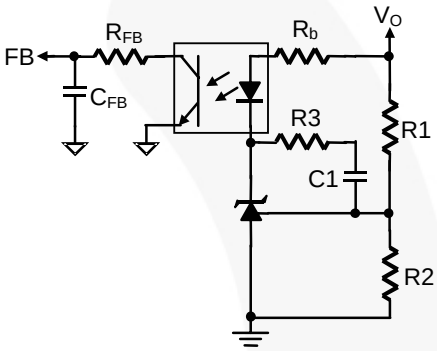

Figure 6. Feedback Circuit

Oscillator and Green Mode

One external resistor, R_I, connected between the RI and GND pins is used to program the PWM frequency of the SG6858. The approximated formula is:

$$f_{OSC}(KHz) = \frac{6650}{R_I(K\Omega)} \quad (3)$$

The recommended f_{OSC} is from 50 to 100KHz.

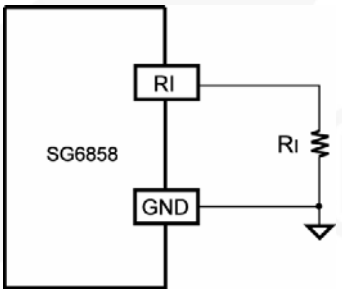

Figure 7. Setting PWM Frequency

The proprietary green mode provides off-time modulation to reduce the PWM frequency in light-load and no-load conditions. The feedback voltage of the FB pin is taken as a reference. When the feedback voltage is lower than about 2.85V, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the

PWM frequency, the off-time modulation reduces the power consumption of the power supply at light-load and no-load conditions. For a typical case of R_I = 95KΩ, the PWM frequency is 70KHz at nominal load, and decreases to 22KHz at light load. The power supply enters "adaptive off-time modulation" in zero-load conditions.

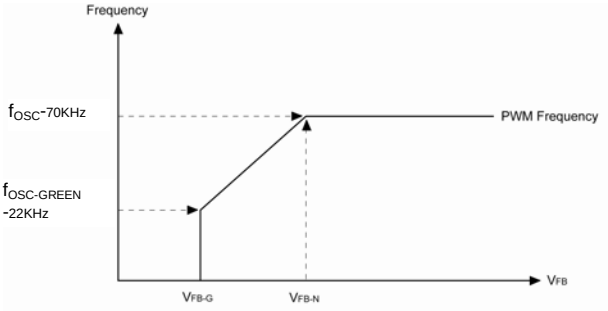

Figure 8. PWM Frequency vs. FB Voltage (R_I = 95KΩ)

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating the converter in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor currents than in DCM; therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice that of CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation also results in higher output voltage spikes. A large LC filter must be added. A flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of operating in CCM, there is one concern – stability. Operating in CCM, the output power is proportional to the average inductor current, while the peak current is controlled. This causes a well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent this oscillation. The SG6858 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. The sensed voltage together with this slope compensation signal (V_{SLOPE}) is fed into the non-inverting input of the PWM comparator. The resulting voltage is compared with the FB signal to adjust the PWM duty cycle, such that the output voltage is regulated. Therefore, users can use the SG6858 to design a cost-effective, highly efficient, and compact flyback power supply operating in CCM without adding external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \times D \quad (4)$$

where V_{SL} = 0.33V and D = duty cycle.

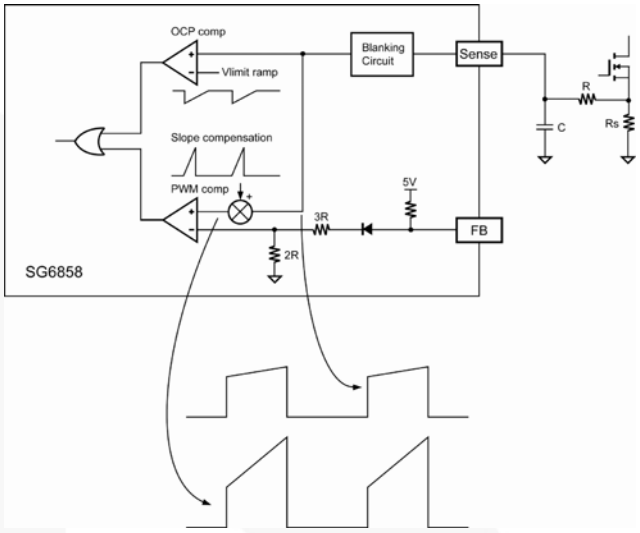

Figure 9. Synchronized Slope Compensation

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor RS. When the load increases, the peak inductor current increases accordingly. Once the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, t_{PD}. The delay time results in unequal power-limit level under universal input. In the SG6858, a sawtooth power-limiter (saw limiter) is designed to solve the unequal power-limit problem. As shown in Figure 10, the saw limiter is designed as a positive ramp (V_{limit_ramp}) signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit in high-line inputs than in low-line inputs. However, with fixed propagation delay, t_{PD}, the peak primary current would be the same for various line input voltages. Therefore the maximum output power can practically be limited to a constant value within a wide input voltage range without adding external circuitry.

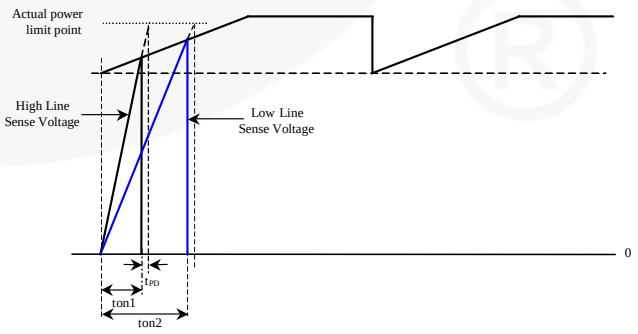

Figure 10.Constant Power Limit Compensation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection has been built in to prevent damage due to over-voltage conditions. When the voltage V_{DD} exceeds the internal threshold due to abnormal conditions, PWM output turns off until V_{DD} voltage drops below the UVLO, then starts again. Over-voltage conditions are usually caused by open feedback loops.

Short-Circuit Protection (SCP)

When the output of a flyback power supply is shorted, the primary V_{DD} decreases due to the coupling polarity, between the auxiliary winding and the secondary winding of a transformer. When V_{DD} drops below UVLO level, the power supply enter "hiccup" operation mode and limits the output power. However it is possible that the VDD voltage remains higher than the UVLO level even if the output is shorted. This happens when the coupling between the auxiliary and the primary winding is too good. Therefore, the construction of the transformer becomes a dominant factor. The recommended construction layout is to increase the insulation thickness for the auxiliary winding and place the primary auxiliary winding in one side of the bobbin. For low-output voltage applications, using a low-dropout voltage diode and a larger secondary winding also helps.

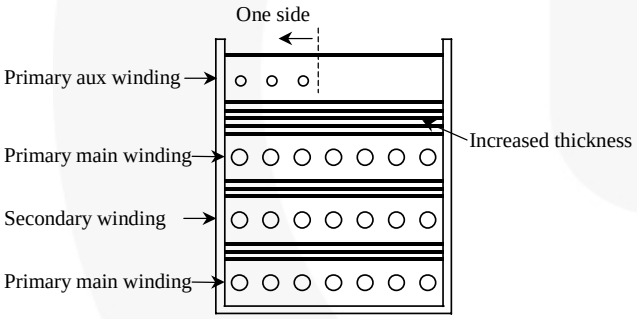

Figure 11. Transformer Construction

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sensing resistor, R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, appears on the sensed signal. A leading-edge blanking time of about 300ns is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended,

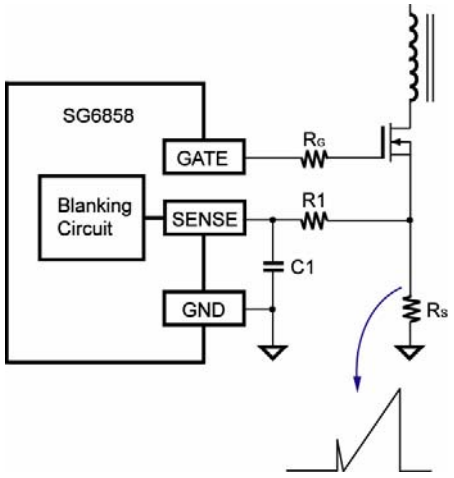

Figure 12. Turn-on Spike

Gate Drive

The SG6858's output stage is a fast totem-pole driver that can drive a MOSFET gate directly. It is also equipped with a voltage clamping Zener diode to protect the MOSFET from damage caused by over-drive voltage. The output voltage is clamped at 17V. An internal pull-down resistor is used to avoid a floating state of the gate before startup. A gate drive resistor in the range of 47 to 100Ω is recommended. This resistor limits the peak gate drive current and provides damping to prevent oscillations at the MOSFET gate terminal.

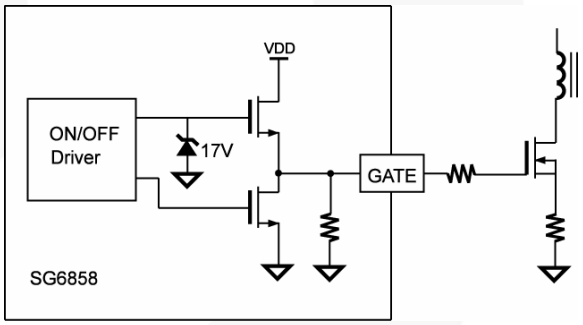

Figure 13. Gate Drive

Lab Note

Before reworking or soldering/de-soldering on the power supply, discharge the primary capacitors by an external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during soldering or de-soldering.

This device is sensitive to ESD discharge. To improve the production yield, the production line should be ESD protected in accordance to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board Layout

High-frequency switching current/voltage make PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in C1 – Transformer – MOSFET – RS – C1. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High voltage traces related to the drain of the MOSFET and the RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.
- As indicated by **3**, the control circuits' ground should be connected first, before other circuitry.
- As indicated by **2**, the area enclosed by the transformer auxiliary winding, D1 and C2 should also be kept small. Place C2 close to the SG6858 for good decoupling.

Two suggestions with different pros and cons for ground connections are offered:

- GND**3**→**2**→**4**→**1**: This should avoid common impedance interference for the sense signal.
- GND**3**→**2**→**1**→**4**: Potentially better for ESD testing where a ground is not available for the power supply. The ESD discharge charges go from secondary through the transformer stray capacitance to the GND**2** first. Then charges go from GND**2** to GND**1** and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the positive terminal of the C1 (V_{DC}). If this Y-cap is connected to the primary GND, it should be connected to the negative terminal of the C1 (GND**1**) directly. Point discharge of the Y-cap also helps with ESD; however, the distance between these two points should be at least 5mm according to safety requirements.

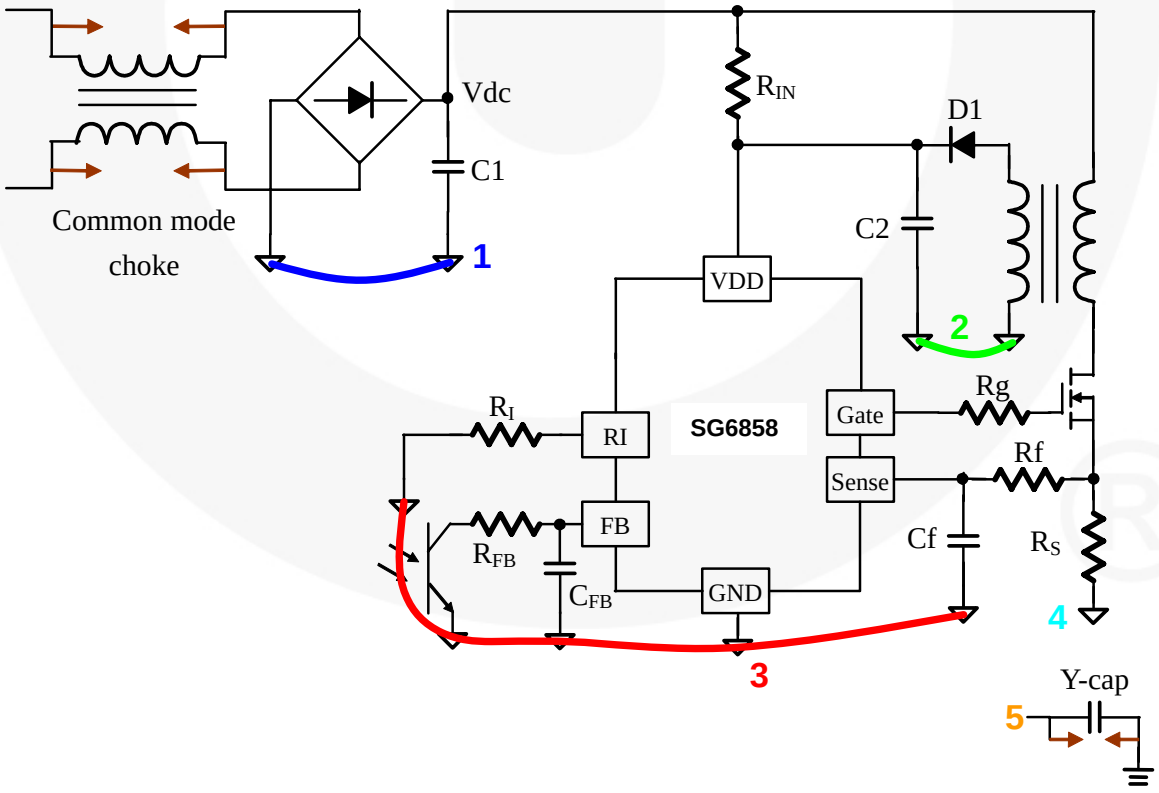

Figure 14. Layout Considerations

Related Datasheets

SG6858— Low Cost Green-Mode PWM Controller for Flyback Converter