Data Sheet | April 7, 2009 | FN6641.1

Dual/n-Phase Buck PWM Controller with Integrated Drivers

The ISL8120 integrates two voltage-mode synchronous buck PWM controllers to control a dual independent voltage regulator or a 2-phase single output regulator. It has PLL circuits and can output a phase-shift-programmable clock signal for the system to be expanded to 3-, 4-, 6-, 12- phases with desired interleaving phase shift. It also integrates current sharing control for the power module to operate in parallel, which offers high system flexibility.

It has voltage feed forward compensation to maintain a constant loop gain for optimal transient response, especially for applications with a wide input voltage range. Its integrated high speed MOSFET drivers and multi-feature functions provide complete control and protection for a 2/n-phase synchronous buck converter, dual independent regulators, or DDR tracking applications (VDDQ and VTT outputs).

The output voltage of a ISL8120-based converter can be precisely regulated to as low as the internal reference voltage 0.6V, with a system accuracy of ±0.6% over commercial temperature and line load variations. Channel 2 can track an external ramp signal for DDR/tracking applications.

The ISL8120 integrates an internal linear regulator, which generates VCC from input rail for applications with only one single supply rail. The internal oscillator is adjustable from 150kHz to 1.5MHz, and is able to track an external clock signal for frequency synchronization and phase paralleling applications. The integrated Pre-Biased Digital Soft-Start, Differential Remote Sensing Amplifier, and Programmable Input Voltage POR features enhance the value of ISL8120.

The ISL8120 protects against overcurrent conditions by inhibiting the PWM operation while monitoring the current with $r_{DS(ON)}$ of the lower MOSFET, DCR of the output inductor, or a precision resistor. It also has a PRE-POR Overvoltage Protection option, which provides some protection to the load device if the upper MOSFET(s) is shorted. See “PRE-POR Overvoltage Protection (PRE-POR-OVP)” on page 25 for details.

The ISL8120’s Fault Hand Shake feature protects any channel from overloading/stressing due to system faults or phase failure. The undervoltage fault protection features are also designed to prevent a negative transient on the output voltage during falling down. This eliminates the Schottky diode that is used in some systems for protecting the load device from reversed output voltage damage.

Features

- Wide VIN Range Operation: 3V to 22V
  - VCC Operation from 3V to 5.60V
- Fast Transient Response
  - 80MHz Bandwidth Error Amplifier
  - Voltage-Mode PWM Leading-edge Modulation Control
  - Voltage Feed-forward
- Dual Channel 5V High Speed 4A MOSFET Gate Drivers
  - Internal Bootstrap Diodes
- Internal Linear Regulator Provides a 5.4V Bias from VIN
- External Soft-Start Ramp Reference Input for DDR/Tracking Applications
- Excellent Output Voltage Regulation
  - 0.6V ±0.6%/±0.9% Internal Reference Over Commercial/Industrial Temperature
  - True Differential Remote Voltage Sensing
- Oscillator Programmable from 150kHz to 1.5MHz
- Frequency Synchronization
- Scale for 1-, 2-, 3-, 4-, 6-, up to 12- Phase with Single Output
  - Excellent Phase Current Balancing
  - Programmable Phase Shift Between the 2 Phases Controlled by the ISL8120 and Programmable Phase Shift for Clockout Signal
  - Interleaving Operation Results in Minimum Input RMS Current and Minimum Output Ripple Current
- Fault Hand Shake Capability for High System Reliability
- Overcurrent Protection
  - DCR, $r_{DS(ON)}$, or Precision Resistor Current Sensing
  - Independent and Average Phase Current OCP
- Output Overvoltage and Undervoltage Protections
- Programmable Phase Shift in Dual Mode Operation
- Digital Soft-Start with Pre-Charged Output Start-up Capability
- Power-Good Indication
- Dual Independent Channel Enable Inputs with Precision Voltage Monitor and Voltage Feed-forward Capability
  - Programmable Input Voltage POR and its Hysteresis with a Resistor Divider at EN Input
- Over-Temperature Protection
- Pre-Power-On-Reset Overvoltage Protection Option
- 32 Ld 5x5 QFN Package - Near Chip-Scale Footprint
  - Enhanced Thermal Performance for MHz Applications
- Pb-free (RoHS compliant)

Applications

- Power Supply for Datacom/Telecom and POL
- Paralleling Power Module
- Wide and Narrow Input Voltage Range Buck Regulators
- DDR I and II Applications
- High Current Density Power Supplies
- Multiple Outputs VRM and VRD

Related Literature

- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages”

Ordering Information

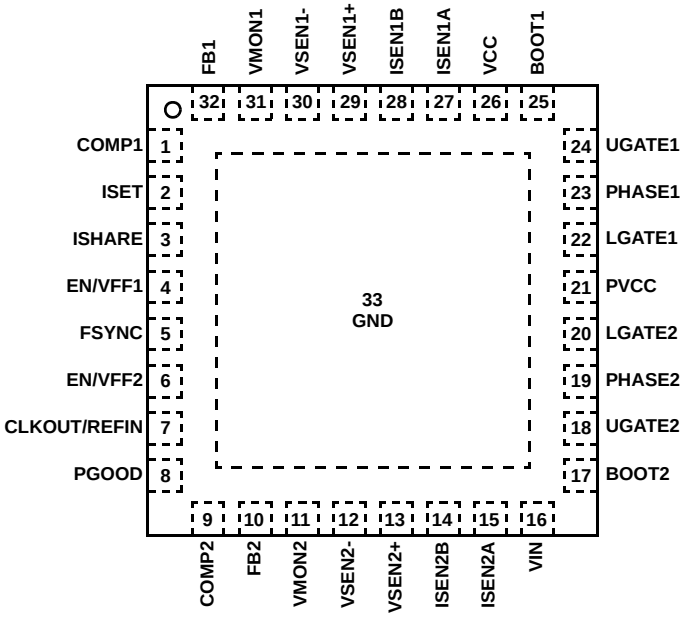
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8120CRZ	ISL8120 CRZ	0 to +70	32 Ld QFN	L32.5x5B
ISL8120CRZ-T*	ISL8120 CRZ	0 to +70	32 Ld QFN	L32.5x5B
ISL8120IRZ	ISL8120 IRZ	-40 to +85	32 Ld QFN	L32.5x5B
ISL8120IRZ-T*	ISL8120 IRZ	-40 to +85	32 Ld QFN	L32.5x5B

* Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL8120
(32 LD QFN)
TOP VIEW



Block Diagram

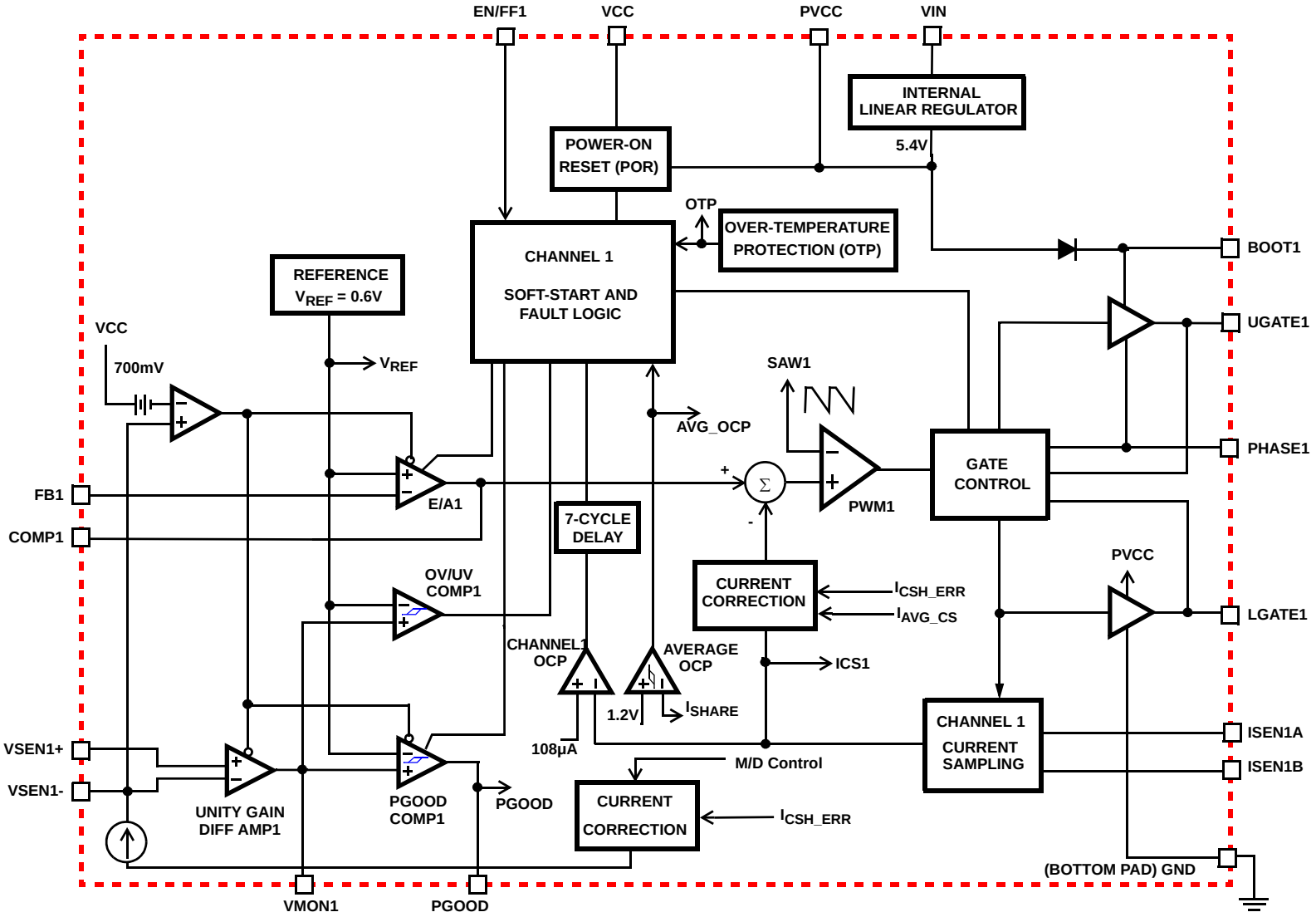


FIGURE 1. CHANNEL/PHASE 1 (VDDQ)

Block Diagram (Continued)

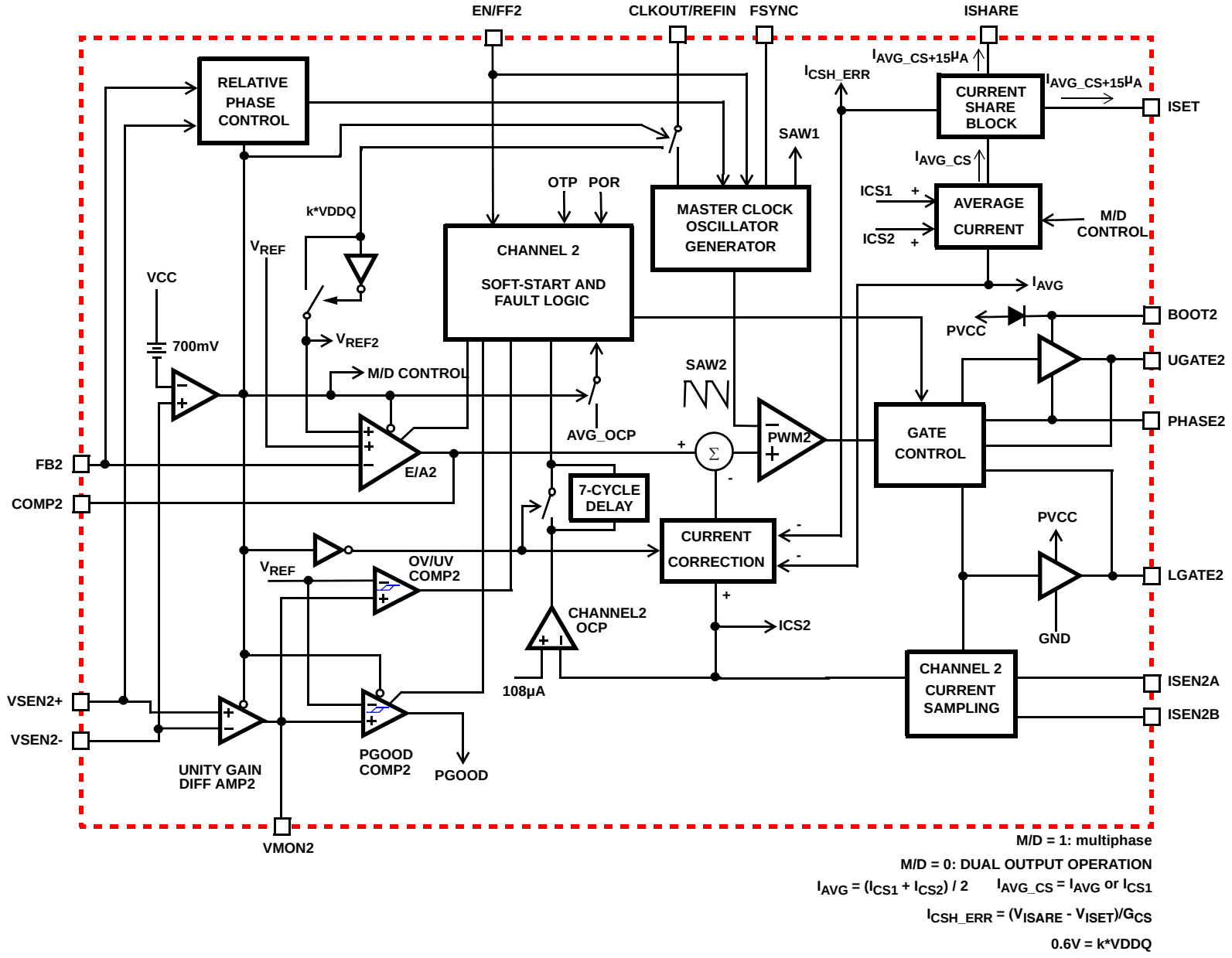
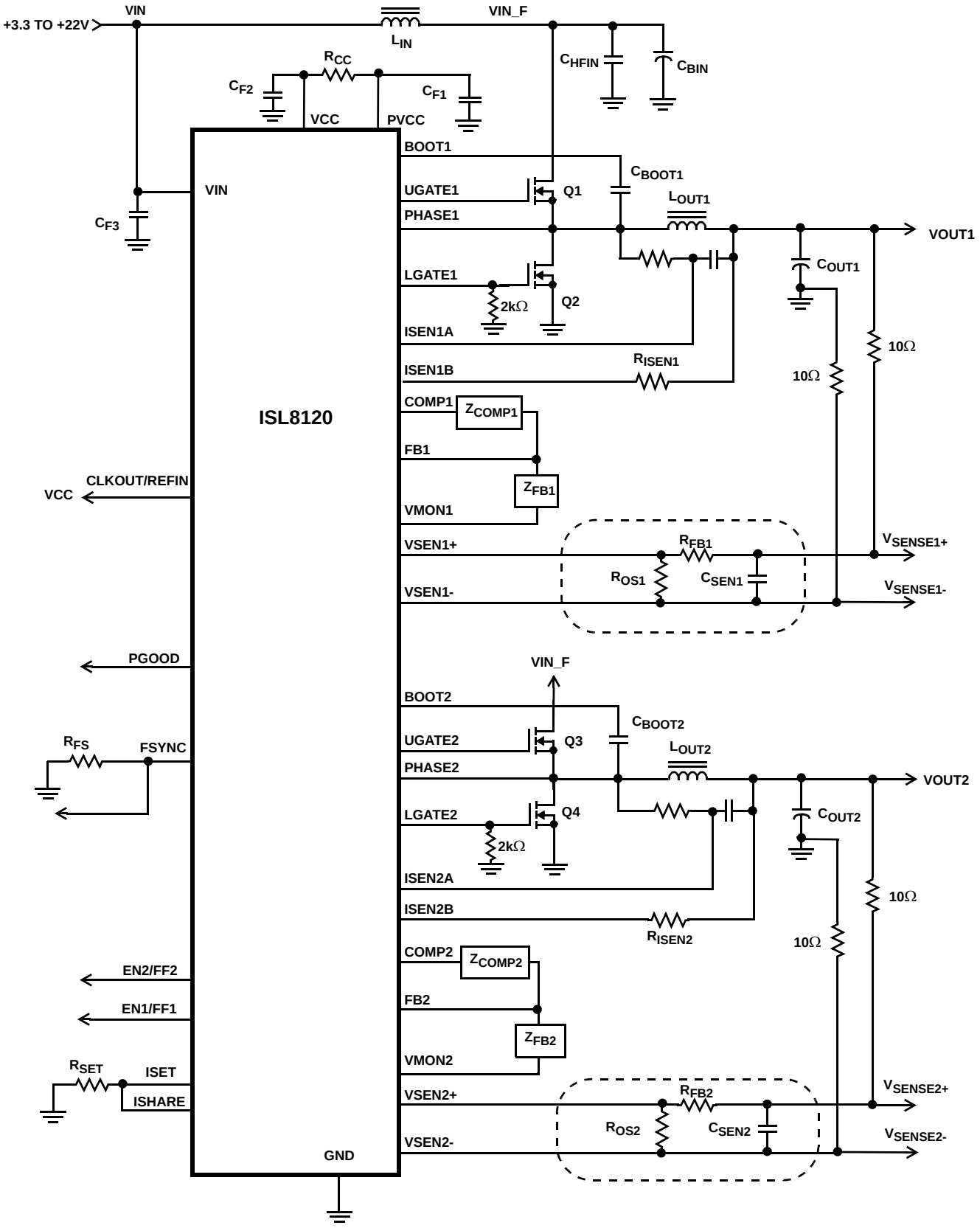
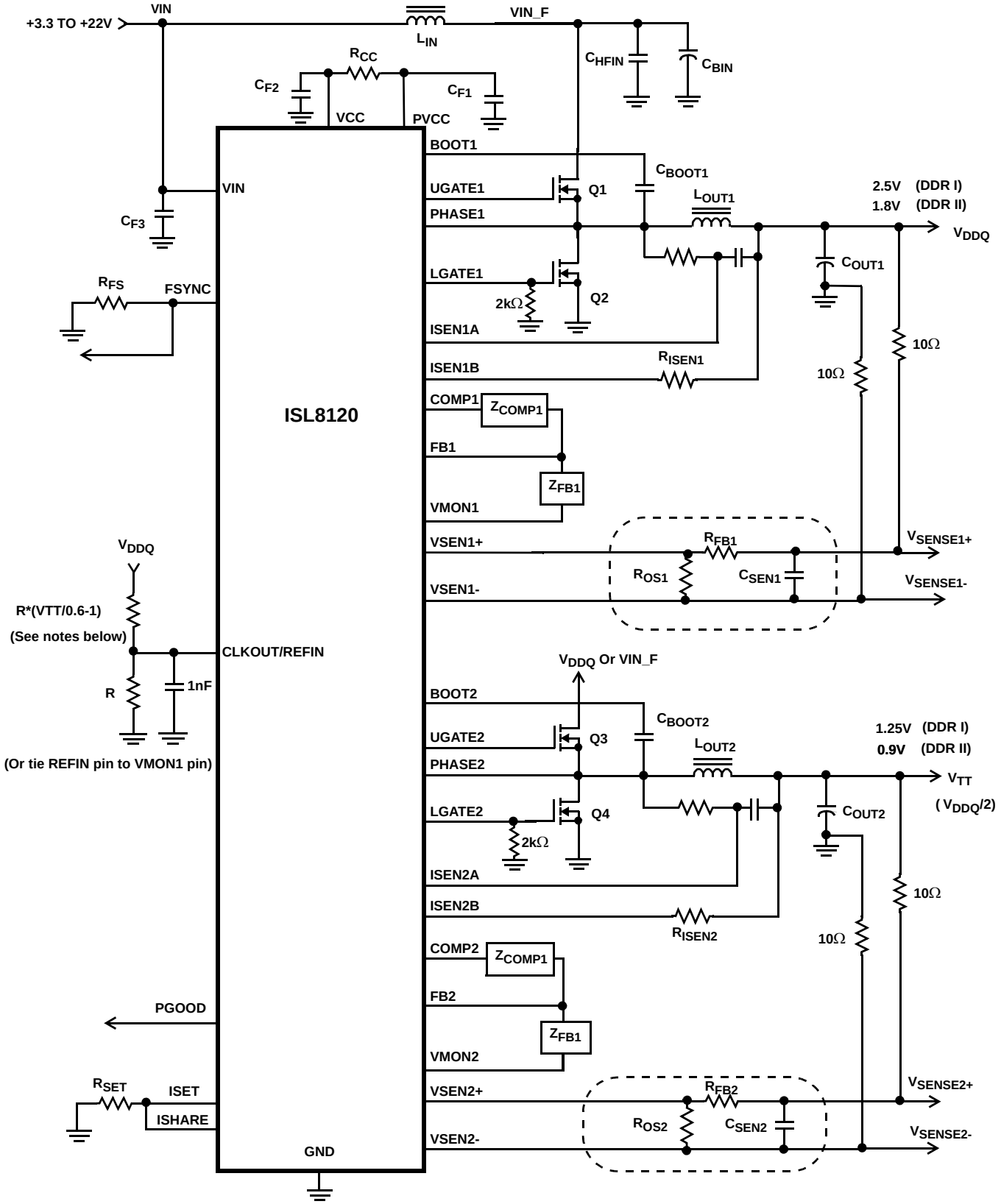


FIGURE 2. CHANNEL/PHASE 2 (VTT)

Typical Application I (Dual Regulators with DCR Sensing and Remote Sense)



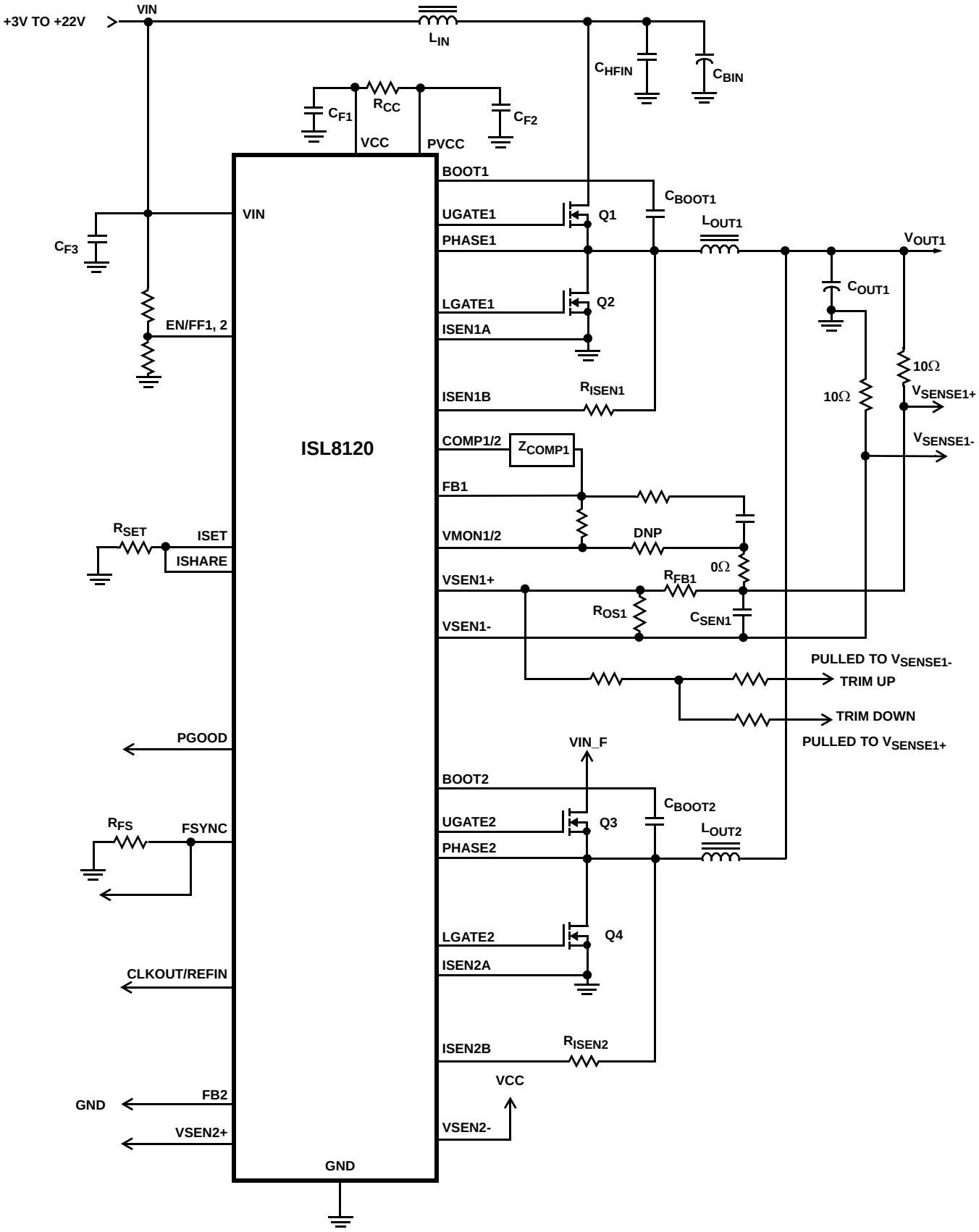
Typical Application II (Double Data Rate I or II)



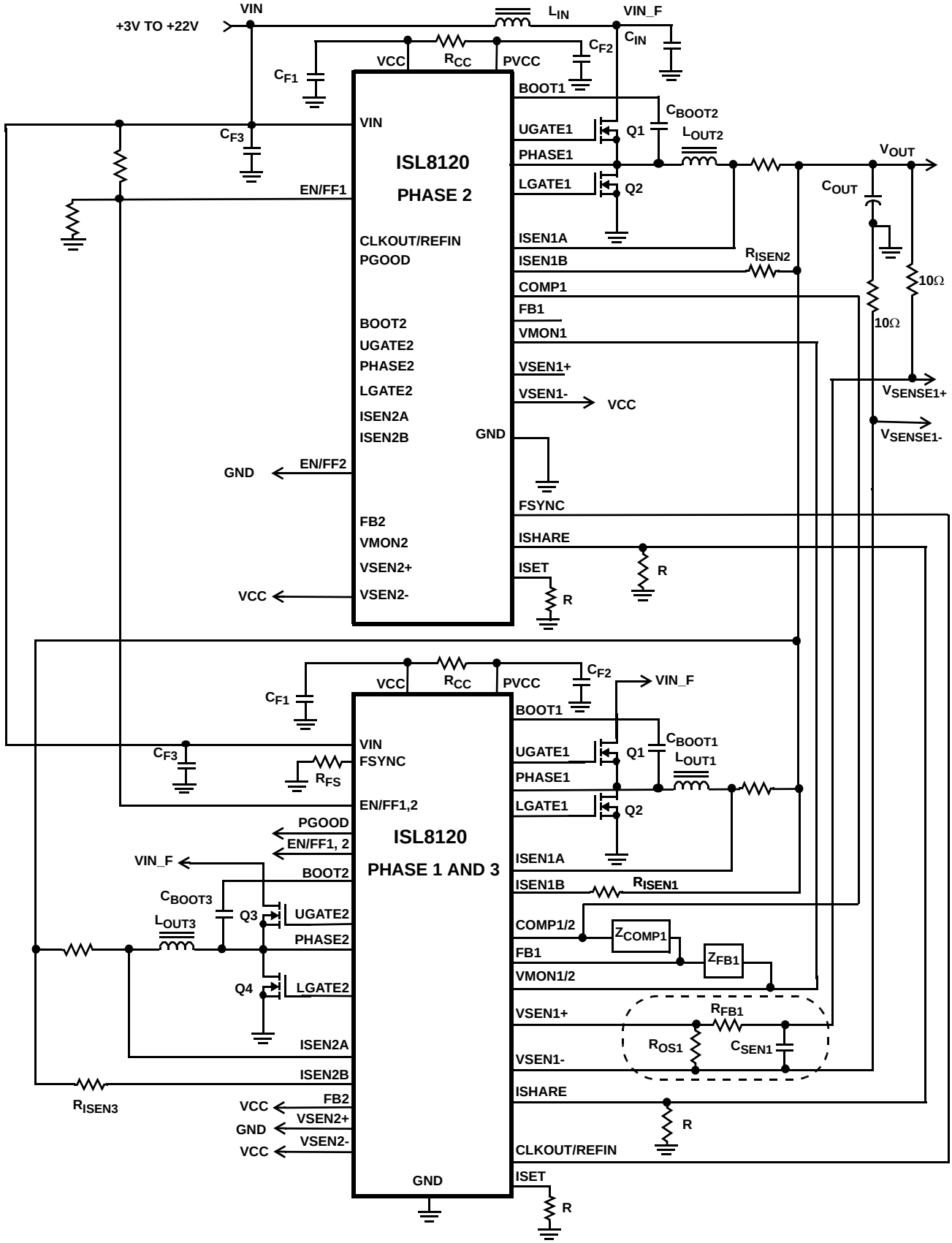
Note 1: Set the upper resistor to be a little higher than R*(VDDQ/0.6 - 1) will set the final REFIN voltage (stead state voltage after soft-start) derived from the VDDQ to be a little higher than internal 0.6V reference. In this way, the VTT final voltage will use the internal 0.6V reference after soft-start. The other way is to add more delay at EN/FF1 pin to have Channel 2 tracking VDDQ (check the DDR section for more details).

Note 2: Another way to set REFIN voltage is to connect VMON1 directly to REFIN pin.

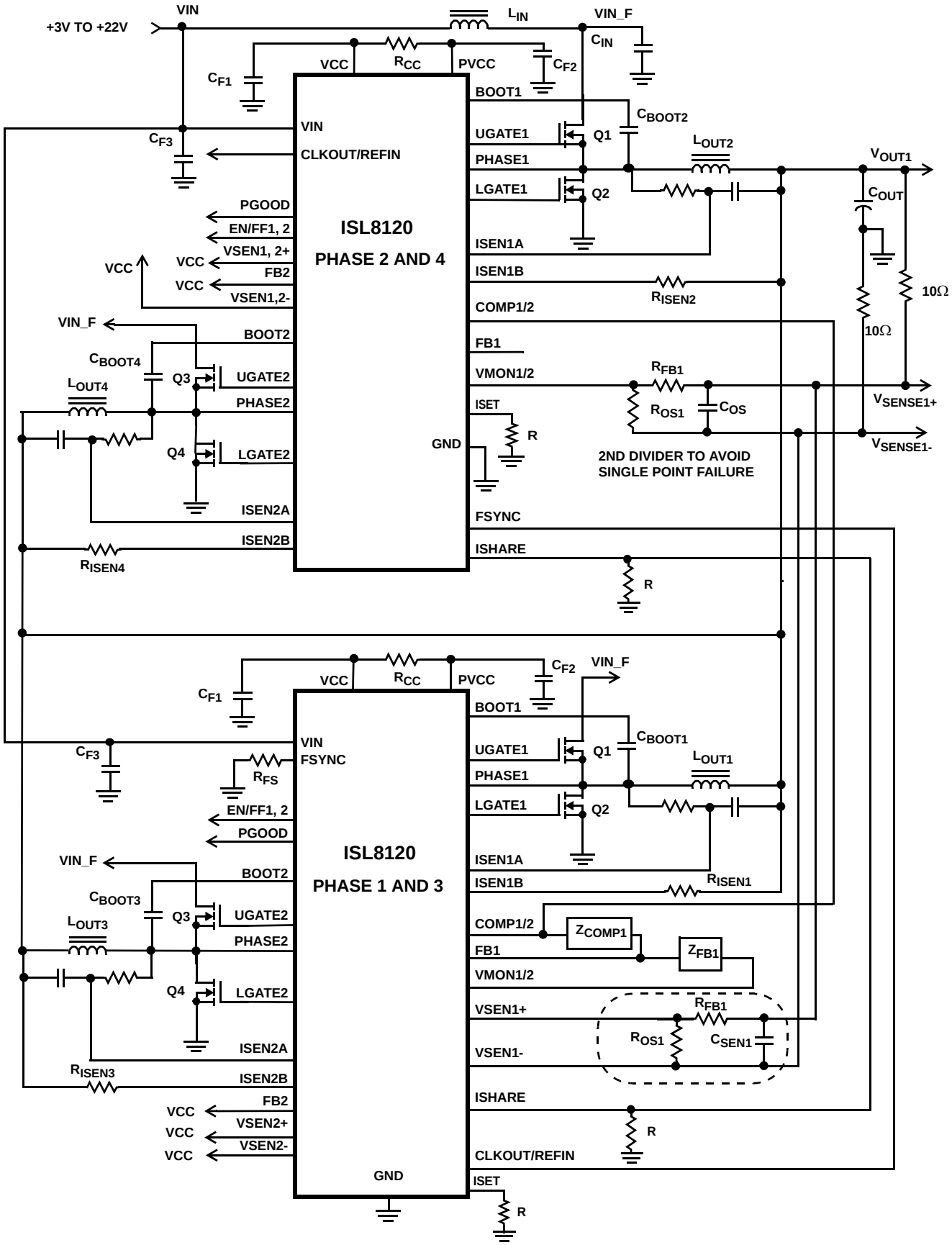
Typical Application III (2-Phase Operation with $r_{DS(ON)}$ Sensing and Voltage Trimming)



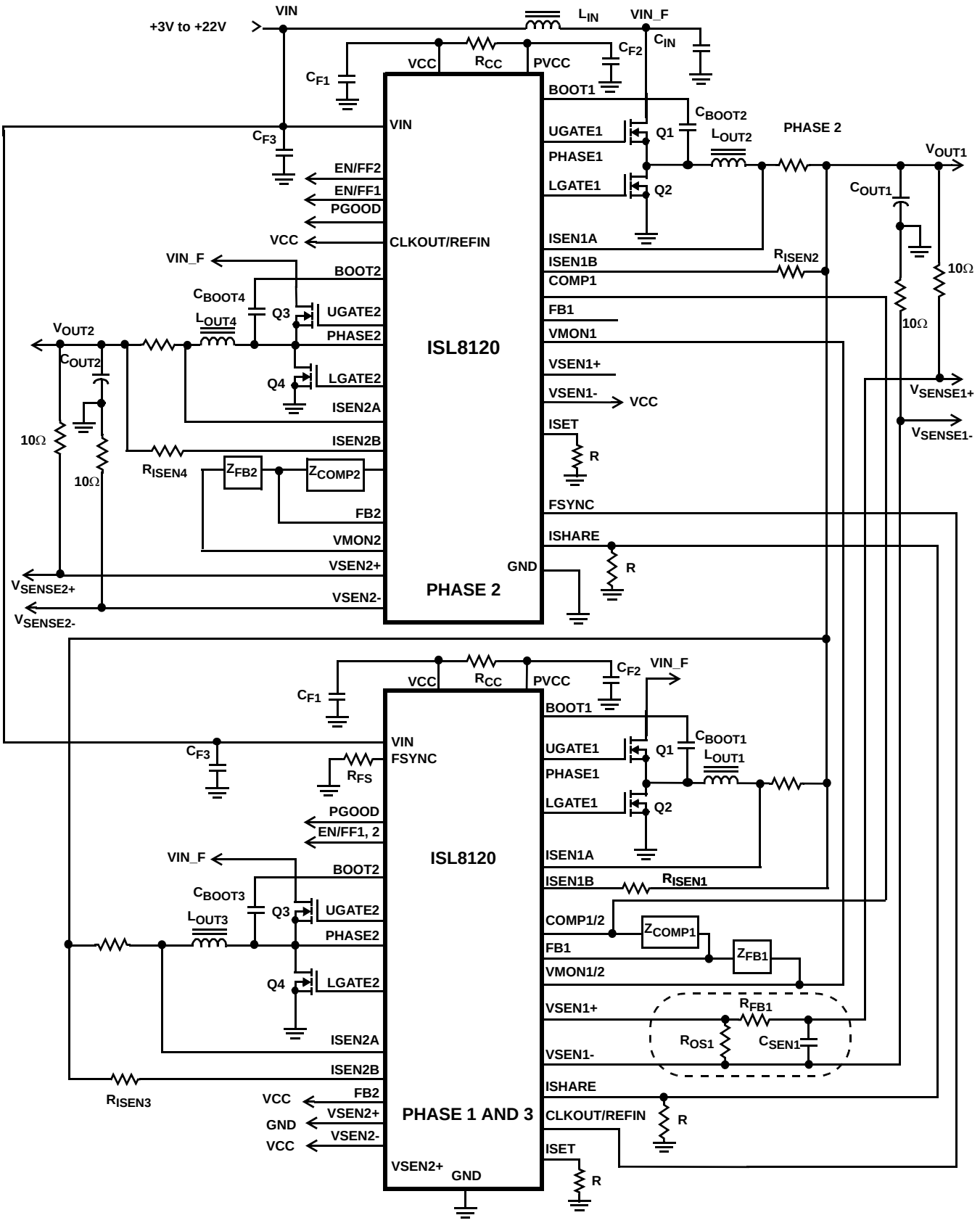
Typical Application IV (3-Phase Regulator with Precision Resistor Sensing)



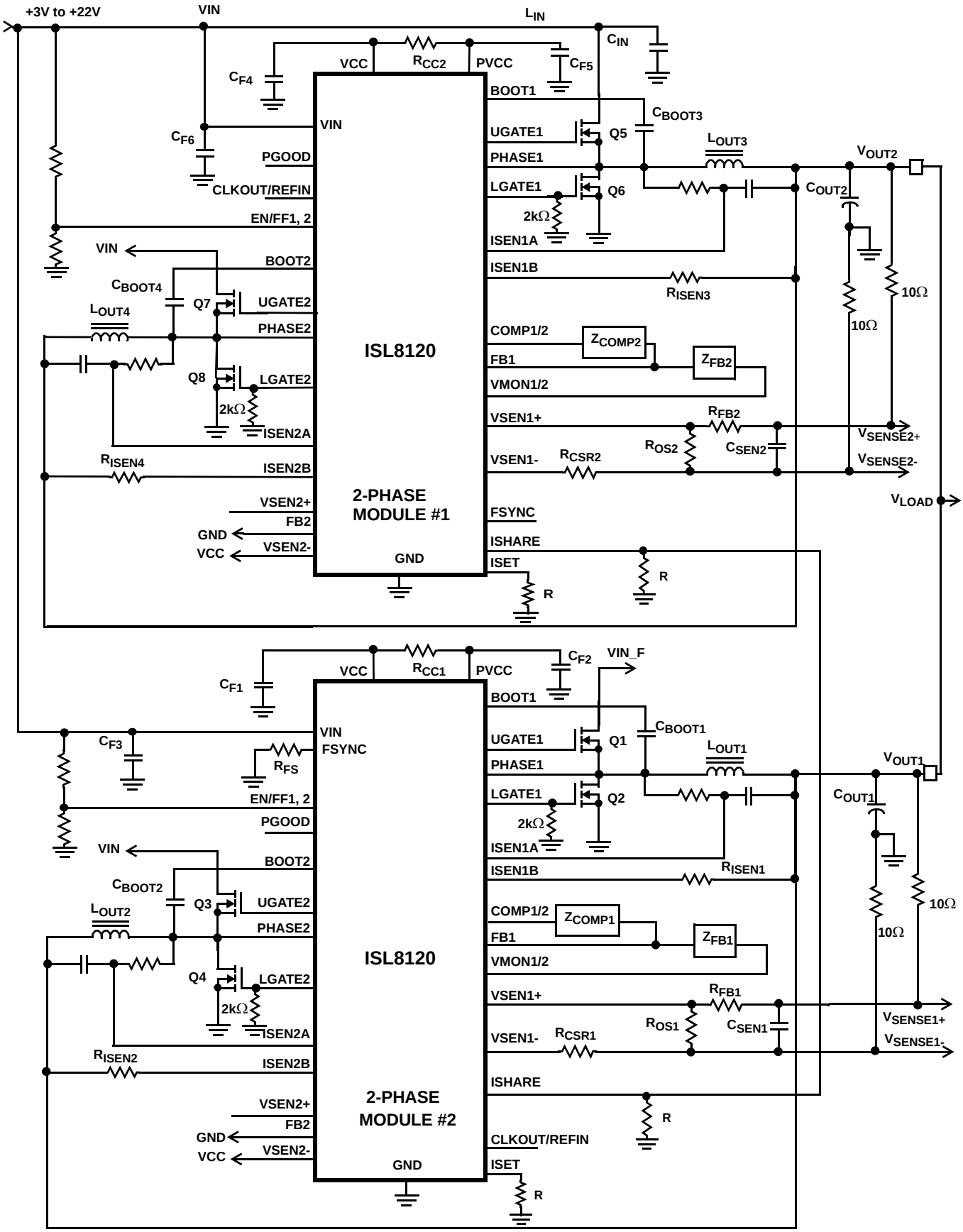
Typical Application V (4 Phase Operation with DCR Sensing)



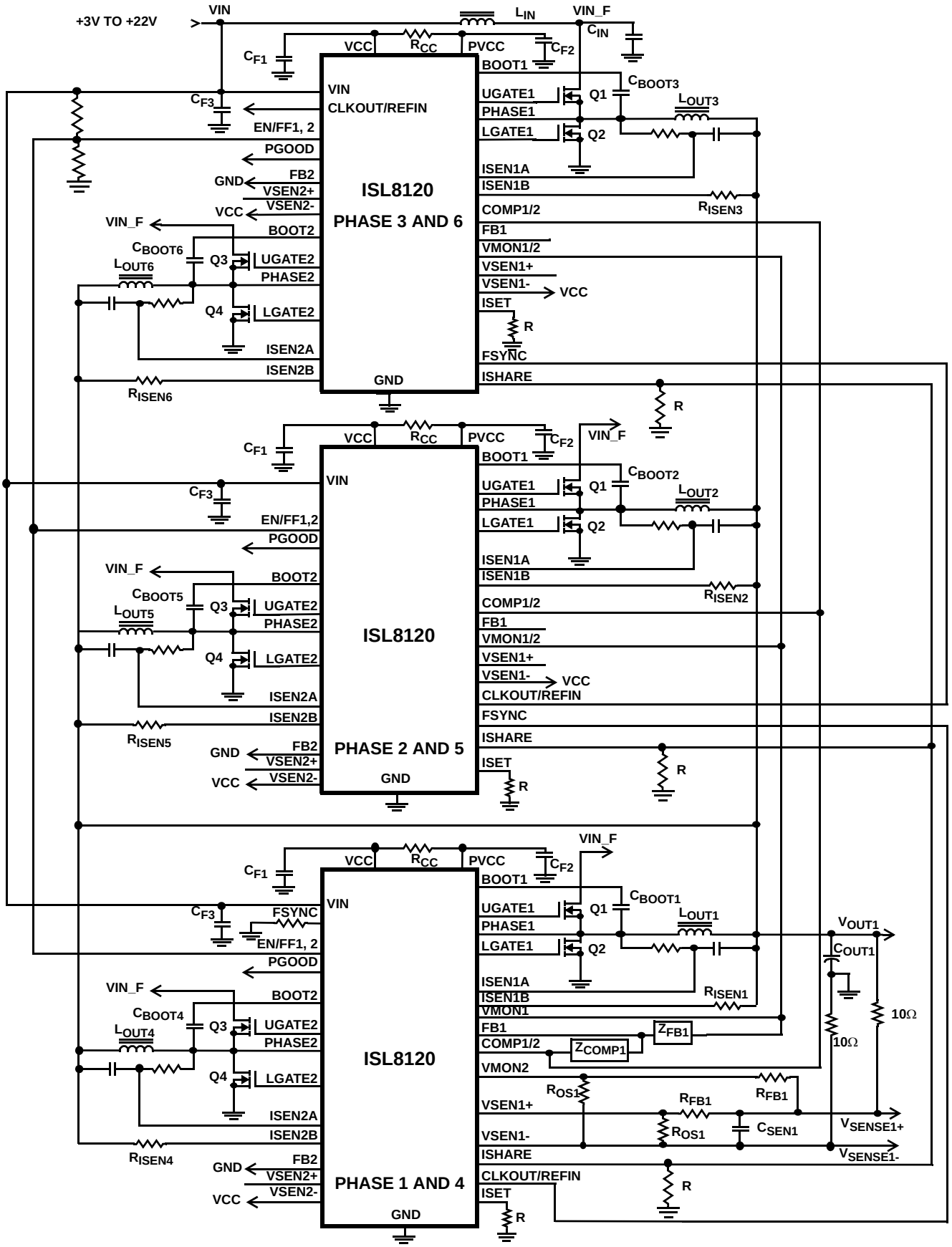
Typical Application VI (3-Phase Regulator with Resistor Sensing and 1 Phase Regulator)



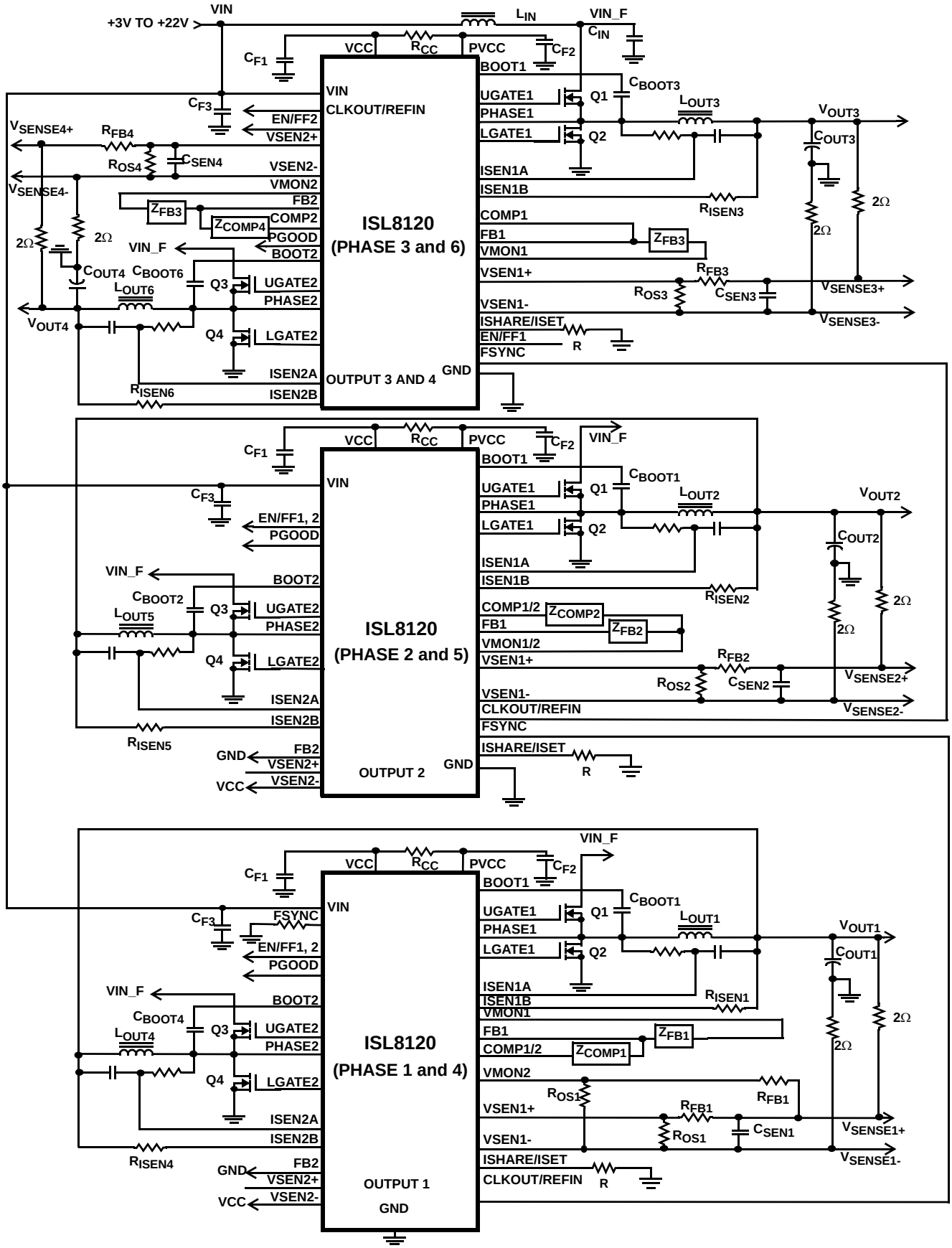
Typical Application VIII (Multiple Power Modules in Parallel with Current Sharing Control)



Typical Application VII (6 Phase Operation with DCR Sensing)



Typical Application VIIII (4 Outputs Operation with DCR Sensing)



Absolute Maximum Ratings

Input Voltage, VIN . . . . . -0.3V to +27V
Driver Bias Voltage, PVCC . . . . . -0.3V to +6.5V
Signal Bias Voltage, VCC . . . . . -0.3V to +6.5V
BOOT/UGATE Voltage, V_{BOOT} . . . . . -0.3V to +36V
Phase Voltage, V_{PHASE} . . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
BOOT to PHASE Voltage, V_{BOOT} - V_{PHASE} . . -0.3V to VCC +0.3V
Input, Output or I/O Voltage . . . . . -0.3V to VCC +0.3V

Recommended Operating Conditions

Input Voltage, VIN . . . . . 3V to 22V
Driver Bias Voltage, PVCC . . . . . 3V to 5.6V
Signal Bias Voltage, VCC . . . . . 3V to 5.6V
Boot to Phase Voltage (Overcharged), V_{BOOT} - V_{PHASE} . . . . . <6V
Commercial Ambient Temperature Range . . . . . 0°C to +70°C
Industrial Ambient Temperature Range . . . . . -40°C to +85°C
Maximum Junction Temperature Range . . . . . +125°C

Thermal Information

Thermal Resistance (Typical Notes 1, 2)	θ_{JA}(°C/W)	θ_{JC}(°C/W)
32 Ld QFN Package	32	3.5

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
VCC SUPPLY CURRENT						
Nominal Supply VIN Current	I_{Q_VIN}	VIN = 20V; VCC = PVCC; No Load; F_{SW} = 500kHz	11	15	20	mA
Nominal Supply VIN Current	I_{Q_VIN}	VIN = 3.3V;VCC = PVCC; No Load; F_{SW} = 500kHz	8	12	14	mA
Shutdown Supply PVCC Current	I_{PVCC}	EN = 0V, PVCC = 5V	0.5	1	1.4	mA
Shutdown Supply VCC Current	I_{VCC}	EN = 0V, VCC = 3V	7	10	12	mA
INTERNAL LINEAR REGULATOR						
Maximum Current (Note 3)	I_{PVCC}	PVCC = 4V TO 5.6V		250		mA
		PVCC = 3V TO 4V		150		mA
Saturated Equivalent Impedance (Note 3)	R_{LDO}	P-Channel MOSFET (VIN = 5V)		1		Ω
PVCC Voltage Level	PVCC	I_{PVCC} = 0mA to 250mA	5.1	5.4	5.6	V
POWER-ON RESET						
Rising VCC Threshold				2.85	2.97	V
Falling VCC Threshold				2.65	2.75	V
Rising PVCC Threshold		ISL8120CRZ		2.85	2.97	V
		ISL8120IRZ		2.85	3.05	
Falling PVCC Threshold				2.65	2.75	V
System Soft-start Delay (Note 3)	t_{SS_DLY}	After PLL, VCC, and PVCC PORs, and EN(s) above their thresholds		384		Cycles
ENABLE						
Turn-On Threshold Voltage			0.75	0.8	0.86	V
Hysteresis Sink Current	I_{EN_HYS}		25	30	35	µA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
Undervoltage Lockout Hysteresis (Note 3)	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.5		V
Sink Current	I_{EN_SINK}				15	mA
Sink Impedance	R_{EN_SINK}	I_{EN_SINK} = 5mA			65	Ω
OSCILLATOR						
Oscillator Frequency Range			150		1500	kHz
Oscillator Frequency		R_{FS} = 100k, Figure 21	344	377	406	kHz
Total Variation		VCC = 5V; -40°C < T_A <+85°C	-9		+9	%
Peak-to-Peak Ramp Amplitude	ΔV_{RAMP}	VCC = 5V, V_{EN} = 0.8V		1		V_{P-P}
Linear Gain of Ramp Over V_{EN}	G_{RAMP}	$G_{RAMP} = \Delta V_{RAMP}/V_{EN}$		1.25		
Ramp Peak Voltage	V_{RAMP_PEAK}	V_{EN} = VCC		VCC - 1.4		V
Peak-to-Peak Ramp Amplitude	ΔV_{RAMP}	V_{EN} = VCC = 5.4V, R_{UP} = 2k		3		V_{P-P}
Peak-to-Peak Ramp Amplitude	ΔV_{RAMP}	V_{EN} = VCC = 3V; R_{UP} = 2k		0.6		V_{P-P}
Ramp Amplitude Upon Disable	ΔV_{RAMP}	V_{EN} = 0V; VCC = 3.5V to 5.5V		1		V_{P-P}
Ramp Amplitude Upon Disable	ΔV_{RAMP}	V_{EN} = 0V; VCC < 3.4V		VCC - 2.4		V_{P-P}
Ramp DC Offset	V_{RAMP_OS}			1		V
FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP						
Synchronization Frequency		VCC = 5.4V (2.97V)	150		1500	kHz
PLL Locking Time		VCC = 5.4V (2.97V); F_{SW} = 400kHz;		105		µs
Input Signal Duty Cycle Range (Note 3)			10		90	%
PWM						
Minimum PWM OFF Time	t_{MIN_OFF}		310	345	410	ns
Current Sampling Blanking Time (Note 3)	$t_{BLANKING}$			175		ns
REFERENCE						
Channel 1 Reference Voltage (Include Error and Differential Amplifiers' Offsets)	V_{REF1}	ISL8120CRZ		0.6		V
			-0.6		0.6	%
		ISL8120IRZ		0.6		V
			-0.7		0.7	%
Channel 2 Reference Voltage (Include Error and Differential Amplifiers' Offsets)	V_{REF2}	ISL8120CRZ		0.6		V
			-0.75		0.75	%
		ISL8120IRZ		0.6		V
			-0.75		0.95	%
ERROR AMPLIFIER						
DC Gain (Note 3)		R_L = 10k, C_L = 100pF, at COMP Pin		98		dB
Unity Gain-Bandwidth (Note 3)	UGBW_EA	R_L = 10k, C_L = 100pF, at COMP Pin		80		MHz
Input Common Mode Range (Note 3)			-0.2		VCC - 1.8	V
Output Voltage Swing		VCC = 5V	0.85		VCC - 1.0	V
Slew Rate (Note 3)	SR_EA	R_L = 10k, C_L = 100pF, at COMP Pin		20		V/µs
Input Current (Note 3)	I_{FB}	Positive Direction Into the FB pin		100		nA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
Output Sink Current	I_{COMP}			3		mA
Output Source Current	I_{COMP}			6		mA
Disable Threshold (Note 3)	V_{VSEN-}			VCC - 0.4		V
DIFFERENTIAL AMPLIFIER						
DC Gain (Note 3)	UG_DA	Unity Gain Amplifier		0		dB
Unity Gain Bandwidth (Note 3)	UGBW_DA			5		MHz
Negative Input Source Current (Note 3)	I_{VSEN-}			100		nA
Maximum Source Current for Current Sharing (Typical Application VIII) (Note 3)	I_{VSEN1-}	VSEN1- Source Current for Current Sharing when parallel multiple modules each of which has its own voltage loop		350		µA
Input Impedance	$R_{VSEN+\_to\_VSEN-}$			1		MΩ
Output Voltage Swing (Note 3)			0		VCC - 1.8	V
Input Common Mode Range (Note 3)			-0.2		VCC - 1.8	V
Disable Threshold (Note 3)	V_{VSEN-}	$V_{MON1, 2}$ = Tri-State		VCC - 0.4		V
GATE DRIVERS						
Upper Drive Source Resistance	R_{UGATE}	45mA Source Current		1.0		Ω
Upper Drive Sink Resistance	R_{UGATE}	45mA Sink Current		1.0		Ω
Lower Drive Source Resistance	R_{LGATE}	45mA Source Current		1.0		Ω
Lower Drive Sink Resistance	R_{LGATE}	45mA Sink Current		0.4		Ω
OVERCURRENT PROTECTION						
Channel Overcurrent Limit (Note 3)	I_{SOURCE}	VCC = 2.97V to 5.6V		108		µA
Channel Overcurrent Limit	I_{SOURCE}	VCC = 5V; ISL8120CRZ	94	108	122	µA
		VCC = 5V; ISL8120IRZ	89	108	122	µA
Share Pin OC Threshold	V_{OC_SET}	VCC = 2.97V to 5.6V (comparator offset included)	1.16	1.20	1.22	V
Share Pin OC Hysteresis (Note 3)	$V_{OC\_SET\_HYS}$	VCC = 2.97V to 5.6V (comparator offset included)		50		mV
CURRENT SHARE						
Internal Balance Accuracy (Note 3)		VCC = 2.97V and 3.6V, 1% Resistor Sense, 10mV Signal		±5		%
Internal Balance Accuracy (Note 3)		VCC = 4.5V and 5.6V, 1% Resistor Sense, 10mV Signal		±5		%
External Current Share Accuracy (Note 3)		VCC = 2.97V and 5.6V, 1% Resistor Sense, 10mV Signal		±5		%
POWER GOOD MONITOR						
Undervoltage Falling Trip Point	V_{UVF}	Percentage Below Reference Point	-15	-13	-11	%
Undervoltage Rising Hysteresis	V_{UVR_HYS}	Percentage Above UV Trip Point		4		%
Overvoltage Rising Trip Point	V_{OVR}	Percentage Above Reference Point	11	13	15	%
Overvoltage Falling Hysteresis	V_{OVF_HYS}	Percentage below OV Trip Point		4		%
PGOOD Low Output Voltage		I_{PGOOD} = 2mA			0.35	V
Sinking Impedance		I_{PGOOD} = 2mA			70	Ω

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
Maximum Sinking Current (Note 3)		V_{PGOOD} <0.8V		10		mA
OVERVOLTAGE PROTECTION						
OV Latching Up Trip Point		EN/FF= UGATE = LATCH Low, LGATE = High	118	120	122	%
OV Non-Latching Up Trip Point (Note 3)		EN/FF = Low, UGATE = Low, LGATE = High		113		%
LGATE Release Trip Point		EN/FF = Low/HIGH, UGATE = Low, LGATE = Low		87		%
OVER-TEMPERATURE PROTECTION						
Over-Temperature Trip (Note 3)				150		°C
Over-Temperature Release Threshold (Note 3)				125		°C

NOTES:

3. Limits should be considered typical and are not production tested
4. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Functional Pin Descriptions

GND (Pin 33)

The bottom pad is the signal and power ground plane. All voltage levels are referenced to this pad. This pad provides a return path for the low-side MOSFET drives and internal power circuitries as well as all analog signals. Connect this pad to the circuit ground with the shortest possible path (more than 5 to 6 vias to the internal ground plane, placed on the soldering pad are recommended).

VIN (Pin 16)

This pin is the input of the internal linear regulator. It should be tied directly to the input rail. When used with an external 5V supply, this pin should be tied directly to PVCC. The internal linear device is protected against reverse bias generated by the remaining charge of the decoupling capacitor at PVCC when losing the input rail.

VCC (Pin 26)

This pin provides bias power for the analog circuitry. An RC filter is recommended between the connection of this pin to a 3V to 5.6V bias (typically PVCC). R is suggested to be a 5Ω resistor. And in 3.3V applications, the R could be shorted to allow the low end input in concerns of the VCC falling threshold. The VCC decoupling capacitor C is strongly recommended to be as large as a 10µF ceramic capacitor. This pin can be powered either by the internal linear regulator or by an external voltage source.

BOOT1, 2 (Pins 25, 17)

This pin provides the bootstrap bias for the high-side driver. Internal bootstrap diodes connected to the PVCC pin provide the necessary bootstrap charge. Its typical operational voltage range is 2.5V to 5.6V.

UGATE1, UGATE2 (Pin 24, 18)

These pins provide the drive for the high-side devices and should be connected to the MOSFETs' gates.

PHASE1, PHASE2 (Pins 23,19)

Connect these pins to the source of the high-side MOSFETs and the drain of the low-side MOSFETs. These pins represent the return path for the high-side gate drives.

PVCC (Pin 21)

This pin is the output of the internal series linear regulator. It provides the bias for both low-side and high-side drives. Its operational voltage range is 3V to 5.6V. The decoupling ceramic capacitor in the PVCC pin is 10µF.

LGATE1, LGATE2 (Pins 22, 20)

These pins provide the drive for the low-side devices and should be connected to the MOSFETs' gates.

FSYNC (Pin 5)

The oscillator switching frequency is adjusted by placing a resistor (R_{FS}) from this pin to GND. The internal oscillator will lock to an external frequency source if this pin is connected to a switching square pulse waveform, typically the CLKOUT input signal from another ISL8120 or an external clock. The internal oscillator synchronizes with the leading edge of the input signal.

EN/FF1, EN/FF2 (Pins 4, 6)

These pins have triple functions. The voltage on EN/FF_ pin is compared with a precision 0.8V threshold for system enable to initiate soft-start. With a voltage lower than the threshold, the corresponding channel can be disabled independently. By connecting these pins to the input rail through a voltage resistor divider, the input voltage can be monitored for UVLO (undervoltage lockout) function. The undervoltage lockout and its hysteresis levels can be programmed by these resistor dividers. The voltages on these pins are also fed into the controller to adjust the sawtooth amplitude of each channel independently to realize the feed-forward function.

Furthermore, during fault (such as overvoltage, overcurrent, and over-temperature) conditions, these pins (EN/FF_) are pulled low to communicate the information to other cascaded ICs.

PGOOD (Pin 8)

Provides an open drain Power-Good signal when both channels are within 9% of the nominal output regulation point with 4% hysteresis (13%/9%) and soft-start complete. PGOOD monitors the outputs (VMON1/2) of the internal differential amplifiers.

ISEN1A, ISEN2A (Pins 27, 15)

These pins are the non-inverting (+) inputs of the current sensing amplifiers to provide $r_{DS(ON)}$, DCR, or precision resistor current sensing together with the ISEN1B, ISEN2B pins.

ISEN1B, ISEN2B (Pins 28, 14)

These pins are the inverting (-) inputs of the current sensing amplifiers to provide rDS(ON), DCR, or precision resistor current sensing together with the ISEN1A, ISEN2A pins. Refer to "Typical Application III (2-Phase Operation with $r_{DS(ON)}$ Sensing and Voltage Trimming)" on page 7 for $r_{DS(ON)}$ sensing set up and "Typical Application V (4 Phase Operation with DCR Sensing)" on page 9 for DCR sensing set up.

ISET (Pin 2)

This pin sources a 15µA offset current plus the average current of both channels in multiphase mode or only Channel 1's current in independent mode. The voltage (V_{ISET}) set by an external resistor (R_{ISET}) represents the average current level of the local active channel(s).

ISHARE (Pin 3)

This pin is used for current sharing purposes and is configured to current share bus representing all modules'

average current. It sources 15µA offset current plus the average current of both channels in multiphase mode or Channel 1's current in independent mode. The share bus (ISHARE pins connected together) voltage (V_{ISHARE}) set by an external resistor (R_{ISHARE}) represents the average current level of all active channel(s). The ISHARE bus voltage compares with each reference voltage set by each R_{ISET} and generates current share error signal for current correction block of each cascaded controller. The share bus impedance R_{ISHARE} should be set as R_{ISET}/N_{CTRL} (R_{ISET} divided by number of active current sharing controllers). There is a 1.2V threshold for average overcurrent protection on this pin. V_{ISHARE} is compared with a 1.2V threshold for average overcurrent protections. For full-scale current, R_{ISHARE} should be 1.2V/123µA = ~10kΩ. Typically 10kΩ is used for $R_{SHARE\ and}$ R_{SET}.

CLKOUT/REFIN (Pin 7)

This pin has a dual function depending on the mode in which the chip is operating. It provides a clock signal to synchronize with other ISL8120(s) with its VSEN2- pulled within 700mV of VCC for multiphase (3-, 4-, 6-, 8-, 10-, or 12-phase) operation. When the VSEN2- pin is not within 700mV of VCC, ISL8120 is in dual mode (dual independent PWM output). The clockout signal of this pin is not available in this mode, but the ISL8120 can be synchronized to external clock. In dual mode, this pin works as the following two functions:

1. An external reference (0.6V target only) can be in place of the Channel 2's internal reference through this pin for DDR/tracking applications (see "Internal Reference and System Accuracy" on page 33).
2. The ISL8120 operates as a dual-PWM controller for two independent regulators with selectable phase degree shift, which is programmed by the voltage level on REFIN (see "DDR and Dual Mode Operation" on page 32).

FB1, FB2 (Pins 32, 10)

These pins are the inverting inputs of the error amplifiers. These pins should be connected to VMON1, 2 with the compensation feedback network. No direct connection between FB and VMON pins is allowed. With VSEN2- pulled within 700mV of VCC, the corresponding error amplifier is disabled and the amplifier's output is high impedance. FB2 is one of the two pins to determine the relative phase relationship between the internal clock of both channels and the CLKOUT signal. See "DDR and Dual Mode Operation" on page 32.

COMP1, COMP2 (Pins 1, 9)

These pins are the error amplifier outputs. They should be connected to FB1, FB2 pins through desired compensation networks when both channels are operating independently. When VSEN1-, VSEN2- are pulled within 700mV of VCC, the corresponding error amplifier is disabled and its output (COMP pin) is high impedance. Thus, in multiphase operations, all other SLAVE phases' COMP pins can tie to the MASTER phase's COMP1 pin (1^{st} phase), which modulates each phase's PWM pulse with a single voltage feedback loop. While the error amplifier is not disabled, an independent compensation network is required for each cascaded IC.

VSEN1+, VSEN2+ (Pins 29, 13)

These pins are the positive inputs of the standard unity gain operational amplifier for differential remote sense for the corresponding channel (Channels 1 and 2), and should be connected to the positive rail of the load/processor. These pins can also provide precision output voltage trimming capability by pulling a resistor from this pin to the positive rail of the load (trimming down) or the return (typical VSEN1-, VSEN2- pins) of the load (trimming up). The typical input impedance of VSEN+ with respect to VSEN- is 500kΩ. By setting the resistor divider connected from the output voltage to the input of the differential amplifier, the desired output voltage can be programmed. To minimize the system accuracy error introduced by the input impedance of the differential amplifier, a resistor below 1k is recommended to be used for the lower leg (R_{OS}) of the feedback resistor divider.

With VSEN2- pulled within 700mV of VCC, the corresponding error amplifier is disabled and VSEN2+ is one of the two pins to determine the relative phase relationship between the internal clock of both channels and the CLKOUT signal. See "DDR and Dual Mode Operation" on page 32 for details.

VSEN1-, VSEN2- (Pins 30, 12)

These pins are the negative inputs of standard unity gain operational amplifier for differential remote sense for the corresponding regulator (Channels 1and 2), and should be connected to the negative rail of the load/processor.

When VSEN1-, VSEN2- are pulled within 700mV of VCC, the corresponding error amplifier and differential amplifier are disabled and their outputs are high impedance. Both VSEN2+ and FB2 input signal levels determine the relative phases between the internal controllers as well as the CLKOUT signal. See "DDR and Dual Mode Operation" on page 32 for details.

When configured as multiple power modules (each module with independent voltage loop) operating in parallel, in order to implement the current sharing control, a resistor (100Ω typ) needs to be inserted between the VSEN1- pin and the output voltage negative sense point (between VSEN1- and lower voltage sense resistor), as shown in the "Typical Application VIII (Multiple Power Modules in Parallel with Current Sharing Control)" on page 11. This introduces a correction voltage for the modules with lower load current to keep the current distribution balanced among modules. The module with the highest load current will automatically become the master module. The recommended value for the

VSEN1- resistor is 100Ω and it should not be large in order to keep the unit gain amplifier input impedance compatibility.

VMON1, VMON2 (Pins 31, 11)

These pins are outputs of the unity gain amplifiers. They are connected internally to the OV/UV/PGOOD comparators. These pins should be connected to the FB1, FB2 pins by a standard feedback network when both channels are operating independently. When VSEN1-, VSEN2- are pulled within 700mV of VCC, the corresponding differential amplifier is disabled and its output (VMON pin) is high impedance. In such an event, the VMON pin can be used as an additional monitor of the output voltage with a resistor divider to protect the system against single point of failure, which occurs in the system using the same resistor divider for both of the UV/OV comparator and output voltage feedback.

Modes of Operation

There are 9 typical operation modes depending upon the signal levels on EN1/FF1, EN2/FF2, VSEN2+, VSEN2-, FB2, and CLKOUT/REFIN.

MODE 1: The IC is completely disabled when EN1/FF1 and EN2/FF2 are pulled below 0.8V.

MODE 2: With EN1/FF1 pulled low and EN2/FF2 pulled high (Mode 2A), or EN1/FF1 pulled high and EN2/FF2 pulled low (Mode 2B), the ISL8120 operates as a single phase regulator. The current sourcing out from the ISHARE pin represents the first channel current plus 15µA offset current.

MODE 3: When VSEN2- is used as a negative sense line, both channels' phase shift depends upon the voltage level of CLKOUT/REFIN. When the CLKOUT/REFIN pin is within 29% to 45% of VCC, Channel 2 delays 0° over Channel 1 (Mode 3A); when within 45% to 62% of VCC, 90°delay (Mode 3B); when greater than 62% to VCC, 180° delay (Mode 3C). Refer to the "DDR and Dual Mode Operation" on page 32.

MODE 4: When VSEN2- is used as a negative remote sense line, and CLKOUT/REFIN is connected to an external voltage ramp lower than the internal soft-start ramp and lower than 0.6V, the external ramp signal will replace Channel 2's internal soft-start ramp to be tracked at start-up, controller operating in DDR mode. The controller will use the lowest voltage among the internal 0.6V reference, the external voltage in CLKOUT/REFIN pin and the soft-start ramp signal. Channel 1 is delayed 60° behind Channel 2. Refer to the "DDR and Dual Mode Operation" on page 32.

MODE 5: With VSEN2- pulled within 700mV of VCC and FB2 pulled to ground, the internal channels are 180° out-of-phase and operate in 2-phase single output mode (5A). The CLKOUT/REFIN pin (rising edge) also signals out clock with 60° phase shift relative to the Channel 1's clock signal (falling edge of PWM) for 6-phase operation with two other ISL8120s (5B). When the share pins are not connected to each other for the three ICs in sync, two of which can operate in Mode 5A (3 independent outputs can be generated (Mode 5D)) and Modes 3 and 4 (to generate 4 independent outputs (Mode 5C)) respectively.

MODE 6: With VSEN2- pulled within 700mV of VCC, FB2 pulled high and VSEN2+ pulled low, the internal channels (as 1st and 3rd Phase, respectively) are 240° out-of-phase and operate in 3-phase single output mode, combined with another ISL8120 at MODE 2B. The CLKOUT/REFIN pin signals out 120° relative phases to the falling edge of Channel 1's clock signal to synchronize with the second ISL8120's Channel 1 (as 2nd Phase).

MODE 7: With VSEN2- pulled within 700mV of VCC and FB2 and VSEN2+ pulled high, the internal channel is 180° out-of-phase. The CLKOUT/REFIN pin (rising edge) signals out 90° relative phase to the Channel 1's clock signal (falling edge of PWM) to synchronize with another ISL8120, which can operate at Mode 3, 4, 5A, or 7A. A 4-phase single output converter can be constructed with two ISL8120s operating in Mode 5A or 7A (Mode 7A). If the share bus is not connected between ICs, each IC could generate an independent output (Mode 7B). When the second ISL8120 operates as two independent regulators (Mode 3) or in DDR mode (Mode 4), then a three independent output system is generated (Mode 7C). Both ICs can also be constructed as a 3-phase converter (0°, 90°, and 180°, not a equal phase shift for 3-phase) with a single phase regulator (270°).

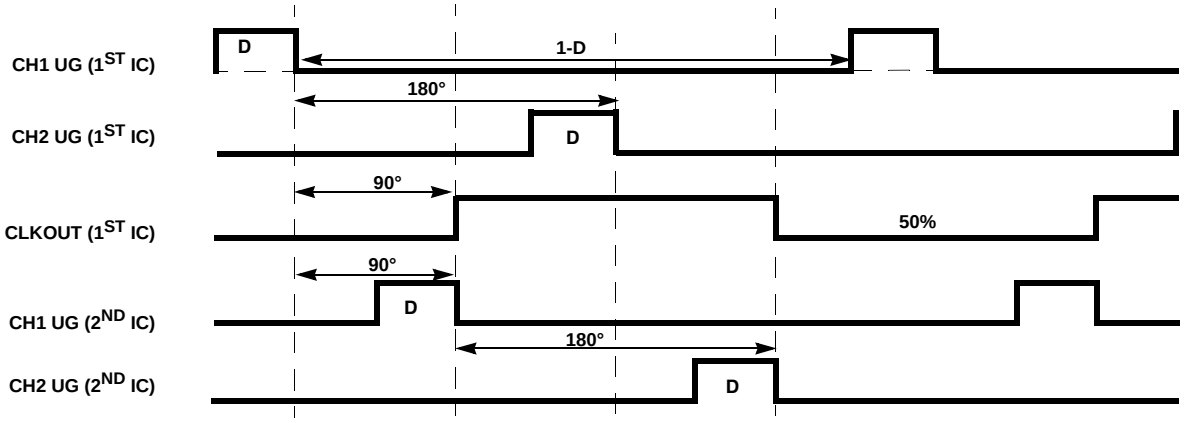
MODE 8: The output CLKOUT signal allows expansion for 12-phase operation with the cascaded sequencing, as shown in Table 1. No external clock is required in this mode for the desired phase shift.

MODE 9: With an external clock, the part can be expanded for 5, 7, 8, 9 10 and 11 phase single output operation with the desired phase shift.

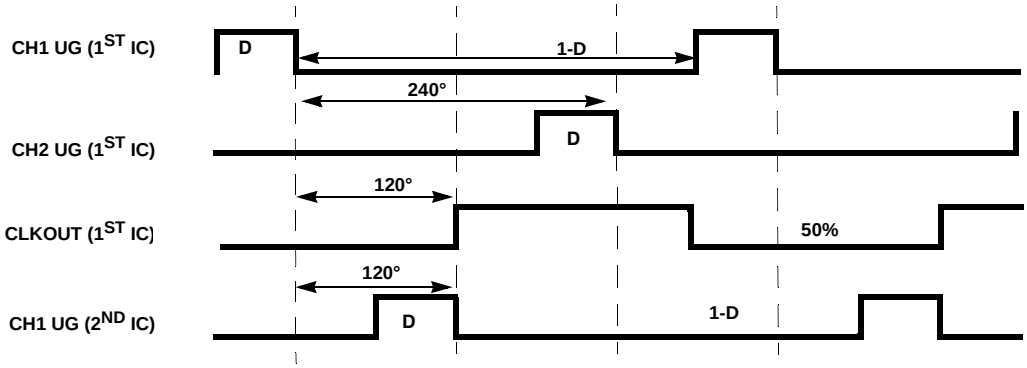
TABLE 1.

1ST IC (I = INPUT; O = OUTPUT; I/O = INPUT AND OUTPUT, Bi-DIRECTION)									MODES OF OPERATION		
MODE	EN1/ FF1 (I)	EN2/ FF2 (I)	VSEN2- (I)	FB2 (I)	VSEN2 + (I)	CLKOUT/REFIN WRT 1ST (I or O)	ISHARE (I/O) REPRESENTS WHICH CHANNEL(S) CURRENT	2ND CHANNEL WRT 1ST (O)*	OPERATION MODE of 2ND IC	OPERATION MODE of 3RD IC	OUTPUT (See Description for Details)
1	0	0	-	-	-	-	-	-	-	-	DISABLED
2A	0	1	ACTIVE	ACTIVE	ACTIVE	-	N/A	VMON1 = VMON2 to Keep PGOOD Valid	-	-	SINGLE PHASE
2B	1	0	-	-	-	-	1ST CHANNEL	VMON1 = VMON2 to Keep PGOOD Valid	-	-	SINGLE PHASE
3A	-	-	<VCC - 0.7V	ACTIVE	ACTIVE	29% to 45% of VCC (I)	1ST CHANNEL	0°	-	-	DUAL REGULATOR
3B	-	-	<VCC - 0.7V	ACTIVE	ACTIVE	45% to 62% of VCC (I)	1ST CHANNEL	90°	-	-	DUAL REGULATOR
3C	-	-	<VCC - 0.7V	ACTIVE	ACTIVE	> 62% of VCC (I)	1ST CHANNEL	180°	-	-	DUAL REGULATOR
4	-	-	<VCC- 0.7V	ACTIVE	ACTIVE	< 29% of VCC (I)	1ST CHANNEL	-60°	-	-	DDR MODE
5A	-	-	VCC	GND	-	60°	BOTH CHANNELS	180°	-	-	2-PHASE
5B	-	-	VCC	GND	-	60°	BOTH CHANNELS	180°	5A	5A or 7A	6-PHASE
5C	-	-	VCC	GND	-	60°	BOTH CHANNELS	180°	5A	5A or 7A	3 OUTPUTs
5D	-	-	VCC	GND	-	60°	BOTH CHANNELS	180°	5A	3 or 4	4 OUTPUTs
6	-	-	VCC	VCC	GND	120°	BOTH CHANNELS	240°	2B	-	3-PHASE
7A	-	-	VCC	VCC	VCC	90°	BOTH CHANNELS	180°	5A or 7A	-	4-PHASE
7B	-	-	VCC	VCC	VCC	90°	BOTH CHANNELS	180°	5A or 7A	-	2 OUTPUTs (1st IC in Mode 7A)
7C	-	-	VCC	VCC	VCC	90°	BOTH CHANNELS	180°	3, 4	-	3 OUTPUTs (1st IC in Mode 7A)
8	Cascaded IC Operation MODEs 5A+5A+7A+5A+5A+5A/7A, No External Clock Required										12-PHASE
9	External Clock or External Logic Circuits Required for Equal Phase Interval										5, 7, 8, 9, 10, 11, or (PHASE >12)

NOTE: "**2ND CHANNEL WRT 1ST**" is referred to as "channel 2 lag channel 1 by the degrees specified by the number in the corresponding table cells". For example, 90° with **2ND CHANNEL WRT 1ST** means channel 2 lags channel 1 by 90 degree; -60° with **2ND CHANNEL WRT 1ST** means channel 2 leads channel 1 by 60 degree.



4 PHASE TIMING DIAGRAM (MODE 7A)



CH2 UG(2ND IC, OFF, EN2/FF2 = 0)

3-PHASE TIMING DIAGRAM (MODE 6)

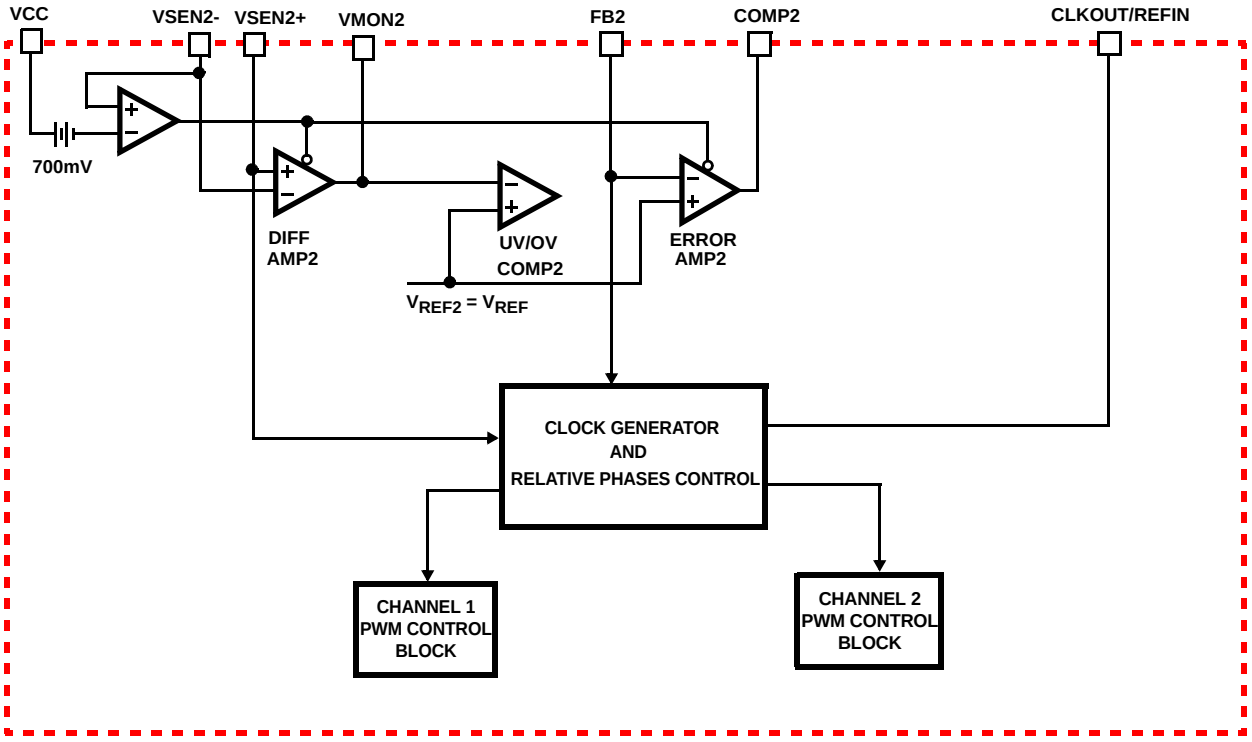


FIGURE 3. SIMPLIFIED RELATIVE PHASES CONTROL

Functional Description

Initialization

Initially, the ISL8120 Power-On Reset (POR) circuits continually monitor the bias voltages (PVCC and VCC) and the voltage at the EN pin. The POR function initiates soft-start operation 384 clock cycles after the EN pin voltage is pulled to be above 0.8V, all input supplies exceed their POR thresholds and the PLL locking time expires, as shown in Figure 4. The enable pin can be used as a voltage monitor and to set desired hysteresis with an internal 30µA sinking current going through an external resistor divider. The sinking current is disengaged after the system is enabled. This feature is especially designed for applications that require higher input rail POR for better undervoltage protection. For example, in 12V applications, R_{UP} = 53.6k and R_{DOWN} = 5.23k will set the turn-on threshold (V_{EN_RTH}) to 10.6V and turn-off threshold (V_{EN_FTH}) to 9V, with 1.6V hysteresis (V_{EN_HYS}).

During shutdown or fault conditions, the soft-start is reset quickly while UGATE and LGATE change states immediately (<100ns) upon the input drop below falling POR.

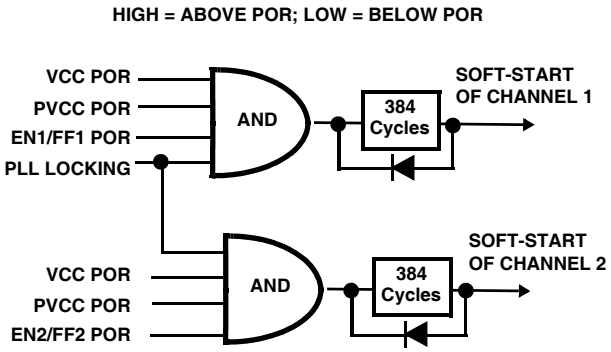


FIGURE 4. SOFT-START INITIALIZATION LOGIC

Voltage Feed-forward

Other than used as a voltage monitor described in the previous section, the voltages applied to the EN/FF pins are also fed to adjust the amplitude of each channel's individual sawtooth. The amplitude of each channel's sawtooth is set to 1.25 times the corresponding EN/FF voltage upon its enable (above 0.8V). This helps to maintain a constant gain ($G_M = VIN \cdot D_{MAX} / \Delta V_{RAMP}$) contributed by the modulator and the input voltage to achieve optimum loop response over a wide input voltage range. The sawtooth ramp offset voltage is 1V (equal to 0.8V*1.25), and the peak of the sawtooth is limited to VCC - 1.4V. With VCC = 5.4V, the ramp has a maximum peak-to-peak amplitude of VCC - 2.4V (equal to 3V); so the feed-forward voltage effective range is typically 3x as the ramp amplitude ranges from 1V to 3V.

A 384 cycle delay is added after the system reaches its rising POR and prior to the soft-start. The RC timing at the EN/FF pin should be sufficiently small to ensure that the input bus reaches its static state and the internal ramp circuitry stabilizes before soft-start. A large RC could cause the internal ramp amplitude not to synchronize with the input bus voltage during output start-up or when recovering from faults. It is recommended to use open drain or open collector to gate this pin for any system delay, as shown in Figure 5.

The multiphase system can immediately turn off all ICs under fault conditions of one or more phases by pulling all EN/FF pins low. Thus, no bouncing occurs among channels at fault and no single phase could carry all current and be over stressed.

$$R_{UP} = \frac{V_{EN\_HYS}}{I_{EN\_HYS}} \qquad R_{DOWN} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

$$\Delta V_{RAMP} = LIMIT(V_{CC\_FF} \times G_{RAMP}, VCC - 1.4V - V_{RAMP\_OFFSET})$$

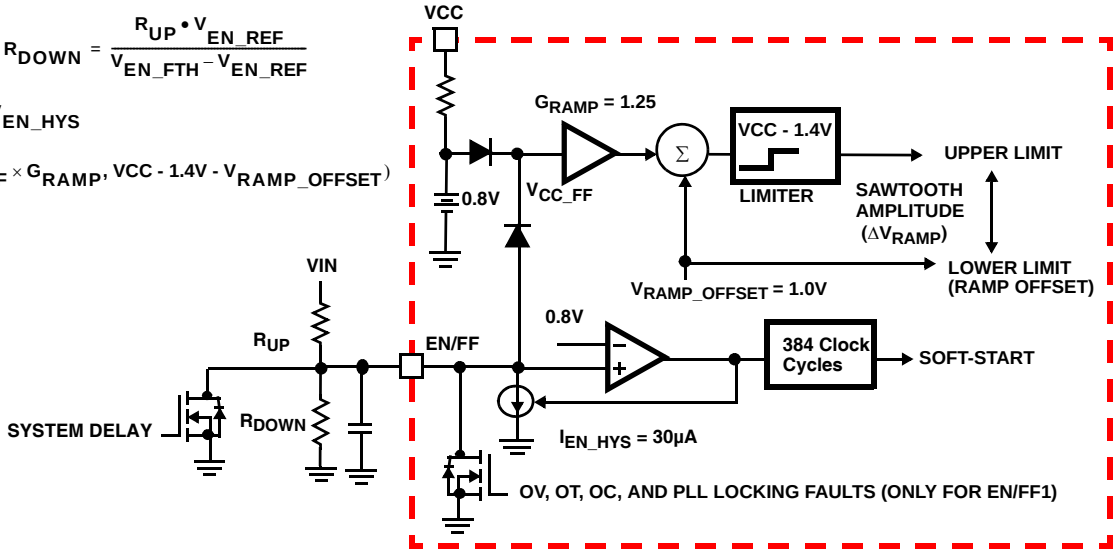


FIGURE 5. SIMPLIFIED ENABLE AND VOLTAGE FEEDFORWARD CIRCUIT

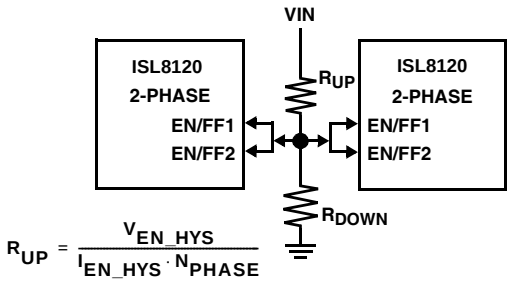


FIGURE 6. TYPICAL 4-PHASE WITH FAULT HANDSHAKE

While EN/FF is pulled to ground, a constant voltage (0.8V) is fed into the ramp generator to maintain a minimum peak-to-peak ramp.

Since the EN/FF pins are pulled down under fault conditions, the pull-up resistor (R_{UP}) should be scaled to sink no more than 5mA current from EN/FF pin. Essentially, the EN/FF pins cannot be directly connected to VCC.

Soft-start

The ISL8120 has two independent digital soft-start circuitry with fixed 1280 switching cycles. The soft-start time is inversely proportional to the switching frequency and is determined by the 1280-cycle digital counter. Refer to Figure 7. The full soft-start time from 0V to 0.6V can be estimated using Equation 1.

$$t_{SS} = \frac{1280}{f_{SW}} \quad \text{(EQ. 1)}$$

The ISL8120 has the ability to work under a pre-charged output (see Figure 8). The output voltage would not be yanked down during pre-charged start-up. If the pre-charged output voltage is greater than the final target level but prior to 113% setpoint, the switching will not start until the output voltage reduces to the target voltage and the first PWM pulse is generated (see Figure 9). The maximum allowable pre-charged level is 113%. If the pre-charged level is above 113% but below 120%, the output will hiccup between 113% (LGATE turns on) and 87% (LGATE turns off) while EN/FF is pulled low. If the pre-charged load voltage is above 120% of the targeted output voltage, then the controller will be latched off and not be able to power-up.

For above-target level pre-charged start-up, the output voltage would not change until the end of the soft-start. If the initial dip is below the UV level, the LGATE could be turned off. In such an event, the body-diode drop of the low-side FET will be sensed and could potentiality cause an OCP event for $r_{DS(ON)}$ current sensing applications.

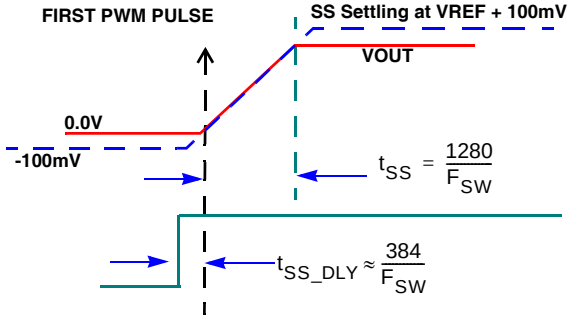


FIGURE 7. SOFT-START WITH VOUT = 0V

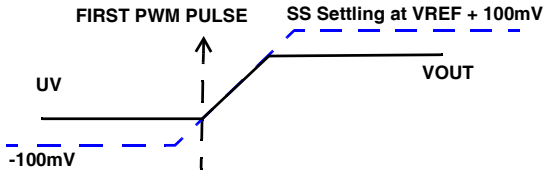


FIGURE 8. SOFT-START WITH VOUT = UV

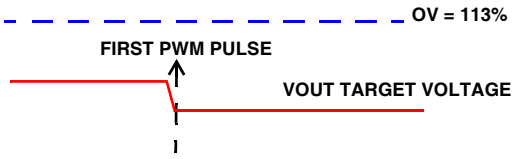


FIGURE 9. SOFT-START WITH VOUT BELOW OV BUT ABOVE FINAL TARGET VOLTAGE

Power-Good

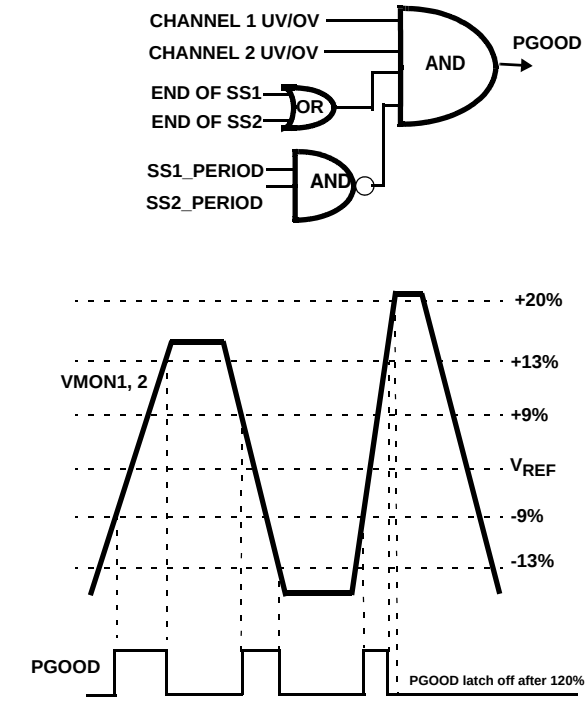


FIGURE 10. POWER-GOOD THRESHOLD WINDOW

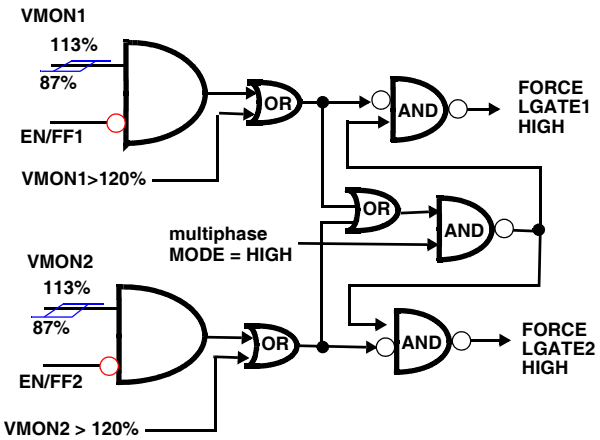


FIGURE 11. FORCE LGATE HIGH LOGIC

Both channels share the same PGOOD output. Either of the channels indicating out-of-regulation will pull-down the PGOOD pin. The Power-Good comparators monitor the voltage on the VMON pins. The trip points are shown in Figure 10. PGOOD will not be asserted until after the completion of the soft-start cycle of both channels. If Channels 1 or 2 are not used, the Power-Good can stay in operation by connecting 2 channels' VMON pins together. The PGOOD pulls low upon both EN/FF's disabling it if one of the VMON pins' voltage is out of the threshold window. PGOOD will not pull low until the fault presents for three consecutive clock cycles. In Dual/DDR application, if the turn-off channel pre-charges its VMON within the PGOOD threshold window, it could indicate Power-Good, however, the PGOOD signal can pull low with an external PNP or PMOS transistor via the EN/FF of the corresponding off channel.

Overvoltage and Undervoltage Protection

The Overvoltage (OV) and Undervoltage (UV) protection circuitry monitor the voltage on the VMON pins.

OV protection is active from the beginning of soft-start. An OV condition (>120%) would latch IC off (the high-side MOSFET to latch off permanently; the low-side MOSFET turns on immediately at the time of OV trip and then turns off permanently after the output voltage drops below 87%). The EN/FF and PGOOD are also latched low at OV event. The latch condition can be reset only by recycling VCC. In Dual/DDR mode, each channel is responsible for its own OV event with the corresponding VMON as the monitor. In multiphase mode, both channels respond simultaneously when either triggers an OV event.

There is another non-latch OV protection (113% of target level). At the condition of EN/FF low and the output over 113% OV, the lower side MOSFET will turn on until the output drops below 87%. This is to protect the overall power trains in case of only one channel of a multiphase system detecting OV. The low-side MOSFET always turns on at the conditions of EN/FF = LOW and the output voltage above 113% (all VMON pins and EN pins are tied together) and turns off after the output drops below 87%. Thus, in a high phase count application (Multiphase Mode), all cascaded ICs can latch off simultaneously via the EN pins (EN pins are tied together in multiphase mode), and each IC shares the same sink current to reduce the stress and eliminate the bouncing among phases.

The UV functionality is not enabled until the end of soft-start. In a UV event, if the output drops below -13% of the target level due to some reason (cases when EN/FF is not pulled low) other than OV, OC, OT, and PLL faults, the lower MOSFETs will turn off to avoid any negative voltage ringing.

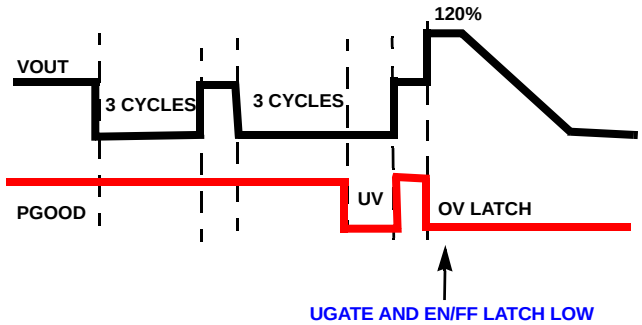


FIGURE 12. PGOOD TIMING UNDER UV AND OV

PRE-POR Overvoltage Protection (PRE-POR-OVP)

When both the VCC and PVCC are below PORs (not including EN POR), the UGATE is low and LGATE is floating (high impedance). EN/FF has no control on LGATE when below PORs. When above PORs, the LGATE would not be floating but toggling with its PWM pulses. An internal 10kΩ resistor, connected in between PHASE and LGATE nodes, implements the PRE-POR-OVP circuit. The output of the converter that is equal to phase node voltage via output inductors is then effectively clamped to the low-side MOSFET's gate threshold voltage, which provides some protection to the microprocessor if the upper MOSFET(s) is shorted during start-up, shutdown, or normal operations. For complete protection, the low-side MOSFET should have a gate threshold that is much smaller than the maximum voltage rating of the load.

The PRE-POR-OVP works against pre-biased start-up when pre-charged output voltage is higher than the threshold of the low-side MOSFET, however, it can be disabled by placing a 2k resistor from LGATE to ground.

Over-Temperature Protection (OTP)

When the junction temperature of the IC is greater than +150°C (typically), both EN/FF pins pull low to inform other cascaded channels via their EN/FF pins. All connected EN/FFs stay low and release after the IC's junction temperature drops below +125°C (typically), with a +25°C hysteresis (typical).

Current Loop

When the ISL8120 operates in 2-phase mode, the current control loop keeps the channel's current in balance. After 175ns blanking period with respect to the falling edge of the PWM pulse of each channel, the voltage developed across the DCR of the inductor, $r_{DS(ON)}$ of the low-side MOSFETs, or a precision resistor, is filtered and sampled for 175ns. The current (I_{CS1}/I_{CS2}) is scaled by the R_{ISEN} resistor and provides feedback proportional to the average output current of each channel.

For DCR sensing, the sampling current ICS can be derived from Equation 2:

$$ICS = \frac{\left(IL + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet DCR}{RISEN} \quad \text{(EQ. 2)}$$

where IL is the inductor DC current, DCR is its DC resistance, and t_{MIN_OFF} is 350ns.

For low-side MOSFET $r_{DS(ON)}$ sensing, the ICS can be derived from Equation 3:

$$ICS = \frac{\left(IL + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet r_{DS(ON)}}{RISEN} \quad \text{(EQ. 3)}$$

In multiphase mode (VSEN2- pulled high), the scaled output currents from both active channels are combined to create an average current reference (IAVG) which represents average current of both channel outputs as calculated in Equation 4.

$$IAVG = \frac{ICS1 + ICS2}{2} \quad \text{(EQ. 4)}$$

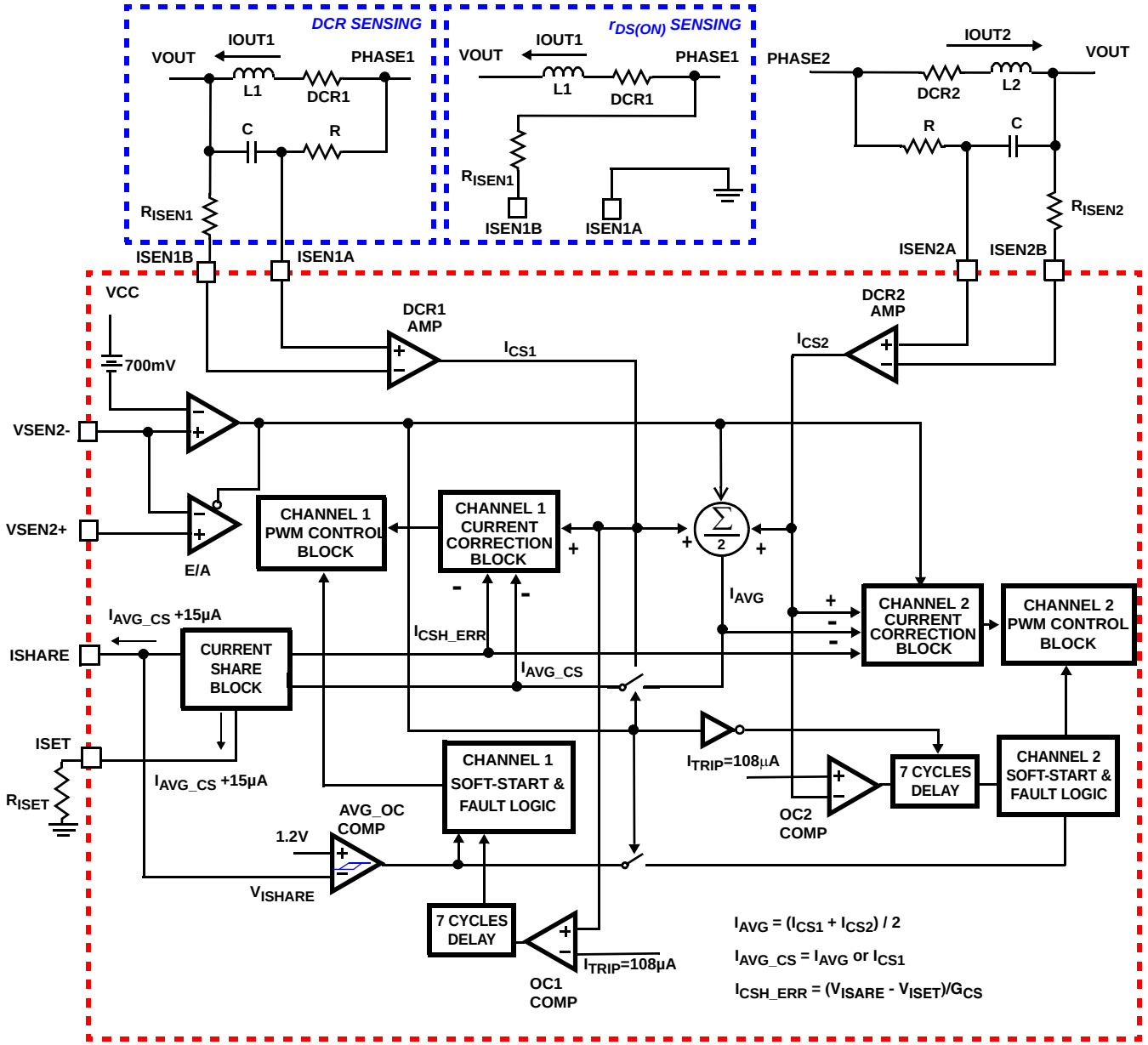


FIGURE 13. SIMPLIFIED CURRENT SAMPLING AND OVERCURRENT PROTECTION

The signal I_{AVG} is then subtracted from the individual channel's scaled current (I_{CS1} or I_{CS2}) to produce a current correction signal for each channel. The current correction signal keeps each channel's output current contribution balanced relative to the other active channel.

For multiphase operation, the share bus (V_{ISHARE}) represents the average current of all active channels and compares with each IC's average current (I_{AVG_CS} equals to I_{AVG} or I_{CS1} depending upon the configuration, represented by V_{ISET}) to generate current share error signal (I_{CS_ERR}) for each individual channel. Each current correction signal is then subtracted from the error amplifier output and fed to the individual channel PWM circuits.

When both channels operate independently, the average function is disabled and generates zero average current (I_{AVG} = 0), and the current correction block of Channel 2 is also disabled. The I_{AVG_CS} is the Channel 1 current I_{CS1}. The Channel 1 makes any necessary current correction by comparing its channel current (represented by V_{ISET}) with the share bus (V_{ISHARE}). When the share bus does not connect to other ICs, the ISET and ISHARE pins can be shorted together and grounded via a single resistor to ensure zero share error.

Note that the common mode input voltage range of the current sense amplifiers is VCC - 1.8V. Therefore, the $r_{DS(ON)}$ sensing should be used for applications with output voltage greater than VCC - 1.8V. For example, an application of 3.3V output is suggested to use $r_{DS(ON)}$ sensing.

In addition, the R-C network components (for DCR sensing) are selected such that the RC time constant matches the inductor L/DCR time constant. Otherwise, it could cause undershoot/overshoot during load transient and start-up. C is typically set to 0.1µF or higher, while R is calculated with Equation 5.

$$R = \frac{L}{C \bullet DCR} \quad \text{(EQ. 5)}$$

Figure 13 shows a simple and flexible configuration for both $r_{DS(ON)}$ and DCR sensing.

Current Share Control in Multiphase Single Output

The I_{AVG_CS} is the average current of both channels (I_{AVG}, 2-phase mode) or only Channel 1 (I_{CS1}, any other modes). ISHARE and ISET pins source a copy of I_{AVG_CS} with 15µA offset, for example, the full-scale will be 123µA. If one single external resistor is used as R_{ISHARE} connecting the ISHARE bus to ground for all the ICs in parallel, R_{ISHARE} should be set equal to R_{ISET}/N_{CTRL} (where N_{CNTL} is the number of the ISL8120 controllers in parallel or multiphase operations), and the share bus voltage (V_{ISHARE}) set by the R_{ISHARE} represents the average current of all active channels. Another way to set R_{ISHARE} is to put one resistor in each IC' s ISHARE pin and use the same value with R_{ISET} (R_{ISHARE} = R_{ISET}), in which case the total equivalent resistance value is also R_{ISET}/N_{CTRL}. The voltage (V_{ISET}) set by R_{ISET} represents the average current of the corresponding device and compared with the share bus (V_{ISHARE}). The current share error signal (I_{CSH_ERR}) is then fed into the current correction block to adjust each channel's PWM pulse accordingly.

The current share function provides at least 10% overall accuracy between ICs, 5% within the IC when using a 1% resistor to sense a 10mV signal. The current share bus works for up to 12-phase.

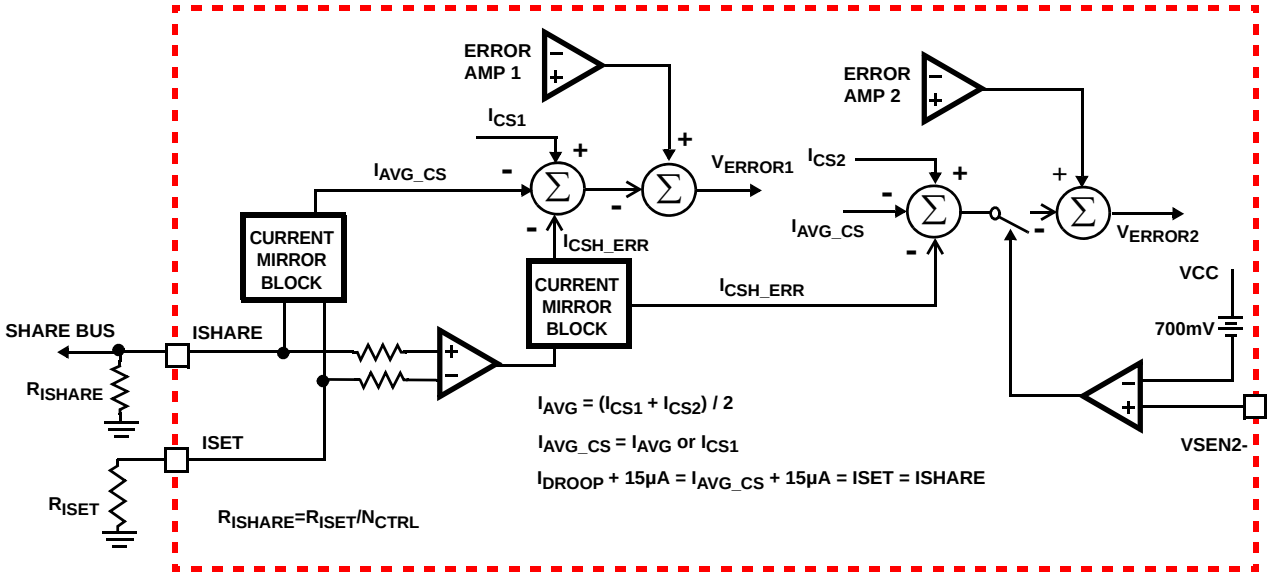


FIGURE 14. SIMPLIFIED CURRENT SHARE AND INTERNAL BALANCE IMPLEMENTATION

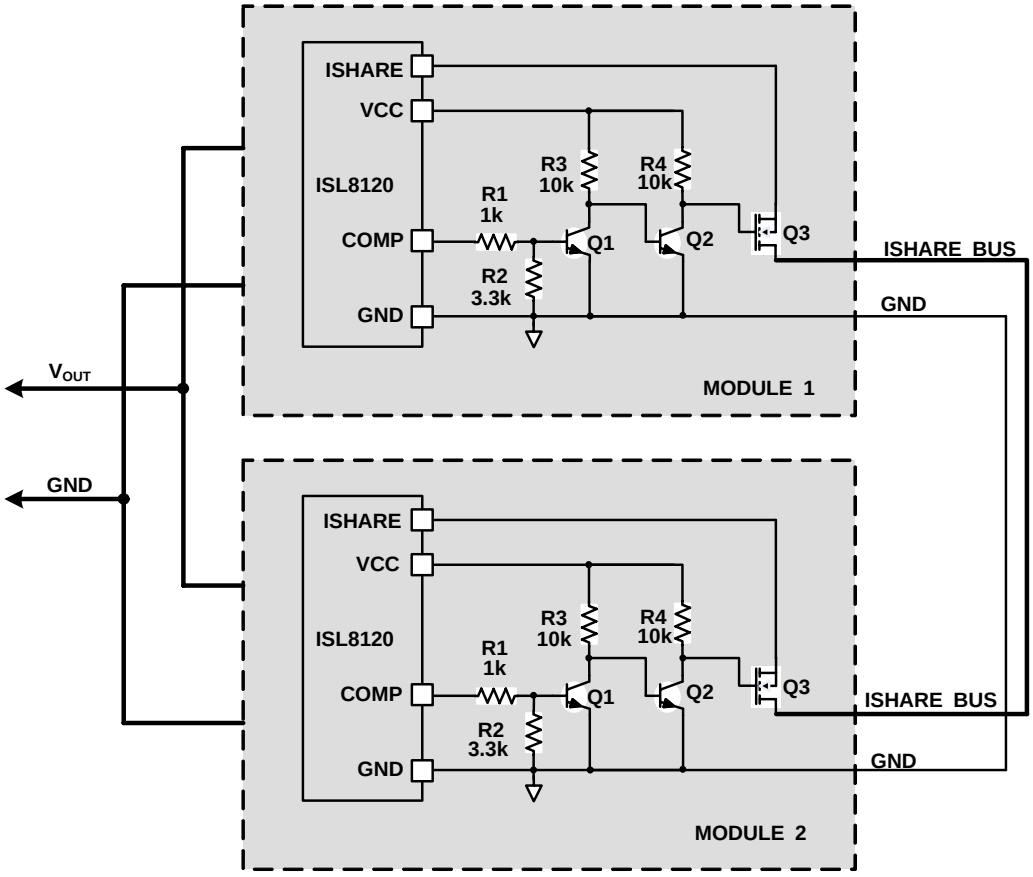
For multiphase implementation, one single error amplifier should be used for the voltage loop. Therefore, all other channels' error amplifiers should be disabled with their corresponding VSEN- pulled to VCC, as shown in Figure 16.

Current Share Control Loop in Multi-Module with Independent Voltage Loop

The power module controlled by ISL8120 with its own voltage loop can be paralleled to supply one common output load with its integrated Master-Slave current sharing control, as shown in "Typical Application VIII (Multiple Power Modules in Parallel with Current Sharing Control)" on page 11. A resistor R_{CSR} needs to be inserted between VSEN1- pin and the lower resistor of the voltage sense resistor divider for each module. With this resistor, the correction current sourcing from VSEN1- pin will create a voltage offset to maintain even current sharing among modules. The recommended value for the VSEN1- resistor R_{CSR} is 100Ω and it should not be large in order to keep the unity gain amplifier input pin impedance compatibility. The maximum source current from VSEN1- pin is 350µA, which is combined with R_{CSR} to determine the current sharing regulation range. The generated correction voltage on R_{CSR} is suggested to be within 5% of VREF (0.6V) to avoid fault triggering of UV/OV and PGOOD during dynamic events.

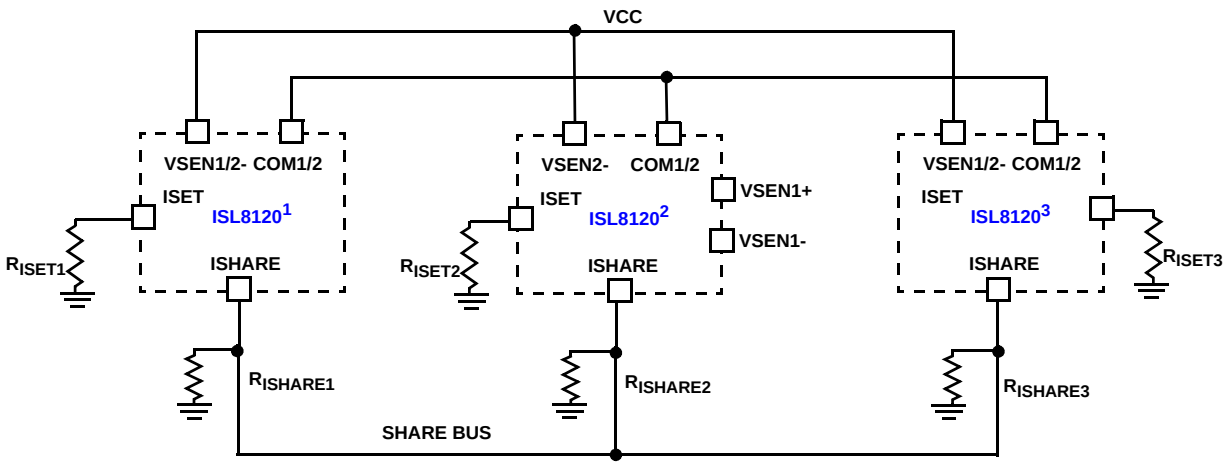
There are basically two options for the configuration of the communication wires between the modules. Each of option has its own unique features.

One option is to synchronize all the modules where the system has 3 analog signal communication wires (CLKOUT-SYNC, ISHARE, EN/FF). In this option, all the modules are synchronized and the phase shift can also be configured to optimal to reduce the input current ripple by interleaving effects. The connections of these three wires allows the system to be started at the same time and achieve good current balance in start-up without overcurrent trip. To have different phase shift, each module has different circuitry configuration to program the phase shift, thus to make only one standard module is difficult.



Q1: MMBT3904
Q2: MMBT3904
Q3: 2N7002

FIGURE 15. SINGLE COMMUNICATION WIRE CONNECTION



$R_{ISHARE\_} = R_{ISET\_}$

FIGURE 16. SIMPLIFIED 6-PHASE SINGLE OUTPUT IMPLEMENTATION

The second option for multi-module parallel system is to have only one signal (ISHARE) wire connection. The signal wire connection scheme is targeted for a N+1 system, where each module is a standard one that can be paralleled to build up power systems with different capacity, and each module can start-up at different time, and each module can be shut down and removed without the system shutdown. Figure 15 shows some extra circuits needed for such a parallel module system (each module with independant voltage feedback loop where only one analog signal (ISHARE) wire is connected between the module) besides the circuits shown in "Typical Application VIIII (4 Outputs Operation with DCR Sensing)" on page 13. The circuitry shown in Figure 15 is to ensure the successful start-up of the system with the individual module starting up at different time. With this circuitry, each module's local ISHARE signal is connected to the system share bus only when it starts switching (finishing of pre-biased start-up). In addition, when the module is shut off, its ISHARE signal will be removed from the ISHARE bus. The validated signal transistors shown in Figure 15 are: MMBT3904 for Q1 and Q2; 2N7002 for Q3.

With the circuits of Figure 15 implemented, the system can also be further implemented with the CLKOUT-SYNC connection to have the modules synchornized and phase-shifted, which is the third option of system configuration. However, the lose of CLKOUT signal will cause the shutdown of the other module receiving the signal. Compared with the second option (single wire (ISHARE) connection), this option has one more wire connection, but all the modules are synchronized and phase-shifted.

In summary, the communication wire connection in parallel systems offers flexibility. Each configuration option has its own unique features. The selection of the connections of the conmmunication wire should be based upon evaluation of the priorities of system requirements and features, such as reliability, number of wire connections, synchronizations and fault tolerance, etc.

In dual mode, the current sharing block for current sharing of modules with independant voltage loop is disabled.

Overcurrent Protection

The OCP function is enabled at start-up. When both channels operate independently, the average function is disabled and generates zero average current (IAVG = 0). The Channel 2 current (ICS2) is compared with ITRIP (108µA) as its own independent overcurrent protection and the 7 clock cycles delay is bypassed. The Channel 1's current (ICS1) plus 15µA offset forms a voltage (VISHARE) with an external resistor R_{ISHARE} and compares with a precision 1.2V threshold for OCP; while the 108µA OCP comparator with 7-cycle delay is also activated.

In multiphase operation, the VISHARE represents the average current of all active channels and compares with the ISHARE pin precision 1.2V threshold to determine the overcurrent condition. At the same time, each channel has additional overcurrent trip point at 108µA with 7-cycle delay for phase overcurrent protection. This scheme helps protect against loss of channel(s) in multi-phase mode so that no single channel could carry more than 108µA in such event. See Figure 13. Note that it is not necessary for the R_{ISHARE} to be scaled to trip at the same level as the 108µA OCP comparator if the application allows. Typically the ISHARE pin average current protection level should be higher than the phase current protection level. For instance, when Channel 1 operates independently, the OC trip set by 1.2V comparator can be lower than 108µA trip point as shown in Equation 6.

$$R_{ISEN1} = \frac{\left(\frac{I_{OC}}{N} + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - t_{MIN\_OFF}\right)\right) \bullet DCR}{I_{TRIP}} \quad \text{(EQ. 6)}$$

$$R_{ISHARE} = \frac{1.2V}{I_{TRIP}} \qquad R_{ISET} = R_{ISHARE} \cdot N_{CNTL}$$

where N is the number of phases; NCNTL is the number of the ISL8120 controllers in parallel or multiphase operations;

ITRIP = 108µA; IOC is the load overcurrent trip point; t_{MIN_OFF} is the minimum Ugate turn off time that is 350ns; R_{ISHARE} in Equation 6 represents the total equivalent resistance in ISHARE pin bus of all ICs in multiphase or module parallel operation.

For the R_{ISEN} chosen for OCP setting, the final value is usually higher than the number calculated from Equation 6. The reason of which is practical especially for low DCR applications since the PCB and inductor pad soldering resistance would have large effects in total impedance, affecting the DCR voltage to be sensed.

When OCP is triggered, the controller pulls EN/FF low immediately to turn off UGATE and LGATE.

For overload and hard short condition, the overcurrent protection reduces the regulator RMS output current much less than full load by putting the controller into hiccup mode. A delay time, equal to 3 soft-start intervals, is inserted to allow the disturbance to be cleared out. After the delay time, the controller then initiates a soft-start interval. If the output voltage comes up and returns to the regulation, PGOOD transitions high. If the OC trip is exceeded during the soft-start interval, the controller pulls EN/VFF low again. The PGOOD signal will remain low and the soft-start interval will be allowed to expire. Another soft-start interval will be initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed.

Internal Series Linear and Power Dissipation

The VIN pin is connected to PVCC with an internal series linear regulator. The PVCC and VIN pins should have the recommended bypass ceramic capacitors (10µF) connected to GND for proper operation. The internal linear regulator's input (VIN) can range between 3V to 22V. PVCC pin is the output of the internal linear regulator and it provides power for both the internal MOSFET drivers through the PVCC pin. VCC pin is the bias input for the IC small signal analog circuitry. By connecting PVCC to VCC pin, the internal linear regulator supplies bias power to VCC. The VCC pin should be connected to the PVCC pin with an RC filter to prevent high frequency driver switching noise from the analog circuitry. When VIN drops below 5.0V, the pass element will saturate; PVCC will track VIN with a dropout of the linear regulator. When used with an external 5V supply, the VIN pin is recommended to be tied directly to PVCC.

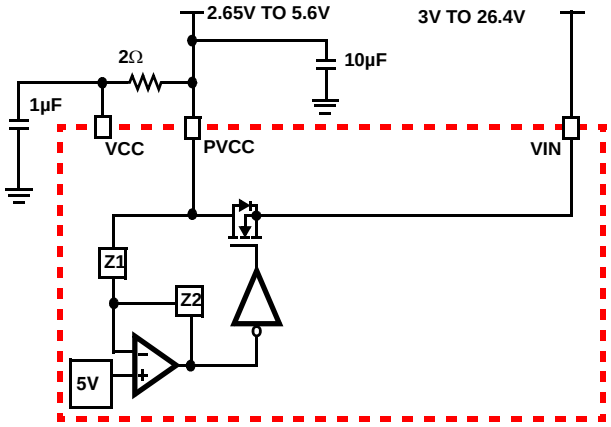


FIGURE 17. INTERNAL REGULATOR IMPLEMENTATION

The LDO is capable of supplying 250mA with regulated 5.4V output. In 3.3V input applications, when the VIN pin voltage is 3V, the LDO can still supply 150mA while maintaining LDO output voltage higher than VCC falling threshold to keep IC operating. Figure 18 shows the LDO voltage drop under different load current. However, its thermal capability should not be exceeded. The power dissipation inside the IC could be estimated with Equation 7.

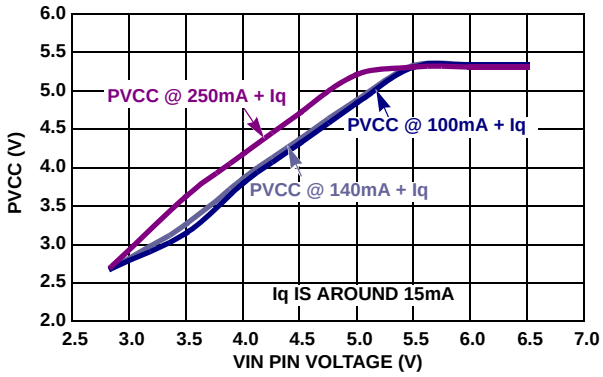


FIGURE 18. PVCC vs VIN VOLTAGE

$$P_{IC} = (VIN - PVCC) \cdot I_{VIN} + P_{DR} \quad \text{(EQ. 7)}$$

$$I_{VIN} = \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}} \right) \bullet PVCC \bullet F_{SW} + I_{Q\_VIN}$$

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} \quad \text{(EQ. 8)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1}+R_{EXT1}} + \frac{R_{LO1}}{R_{LO1}+R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2}+R_{EXT2}} + \frac{R_{LO2}}{R_{LO2}+R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet PVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet PVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage ($V_{GS1}$and V_{GS2}) in the corresponding MOSFET datasheet; I_{Q_VIN} is the driver's total quiescent current with no load at drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively.

To keep the IC within its operating temperature range, an external power resistor could be used in series with VIN pin to bring the heat out of the IC, or and external LDO could be used when necessary.

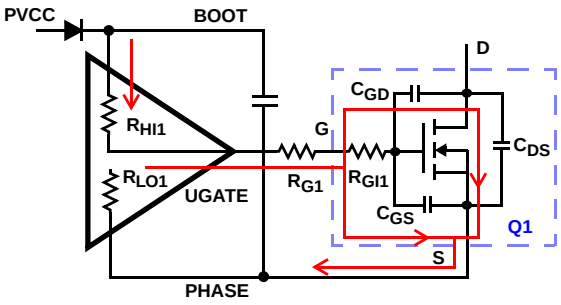


FIGURE 19. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

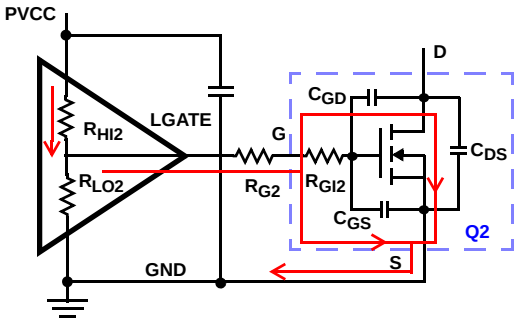


FIGURE 20. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Oscillator

The Oscillator is a sawtooth waveform, providing for leading edge modulation with 350ns minimum dead time. The oscillator (Sawtooth) waveform has a DC offset of 1.0V. Each channel's peak-to-peak of the ramp amplitude is set proportional the voltage applied to its corresponding EN/FF pin. See "Voltage Feed-forward" on page 23.

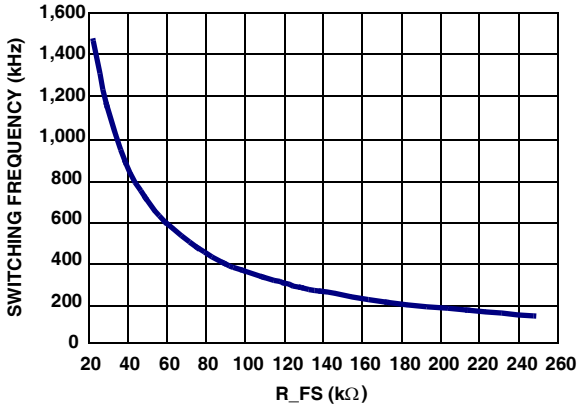


FIGURE 21. R_{FS} vs SWITCHING FREQUENCY

Frequency Synchronization and Phase Lock Loop

The FSYNC pin has two primary capabilities: fixed frequency operation and synchronized frequency operation. By tying a resistor (R_{FSYNC}) to GND from the FSYNC pin, the switching frequency can be set at any frequency between 150kHz and 1.5MHz. The frequency setting curve shown in Figure 21 is provided to assist in selecting the correct value for R_{FSYNC}.

By connecting the FSYNC pin to an external square pulse waveform (such as the CLOCK signal, typically 50% duty cycle from another ISL8120), the ISL8120 will synchronize its switching frequency to the fundamental frequency of the input waveform. The maximum voltage to the FSYNC pin is VCC + 0.3V. The Frequency Synchronization feature will synchronize the leading edge of CLKOUT signal with the falling edge of Channel 1's PWM clock signal. The CLKOUT is not available until the PLL locks.

The locking time is typically 130µs for F_{SW} = 500kHz. EN/VFF1 is released for a soft-start cycle until the FSYNC stabilized and the PLL is in locking. The PLL circuits control only EN/FF1, and control Channel 2's soft-start instead of EN/FF2. Therefore, it is recommended to connect all EN/FF pins together in multiphase configuration.

The loss of a synchronization signal for 13 clock cycles causes the IC to be disabled until the PLL returns locking, at which point a soft-start cycle is initiated and normal operation resumes. Holding FSYNC low will disable the IC.

Differential Amplifier for Remote Sense

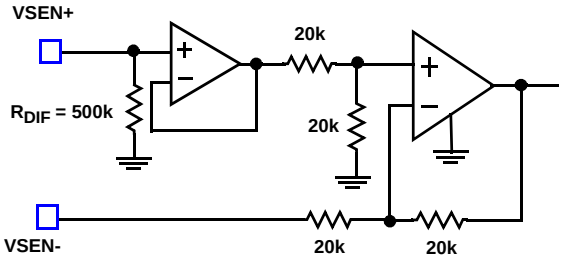


FIGURE 22. EQUIVALENT DIFFERENTIAL AMPLIFER

The differential remote sense buffer has a precision unity gain resistor matching network, which has a ultra low offset of 1mV. This true remote sensing scheme helps compensate the droop due to load on the positive and negative rails and maintain the high system accuracy of ±0.6%.

The output of the remote sense buffer is connected directly to the internal OV/UV comparator. As a result, a resistor divider should be placed on the input of the buffer for proper regulation, as shown in Figure 24. The VMON pin should be connected to the FB pin by a standard feedback network.

Since the input impedance of VSEN+ pin in respect to VSEN- pin is about 500kΩ, it is highly recommended to include this impedance into calculation and use 100Ω or less for the lower leg (R_{OS}) of the feedback resistor divider to optimize system accuracy. Note that any RC filter at the inputs of the differential amplifier will contribute as a pole to the overall loop compensation.

As some applications will not need the differential remote sense, the output of the remote sense buffer can be disabled and be placed in high impedance by pulling VSEN- within 700mV of VCC. In such an event, the VMON pin can be used as an additional monitor of the output voltage with a resistor divider to protect the system against single point of failure, which occurs in the system using the same resistor divider for the UV/OV comparator and the output regulation. The resistor divider ratio should be the same as the one for the output regulation so that the correct voltage information is provided to the OV/UV comparator. Figure 23 shows the differential sense amplifier can be directly used as a monitor without pulling VSEN- high.

DDR and Dual Mode Operation

If the CLKOUT/REFIN is less than 800mV, an external soft-start ramp (0.6V) can be in parallel with the Channel 2's internal soft-start ramp for DDR/tracking applications (DDR Mode).

The output voltage (typical VTT output) of Channel 2 tracks with the input voltage (typical VDDQ*(1+k) from Channel 1) at the CLKOUT/REFIN pin. As for the external input signal and internal reference signal (ramp and 0.6V), the one with the lowest voltage will be the one to be used as the reference comparing with FB signal. So in DDR configuration, VTT channel should start-up later after its internal soft-start ramp in which way the VTT will track the voltage on REFIN pin derived from VDDQ. This can be achieved by adding more filtering at EN//FF1 compared with EN/FF2.

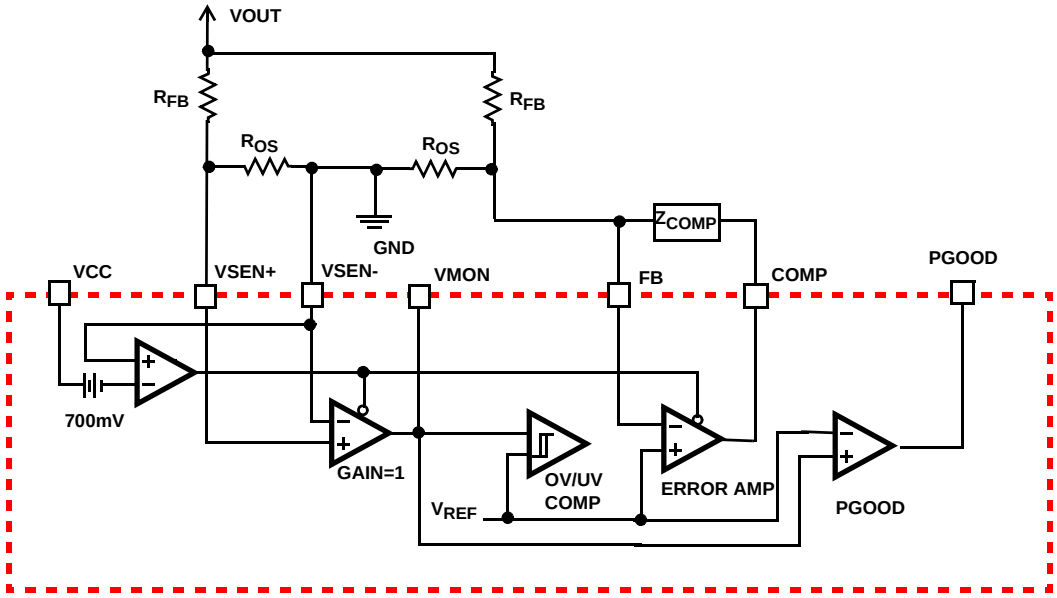


FIGURE 23. DUAL OUTPUT VOLTAGE SENSE FOR SINGLE POINT OF FAILURE PROTECTION

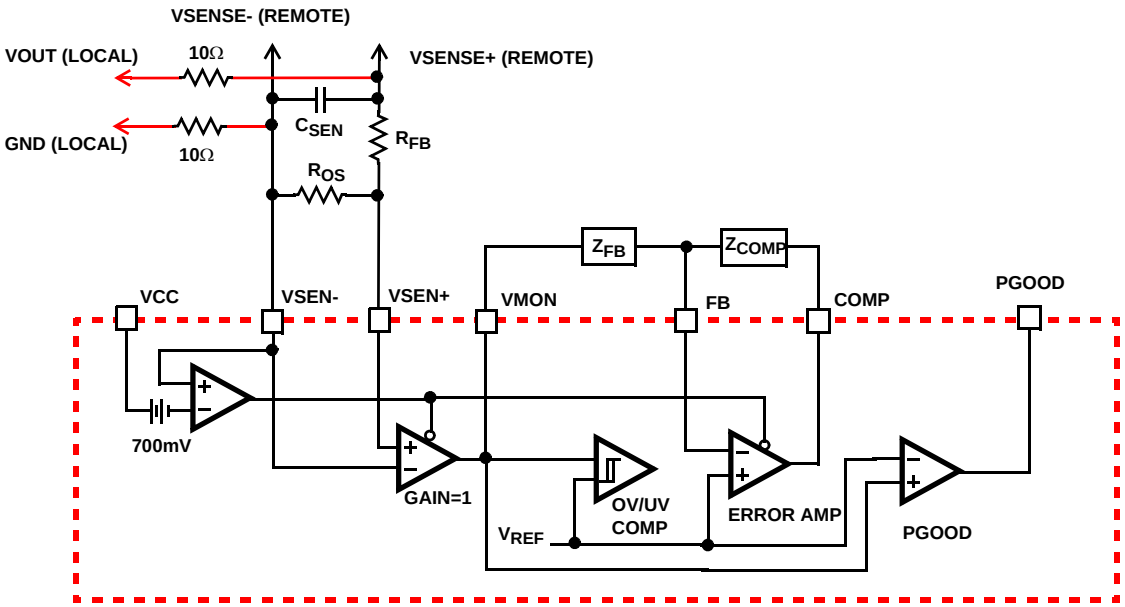


FIGURE 24. SIMPLIFIED REMOTE SENSING IMPLEMENTATION

Since the UV/OV comparator uses the same internal reference 0.6V, to guarantee UV/OV and Pre-charged start-up functions of Channel 2, the target voltage derived from Channel 1 (VDDQ) should be scaled close to 0.6V, and it is suggested to be slightly above (+2%) 0.6V with an external resistor divider, which will have Channel 2 use the internal 0.6V reference after soft-start. Any capacitive load at REFIN pin should not slow down the ramping of this input 150mV lower than the Channel 2' internal ramp. Otherwise, the UV protection could be fault triggered prior to the end of the soft-start. The start-up of Channel 2 can be delayed to avoid such situation happening, if high capacitive load presents at REFIN pin for noise decoupling. During shutdown, Channel 2 will follow Channel 1 until both channels drops below 87%, at which point both channels enter UV protection zone. Depending on the loading, Channel 1 might drop faster than Channel 2. To solve this race condition, Channel 2 can either power up from Channel 1 or bridge the Channel 1 with a high current Schottky diode. If the system requires to shutdown both channels when either has a fault, tying EN/FF1 and EN/FF2 will do the job. In DDR mode, Channel 1 delays 60° over Channel 2.

In Dual mode, depending upon the resistor divider level of REFIN from VCC, the ISL8120 operates as a dual-PWM controller for two independent regulators with a phase shift, as shown in Table 2. The phase shift is latched as VCC raises above POR and cannot be changed on the fly.

TABLE 2.

MODE	DECODING REFIN RANGE	PHASE for CHANNEL 2 WRT CHANNEL 1	REQUIRED REFIN
DDR	<29% of VCC	-60°	0.6V
Dual	29% to 45% of VCC	0°	37% VCC
Dual	45% to 62% of VCC	90°	53% VCC
Dual	62% to VCC	180°	VCC

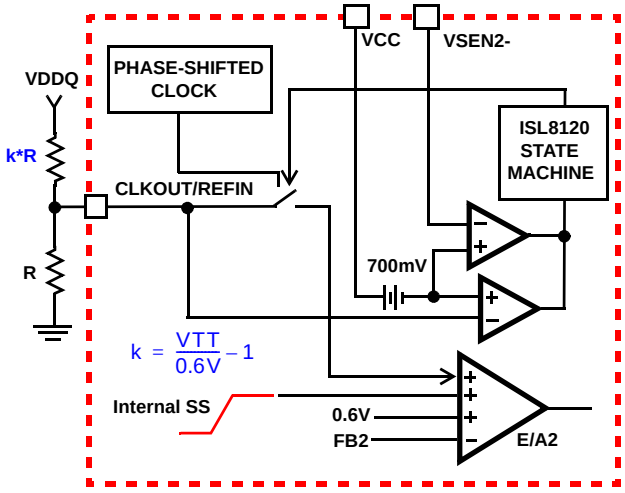


FIGURE 25. SIMPLIFIED DDR IMPLEMENTAION

Internal Reference and System Accuracy

The internal reference is set to 0.6V. Including bandgap variation and offset of differential and error amplifiers, it has an accuracy of ±0.6% over commercial temperature range, and 0.9% over industrial temperature range. While the remote sense is not used, its offset (V_{OS_DA}) should be included in the tolerance calculation. Equations 9 and 10 show the worst case of system accuracy calculation. V_{OS_DA} should set to zero when the differential amplifier is in the loop, the differential amplifier's input impedance (R_{DIF}) is typically 500kΩ with a tolerance of 20% (RDIF%) and can be neglected when R_{OS} is less than 100Ω. To set a precision setpoint, R_{OS} can be scaled by two paralleled resistors.

Figure 26 shows the tolerance of various output voltage regulation for 1%, 0.5%, and 0.1% feedback resistor

dividers. Note that the farther the output voltage setpoint away from the internal reference voltage, the larger the tolerance; the lower the resistor tolerance (R%), the tighter the regulation.

$$\%min = (Vref \cdot (1 - Ref\%) - V_{OS\_DA}) \cdot \left(1 + \frac{R_{FB} \cdot (1 - R\%)}{R_{OSMAX}}\right) \quad \text{(EQ. 9)}$$

$$R_{OSMAX} = \frac{1}{\frac{1}{R_{OS} \cdot (1 + R\%)} + \frac{1}{R_{DIF} \cdot (1 + R_{DIF}\%)}}$$

$$\%max = (Vref \cdot (1 - Ref\%) - V_{OS\_DA}) \cdot \left(1 + \frac{R_{FB} \cdot (1 - R\%)}{R_{OSMIN}}\right) \quad \text{(EQ. 10)}$$

$$R_{OSMIN} = \frac{1}{\frac{1}{R_{OS} \cdot (1 - R\%)} + \frac{1}{R_{DIF} \cdot (1 - R_{DIF}\%)}}$$

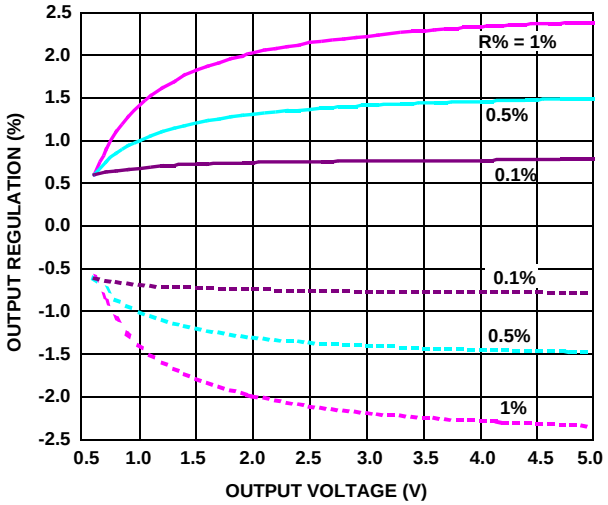
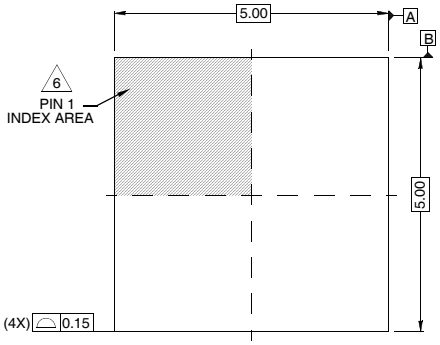


FIGURE 26. OUTPUT REGULATION WITH DIFFERENT RESISTOR TOLERANCE FOR Ref% = ±0.6%

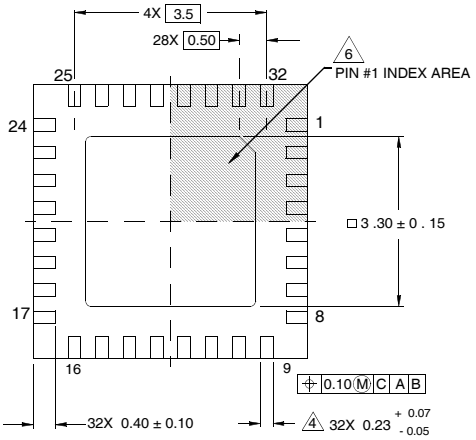
Package Outline Drawing

L32.5x5B

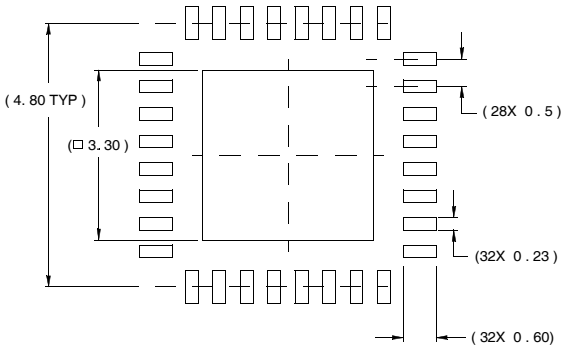
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 11/07



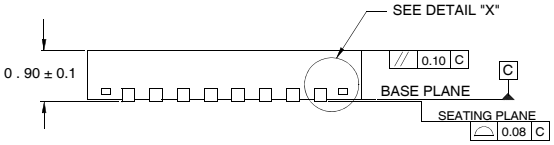
TOP VIEW



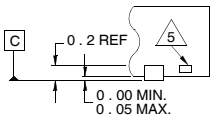
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.