

# M220x Series

9x14 mm, 3.3/2.5/1.8 Volt, PECL/LVDS/CML, Clock Oscillator



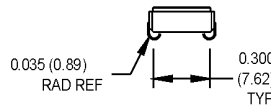
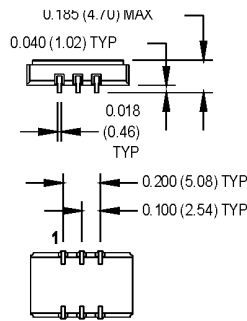
- Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

### Applications:

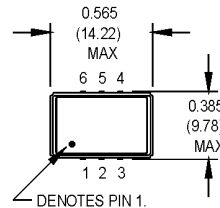
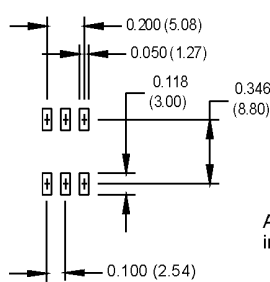
- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

### Ordering Information

|                                |                        |   |   |   |   |   |   |         |     |
|--------------------------------|------------------------|---|---|---|---|---|---|---------|-----|
|                                | M220                   | 0 | 6 | 8 | B | P | J | 00.0000 | MHz |
| Product Series                 |                        |   |   |   |   |   |   |         |     |
| Supply Voltage                 |                        |   |   |   |   |   |   |         |     |
| 0: 3.3 V                       | 1: 2.5 V               |   |   |   |   |   |   |         |     |
| 2: 1.8 V                       |                        |   |   |   |   |   |   |         |     |
| Temperature Range              |                        |   |   |   |   |   |   |         |     |
| 2: -40°C to +85°C (see note 1) | 6: -20°C to +70°C      |   |   |   |   |   |   |         |     |
| Stability                      |                        |   |   |   |   |   |   |         |     |
| 4: ±50 ppm                     | 3: ±100 ppm            |   |   |   |   |   |   |         |     |
| 8: ±20 ppm                     |                        |   |   |   |   |   |   |         |     |
| Enable/Disable                 |                        |   |   |   |   |   |   |         |     |
| B: Enable High (pin 1)         | G: Enable High (pin 2) |   |   |   |   |   |   |         |     |
| S: Enable Low (pin 1)          | M: Enable Low (pin 2)  |   |   |   |   |   |   |         |     |
| U: No Enable/Disable           |                        |   |   |   |   |   |   |         |     |
| Logic Type                     |                        |   |   |   |   |   |   |         |     |
| P: LVPECL                      | L: LVDS                |   |   |   |   |   |   |         |     |
| M: CML                         |                        |   |   |   |   |   |   |         |     |
| Package/Lead Configuration     |                        |   |   |   |   |   |   |         |     |
| J: 9x14 mm J-lead              |                        |   |   |   |   |   |   |         |     |
| Frequency (customer specified) |                        |   |   |   |   |   |   |         |     |



#### SUGGESTED SOLDER PAD LAYOUT



All dimensions in inches (mm).

#### PIN 1 ENABLE

- Pin1: Enable/Disable
- Pin2: N/C
- Pin3: Ground
- Pin4: Output Q (LVPECL, LVDS, CML)
- Pin5: Output  $\bar{Q}$  (LVPECL, LVDS, CML)
- Pin6: Vcc

#### PIN 2 ENABLE

- Pin1: N/C
- Pin2: Enable/Disable
- Pin3: Ground
- Pin4: Output Q (LVPECL, LVDS, CML)
- Pin5: Output  $\bar{Q}$  (LVPECL, LVDS, CML)
- Pin6: Vcc

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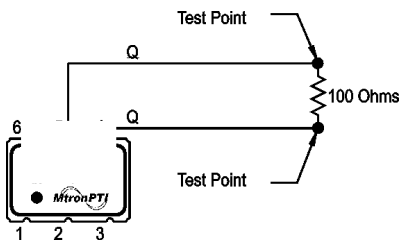
| PARAMETER                    | Symbol                         | Min.  | Typ. | Max.                   | Units             | Condition/Notes                                    |            |
|------------------------------|--------------------------------|---|------|------------------------|-------------------|--|------------|
| Frequency Range              | F                              | 150   |      | 1400                   | MHz               | See Note 2   |            |
| Operating Temperature        | T <sub>A</sub>                 | (See ordering information)  |      |                        |                   |  | See Note 1 |
| Storage Temperature          | T <sub>S</sub>                 | -55   |      | +125                   | °C                |  |            |
| Frequency Stability          | ΔF/F                           | (See ordering information)  |      |                        |                   |  | See Note 3 |
| Aging                        |                                |   |      |                        |                   |  |            |
| 1st Year                     |                                | -3  |      | +3                     | ppm               |  |            |
| Thereafter (per year)        |                                | -1  |      | +1                     | ppm               |  |            |
| Supply Voltage               | V <sub>cc</sub>                | 1.71  | 1.8  | 1.89                   | V                 |  |            |
|                              |                                | 2.375   | 2.5  | 2.625                  | V                 |  |            |
|                              |                                | 3.135   | 3.3  | 3.465                  | V                 |  |            |
| Input Current                | I <sub>cc</sub>                |   |      | 125                    | mA                | LVPECL/LVDS/CML                                    |            |
| Load                         |                                | 50 Ohms to (V <sub>cc</sub> - 2) V <sub>dc</sub><br>100 Ohm differential load                         |      |                        |                   | See Note 4<br>LVPECL Waveform<br>LVDS/CML Waveform |            |
| Symmetry (Duty Cycle)        |                                | 45  |      | 55                     | %                 | @ 50% of waveform                                  |            |
| Output Skew                  |                                |   | TBD  |                        |                   |  |            |
| Differential Voltage         |                                | 350   | 425  | 500                    | mV <sub>ppd</sub> | LVDS<br>CML  |            |
| Common Mode Output Voltage   | V <sub>cm</sub>                |   | 1.2  |                        | V                 | LVDS   |            |
| Logic "1" Level              | V <sub>oh</sub>                | V <sub>cc</sub> - 1.02  |      |                        | V                 | LVPECL   |            |
| Logic "0" Level              | V <sub>ol</sub>                |   |      | V <sub>cc</sub> - 1.63 | V                 | LVPECL   |            |
| Rise/Fall Time               | T <sub>r</sub> /T <sub>f</sub> |   | 0.23 | 0.50                   | ns                | @ 20/80% LVPECL                                    |            |
| Enable Function              |                                | 80% V <sub>cc</sub> min. or N/C: output active<br>20% V <sub>cc</sub> max.: output disables to high-Z |      |                        |                   | Output Option B or G                               |            |
|                              |                                | 20% V <sub>cc</sub> max.: output active<br>80% V <sub>cc</sub> min.: output disables to high-Z        |      |                        |                   | Output Option S or M                               |            |
| Start up Time                |                                |   | 10   |                        | ms                |  |            |
| Phase Jitter<br>@ 622.08 MHz | φ <sub>J</sub>                 |   | 0.3  |                        | ps RMS            | Integrated 12 kHz – 20 MHz                         |            |
| Phase Noise                  |                                |   |      |                        |                   | @ 622.08 MHz                                       |            |
| 10 Hz                        |                                |   | -50  |                        |                   | dBc/Hz   |            |
| 100 Hz                       |                                |   | -80  |                        |                   | dBc/Hz   |            |
| 1 KHz                        |                                |   | -106 |                        |                   | dBc/Hz   |            |
| 10 KHz                       |                                |   | -117 |                        |                   | dBc/Hz   |            |
| 100 KHz                      |                                |   | -120 |                        |                   | dBc/Hz   |            |
| 1 MHz                        |                                |   | -130 |                        |                   | dBc/Hz   |            |
| 10 MHz                       |                                |   | -147 |                        |                   | dBc/Hz   |            |
| 40 MHz                       |                                |   | -150 |                        |                   | dBc/Hz   |            |
| Mechanical Shock             |                                | Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms duration, ½ sinewave)                         |      |                        |                   |  |            |
| Vibration                    |                                | Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)  |      |                        |                   |  |            |
| Hermeticity                  |                                | Per MIL-STD-202, Method 112, (1x10 <sup>-8</sup> atm. cc/s of Helium)                                 |      |                        |                   |  |            |
| Thermal Cycle                |                                | Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)                 |      |                        |                   |  |            |
| Solderability                |                                | Per EIAJ-STD-002  |      |                        |                   |  |            |
| Soldering Conditions         |                                | +240°C max. for 10 secs.  |      |                        |                   |  |            |

Note 1: If the device is powered up below -20°C and then the ambient temperature rises 105°C during normal operation, the output will be interrupted for approximately 2-3 ms. A correction is in process and will be available Q1 2007.

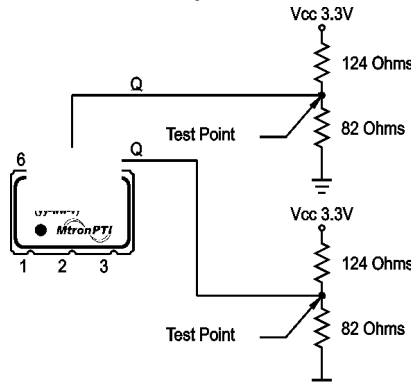
Note 2: Contact factory for exact frequency availability over 945 MHz

Note 3: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.

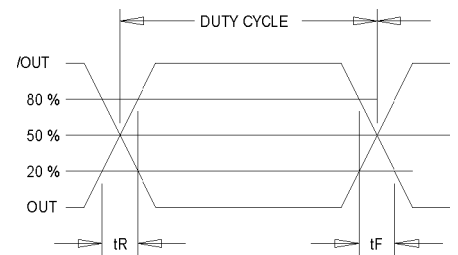
Note 4: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



LVDS Load Circuit



3.3V LVPECL Load Circuit



Output Waveform: LVDS/CML/PECL

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