

Features

- Duplex LC Single Mode Transceiver
- Small Form Factor Multi-sourced 2x5 Pin Package
- 1310nm, FP Laser
- SONET SR/SDH STM-16 Compliant
- Single +3.3V Power Supply
- LVPECL/CML Differential level Inputs and Outputs
- LVTTL or LVPECL logic level signal-detect output choice (C-13-2500-F-SLC for LVPECL and C-13-2500C-F-SLC for LVTTL)
- LVTTL disable input
- Temperature Range: 0 to 70° C
- Class 1 Laser International Safety Standard IEC 825 Compliant
- Complies with Bell Core TA-NWT-000983

General Operating					
Parameter	Symbol	Min	Typical	Мах	Unit
Supply Voltage	V _{cc}	3.135	3.3	3.465	V
Total Current	I _{cc}			300	mA
Inrush Current	l _{cc} '			30	mA
Power Supply Noise Rejection ^a		100			mV _{p-p}
Operating Temperature (case)	T _{op}	0		70	°C
Storage Temperature	T _{st}	-40		85	°C
Data Rate OC48/STM-16	DR		2488		Mb/s

a) 20Hz to 155MHz

Transmitter Specifications						
Parameter	Symbol	Min	Typical	Max	Unit	
Optical Power	Pop	-10		-3	dBm	
Average Launch power of off Tx	Poff			-30	dBm	
Extinction Ratio (dynamic)	ER	8.2			dB	
Eye Mask					SONET/SDH compliant	
Optical Jitter generation	Jgen			0.002	UI	
Optical Rise time ^b	t _r		130		ps	
Optical Fall time ^b	t _f		130		ps	
Mean Wavelength	λ	1266	1310	1360	nm	
Maximum RMS width (s)	Δλ			4	nm	
Relative Intensity Noise	RIN			-120	dB/Hz	

b) 20%-80% values

Transmitter Electrical						
Parameter	Symbol	Min	Typical	Max	Unit	
Input Differential	R _{in}	80	100	120	Ohm	
PECL Single Ended data input swing	V _{in}	200		800	mV _{p-p}	
PECL Differential data input swing	V _{in}	400		1600	mV _{p-p}	
TxFault_Fault	V _{fault}	2		V _{cc}	V	
TxFault_Normal	V _{normal}	V _{ee}		0.8	V	
TxDisable_Disable	V _d	2		V _{cc}	V	
TxDisable_Enable	V _{en}	V _{ee}		V _{ee} +0.8	V	

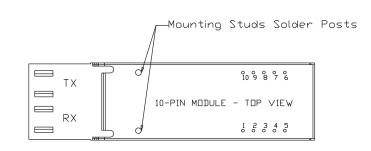
D ;					Unit dBm
Receiver Specifications	Gumbal	D.C.	Turiant	Mari	dBm
Parameter	Symbol	Min	Typical	Max	-ID
Receive Power Low ^d	R _{sens,low}	-18			dBm
Receive Power High	R _{sens,high}			-3	nm
Damage Threshold for Receiver	P _{in,damage}			0	dBm
Wavelength	λ	1100		1600	dBm
LOS Assert		-28			dB
LOS De-assert				-18	
LOS hysteresis		1			

d) at 10⁻¹⁰ BER, PRBS 2²³-1

Electrical Output					
Parameter	Symbol	Min	Typical	Мах	Unit
PECL Single ended data output swing	V _{out}	250		500	mV _{p-p}
PECL Differential data output swing	V _{out}	500		1000	mV _{p-p}
Data output rise time	Tr		130		ps
Data output fall time	T _f		130		ps

Timing and Electrical					
Parameter	Symbol	Min	Typical	Мах	Unit
Tx Disable Negate time	t_on			1	ms
Tx Disable assert time	t_off			10	μs
Time to initialize, including reset of TX fault	t_init			300	ms
Tx fault Assert time	t_fault			100	μs
Tx Disable to reset	t_reset	10			μs
LOS Assert time	t_loss_on			100	μs
LOS De-assert time	t_loss_off			100	μs
Serial ID Clock Rate	f_serial_clock			100	KHz
RX_LOS Voltage (high)		2		V _{ee} +0.3	V
RX_LOS Voltage (low)		0		0.8	V
LOS output voltage-Fault	V _{LOS} fault	2		V _{cc}	V
LOS output voltage-Normal	V _{LOS} normal	V _{ee}		V _{ee} +0.3	V
MOD_DEF (0:2)-High	V _h	2		V _{cc}	V
MOD_DEF (0:2)-Low	VI	V _{ee}		V _{ee} +0.3	V

Outline Drawing



Pinout Definitions

Pin	Symbol	Notes
1	RxGND	Directly connect this pin to the receiver ground plane
2	RxVcc	+3.3V dc power for the receiver section
3	SD	Active high on this indicates a received optical signal (LVTTL or LVPECL)
4	RD-	eceiver Data out Bar(LVPECL/CML)
5	RD+	Receiver Data out (LVPECL/CML)
6	TxVcc	+3.3V dc power for the transmitter section
7	TxGND	Directly connect this pin to the transmitter ground plane
8	TxDIS	Transmitter disable (LVTTL)
9	TD+	Transmitter Data In (LVPECL/CML)
10	TD-	Transmitter Data In Bar (LVPECL/CML)
Attack	ning Posts	The attaching posts are at the case potential and may be connected chassis ground. They are not isolated from circuit ground.

Recommended Circuit Schematics

Inputs to the C-1x-2500/C-Fx-SLCx series transmitters are AC coupled and internally terminated through 50 ohm to AC ground. These transceivers can operate with LVPECL or CML logic levels. The input signal must have at least a 200 mV peak to peak (single ended) signal swing. Output from the receiver section of the module is also AC coupled and is expected to drive into 50 ohm load. Different termination strategies may be required depending on the particular Serializer/Deserializer chip set used. The C-1x-2500/C-Fx-SLCx series product family are designed with AC coupled data inputs and outputs to provide the following a advantages:

- Close positioning of SERDES with respect to transceiver; allow for shorter line lengths and at gigabit speeds reduces EMI.
- Mininum number of external components.
- Internal termination reduces the potential for unterminated stubs which would otherwise increase jitter and reduce transmission margin.

Figure 1 & 2 illustrates the recommended transmit and receive data line terminations for SERDES with CML and LVPECL Inputs/outputs respectively.

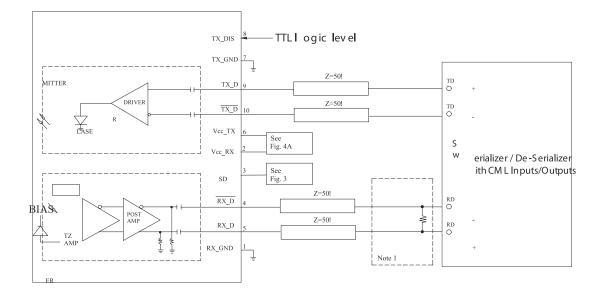


Figure 1. Recommended TRANSMIT adn RECEIVE Data Termination for SERDES with CML I/Os Note 1. Consult SERDES manufacurer's data sheet and application data for appropriate receiver iput biasing network. Some deserializer inputs are internally terminated and may not need external termination resistors.

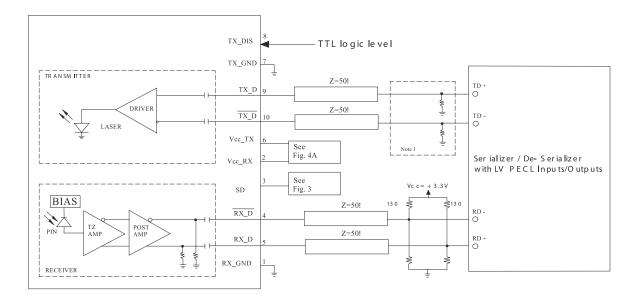
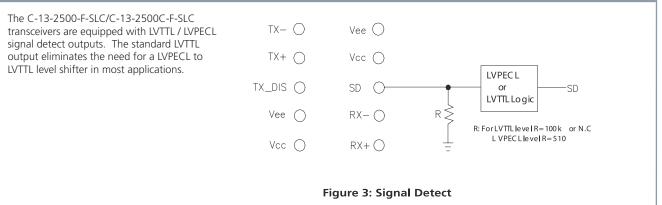


Figure 2. Recommended TRANSMIT and RECEIVE Data Terminations for SERDES with LV PECL I/Os. Note 1. Consult SERDES manufacurer's data sheet and application data for appropriate receiver iput biasing network. Some deserializer inputs are internally termintated and may not need external termination resistors.

SIGNAL DETECT



POWER COUPLING

A suggested layout for power and ground connections is given in figure 4B below. Connections are made via separate voltage and ground planes. The mounting posts are at case ground and should not be connected to circuit ground. The mounting posts are at case gound and should not be connected to circuit ground. The ferrite gead should provide a real impedance of 50 to 100 ohms at 100 to 1000MHz. Bypass capacitors should be placed as close to the 10-pin connector as possible.

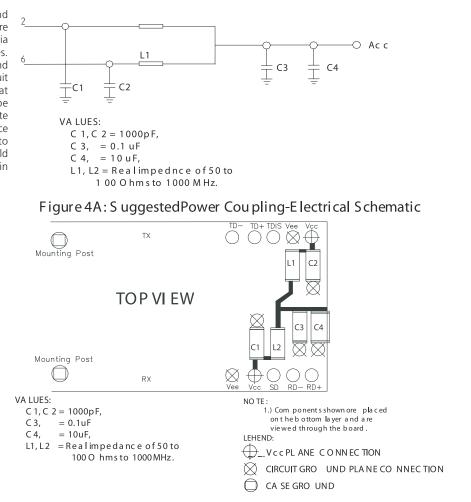


Figure 4B: Suggest ed Power Coupling-Com ponent Placement

Printed Circuit Board Layout Consideration

A fiber-optic receiver employs a very high gain, wide bandwidth transimpedance amplifier. This ampifier detects and amplifies signals that are only tens of nA in amplitude when the receiver is operating near its limit. Any unwanted signal current that couples into the receiver circuitry causes a decrease in the receiver's senitivity and can also degrade the receiver's signal detect(SD) circuit. To minimize the coupling of unwanted noise into the receiver, careful attention must be given to the printed circuit board. At a minimun, a double-sided printed circuit board (PCB) with a large component side ground plane beneath the transceiver must be used. In applications that include many other high speed devices, a multi-layer PCB is highly recommended. This permits the placement of power and ground on separate layers, which allows them to be isolated from the signal lines. Multilayer construction also permits the routing of signal traces away from high level, high speed signal lines. To minimize the possibility of coupling noise into the receiver pins. Noise that couples into the receiver through the power supply pins can also degrade performance. It is recommended that a pi filter in both the transmitter and receiver be supplied.

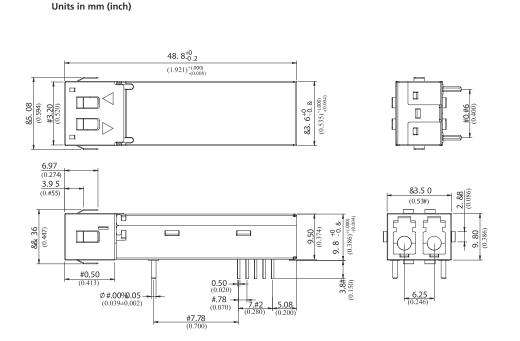
EMI and ESD Considerations

OIC transceivers offer a metalized plastic case and a special chassis grounding clip. As shown in the drawing, this clip connects the module case to chassis grounding clip then installs flush through the panel cutout. The grounding clip in this way brushes the edge of the cutout in order to make a proper contact. The use of a grounding clip also provides increased electrostatic protection and helps reduce radiated emissions from the module or the host circuit board through the chassis faceplate. The attaching posts are at case potential and may be connected to chassis ground. They should not be connected to circuit ground. Plastic optical subassemblies are used to further reduce the possibility of radiated emissions by eliminating the metal from the transmitter and receiver diode housings, which extend into connector space. By proficing a non-metal receptacle for the optical cable ferrule, the gigabit speed RF electrical signal is isolated from the connector area thus preventing radiated energy leakage from these surfaces to the outside of the panel.

Laser Safety

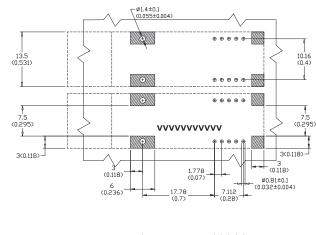
This single mode transceiver is a Class 1 laser product. It complies with IEC 825 and FDA 21 DFR 1040.10 and 1040.11. The transceiver must be operated within the specified temperature and voltage limits. The optical ports of the module shall determinate with an optical connector or with a dust plug.

Package Diagram



Case with EMI Shielding Finger

Recommended Board layout Hole Pattern





DIMENSION IN MILLIMETER (IN CHES)

NOTES:

1.THIS FIGURE DESCRIBE THE RECOMMAND CIRCUIT BOARD LAYOUT FOR THE SFF TRANSCEIVER. 2.THE HATCHED AREAS ARE KEEP-OUT AREAS RESERVED FOR HOUS ING STANDOFF. NO METAL TRACES OR GROUND CONNE CTION IN KEEP-OUT AREAS. 3.THE MOUNTING STUDS SHOULD BE SOLDERED TO CHASSIS GROUND FOR MECHANICAL INTEGRITY.

Recommended Panel mounting •••• 15.24 \oplus •••• А ιA \oplus 15.24 1 (0.039) 10.16±0.1 (0.4±0.004) SOLDER POSTS 15.5 typ. (0.61) -14.22 SECTION A-A DIMENSION IN MILLIMETER (INCHES)

Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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