F71808E

Super Hardware Monitor + LPC I/O

with Power Saving Control

Release Date: Aug, 2010
Version: V0.21P

F71808E Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2009/6	-	Preliminary Version
V0.11P	2009/7	-	Update Package Dimensions
V0.12P	2009/7	76	Add EuP relative registers
V0.13P	2009/8	-	Rvise typo
V0.14P	2009/8	12 28	Revise 3VSBSW# description Add 3VBSW# timing chart
V0.15P	2009/8	12 -	Add Pin 27 internal pull-high description Modify register typo.
V0.16P	2009/9	31 34 36 37 41 49 52	Revise CR27 default to 1 Add “Power Saving” in LDN=0A description Revise CR2Ah bit[3:2] description Revise CR2Bh bit3 and 1 description Remove redundant register CR02h[2] Revise CR94h description Add bit 6 description in CR9Bh
V0.17P	2009/10	76	Swap LDN(CR=0Ah) CRF1h and CRF2h
V0.18P	2009/11	34	Add Chip/Vendor ID register description
		10	Remove pin 57 WDT_EN function
		79	Add EuP register index E8/EE/EDh
		86	Modify TopMarking description for LAB Version
		88-89	Modify application circuit strapping table and UART circuit
V0.19P	2009/12	7,84	Modify average operation supply current
		86	Modify typo of version identification
		41,77	Reserved Config register index 02h bit 2 and WDT PME register index 07h bit 0.
		90	Modify application circuit (Remove Case Open circuit)
V0.20P	2010/01	88,90,92	Modify application circuit (Remove pin 57), RC protection and typo
		35	Modify Configuration Port Select Register (Index 27h, bit0) to TIMING_EN
		79-81	Remove RI# wakeup function
		5, 18, 40	Modify typo
V0.21P	2010/08	41 10	1. Update RS485 enable register description 2. Correct Pin Type
		6-9, 12-13, 30	Remove Ibex and TSI function and pin descriptions
		20, 23	Remove Monitor Temp from SMBus
		42	Remove TSI Register Description in Device Registers
		43	1. Remove Configuration Register — Index 08h 2. Modify Configuration Register — Index 0Ah bit 0:1
		44	1. Modify Configuration Register (Index 0Ch 2. Modify Configuration Register (Index 0Fh bit 1:0
		47	Modify T1 Over-OVT and Over-High Limit Temperature Select Register (Index 64h
		48	Modify DIODE OPEN Status Register -- Index 6Fh bit 4
		49	Remove index 7Ah – 7Dh
		58	Modify FAN1 Temperature Mapping Select - Index AFh [1:0]
		61	Modify FAN2 Temperature Mapping Select - Index BFh [1:0]
		64	1. Modify FAN3 Temperature Mapping Select - Index CFh [1:0]

			2. Remove index E0h – E4h, EDh
		67	Modify GPIO3 Pin Status Register — Index C2h bit 3:2
		87	Update Reference Circuit

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LIFE SUPPORT APPLICATIONS

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Table of Content

1. General Description

The F71808E which is the featured IO chip for PC system equippes one UART Port, Hardware Keyboard Controller, Hardware Monitor, ACPI management function and some GPIO pins. The F71808E integrated with hardware monitor, 8 sets of voltage sensor, 3 sets of creative auto-controlling fans and temperature sensor pins for the accurate dual current type temperature measurement for CPU thermal diode or external for temperature sensing. Besides, HWM also integrated Intel PECI interface for new platform temperature reading. For AMD platform, the F71808E provides the power sequence controller function which is selected by register.

The F71808E provides flexible features for multi-directional application. For instance, provides GPIO pins which can be programmed by register setting, accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Auto-Linear, Auto-Stage and Manual Mode for users' selection.

A power saving function which is in order to save the current consumption when the system is in the soft off state is also integrated a power saving function. The power saving function supports that system boot-on not only by pressing the power button but also by the wake-up event. When the system enters the S4/S5 state, F71808E can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be simulated to G3-like state when system enters the S4/S5 states. At the G3-like state, the F71808E consumes the 5VSB power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfil a low power consumption system which supports a wake up function.

The F71808E is powered by 3.3V and 5VSB voltage, with the LPC interface in 64-TQFP green package.

2. Feature List

- **General Functions**
  - Comply with LPC Spec. 1.1
  - Support DPM (Device Power Management), ACPI
  - Support AMD power sequence controller
  - Provides one UART, Hardware KBC
  - H/W monitor functions
  - Watch Dog Timer function
  - LED blink funciton
  - Intel PECI interface
  - 28 GPIO pins for flexible application

- GPIO22-25 supports High/Low/Pulse/Level mode option
- GPIO22-25 supports interrupt event by PME/SERIRQ
- 24/48 MHz clock input
- Packaged in 64-TQFP and powered by 3.3VCC

UART

- High-speed 16C550 compatible UART with 16-byte FIFOs
- Fully programmable serial-interface characteristics
- Baud rate up to 115.2K

Keyboard Controller

- LPC interface support serial interrupt channel 1, 12.
- Two 16bit Programmable Address fully decoder, default 0x60 and 0x64.
- Support two PS/2 interface, one for PS/2 mouse and the other for keyboard.
- Keyboard's scan code support set1, set2.
- Programmable compatibility with the 8042.
- Support both interrupt and polling modes.
- Hardware Gate A20 and Hardware Keyboard Reset.

Hardware Monitor Functions

- 2 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- Temperature range -40℃~127℃
- Integrate PECI 1.1a spec.
- 8 sets voltage monitoring (5 external and 3 internal powers)
- Voltage monitor supports Over Voltage Protection
- 3 fan speed monitoring inputs
- 3 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- Auto Stage mode (2-Limit and 3-Stage)/Auto Linear mode/Manual mode
- Issue PME# and OVT# hardware signals output
- WATCHDOG comparison of all monitored values

Watch Dog Timer

- Time resolution minute/second by option
- Maximum 256 minutes or 256 seconds
- Output signal from WDTRST# pin

Support AMD Power Sequence Controller

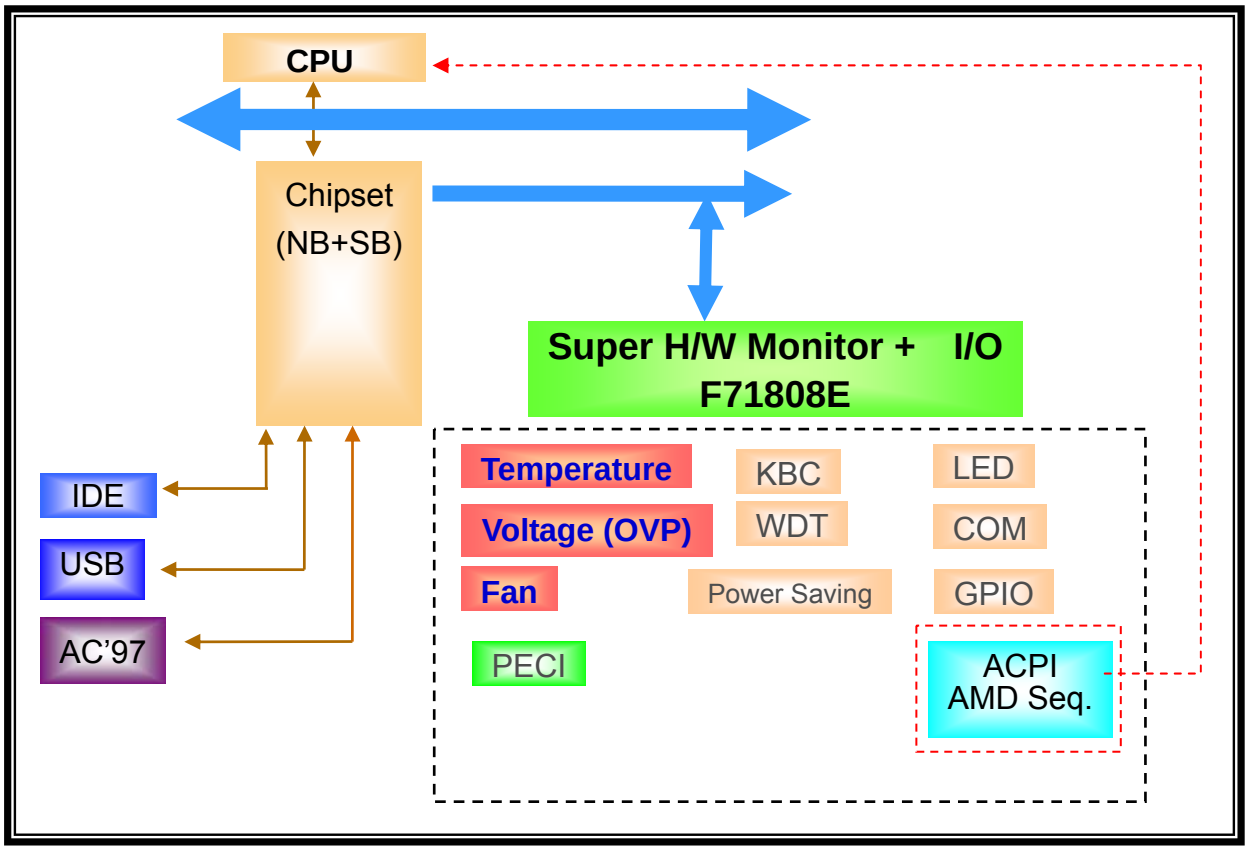
- **Power Saving Controller**
  - ACPI Timing and Power Control
  - Wake-up Supported

- **Package**
  - 64-pin TQFP Green Package

3. Key Specification

Supply Voltage	3.0V to 3.6V
Average Operating Supply Current	8 mA typ.

4. Block Diagram



5. Pin Configuration

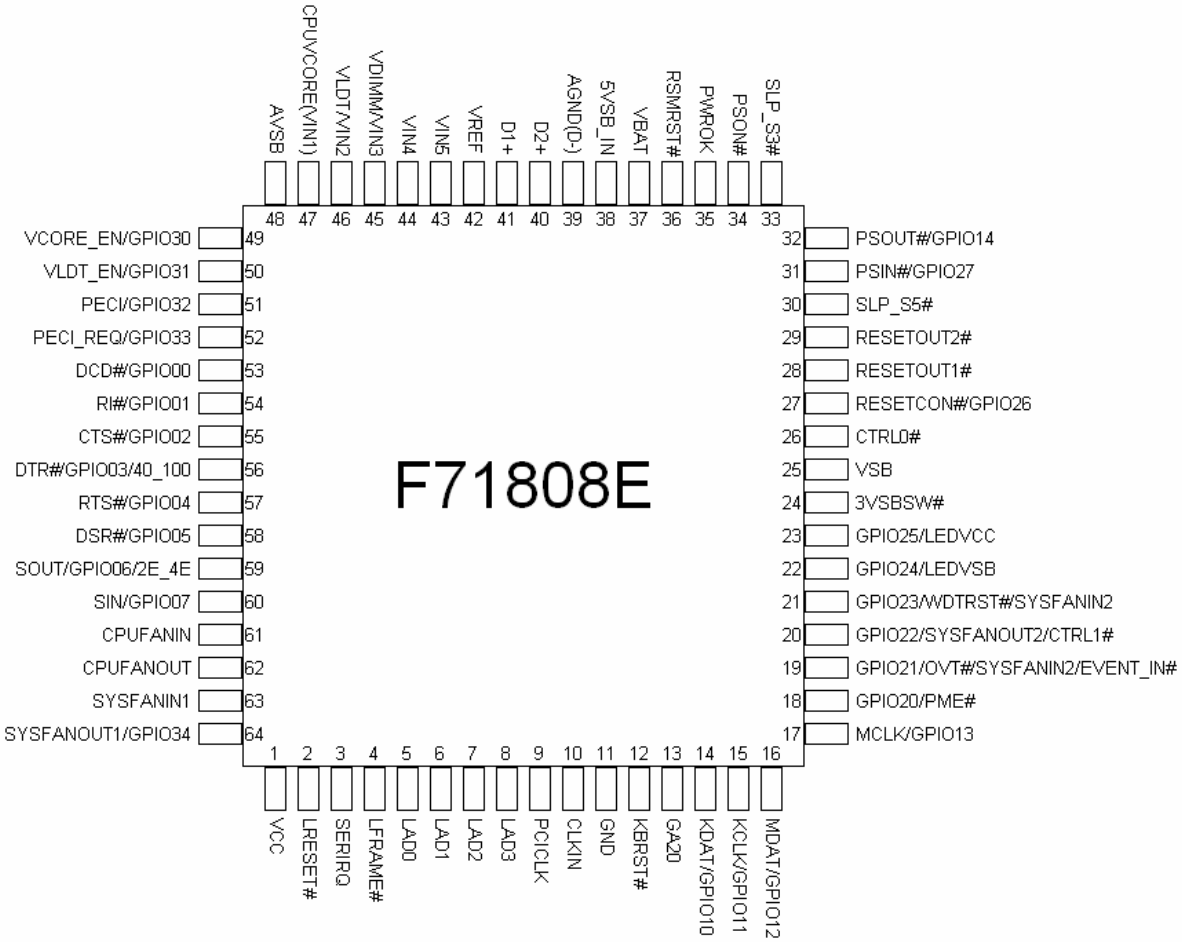


Figure1. F71808E pin configuration

6. Pin Description

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink cap ability.
I/O_{12ts5v} - TTL level bi-directional pin with schmitt trigger, 12 mA source-sink capability and 5V tolerance.
I/OOD_{12ts5v} - TTL level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability and and 5V tolerance
I/OD_{16t5v} - TTL level bi-directional pin,Open-drain output with 16 mA source-sink capability, 5V tolerance.
$OD_{16\text{-}u10\text{-}5v}$ - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
I/OD_{12ts5v} - TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
I/OD_{12tslv} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 12mA sink capability.
I/O_{8tslv} - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive and 1mA sink capability.
$O_{8\text{-}u47\text{-}5v}$ - Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
O_8 - Output pin with 8 mA source-sink capability.
O_{12} - Output pin with 12 mA source-sink capability.
O_{24} - Output pin with 24 mA source-sink capability.
AOUT - Output pin(Analog).
OD_{12} - Open-drain output pin with 12 mA sink capability.
$OD_{12\text{-}5v}$ - Open-drain output pin with 12 mA sink capability, 5V tolerance.
OD_{24} - Open-drain output pin with 24 mA sink capability.
IN_{t5v} - TTL level input pin,5V tolerance.
IN_{ts} - TTL level input pin and schmitt trigger.
IN_{ts5v} - TTL level input pin and schmitt trigger, 5V tolerance.
AIN - Input pin(Analog).
P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
1	VCC	P	Power supply voltage input with 3.3V (OVP function default is disabled).
11	GND	P	Digital GND
25	VSB	P	Stand-by power supply voltage input 3.3V
37	VBAT	P	Battery voltage input
38	5VSB	P	5V stand by power input
39	AGND(D-)	P	Analog GND
48	AVSB	P	Analog Stand-by power supply voltage input 3.3V

6.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
2	LRESET#	IN_{ts}	VCC	Reset signal. It can connect to PCIRST# signal on the host.
3	SERIRQ	I/O_{12t}	VCC	Serial IRQ input/Output. Internal pull high 47k ohms.
4	LFRAM#	IN_{ts}	VCC	Indicates start of a new cycle or termination of a

				broken cycle. Internal pull high 47k ohms.
8-5	LAD[3:0]	I/O_{12t}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral. Internal pull high 47k ohms.
9	PCICLK	IN_{ts}	VCC	33MHz PCI clock input.
10	CLKIN	IN_{ts}	VCC	System clock input. According to the input frequency 24/48MHz.

6.3 UART Function

Pin No.	Pin Name	Type	PWR	Description
53	DCD#	IN_{ts5v}	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	GPIO00	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
54	RI#	IN_{ts5v}	AVSB	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	GPIO01	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
55	CTS#	IN_{ts5v}	VCC	Clear To Send is the modem control input.
	GPIO02	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
56	DTR#	$O_{8\text{-}u47,5v}$	VCC	UART Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	GPIO03	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
	FAN40_100	IN_{t5v}		Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 40%.(PWM) The value can be programmed and register power by VSB3V. 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
57	RTS#	$O_{8\text{-}u47,5v}$	VCC	UART Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	GPIO04	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
58	DSR#	IN_{ts5v}	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	GPIO05	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.

59	SOUT	$O_{8\text{-}u47,5v}$	VCC	UART Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	GPIO06	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
	Config4E_2E	IN_{t5v}		Power on strapping: 1(Default)Configuration register:4E 0 Configuration register:2E
60	SIN	IN_{ts5v}	VCC	Serial Input. Used to receive serial data through the communication link.
	GPIO07	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.

6.4 Hardware Monitor

Pin No.	Pin Name	Type	PWR	Description
40	D2+	AIN	AVSB	Thermal diode/transistor temperature sensor input2.
41	D1+	AIN	AVSB	Thermal diode/transistor temperature sensor input1. This pin is for CPU use.
42	VREF	AOUT	AVSB	Voltage sensor output. Power down by VCC.
43	VIN5	AIN	AVSB	Voltage Input. This pin supports over voltage protection function (OVP function default is disable).
44	VIN4	AIN	AVSB	Voltage Input. This pin supports over voltage protection (OVP function default is disable).
45	VDIMM	AIN	AVSB	Voltage Input for VDIMM DUAL STR (2.5V/1.8V). 0.9V power ok.
	VIN3			Voltage Input 3.
46	VLDT	AIN	AVSB	Voltage Input for VLDT (1.2V). 0.9V power ok.
	VIN2			Voltage Input 2.
47	Vcore	AIN	AVSB	Voltage Input for Vcore. 0.6V power ok.
61	CPUFANIN	IN_{ts5v}	VCC	CPU Fan tachometer input.
62	CPUFANOUT	$OD_{12\text{-}5v}$	VCC	CPU Fan control output. This pin provides PWM duty-cycle output. 40% or 100% fan speed is optioned by pin 56 power on strapping.
63	SYSFANIN1	IN_{ts5v}	VCC	System Fan 1 tachometer input.
64	SYSFANOUT1	$OD_{12\text{-}5v}$ AOUT	VCC	System Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output. Pull up 4.7K to VCC to for PWM mode option. 40% or 100% fan speed is optioned by pin 56 power on strapping.
	GPIO34	I/OOD_{12ts5v}		General purpose IO.
51	PECI	$I/O_{s1D8tslv}$	VCC	Intel PECI hardware monitor interface.
	GPIO32	$I/OOD_{12t\ ts5v}$		General purpose IO. GPIO function selected by register setting.
52	PECI_REQ	OD_{12}	VCC	PECI request pin.

	GPIO33	$I/OOD_{12t\ ts5v}$		General purpose IO. GPIO function selected by register setting.

6.5 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
24	3VSBSW#	O_{12}	VSB	Switch 3VSB power to memory when in S3 state In S0# (Low level In S3# (Drive high In S5# (Default is Low level, and can be programmed to drive high
27	RESETCON#	INts5v	VSB	Connect to reset button. Internal with de-bounce circuit which is at least 50ms. Pull-high 10Kohm to VSB3V internally.
	GPIO26	$I/OOD_{12t\ ts5v}$		General purpose IO. Support High/Low/Pulse/Level selection. GPIO function selected by register setting.
28	RESETOUT1#	OD_{12}	VSB	It is an output buffer of LRESET#. This pin supports software reset by program.
29	RESETOUT2#	O_{24}	VSB	It is an output buffer of LRESET#. This pin supports software reset by program.
30	SLP_S5#	IN_{ts5v}	VSB	S5# signal input. Internal pull high 10k ohms to VSB3V.
31	PSIN#	IN_{ts5v}	VSB	Main power switch button input.
	GPIO27	$I/OOD_{12t\ ts5v}$		General purpose IO. Support High/Low/Pulse/Level selection. GPIO function selected by register setting.
32	PSOUT#	OD_{12}	VSB	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
	GPIO14	$I/OOD_{12t\ ts5v}$		General purpose IO. GPIO function selected by register setting.
33	SLP_S3#	IN_{ts5v}	VSB	S3# Input is Main power on-off switch input. Internal pull high 10k ohms to VSB3V
34	PSON#	$OD_{12\text{-}5v}$	VSB	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
35	PWROK	OD_{12}	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V.
36	RSMRST#	OD_{12}	VBAT	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.3V. Internal pull high 10k ohms to VSB3V
49	VCORE_EN	OD_{12}	AVSB	Active high. The function of this pin is to enable the PWM for CPU Vcore. The external pull high resistor is required.
50	VLDT_EN	OD_{12}	AVSB	Active high. The function of this pin is to enable the VLDT voltage. The external pull high resistor is required.

6.6 KBC Function

Pin No.	Pin Name	Type	PWR	Description
12	KBRST#	$OD_{16\text{-}u10,5v}$	VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
13	GA20	$OD_{16\text{-}u10,5v}$	VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
14	KDAT	$I/OD_{16t,5v}$	VSB	Keyboard Data.
	GPIO10	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
15	KCLK	$I/OD_{16t,5v}$	VSB	Keyboard Clock.
	GPIO11	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
16	MDAT	$I/OD_{16t,5v}$	VSB	PS2 Mouse Data.
	GPIO12	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.
17	MCLK	$I/OD_{16t,5v}$	VSB	PS2 Mouse Clock.
	GPIO13	I/OOD_{12ts5v}		General purpose IO. GPIO function selected by register setting.

6.7 Others

Pin No.	Pin Name	Type	PWR	Description
18	GPIO20	I/OOD_{12ts5v}	VSB	General purpose IO. Support High/Low/Pulse/Level selection.
	PME#	$OD_{12\text{-}5v}$		Generated PME event. It supports the PCI PME# nterface. This signal allows the peripheral to request the system to wake up from the S3 state.
19	GPIO21	I/OOD_{12ts5v}	VSB	General purpose IO. Support High/Low/Pulse/Level selection.
	OVT#	$OD_{12\text{-}5v}$		Over temperature signal output. OVT# function selected by register setting.
	SYSFANIN2	IN_{ts5v}		System Fan 2 tachometer input. SYSFANIN2 function selected by register setting.
	EVENT_IN#	IN_{ts5v}		Wake-up event input. The signal input wakes the system up from the sleep state.
20	GPIO22	I/OOD_{12ts5v}	VSB	General purpose IO. Support High/Low/Pulse/Level selection.
	SYSFANOUT2	$OD_{12\text{-}5v}$ AOUT		System Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output. Pull up 4.7K to VCC to for PWM mode option. 40% or 100% fan speed is optioned by pin 56 power on strapping. The PWM Frequency can be programmed to 23.5K or 220Hz.
	CTRL1#	OD_{12}		Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
21	GPIO23	I/OOD_{12ts5v}	VSB	General purpose pin. Support High/Low/Pulse/Level selection.

	WDTRST#	$OD_{12\text{-}5v}$		Watch dog timer signal output. WDTRST# function selected by register setting.
	SYSFANIN2	IN_{ts5v}		System Fan 2 tachometer input. SYSFANIN2 function selected by register setting.
22	GPIO24	I/OOD_{12ts5v}	VSB	General purpose pin. Support High/Low/Pulse/Level selection.
	LEDVSB	$OD_{12\text{-}5v}$		Power LED for VSB. Blink frequency selection. LEDVSB function selected by register setting.
23	GPIO25	I/OOD_{12ts5v}	VSB	General purpose pin. Support High/Low/Pulse/Level selection.
	LEDVCC	$OD_{12\text{-}5v}$		Power LED for VCC. Blink frequency selection. LEDVCC function selected by register setting.
26	CTRL0#	OD_{12}	VSB	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.

7. Function Description

7.1 Power on Strapping Option

The F71808E provides four pins for power on hardware strapping to select functions. There is a form to describe how to set the functions you want.

Table1. Power on trap configuration

Pin No.	Symbol	Value	Description
56	FAN_40_100	1	FAN power on speed is the last programmed value.
		0	FAN power on speed is 100%.
59	Config4E_2E	1	Configuration Register I/O port is 4E. (Default)
		0	Configuration Register I/O port is 2E.

7.2 Keyboard Controller

The KBC circuit provides the functions included a keyboard and/or a PS/2 mouse, and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

Output Buffer

The output buffer is an 8-bit read-only register at I/O address 60H. The keyboard controller uses the output buffer to send the scan code received from the keyboard and data bytes required by commands to the system.

Input Buffer

The input buffer is an 8-bit write-only register at I/O address 60H or 64H. Writing to address 60H sets a flag to indicate a data write; writing to address 64H sets a flag to indicate a command write. Data written to I/O address 60H is sent to keyboard through the controller's input buffer only if the input buffer full bit in the status register is “0”.

Status Register

The status register is an 8-bit read-only register at I/O address 64H, that holds information about the status of the keyboard controller and interface. It may be read at any time.

Bit	Bit Function	Description
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller (KCCB). It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Mouse Output Buffer	0: Muse output buffer empty 1: Mouse output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

Commands

<table>
<tr><th>Command</th><th>Fucntion</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
</table>

AAh	Self-test Returns 055h if self test succeeds
ABh	keyboard Interface Test 8'h00: indicate keyboard interface is ok. 8'h01: indicate keyboard clock is low. 8'h02: indicate keyboard clock is high 8'h03: indicate keyboard data is low 8'h04: indicate keyboard data is high
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
C0h	Read Input Port(P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into STATUS register
C2h	Continuously puts the upper four bits of Port1 into STATUS register
CAh	Read the data written by CBh command.
CBh	Written a scratch data. This byte could be read by CAh command.
D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Pulse only RC(the reset line) low for 6μS if Command byte is even

KBC Command Description

PS2 wakeup function

The KBC supports keyboard and mouse wakeup function, keyboard wakeup function has 4 kinds of conditions, when key is pressed combinational key (1) CTRL +ESC (2) CTRL+F1 (3) CTRL+ User Defined Code (4) ANY KEY (5) windows 98 wakeup up key (6) windows 98 power key (7) CTRL + ALT + User Defined Code (8) User Defined Code, KBC will assert PME signal. Mouse wakeup function has 2 kinds of conditions, when mouse (1) BUTTON CLICK or (2) BUTTON CLICK AND MOVEMENT, KBC will assert PME signal. Those wakeup conditions are controlled by configuration register.

7.3 Hardware Monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3VCC/VSB/VBAT is an exception for it is main power of the F71808E. Therefore 3VCC/VSB/VBAT can directly connect to this chip's power pin and need no external resistors. There

are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F71808E and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are five voltage inputs in the F71808E and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

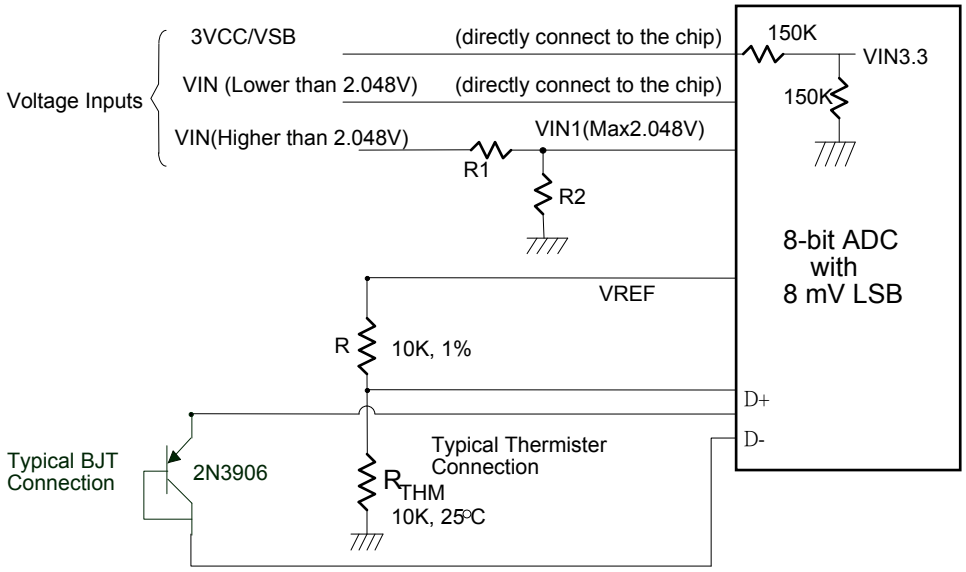


Figure 2. Hardware monitor configuration

The F71808E monitors two remote temperature sensors.These sensors can be measured from -40°C to 127°C. More details, please refer register description.

Table 2. Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

Table Range:

Table 3. Display range is from -40°C to 127°C in 2's complement format.

Temperature	Digital Output
-40°C	1101 1000
-1°C	1111 1111
1°C	0000 0001
90°C	0101 1010
127°C	1111 1111
Open	1000 0000

Monitor Temperature from "Thermistor"

The F71808E can connect three thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) β value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 6-1, the thermistor is connected by a serial resistor with 10K ohm, and then connected to VREF. The temperature measurement range is 0~127°C.

Monitor Temperature from "Thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71808E is capable to these situations. The build-in reference table is for PNP 2N3906 transistor. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Monitor Temperature from "PECI"

F71808E support Intel PECI1.1/PECI_Request interfaces to read temperature from PECI 1.1 device.

Temperature HM_IRQ Signal (HM_IRQ# and PME#)

Over temperature event will trigger HM_IRQ# that shown as figure. When monitored temperature exceeds the high temperature threshold value, HM_IRQ# will be asserted until the

temperature goes below the hysteresis temperature.

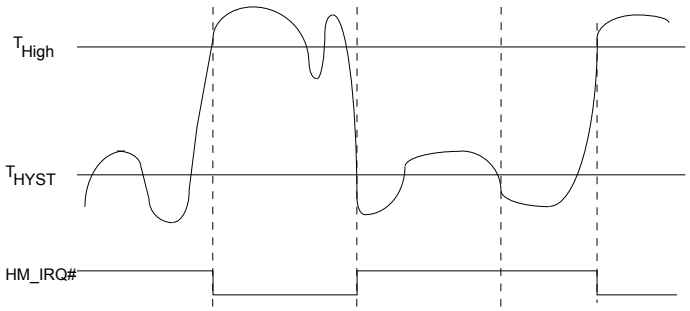
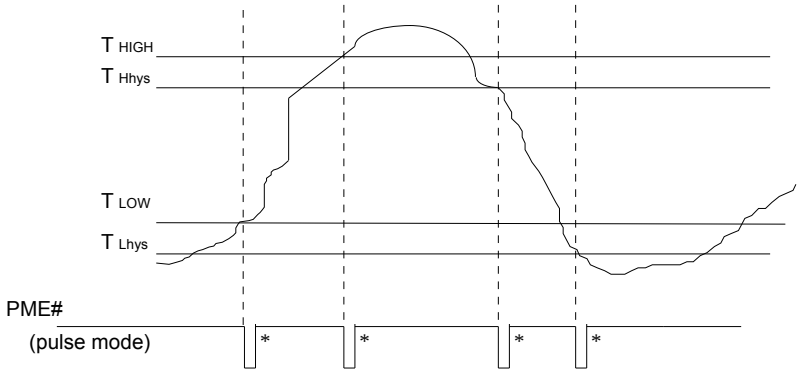


Figure 3

PME# interrupt for temperature is shown as figure. Temperature exceeding high limit (low limit) or going below high hysteresis (low hysteresis) will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Figure 4 Hysteresis mode illustration

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification.

Determine the fan counter according to:

$$Count = \frac{1.5 \times 10^6}{RPM}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by

the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$RPM = \frac{1.5 \times 10^6}{Count}$$

Fan speed control

The F71808E provides 2 fan speed control methods:

1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

The range of DC output is 0~3.3V, controlled by 8-bit register. 1 LSB is about 0.013V. The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = 3.3 \times \frac{\text{Programmed 8bit Register Value}}{255}$$

And the suggested application circuit for linear fan control would be:

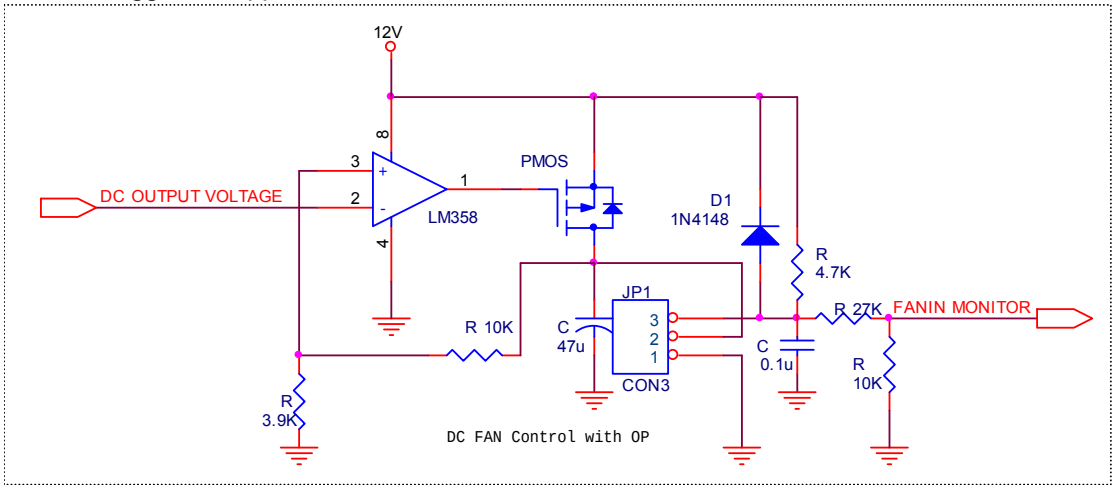


Figure 5 DAC fan control application circuit

PWM duty Fan Control

The duty cycle of PWM can be programmed by a 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

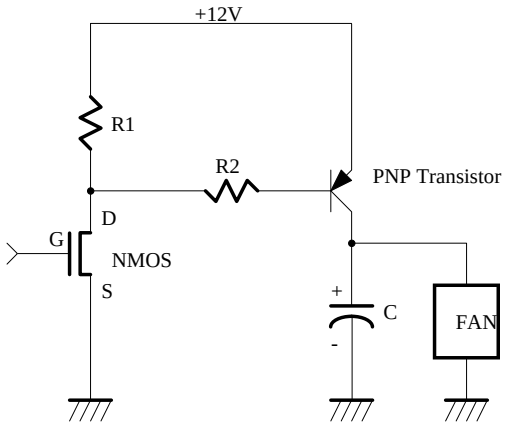


Figure 6 +12/5V PWM fan control application circuit

Fan speed control mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode 3. Linear auto mode. More detail, please refer the description of registers.

Each fan can be controlled by up to 7 kinds of temperature input. (1)D1+ temperature (2)D2+ temperature (3) PECI temperature. Please refer below structure diagram.

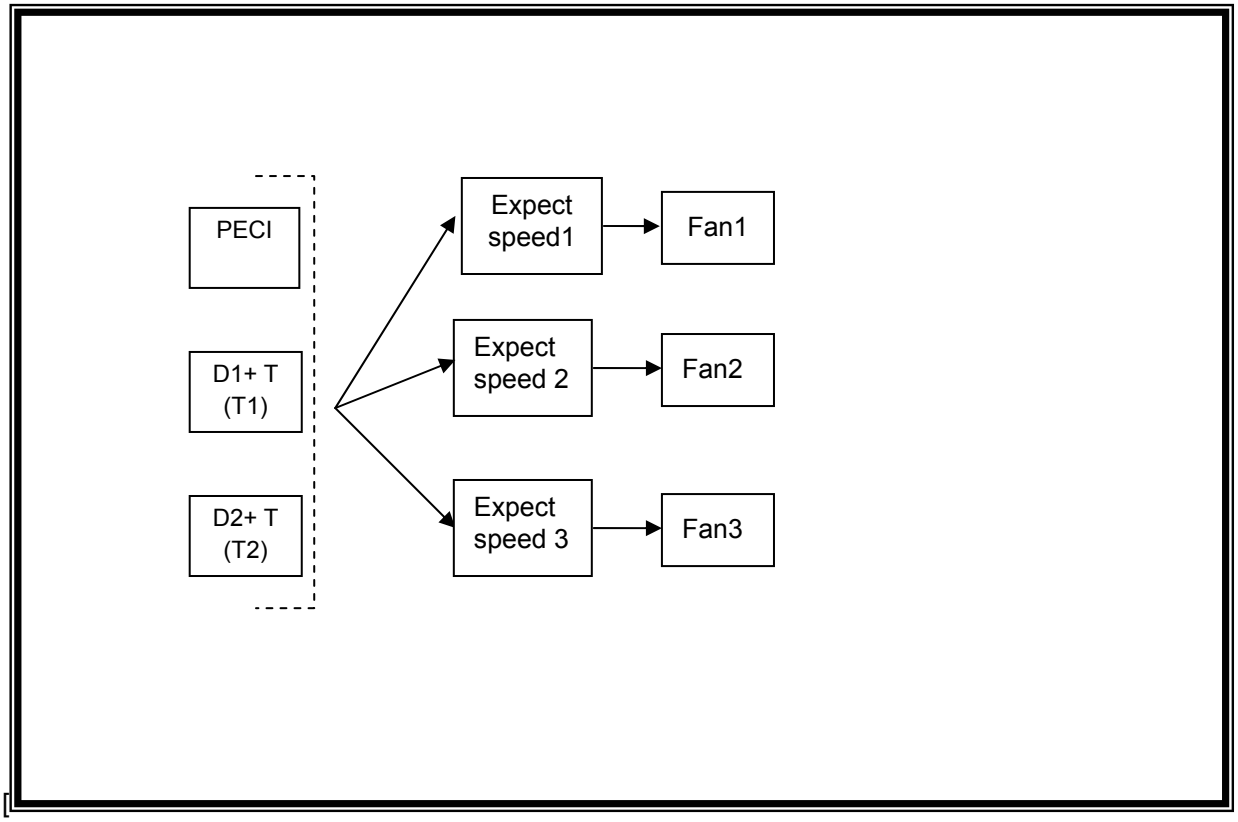


Figure 7 Relative temperature fan control

Manual mode

For manual mode, it generally acts as software fan speed control.

Stage auto mode

At this mode, the F71808E provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F71808E can provide two temperature boundaries and three intervals, and each interval has its related fan speed PWM duty. All these values should be set by BIOS first. Take figure 6-10 as example. When temperature boundaries are set as 45 and 75(C and there are three intervals. The related desired fan speed for each interval are 40%, 80% and 100% (fixed). When the temperature is within 45~75'C, the fan speed will follow 80% PWM duty and that define in registers. It can be said that the fan will be turned on with a specific speed set by BIOS and automatically controlled with the temperature variation. The F71808E will take charge of all the fan speed control and need no software support.

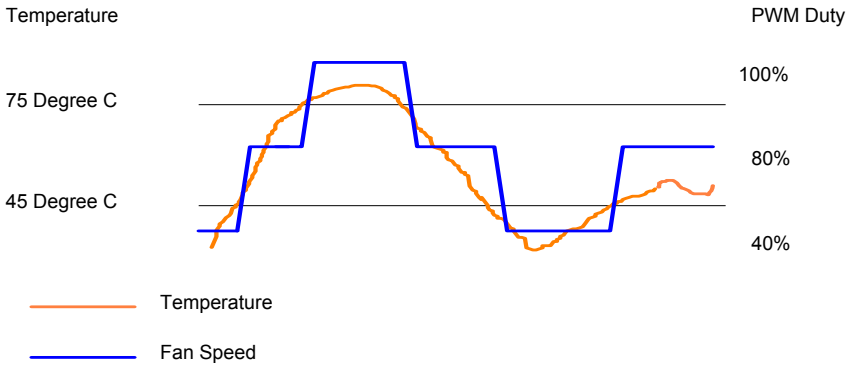


Figure 8 Stage mode fan control illustration-1

Below is a sample for Stage auto mode:

Set temperature as 60°C, 40°C and Duty as 100%, 70%, 50%

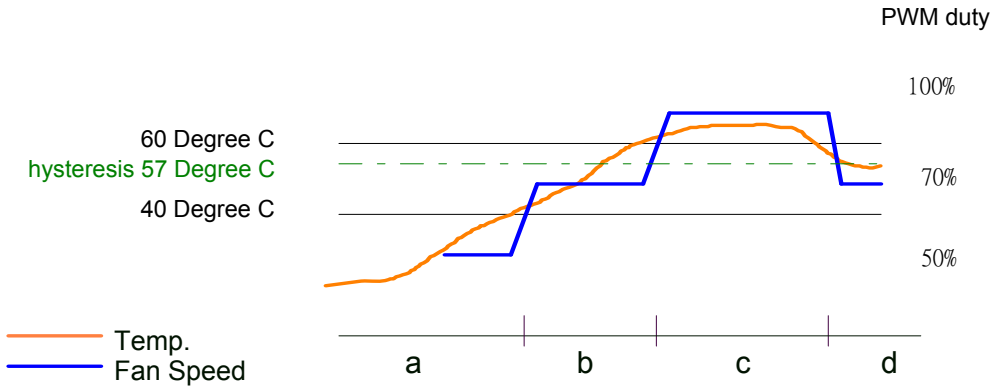


Figure 9 Stage mode fan control illustration-2

a. Once temp. is under 40°C, the lowest fan speed keeps 50% PWM duty

b. Once temp. is over 40°C,60°C, the fan speed will vary from 70% to 100% PWM duty and increase

with temp. level.

c. Once temp. keeps in 55°C, fan speed keeps in 70% PWM duty

d. If set the hysteresis as 3°C (default 4°C), once temp reduces under 57°C, fan speed reduces to 70% PWM duty and stays there.

Linear auto mode

Otherwise, F71863 supports linear auto mode. Below has a example to describe this mode. More detail, please refer the register description.

A. Linear auto mode (PWM Duty I)

Set temperature as 70°C, 40°C and Duty as 100%, 70%, 40%

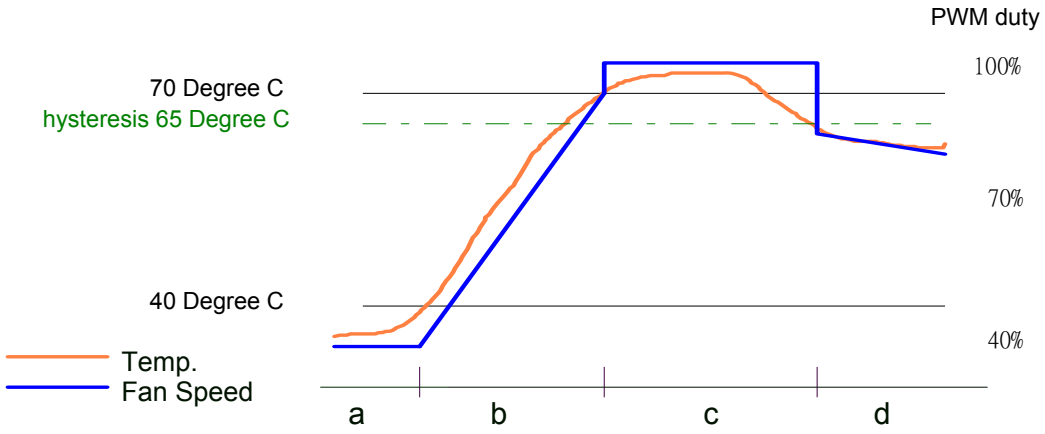


Figure 10 Linear mode fan control illustration

a. Once temp. is under 40°C, the lowest fan speed keeps 40% PWM duty

b. Once temp. is over 40°C and under 70°C, the fan speed will vary from 40% to 70% PWM duty and linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.

c. Once temp. goes over 70°C, fan speed will directly increase to 100% PWM duty (full speed)

d. If set the hysteresis as 5°C(default is 4°C), once temp reduces under 65°C (not 70°C), fan speed reduces from 100% PWM duty and decrease linearly with temp..

7.4 ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored

to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.

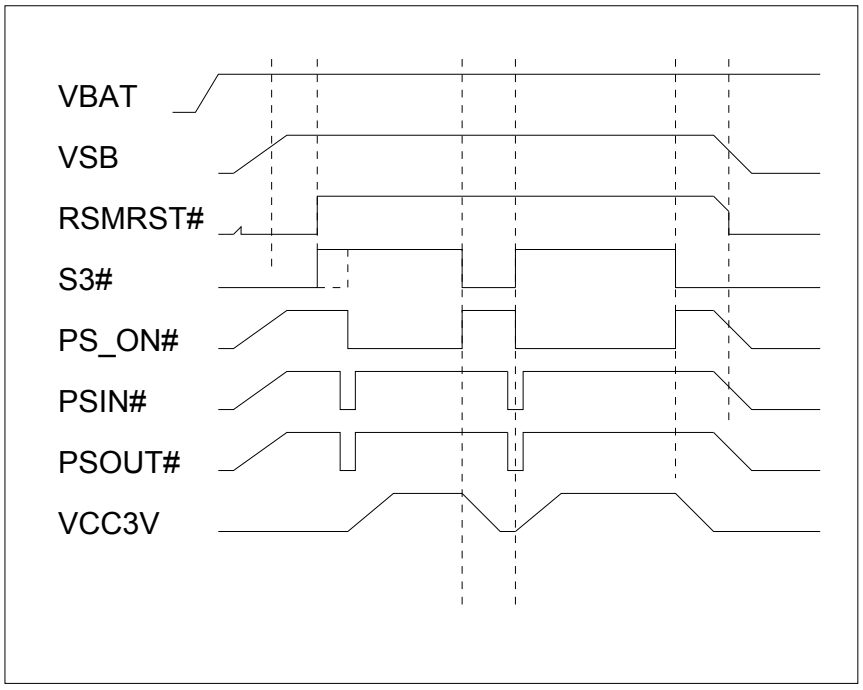


Figure 11 Default timing: Always off

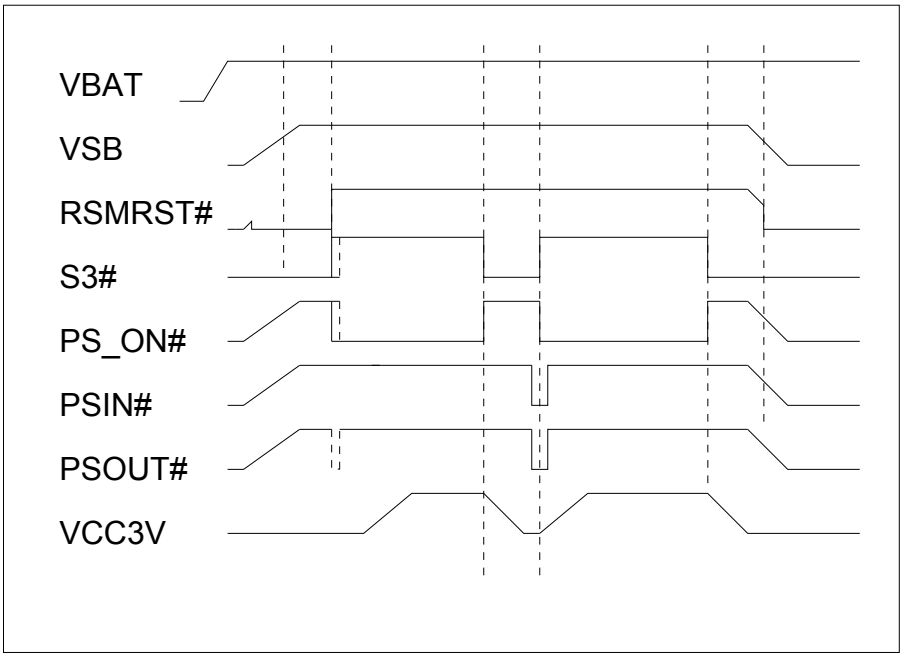


Figure 12 Optional timing: Always on

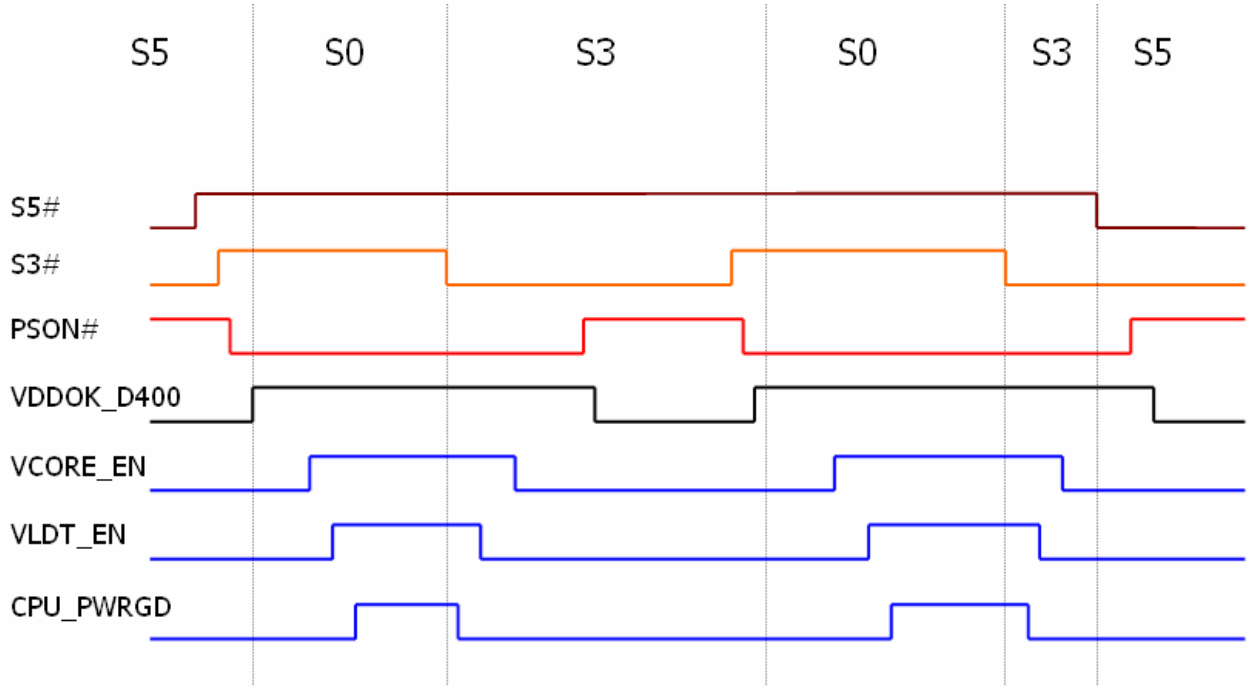


Figure 13 AMD power sequence

3VSBSW# Timing

The 3VSBSW# is used to switch the power source of the 5VDUAL which is combined by the 5VCC and 5VSB rails according to the ACPI state to control the power rail of the DIMM especially. The timing charts of the every ACPI state are mentioned in the following figures.

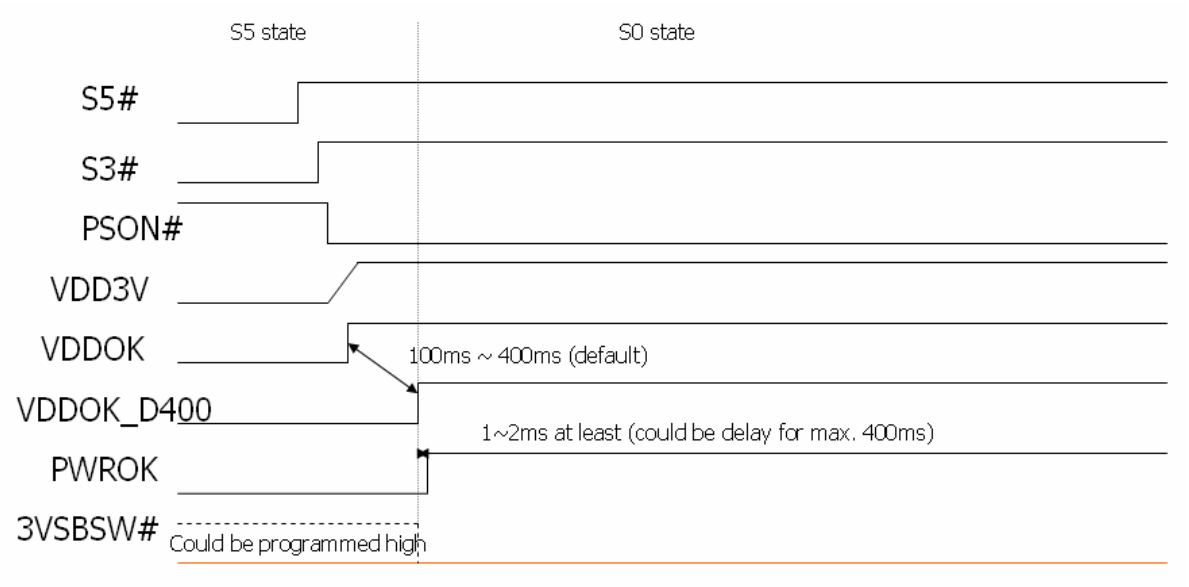


Figure 14 3VSBSW# Timing: S5 → S0

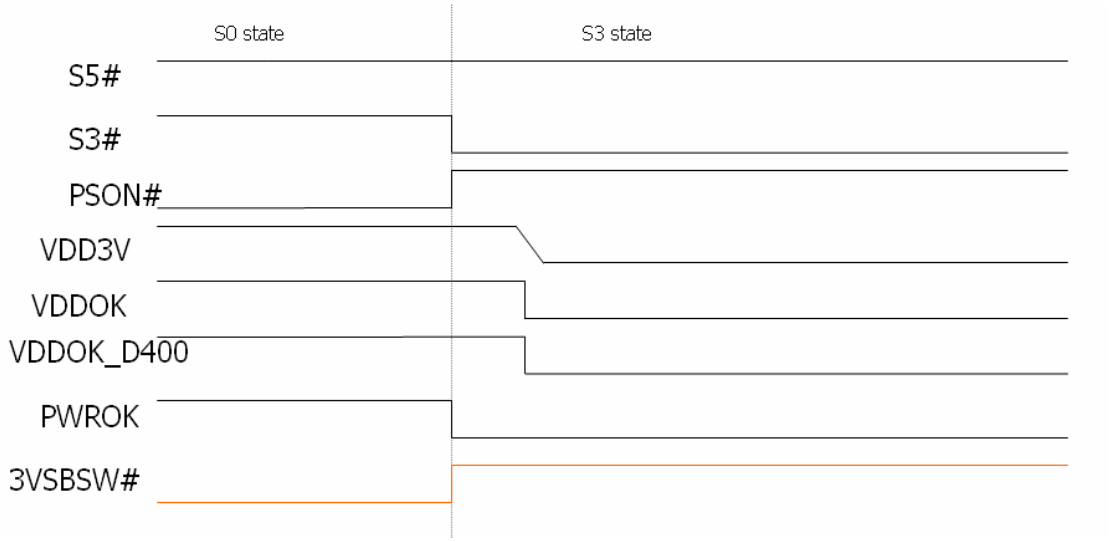


Figure 15 3VSBSW# Timing: S0 → S3

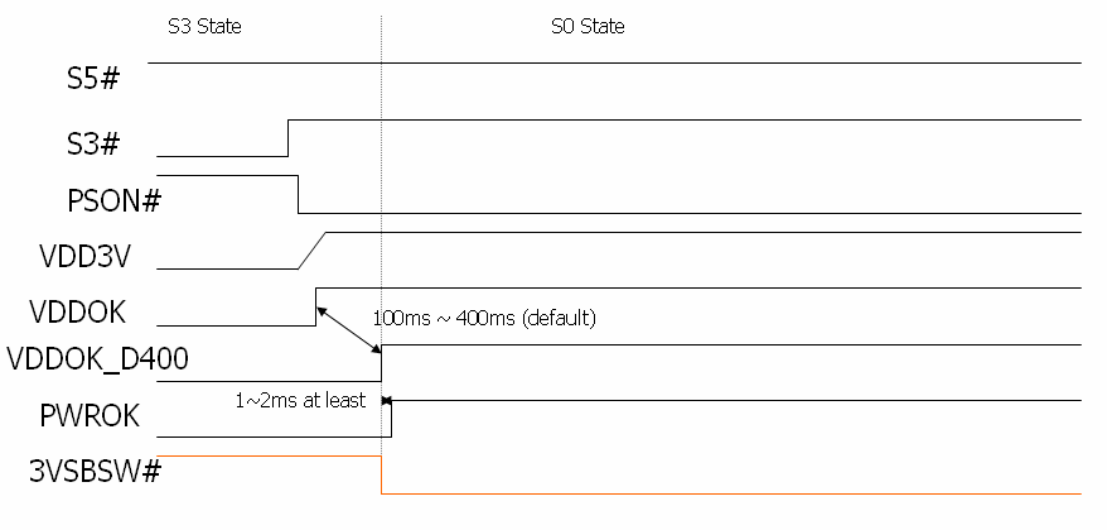


Figure 16 3VSBSW# Timing: S3 → S0

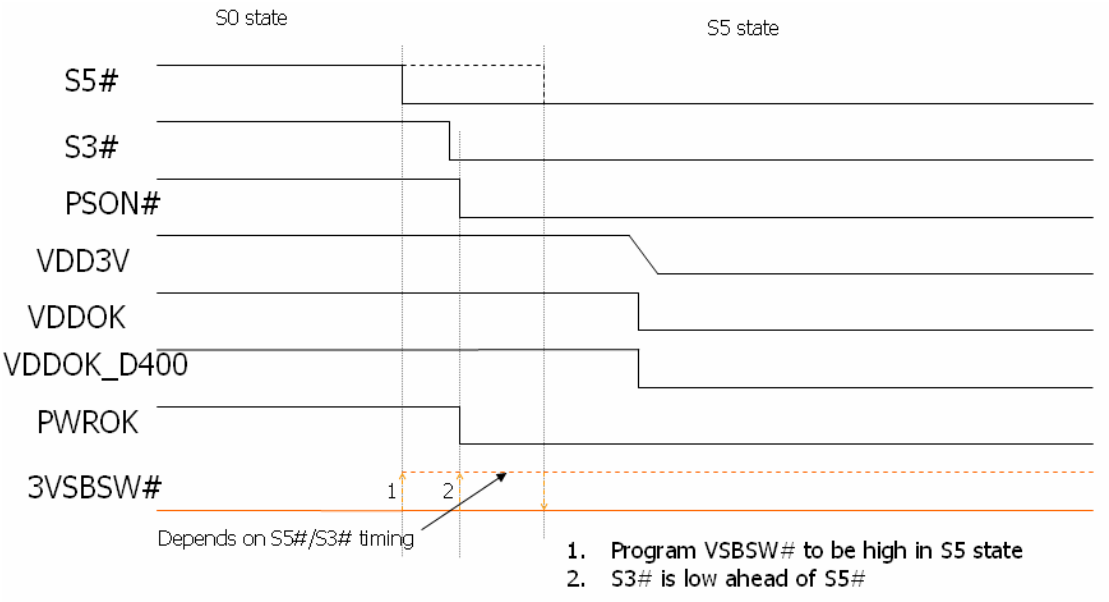
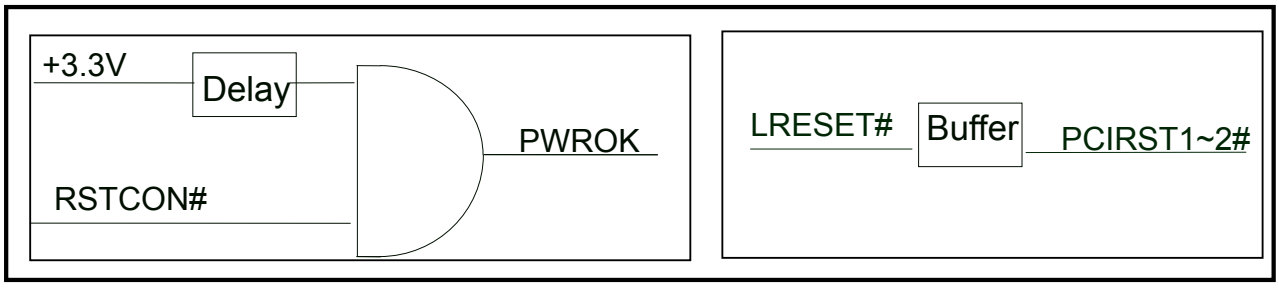


Figure 17 3VSBSW# Timing: S0 → S5

PCI Reset and PWROK Signals

The F71808E supports 2 output buffers for 2 reset signals.



So far as the PWROK issue is as the figure above. PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register (100ms ~ 400ms). An additional delay could be added to PWROK (0ms, 100ms, 200ms and 400ms). Default is 0ms. RSTCON# could be programmed to be asserted via PWROK.

7.5 INTEL PECI Function

The F71808E provides Intel PECI interface for new generational CPU temperature sensing. In Intel PECI interface, the F71808E can connect to CPU directly. The F71808E can read the temperature data from CPU, than the fan control machine of F71808E can implement the Fan to cool down CPU temperature. The application circuit is as below. More detail please refer to the register description.

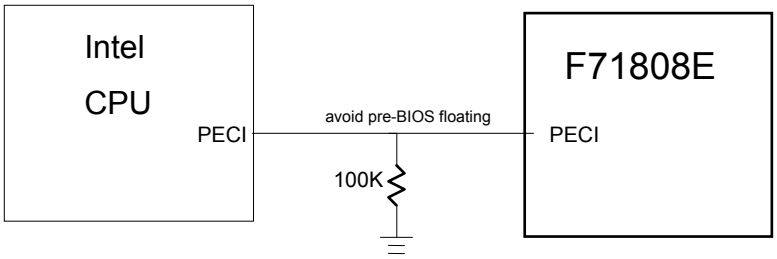


Figure 19 INTEL PECI typical application

7.6 Over Voltage Protection

The F71808E supports Over Voltage Protection (abbreviated in OVP in the following paragraph) function to avoid that the system is damaged by the higher voltage than the expected. The hardware monitors, VIN0, VIN4, and VIN5, monitor the input voltages which exceed the settings (CR31h, 35h, 36h) if OVP function is enabled (CR10h). OVP function is disabled in the default setting.

7.7 Power Saving Controller

The two pins, CTRL0# and CTRL1#, which control the standby power rail on/off to fulfil the purpose which decreases the power consumption when the system in the sleep state or the soft-off state. These two pins connected to the external PMOSs and the defaults are high in the sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, the two

pins can be programmable to set which power rail is turned on. The programmable register is powered by battery. So, the setting is kept even the AC power is lost when the register is set. At the power saving state (FINTEK calls it G3-like state), the F71808E consumes 5VSB power rail only to realize a low power consumption system.

8. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87

-o 4e 87 (enable configuration)

-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

Global Control Registers

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	0	1	0	0	1
21	Chip ID Register	0	0	0	0	0	0	0	1
23	Vendor ID Register	0	0	0	1	1	0	0	1
24	Vendor ID Register	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	-	-	-	-	0	-
26	Clock Select Register	0	-	-	-	-	0	-	-
27	Configuration Port Select Register	0	0	0	0	0	0	0	1
29	Multi-function Select Register1	0	0	0	0	0	0	0	0
2A	Multi-function Select Register2	0	0	0	0	0	0	0	0
2B	Multi-function Select Register3	0	0	1	1	1	1	1	1
2C	VBAT Dummy Register	0	0	0	0	0	0	0	0
2D	Wakeup Control Register	0	0	1	0	1	0	0	0

2E	Reserved	-	-	-	-	-	-	-	-
2F	Reserved	-	-	-	-	-	-	-	-

Device Configuration Registers

"-" Reserved or Tri-State

UART Device Configuration Registers (LDN CR01)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	UART Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	RS485 Enable Register	-	-	0	0	-	-	-	-
Hardware Monitor Device Configuration Registers (LDN CR04)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	1	0	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0
KBC Device Configuration Registers (LDN CR05)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
FE	Swap Register	1	-	-	0	0	0	0	1
FF	User Wakeup Code Register	0	0	1	0	1	0	0	1
GPIO Device Configuration Registers (LDN CR06)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
70	GPIRQ Channel Select Register	-	-	-	-	0	0	0	0
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	0	0	0	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	0	0	0	0	0	0	0	0

D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	0	0	0	0	0	0	0	0
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
D4	GPIO2 PME Enable Register	-	-	0	0	0	0	-	-
D5	GPIO2 Detect Edge Select Register	-	-	0	0	0	0	-	-
D6	GPIO2 PME Status Register	-	-	0	0	0	0	-	-
D7	GPIO2 Outpute Mode Select Register	0	0	0	0	0	0	0	0
D8	GPIO2 Pulse Width Select Register	0	0	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	0	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	0	0	0	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	0	0	0	0	0	0	0	0
F0	GPIO Output Enable Register	0	0	0	0	0	0	0	0
F1	GPIO Output Data Register	1	1	1	1	1	1	1	1
F2	GPIO Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO Drive Enable Register	0	0	0	0	0	0	0	0

WDT Device Configuration Registers (LDN CR07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	WDT Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	WDTRST# Output Enable Register	0	-	-	-	0	0	1	1
F2	Reserved	-	-	-	-	-	-	-	-
F3	Rserved	-	-	-	-	-	-	-	-
F4	Reserved	-	-	-	-	-	-	-	-
F5	WDT Unit Select Register	-	0	0	0	0	0	0	0
F6	WDT Count Register	0	0	0	0	1	0	1	0
F7	Watchdog Timer PME Register	0	0	0	-	-	-	-	-

PME, ACPI, Power Saving Device Configuration Registers (LDN CR0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0
F0	PME Event Enable Register 1	0	0	0	0	-	-	0	-
F1	PME Event Status Register 1	-	-	-	-	-	-	-	-
F2	PME Event Enable Register 2	-	-	-	-	-	-	0	0
F3	PME Event Status Register 2	-	-	-	-	-	-	-	-

F4	Keep Last State Select Register	0	0	0	0	0	1	1	0
F5	VDDOK Delay Select Register	0	0	1	1	1	1	0	0
F6	PCIRST Control Register	0	0	0	1	1	1	1	1
F7	VSBGATE Control Register	-	-	-	-	0	-	0	0
F8	LED VCC Control Register	-	-	0	0	0	0	0	0
F9	LED VSB Control Register	-	-	0	0	0	0	0	0
FE	RI De-bounce Select Register	-	-	-	-	-	-	0	0

8.1 Global Control Registers

8.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

8.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	01h: Select UART device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 0ah: Select PME, ACPI & Power Saving device configuration registers.

8.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	09h	Chip ID 1.

8.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	01h	Chip ID2.

8.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1 of Fintek devices.

8.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2 of Fintek devices.

8.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1	SOFTPD_UR	R/W	0	Write “1” to disable UART clock.
0	Reserved	-	-	Reserved.

8.1.8 UART IRQ Sharing Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R/W	0	0: CLKIN is 48MHz 1: CLKIN is 24MHz
6-3	Reserved	-	-	Reserved.
2	TX_DEL_1BIT	R/W	0	0: UART TX transmits data immediately after writing THR. 1: UART TX transmits data one bit time after writing THR.
1-0	Reserved	-	-	Reserved.

8.1.9 Configuration Port Select Register — Index 27h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	PORT_4E_EN	R/W	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1/ Config4E_2E. Pull down to select port 2E/2F.
3-1	Reserved	-	-	Reserved.
0	TIMING_EN	R/W	1	0: Disable timing sequence. 1: Enable timing sequence.

8.1.10 Multi-Function Select Register 1 — Index 29h (Powered by VSB3V)

Bit	Name	R/W	Default	Description

7-6	UR_GP_EN	R/W	0	UART/GPIO function select. 00 : All Pins for UART 01: SIN/SOUT enable, other pins are GPIOs. 10: SIN/SOUT/RTS# enable, other pins are GPIOs. 11: All pins are GPIOs.
5	Reserved	-	-	Reserved
4	GPIO34_EN	R/W	0	SYSFANOUT/GPIO34 function select. 0: The pin function is SYSFANOUT. 1: The pin function is GPIO34.
3-2	Reserved	-	-	Reserved
1	GPIO31_EN	R/W	0	VLDT_EN/GPIO31 function select. 0: The pin function is VLDT_EN 1: The pin function is GPIO31
0	GPIO30_EN	R/W	0	VCORE_EN/GPIO34 function select. 0: The pin function is VCORE_EN 1: The pin function is GPIO30

8.1.11 Multi-Function Select Register 2 — Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	PSOUT_GP_EN	R/W	0	PSOUT#/GPIO14 function select. 0: The pin function is PSOUT#. 1: The pin function is GPIO14.
3	FANIN2_GP23_EN	R/W	0	GPIO23/WDTRST#/SYSFANIN2 function select. 0: The pin function is GPIO23/WDTRST#. 1: The pin function is FANIN2
2	FANIN2_GP21_EN	R/W	0	GPIO21/OVT#/SYSFANIN2 function select. 0: The pin function is GPIO21/OVT#. 1: The pin function is FANIN2. The priority of FANIN3_GP23_EN is higher than FANIN3_GP21_EN.

1	KB_GP_EN	R/W	0	KBC/GPIO function select. 0: The pin function of pin 14 and 15 are KDATA and KCLK respectively. 1: The pin function of pin 14 and 15 are GPIO10 and GPIO11 respectively.
0	MO_GP_EN	R/W	0	KBC/GPIO function select. 0: The pin function of pin 16 and 17 are MDATA and MCLK respectively. 1: The pin function of pin 16 and 17 are GPIO12 and GPIO13 respectively.

8.1.12 Multi-Function Select Register 3 — Index 2Bh (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO27_EN	R/W	0	PSIN#/GPIO27 function select. 0: The pin function is PSIN#. 1: The pin function is GPIO27.
6	GPIO26_EN	R/W	0	RESETCON#/GPIO26 function select. 0: The pin function is RESETCON#. 1: The pin function is GPIO26.
5	GPIO25_EN	R/W	1	GPIO25/LEDVCC function select. 0: The pin function is LEDVCC. 1: The pin function is GPIO25.
4	GPIO24_EN	R/W	1	GPIO24/LEDVSB function select. 0: The pin function is LEDVSB. 1: The pin function is GPIO24.
3	GPIO23_EN	R/W	1	GPIO23/WDTRST#/SYSFANIN2 function select. 0: The pin function is WDTRST#. 1: The pin function is GPIO23. This bit has effect only if FANIN3_GP23_EN is “0”.
2	GPIO22_EN	R/W	1	GPIO22/SYSFANOUT2 function select. 0: The pin function is SYSFANOUT2. 1: The pin function is GPIO22.

1	GPIO21_EN	R/W	1	GPIO21/OVT#/SYSFANIN2 function select. 0: The pin function is OVT#. 1: The pin function is GPIO21. This bit has effect only if FANIN3_GP21_EN is “0”.
0	GPIO20_EN	R/W	1	GPIO20/PME# function select. 0: The pin function is PME#. 1: The pin function is GPIO20.

8.1.13 Wakeup Control Register — Index 2Dh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	VSBOK_HYS_DIS	R/W	0	0: Enable VSBOK detect hysteresis. 1: Disable VSBOK detect hysteresys.
5	VSBOK_LVL_SEL	R/W	1	0: VSB3V power good level is 3.05V and not good level is 2.95V. 1: VSB3V power good level is 2.8V and not good level is 2.5V. By VSBOK_HYS_DIS and VSBOK_LVL_SEL, RSMRST# falling edge could be determined: 00: when VSB3V is lower than 2.95V. 01: when VSB3V is lower than 2.5V. 10: when VSB3V is lower than 3.05V. 11: when VSB3V is lower than 2.8V.
4	KEY_SEL_ADD	R/W	0	This bit is added to add more wakeup key function.
3	WAKEUP_EN	R/W	1	0: disable keyboard/mouse wake up. 1: enable keyboard/mouse wake up.

<table>
<tr><td>2-1</td><td>KEY_SEL</td><td>R/W</td><td>00</td><td>This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
<table>
<tr><th>KEY_SEL_ADD</th><th>KEY_SEL</th><th>Wakeup Key</th></tr>
<tr><td>0</td><td>00</td><td>Ctrl + Esc</td></tr>
<tr><td>0</td><td>01</td><td>Ctrl + F1</td></tr>
<tr><td>0</td><td>10</td><td>Ctrl + USER_WAKEUP_CODE (SPACE)</td></tr>
<tr><td>0</td><td>11</td><td>Any Key</td></tr>
<tr><td>1</td><td>00</td><td>Windows Wakeup</td></tr>
<tr><td>1</td><td>01</td><td>Windows Power</td></tr>
<tr><td>1</td><td>10</td><td>Ctrl + Alt + USER_WAKEUP_CODE (SPACE)</td></tr>
<tr><td>1</td><td>11</td><td>USER_WAKEUP_CODE (SPACE)</td></tr>
</table></td></tr>
<tr><td>0</td><td>MO_SEL</td><td>R/W</td><td>0</td><td>This register select the mouse wake up key.
0: Wake up by click.
1: Wake up by click and movement.</td></tr>
</table>

8.2 UART Registers (CR01)

8.2.1 UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR_EN	R/W	1	0: disable UART. 1: enable UART.

8.2.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART base address.

8.2.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART base address.

8.2.4 IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELURIRQ	R/W	4h	Select the IRQ channel for UART.

8.2.5 RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	RS485_INV	-	-	Write “1” will invert the RTS# if RS485_EN is set.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. RTS# drive high when transmitting data, otherwise is kept low.
3-0	Reserved	-	-	Reserved.

8.3 Hardware Monitor Register (CR04)

8.3.1 Hardware Monitor Configuration Registers

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description

7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

8.3.2 Device Registers

Before the device registers, the following is a register map order which shows a summary of all registers. Please refer each one register if you want more detail information.

Register CR01 ~ CR03 → Configuration Registers

Register CR0A ~ CR0F → PECI/SST Control Register

Register CR10 ~ CR4F → Voltage Setting Register

Register CR60 ~ CR8E → Temperature Setting Register

Register CR90 ~ CRDF → Fan Control Setting Register

→Fan1 Detail Setting CRA0 ~ CRAF

→Fan2 Detail Setting CRB0 ~ CRBF

→Fan3 Detail Setting CRC0 ~ CRCF

→Fan4 Detail Setting CRD0 ~ CRDF

Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	Reserved	-	-	Reserved
5-4	OVT_MODE	R/W	0	00: The OVT# will be low active level mode. 01: The OVT# will be high active level mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3-0	Reserved	-	-	Reserved

Configuration Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

Configuration Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-2	VTT_SEL	R/W	0	PECI (Vtt) voltage select. 00: Vtt is 1.23V 01: Vtt is 1.13V 10: Vtt is 1.00V 11: Vtt is 1.00V
1-0	FUNC_SEL	R/W	0	Function select bits to select PECI function. 00: Disable PECI Function 01: Reserved 10: Enable PECI Function 11: Reserved

Configuration Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping() command to find CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 1, i.e. PECI address is 0x31. 0100: CPU is in socket 2, i.e. PECI address is 0x32. 1000: CPU is in socket 3, i.e. PECI address is 0x33. Otherwise are reserved.
3-1	Reserved	-	-	Reserved.
0	DOMAIN1_EN	R/W	0	If the CPU selected is dual core. Set this register 1 to read the temperature of domain1.

Configuration Register — Index 0Ch

Bit	Name	R/W	Default	Description

7-0	TCC_TEMP	R/W	55h	TCC Activation Temperature. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127.

Configuration Register — Index 0Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	PECI_REQ_EN	R/W	1	0: disable the PECI_REQ# function. 1: Enable the PECI_REQ# function.
4-2	Reserved	-	-	Reserved.
1-0	DIG_RATE_SEL	R/W	0	The accessing rate for PECI to access external slave device. 0: Access slave device after 1 diode temperature conversion 1: Access slave device after 2 diode temperature conversion 2: Access slave device after 3 diode temperature conversion 3: Access slave device after 4 diode temperature conversion

Voltage Setting

Over-Voltage Shut Down Enable Register — Index 10h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	V5_OVV_EN	R/W	0	A one enables the shut down event when V5 is over V5_OVV_LIMIT.
4	V4_OVV_EN	R/W	0	A one enables the shut down event when V4 is over V4_OVV_LIMIT.
3-1	Reserved	-	-	Reserved.
0	V0_OVV_EN	R/W	0	A one enables the shut down event when V0 is over V0_OVV_LIMIT.

Over-Voltage Status Register (Powered by VBAT) — Index 11h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved

0	V_EXC_OVV	R/WC	0	This bit is over-voltage status. Once one of the monitored voltages (VCC3V, VIN4, VIN5) over its related over-voltage limits and its related over-voltage shut down enable bit is set, this bit will be set to 1. Write a 1 to this bit will clear it to 0. (This bit is powered by VBAT)

Voltage reading and limit— Index 20h- 4Fh

Address	Attribute	Default Value	Description
20h	RO	--	VCC3V reading. The unit of reading is 8mV.
21h	RO	--	V1 (Vcore) reading. The unit of reading is 8mV.
22h	RO	--	V2 reading. The unit of reading is 8mV.
23h	RO	--	V3 reading. The unit of reading is 8mV.
24h	RO	--	V4 reading. The unit of reading is 8mV.
25h	RO	--	V5 reading. The unit of reading is 8mV.
26h	--	--	Reserved
27h	RO	--	VSB3V reading. The unit of reading is 8mV.
28h	RO	--	VBAT reading. The unit of reading is 8mV.
29~2Ch	RO	--	Reserved
2Dh	RO	--	FAN1 present fan duty reading
2Eh	RO	--	FAN2 present fan duty reading
2Fh	RO	--	FAN3 present fan duty reading
30h	--	--	Reserved
31h	R/W	FF	V0 over-voltage limit (V0_OVV_LIMIT). The unit is 9mv.
32~34h	RO	--	Reserved
35h	R/W	FF	V4 over-voltage limit (V4_OVV_LIMIT). The unit is 9mv.
36h	R/W	FF	V5 over-voltage limit (V5_OVV_LIMIT). The unit is 9mv.
37~4Fh	RO	--	Reserved

Temperature Setting

Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	Reserved	R	-	Reserved
6	EN_ T2_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.

5	EN_ T1_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	R	-	Reserved
3	Reserved	R	-	Reserved
2	EN_ T2_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R	-	Reserved

Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	T2_OVT _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
5	T1_OVT _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	T2_EXC _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
1	T1_EXC _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	-	-	Reserved

Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.

4	Reserved	-	-	Reserved
3	Reserved	-	-	Reserved
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	-	-	Reserved

T1 Over-OVT and Over-High Limit Temperature Select Register — Index 64h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-4	T1_OVT_TEMP_SEL	R/W	0	Set this bit to select the temperature source of T1_OVT_LIMIT. 00: Diode T1 Temperature 01: PECI Temperature 10: Reserved 11: Reserved
3-2	Reserved	-	-	Reserved
1-0	T1_HIGH_TEMP_SEL	R/W	0	Set this bit to select the temperature source of T1_HIGH_LIMIT. 00: Diode T1 Temperature 01: PECI Temperature 10: Reserved 11: Reserved

OVT Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	EN_T2_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	-	-	Reserved.

Temperature1 Offset Register -- Index 67-68h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved

2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	-	-	Reserved

TEMP1 Limit Hystersis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	-	-	Reserved

TEMP2 and TEMP3 Limit Hystersis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3-0	TEMP2_HYS	R/W	4h	Limit hysteresis. (0~15 degree C) Temperature and below the (boundary – hysteresis).

DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	PECI_OPEN	RO	0h	When PECI interface is enabled, it indicates an error code (0x0080 or 0x0081) is received from PECI slave.
4-3	Reserved	-	-	Reserved
2	T2_DIODE_OPEN	RO	0h	Set to 1 when external diode 2 is open or short
1	T1_DIODE_OPEN	RO	0h	Set to 1 when external diode 1 is open or short
0	Reserved	-	-	Reserved

Diode T1 Temperature Scale Register -- Index 7Fh

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
3	ADD	R/W	0h	Diode T1 Temperature scale selection. 1: Temp. = Reading Value + Reading Value* $2^{-DIODE\_T1\_SCALE}$ 0: Temp. = Reading Value - Reading Value* $2^{-DIODE\_T1\_SCALE}$
2	Reserved	-	-	Reserved

1-0	SCALE	R/W	0h	When ADD is 1, Diode T1 Temp. is selected by SCALE 00: Temp. = 1 * Reading Value 01: Temp. = 17/16 * Reading Value 10: Temp. = 33/32 * Reading Value 11: Temp. = 65/64 * Reading Value When ADD is 0, Diode T1 Temp. is selected by SCALE 00: Temp. = 1 * Reading Value 01: Temp. = 15/16 * Reading Value 10: Temp. = 31/32 * Reading Value 11: Temp. = 63/64 * Reading Value

Temperature — Index 70h- 8Fh

Address	Attribute	Default Value	Description
70h	Reserved	--	Reserved
71h	Reserved	--	Reserved
72h	RO	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	RO	--	Reserved
74h	RO	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h	RO	--	Reserved
76h	RO	--	Reserved
77-79h	RO	--	Reserved
7Eh	RO	--	The data of CPU temperature from digital interface after IIR filter. (Only available if PECI interface is enabled)
80h	--	--	Reserved
81h	--	--	Reserved
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1°C.
86-8Bh	--	--	Reserved
8C~8Dh	--	--	Reserved

Fan Control Setting

FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	EN_FAN3_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt.. Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	FAN3_STS	R/W	-	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	-	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	-	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved
2	FAN3_EXC	RO	-	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	RO	-	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	RO	-	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

FAN Full Speed Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	FULL_WITH_T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4-0	Reserved	-	-	Reserved.

Fan Type Select Register -- Index 94h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	SYSFAN2_TYPE	R/W	2'b 1S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by SYSFAN2OUT 0: SYSFAN2OUTis pull up by external resistor. 1: SYSFAN2OUT is pull down by internal 100K resistor.
3-2	SYSFAN1_TYPE	R/W	2'b 1S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by SYSFAN1OUT 0: SYSFAN1OUT is pull up by external resistor. 1: SYSFAN1OUT is pull down by internal 100K resistor.
1-0	CPUFAN_TYPE	R/W	2'b 10	00: Output PWM mode (push pull) to control fans. 10: Output PWM mode (open drain) to control Intel 4-wire fans.

S: Register default values are decided by trapping.

Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.

5-4	FAN3_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xC6-0xCE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defined in 0xC6-0xCE. 10: Manual mode fan control, user can write expect **RPM** count to 0xC2-0xC3, and F71808E will auto control duty cycle (PWM fan type) or voltage(linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage(linear fan type) to 0xC3, and F71808E will output this value duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that defined in 0xB6-0xBE. 10: Manual mode fan control, user can write expect **RPM** count to 0xB2-0xB3, and F71808E will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F71808E will output this value duty or voltage to control fan speed.
1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that define in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defined in 0xA6-0xAE. 10: Manual mode fan control, user can write expect **RPM** count to 0xA2-0xA3, and F71808E will auto control duty cycle (PWM fan type) or voltage(linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage(linear fan type) to 0xA3, and F71808E will output this value duty or voltage to control fan speed.

Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description

7-4	FAN2_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Auto Fan3 Boundary Hystersis Select Register -- Index 99h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_HYS	R/W	2h	0000: Boundary hysteresis. (0~15 degree C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Auto Fan Up Speed update Rate Select Register -- Index 9Bh (FAN_PROG_SEL = 0)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	SYSFAN2_ UP_RATE	R/W	1h	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	SYSFAN1_ UP_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	CPUFAN _UP_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

Auto Fan Down Speed update Rate Select Register -- Index 9Bh (FAN_RATE_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	Direct_Update	R/W	0	0: Fan duty update rate is defined in bit[5:0] 1: Fan duty is updated to the desired
5-4	FAN3_DOWN_RAT E	R/W	1h	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_DOWN_RAT E	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

1-0	FAN1_DOWN_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN POWER-ON DEFAULT DUTY-CYCLE/VOLTAGE — Index 9Eh

Bit	Name	R/W	Default	Description
7-0	PWRON_DEF_DUTY	R/W	8'h66	Fan duty value immediately loaded after VDD is powered on. If this byte is ever programmed, it will be used as the power-on default duty.

Fan Fault Time Register -- Index 9Fh

Bit	Name	R/W	Default	Description
7	FAN_PROG_SEL	R/W	0	Set this bit to "1" will enable access registers of other bank.
6-5	Reserved	-	-	Reservd

4	FULL_DUTY_SEL	R/W	-	0: The Fan duty value immediately loaded after VDD is powered-on is 100% if PWRON_DEF_DUTY is not been programmed. 1: The Fan duty value immediately loaded after VDD is powered-on is 40% if PWRON_DEF_DUTY is not been programmed. (pull up by internal 47K resistor). This register is power on trap by DTR#.
3-0	Reserved	-	-	Reserved

Fan1 Index A0h- AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. **Duty mode(CR96 bit0=1):** This byte is reserved byte.
A3h	R/W	8'h01	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit0=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description

7-0	BOUND1TMP1	R/W	3Ch (60^oC)	The 1st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **1** register (index AA)h. When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **2** register (index AAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

VT1 BOUNDARY 2 TEMPERATURE – Index A9

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP1	R/W	1Eh (30^oC)	The 2st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is **exceed** this boundary, FAN1 expect value will load from segment **2** register (index AB)h. When VT1 temperature is **below** this boundary – hysteresis, FAN1 expect value will load from segment **3** register (index ABh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description

7-0	SEC2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 3 SPEED COUNT – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_TEMP_SEL_DIG	R/W	0	This bit companying with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	Reserved	-	0	Reserved
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP_HIGH_EN	R/W	1	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_UP_RATE register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.

2	FAN1_JUMP_LOW_EN	R/W	1	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_DN_RATE register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	1	This registers companying with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR7Eh) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). Otherwise: reserved.

Fan2 Index B0h- BFh

Address	Attribute	Default Value	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (MSB), in auto fan mode(CR96 bit3➔0) this register is auto updated by hardware. **Duty mode(CR96 bit2=1):** This byte is reserved byte.
B3h	R/W	8'h01	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit2=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating

			when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP2	R/W	3Ch (60^oC)	The 1st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **1** register (index BA)h. When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **2** register (index BAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

VT2 BOUNDARY 2 TEMPERATURE – Index B9

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP2	R/W	1Eh (30^oC)	The 2st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is **exceed** this boundary, FAN2 expect value will load from segment **2** register (index BB)h. When VT2 temperature is **below** this boundary – hysteresis, FAN2 expect value will load from segment **3** register (index BBh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description

7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 3 SPEED COUNT – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_TEMP_SEL_DIG	R/W	0	This bit companying with FAN2_TEMP_SEL select the temperature source for controlling FAN2.
6	Reserved	-	-	Reserved

5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_HIGH_EN	R/W	1	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_UP_RATE register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_LOW_EN	R/W	1	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_DN_RATE register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.
1-0	FAN2_TEMP_SEL	R/W	10	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR7Eh) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 3 (CR76h). Otherwise: reserved.

Fan3 Index C0h- CFh

Address	Attribute	Default Value	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hff	FAN3 count reading (LSB).
C2h	R/W	8'h00	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (MSB), in auto fan mode(CR96 bit5➔0) this register is auto updated by hardware.

			Duty mode(CR96 bit4=1): This byte is reserved byte.
C3h	R/W	8'h01	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (LSB) or expect PWM duty , in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit4=1):** The Value programming in this byte is duty value. In auto fan mode(CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	8'hff	FAN3 full speed count reading (LSB).

VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP3	R/W	3Ch (60°C)	The 1st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **1** register (index CA)h. When VT3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **2** register (index CAh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

VT3 BOUNDARY 2 TEMPERATURE – Index C9

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP3	R/W	1Eh (30°C)	The 2st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is **exceed** this boundary, FAN3 expect value will load from segment **2** register (index CB)h. When VT3 temperature is **below** this boundary – hysteresis, FAN3 expect value will load from segment **3** register (index CBh). This byte is a 2's complement value ranging from -128'C ~ 127'C.

FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED3	R/W	FFh (100%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED3	R/W	D9h (85%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 3 SPEED COUNT – Index CEh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED3	R/W	80h (50%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Default	Description
7	FAN3_TEMP_SEL_DIG	R/W	0	This bit companying with FAN3_TEMP_SEL select the temperature source for controlling FAN3.

6	PWM_FREQ_SEL	R/W	0	FAN3 PWM duty selection 0: 23.5KHz 1: 220Hz
5	FAN3_UP_T_EN	R/W	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_INTERPOLATION_EN	R/W	1	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_HIGH_EN	R/W	1	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_UP_RATE register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.
2	FAN3_JUMP_LOW_EN	R/W	1	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_DN_RATE register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	10	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR7Eh) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 3 (CR76h). Otherwise: reserved.

8.4 KBC Registers (CR05)

8.4.1 KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

8.4.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4;

8.4.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

8.4.4 KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	1h	Select the IRQ channel for keyboard interrupt.

8.4.5 Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	Ch	Select the IRQ channel for PS/2 mouse interrupt.

8.4.6 Clock Select Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	SELCLK_KBC	R/W	10	00: select 6MHz clock as KBC clock input. 01: select 8MHz clock as KBC clock input. 10: select 12MHz clock as KBC clock input (default). 11: select 16MHz clock as KBC clock input.

5-2	Reserved	-	-	Reserved.
1	GA20_EN	R/W	1	0: GATE20# software control. 1: GATE20# hardware speed up.
0	HKBRST	R/W	1	0: KBRST# software control. 1: KBRST# hardware speed up.

8.4.7 Auto Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	1b	0: disable auto detect keyboard/mouse swap. 1: enable auto detect keyboard/mouse swap.
6-5	Reserved	-	-	Reserved.
4	KB_MO_SWAP	R/W	0b	0: Keyboard/mouse not swap. 1: Keyboard/mouse swap. This bit is set/clear by hardware if AUTO_DET_EN is set to "1". Users could also program this bit manually.
3-0	Reserved	-	-	Reserved.

8.4.8 User Wakeup Code Register — Index FFh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7-0	USER_WAKEUP_CODE	R/W	29h	This is user define wakeup code. Default is space.

8.5 GPIO Registers (CR06)

8.5.1 GPIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELGPIRQ	R/W	0h	Select the IRQ channel for GPIO interrupt.

8.5.2 GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO34_OE	R/W	0	0: GPIO34 is in input mode. 1: GPIO34 is in output mode.

3	GPIO33_OE	R/W	0	0: GPIO33 is in input mode. 1: GPIO33 is in output mode.
2	GPIO32_OE	R/W	0	0: GPIO32 is in input mode. 1: GPIO32 is in output mode.
1	GPIO31_OE	R/W	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode.
0	GPIO30_OE	R/W	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode.

8.5.3 GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO34_VAL	R/W	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

8.5.4 GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO34_IN	R	-	The pin status of SYSFANOUT1/GPIO34.
3	GPIO33_IN	R	-	The pin status of PECI_REQ/ GPIO33.
2	GPIO32_IN	R	-	The pin status of PECI/ GPIO32.
1	GPIO31_IN	R	-	The pin status of VLDT_EN

8.5.5 GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO34_DRV_EN	R/W	0	0: GPIO34 is open drain in output mode. 1: GPIO34 is push pull in output mode.
3	GPIO33_DRV_EN	R/W	0	0: GPIO33 is open drain in output mode. 1: GPIO33 is push pull in output mode.
2	GPIO32_DRV_EN	R/W	0	0: GPIO32 is open drain in output mode. 1: GPIO32 is push pull in output mode.

1	GPIO31_DRV_EN	R/W	0	0: GPIO31 is open drain in output mode. 1: GPIO31 is push pull in output mode.
0	GPIO30_DRV_EN	R/W	0	0: GPIO30 is open drain in output mode. 1: GPIO30 is push pull in output mode.

8.5.6 GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO26 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

8.5.7 GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	0	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs 1 when in output mode.
6	GPIO26_VAL	R/W	0	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs 1 when in output mode.
5	GPIO25_VAL	R/W	0	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	0	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	0	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	0	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	0	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	0	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

8.5.8 GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of PSIN#/GPIO27.
6	GPIO26_IN	R	-	The pin status of RESETCON#/GPIO26.
5	GPIO25_IN	R	-	The pin status of GPIO25/LEDVCC.
4	GPIO24_IN	R	-	The pin status of GPIO24/LEDVSB.
3	GPIO23_IN	R	-	The pin status of GPIO23/WDTRST#/SYSFANIN2.
2	GPIO22_IN	R	-	The pin status of GPIO22/SYSFANOUT2.
1	GPIO21_IN	R	-	The pin status of GPIO21/OVT#/SYSFANIN2.
0	GPIO20_IN	R	-	The pin status of GPIO20/PME#.

8.5.9 GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Default	Description
7	GPIO27_DRV_EN	R/W	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

8.5.10 GPIO2 PME Enable Register — Index D4h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO25_PME_EN	R/W	0	When GPIO25_PME_STS is 1 and GPIO25_PME_EN is set to 1, a GPIO PME event will be generated.
4	GPIO24_PME_EN	R/W	0	When GPIO24_PME_STS is 1 and GPIO24_PME_EN is set to 1, a GPIO PME event will be generated.
3	GPIO23_PME_EN	R/W	0	When GPIO23_PME_STS is 1 and GPIO23_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO22_PME_EN	R/W	0	When GPIO22_PME_STS is 1 and GPIO22_PME_EN is set to 1, a GPIO PME event will be generated.
1-0	Reserved	-	-	Reserved.

8.5.11 GPIO2 Input Detection Select Register — Index D5h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO25_DET_SEL	R/W	0	When GPIO25 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
4	GPIO24_DET_SEL	R/W	0	When GPIO24 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
3	GPIO23_DET_SEL	R/W	0	When GPIO23 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
2	GPIO22_DET_SEL	R/W	0	When GPIO22 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
1-0	Reserved	-	-	Reserved.

8.5.12 GPIO2 Event Status Register — Index D6h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	GPIO25_PME_STS	R/WC	0	When GPIO25 is in input mode and a GPIO25 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
4	GPIO24_PME_STS	R/WC	0	When GPIO24 is in input mode and a GPIO24 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
3	GPIO23_PME_STS	R/WC	0	When GPIO23 is in input mode and a GPIO23 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
2	GPIO22_PME_STS	R/WC	0	When GPIO22 is in input mode and a GPIO22 input is detected, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1-0	Reserved	-	-	Reserved.

8.5.13 GPIO2 Output Mode Status Register — Index D7h

Bit	Name	R/W	Default	Description
7-6	GPIO25_MODE	R/W	0	GPIO25_MODE is used to select the output mode of GPIO25: 00: High Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode

5-4	GPIO24_MODE	R/W	0	GPIO24_MODE is used to select the output mode of GPIO24: 00: Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode
3-2	GPIO23_MODE	R/W	0	GPIO23_MODE is used to select the output mode of GPIO23: 00: Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode
1-0	GPIO22_MODE	R/W	0	GPIO22_MODE is used to select the output mode of GPIO22: 00: Level Mode 01: Inverted Level Mode 10: High Pulse Mode 11: Low Pulse Mode

8.5.14 GPIO2 Pulse Width of Pulse Mode Status Register — Index D8h

Bit	Name	R/W	Default	Description
7-6	GPIO25_PW_SEL	R/W	0	GPIO25_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms
5-4	GPIO24_PW_SEL	R/W	0	GPIO24_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms
3-2	GPIO23_PW_SEL	R/W	0	GPIO23_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms
1-0	GPIO22_PW_SEL	R/W	0	GPIO22_PW_SEL is used to select the output pulse width of pulse mode: 00: 500us 01: 1ms 10: 20ms 11: 100ms

8.5.15 GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.

3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

8.5.16 GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

8.5.17 GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_IN	R	-	The pin status of PSOUT#/GPIO14.
3	GPIO13_IN	R	-	The pin status of MCLK/GPIO13.
2	GPIO12_IN	R	-	The pin status of MDAT/GPIO12.
1	GPIO11_IN	R	-	The pin status of KCLK/GPIO11.
0	GPIO10_IN	R	-	The pin status of KDAT/GPIO10.

8.5.18 GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO14_DRV_EN	R/W	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.

0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

8.5.19 GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	GPIO07_OE	R/W	0	0: GPIO07 is in input mode. 1: GPIO07 is in output mode.
6	GPIO06_OE	R/W	0	0: GPIO06 is in input mode. 1: GPIO06 is in output mode.
5	GPIO05_OE	R/W	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.
2	GPIO02_OE	R/W	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode.
1	GPIO01_OE	R/W	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode.
0	GPIO00_OE	R/W	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode.

8.5.20 GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	GPIO07_VAL	R/W	1	0: GPIO07 outputs 0 when in output mode. 1: GPIO07 outputs 1 when in output mode.
6	GPIO06_VAL	R/W	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs 1 when in output mode.
5	GPIO05_VAL	R/W	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

8.5.21 GPIO Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	GPIO07_IN	R	-	The pin status of SIN/GPIO07.
6	GPIO06_IN	R	-	The pin status of SOUT/GPIO06/2E_4E.

5	GPIO05_IN	R	-	The pin status of DSR#/GPIO05.
4	GPIO04_IN	R	-	The pin status of RTS#/GPIO04.
3	GPIO03_IN	R	-	The pin status of DTR#/GPIO03/40_100.
2	GPIO02_IN	R	-	The pin status of CTS#/GPIO02.
1	GPIO01_IN	R	-	The pin status of RI#/GPIO01.
0	GPIO00_IN	R	-	The pin status of DCD#/GPIO00.

8.5.22 GPIO Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	GPIO07_DRV_EN	R/W	0	0: GPIO07 is open drain in output mode. 1: GPIO07 is push pull in output mode.
6	GPIO06_DRV_EN	R/W	0	0: GPIO06 is open drain in output mode. 1: GPIO06 is push pull in output mode.
5	GPIO05_DRV_EN	R/W	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode.
4	GPIO04_DRV_EN	R/W	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode.
3	GPIO03_DRV_EN	R/W	0	0: GPIO03 is open drain in output mode. 1: GPIO03 is push pull in output mode.
2	GPIO02_DRV_EN	R/W	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode.
1	GPIO01_DRV_EN	R/W	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode.
0	GPIO00_DRV_EN	R/W	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode.

8.6 WDT Registers (CR07)

Configuration Registers

8.6.1 WDT Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	WDT_EN	R/W	0	0: disable watch dog timer 1: enable watch dog timer

8.6.2 Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of VID base address.

8.6.3 Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of VID base address.

Device Registers

8.6.4 Configuration Register — Index F0h (offset + 00h)

Bit	Name	R/W	Default	Description
7	WDOUT_EN	R/W	0	If this bit is set to 1 and watchdog timeout event occurs, WDTRST# output is enabled.
6-4	Reserved	-	-	Reserved
3-0	Reserved	-	-	Reserved

8.6.5 Register — Index F2h~F4h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

8.6.6 Watchdog Timer Configuration Register 1— Index 05h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1:0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

8.6.7 Watchdog Timer Configuration Register 2 — Index 06h

Bit	Name	R/W	Default	Description
7:0	WD_TIME	R/W	0	Time of watchdog timer

8.6.8 WDT PME Register — Index 07h

Bit	Name	R/W	Default	Description
7	WDT_PME	R	0	WDT PME real time status.
6	WDT_PME_EN	R/W	0	0: Disable WDT PME. 1: Enable WDT PME.

5	WDT_PME_ST	R/W	0	0: No WDT PME occurred. 1: WDT PME occurred. The WDT PME is occurred one unit before WDT timeout.
4-0	Reserved	-	-	Reserved

8.7 PME, ACPI, Power Saving Registers (CR0A)

Configuration Register

8.7.1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

8.7.2 EuP Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	EuP_EN	R/W	0	0 : disable EuP function 1: enable EuP function
6	Reserved	-	0	Reserved.
5	EVENT_EN	R/W	0	Event input enable. 0: disable EVENT_IN# function. 1: Function of pin 19 is EVENT_IN#
4	VSB_CTRL_1_EN	R/W	0	VSB_CTRL_1 enable. 0: disable VSB_CTRL_1 function. 1: Function of pin 20 is VSB_CTRL_1
3-2	Reserved	-	-	Reserved
1	EVENT_PME_EN	R/W	0	EVENT_IN# PME event enable. 0: disable EVENT_IN# PME event. 1: enable EVENT_IN# PME event
0	EVENT_PSOUT_EN	R/W	0	EVENT_IN# PSOUT event enable. 0: disable EVENT_IN# PSOUT event. 1: enable EVENT_IN# PSOUT event

8.7.3 EuP control register — Index E1h

Bit	Name	R/W	Default	Description
7-6	Boot_Mode	R/W	11	Write these two bits to select Boot Mode for Always Off/ Always On/ Keep Last State. 00:Default Always Off 11:Support Always On and Keep Last State 10:Reserved 01:Reserved
5-4	Reserved	-	-	Reserved

3	S5 _CTRL_1_DIS	R/W	1	If clear to “0” CTRL_1 will output Low when S5 state. Else If set to “1” CTRL_1 will output High when S5 state.
2	S5 _CTRL_0_DIS	R/W	1	If clear to “0” CTRL_0 will output Low when S5 state. Else If set to “1” CTRL_0 will output High when S5 state.
1	AC_ CTRL_1_DIS	R/W	0	If clear to “0” CTRL_1 will output Low when after AC lost. Else If set to “1” CTRL_1 will output High when after AC lost.
0	AC_ CTRL_0_DIS	R/W	0	If clear to “0” CTRL_0 will output Low when after AC lost. Else If set to “1” CTRL_0 will output High when after AC lost.

8.7.4 EuP control register — Index E2h

Bit	Name	R/W	Default	Description
7	AC_LOST	R/WC	-	Set 1 if AC lost, and write 1 to clear.
6	Reserved	R/W	0	Reserved
5	VSB_CTRL_EN[1]	R/W	1’b0	0: disable eup_ctrl2 assert rsmrst low 1: enable eup_ctrl2 assert rsmrst low
4	VSB_CTRL_EN[0]	R/W	1’b0	0: disable eup_ctrl1 assert rsmrst low 1: enable eup_ctrl1 assert rsmrst low
3	S5_DET_S5#	R/W	1	Device into S5 state will check S5# signal and VCC_IN pin status, but when user clear this bit to 0. Device into S5 state will not check S5# become low.
2	S5_DET_VCC	R/W	1	Device into S5 state will check S5# signal and VCC_IN pin status, but when user clear this bit to 0. Device into S5 state will not check VCC_IN become low.
1	RSMRST_DET_5V_N	R/W	0	Device detects VSB5V power ok (4.4V) and VSB3V_IN become high, and after 60ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check VSB5V power ok.
0	Reserved	-	-	Reserved.

8.7.5 EuP PSIN deb-register — Index E3h

Bit	Name	R/W	Default	Description
.7-0	PS_DEB_TIME	R/W	0x13	PS_IN pin input de-bounce time default is 20mSec

8.7.6 EuP RSMRST deb-register — Index E4h

Bit	Name	R/W	Default	Description
7-0	RSMRST_DEB_TIME	R/W	0x09	RSMRST internal de-bounce time default is 10mSec

8.7.7 EuP PSOUT deb-register — Index E5h

Bit	Name	R/W	Default	Description
7-0	PS_OUT_PULSE_W	R/W	0xC7	PS_OUT_OUT output Pulse width default is 200mSec low pulse

8.7.8 EuP PSON deb-register — Index E6h

Bit	Name	R/W	Default	Description
7-0	PS_ON_DEB_TIME	R/W	0x09	PSON_IN pin input de-bounce time default is 10mSec

8.7.9 EuP S5 deb-register — Index E7h

Bit	Name	R/W	Default	Description
7-0	S5_DEB_TIME	R/W	0x63	S5# pin input de-bounce time The unit of this byte is 64ms. Default is 6.4Sec

8.7.10 EuP Wakeup Event Enable Register — Index E8h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	Reserved	-	-	Reserved.
4	EVENT_WAKEUP_EN	R/W	1	Enable EVENT_IN# event to wakeup.
3	GP_WAKEUP_EN	R/W	0	Enable GPIO PME event to wakeup.
2	TMOUT_WAKEUP_EN	R/W	0	Enable EuP Watchdog Timer timeout event to wakeup. See index EDh and EEh.
1	MO_WAKEUP_EN	R/W	0	Enable Mouse PME event to wakeup.
0	KB_WAKEUP_EN	R/W	0	Enable Keyboard PME event to wakeup.

8.7.11 EuP Watchdog Control Register —Index EDh

Bit	Name	R/W	Default	Description
7-4	Revered	-	-	Reserved.
4	WD_TMOUT	R/WC	0	EuP watchdog timer timeout status. Write 1 to clear.
3-2	Revered	-	-	Reserved.
1	WD_UNIT	R/W	0	0: unit of WD_TIME is 1 sec. 1: unit of WD_TIME is 1 minute.
0	WD_EN	R/W	0	Enable EuP watchdog timer.

8.7.12 EuP Watchdog Time Register —Index EEh

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	EuP watchdog timer count time register. Start to count down when WD_EN is set. When reaching 0, WD_EN will auto clear and WD_TMOUT is set. A wakeup event will assert if enabled.

8.7.13 PME Event Enable Register 1— Index F0h

Bit	Name	R/W	Default	Description
7	WDT_PME_EN	R/W	0	WDT PME event enable. 0: disable WDT PME event. 1: enable WDT PME event.
6	MO_PME_EN	R/W	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.

5	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3-2	Reserved	-	-	Reserved
1	UR_PME_EN	R/W	0	UART PME event enable. 0: disable UART PME event. 1: enable UART PME event.
0	Reserved	-	-	Reserved

8.7.14 PME Event Enable Register 2 — Index F1h

Bit	Name	R/W	Default	Description
7	WDT_PME_ST	R/WC	-	WDT PME event status. 0: WDT has no PME event. 1: WDT has a PME event to assert. Write 1 to clear to be ready for next PME event.
6	MO_PME_ST	R/WC	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/WC	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/WC	-	Hardware monitor PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
3-2	Reserved	-	-	Reserved
1	UR_PME_ST	R/W	-	UART PME event status. 0: UART has no PME event. 1: UART has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	Reserved	-	-	Reserved

8.7.15 PME Event Status Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved
1	Reserved	-	-	Reserved.
0	GP_PME_EN	R/W	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.

8.7.16 PME Event Status Register — Index F3h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	EUP_PME_ST	R/W	-	EUP PME event status. 0: EUP has no PME event. 1: EUP has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	Reserved	-	-	Reserved
1	Reserved	-	-	Reserved.
0	GP_PME_ST	R/W	-	GPIO PME event status. 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.

8.7.17 Keep Last State Select Register — Index F4h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6-5	Reserved	R/W	0	Reserved
4	EN_KBWAKEUP	R/W	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : Keep last state 10 : Always on 01 : Bypass mode. 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

8.7.18 VDDOK Delay Register — Index F5h

Bit	Name	R/W	Default	Description
7-6	PWROK_DELAY	R/W	0	The additional PWROK delay. 00: no delay 01: 100ms. 10: 200ms 11: 400ms.
5	RSTCON_EN	R/W	1	0: RESETCON# will assert via PWROK. 1: RESETCON# will assert via RESETOUT1# and RESETOUT2#.
4-3	VDD_DELAY	R/W	11	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms
2-0	Reserved	-	-	Reserved.

8.7.19 PCIRST Control Register — Index F6h

Bit	Name	R/W	Default	Description
7	S3_SEL	R/W	0	Select the KBC S3 state. 0: Enter S3 state when internal VDD3VOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	PSON_DEL_EN	R/W	0	0: PSON# is the inverted of S3# signal. 1: PSON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
5-2	Reserved	-	-	Reserved.
1	RESETOUT2_GATE	R/W	1	Write “0” to this bit will force RESETOUT2# to sink low.
0	RESETOUT1_GATE	R/W	1	Write “0” to this bit will force RESETOUT1# to sink low.

8.7.20 Power Sequence Control Register — Index F7h

Bit	Name	R/W	Default	Description
7-4	Reserved	R/W	0	Dummy register.
3	WDT_PWROK_EN	R/W	0	0: Disable WDT assert to PWROK pin. 1: Enable WDT assert to PWROK pin.
2	PWROK_250MS	W	0	Write “1” to generate a 250ms low pulse from PWROK pin.
1	VSB_GATE_TRI	R/W	0	0: 3VSBSW# sinks low in S5 state. 1: 3VSBSW# is tri-state in S5 state.
0	Reserved	-	-	Reserved.

8.7.21 LED VCC Mode Select Register — Index F8h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5-4	LED_VCC_S5_MODE	R/W	0	Select LED_VCC mode in S5 state. 00: Sink low. 01: Tri-state. 10: 0.5Hz clock. 11: 1Hz clock.
3-2	LED_VCC_S3_MODE	R/W	0	Select LED_VCC mode in S3 state. 00: Sink low. 01: Tri-state. 10: 0.5Hz clock. 11: 1Hz clock.
1-0	LED_VCC_S0_MODE	R/W	0	Select LED_VCC mode in S0 state. 00: Sink low. 01: Tri-state. 10: 0.5Hz clock. 11: 1Hz clock.

8.7.22 LED VSB Mode Select Register — Index F9h

Bit	Name	R/W	Default	Description

7-6	Reserved	-	-	Reserved
5-4	LED_VSB_S5_MODE	R/W	0	Select LED_VSB mode in S5 state. 00: Sink low. 01: Tri-state. 10: 0.5Hz clock. 11: 1Hz clock.
3-2	LED_VSB_S3_MODE	R/W	0	Select LED_VSB mode in S3 state. 00: Sink low. 01: Tri-state. 10: 0.5Hz clock. 11: 1Hz clock.
1-0	LED_VSB_S0_MODE	R/W	0	Select LED_VSB mode in S0 state. 00: Sink low. 01: Tri-state. 10: 0.5Hz clock. 11: 1Hz clock.

8.7.23 RI De-bounce Select Register — Index FEh

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved
1-0	RI_DB_SEL	R/W	0	Select RI de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

9.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V) (Note)

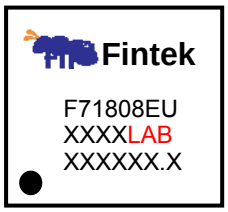
PARAMETER	CONDITONS	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 145 °C, VCC = 3.0V to 3.6V 0 °C <T_D < 60°C 100 °C <T_D < 145°C		± 1 ± 1	± 3 ± 3	°C
Supply Voltage range		3.0	3.3	3.6	V
Average operating supply current			8		mA
Standby supply current			5		uA
Resolution			1		°C
Power on reset threshold			2.2	2.4	V
Diode source current	High Level		95		uA
	Low Level		10		uA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/OD_{12ts5v}-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OD_{16t5v}-TTL level bi-directional pin, Open-drain output with16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.						

Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/O_{12t}- TTL level bi-directional pin, Output pin with 12mA source-sink capability.						
Input Low Threshold Voltage	Vt-			0.6	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	0.9			V	VDD = 3.3 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{ts} - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN_{t5v} - TTL level input pin with 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
IN_{ts5v} - TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
OD_{12}-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{12\text{-}5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
OD_{24}-Open-drain output with 24 mA sink capability.						
Output Low Current	IOL		-24		mA	VOL = 0.4V
$OD_{16\text{-}u10\text{-}5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
O_8- Output pin with 8 mA source-sink capability.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
$O_{8\text{-}u47\text{-}5v}$- Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						

10.Ordering Information

Part Number	Package Type	Production Flow
F71808EU	64-TQFP Green Package	Commercial, 0°C to +70°C



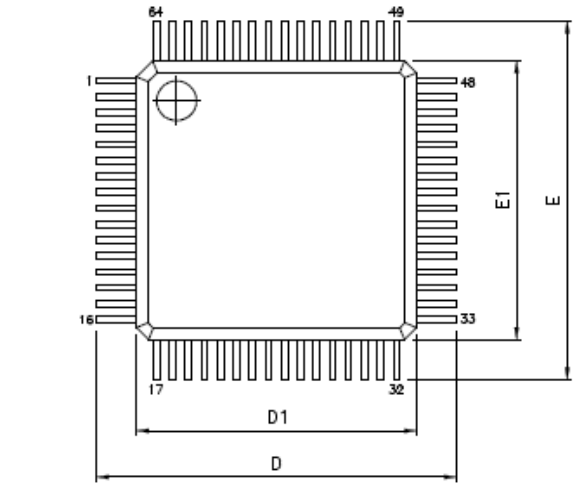
Version Identification:

Ex: For LAB version

The version shows on RED area. Ex: LAB

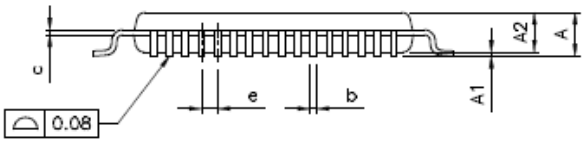
11.Package Dimensions

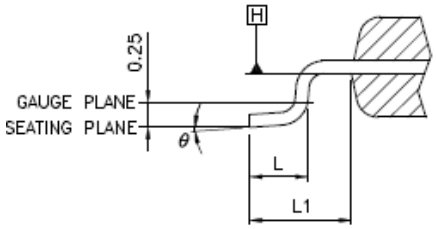
64 TQFP

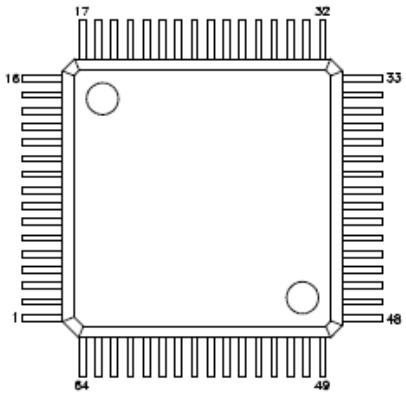


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°







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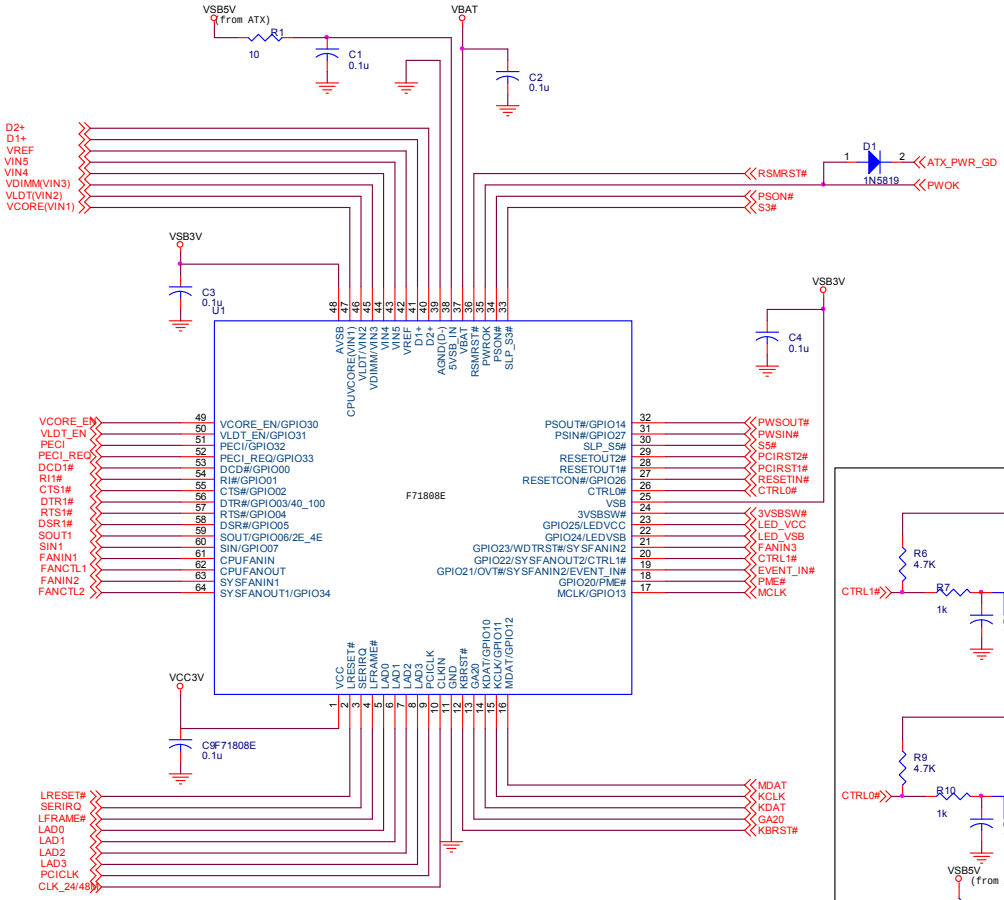
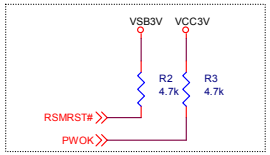
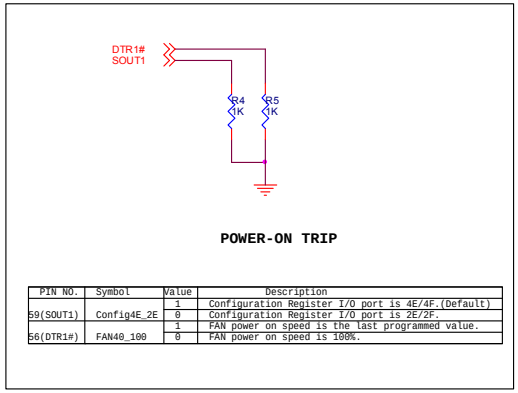
12. Application Circuit

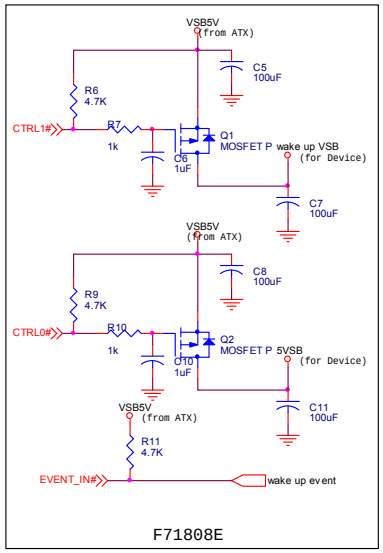


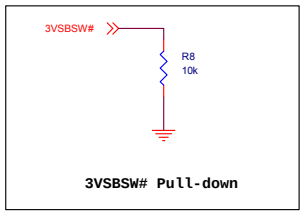


RSMRST# and PWROK pull-up

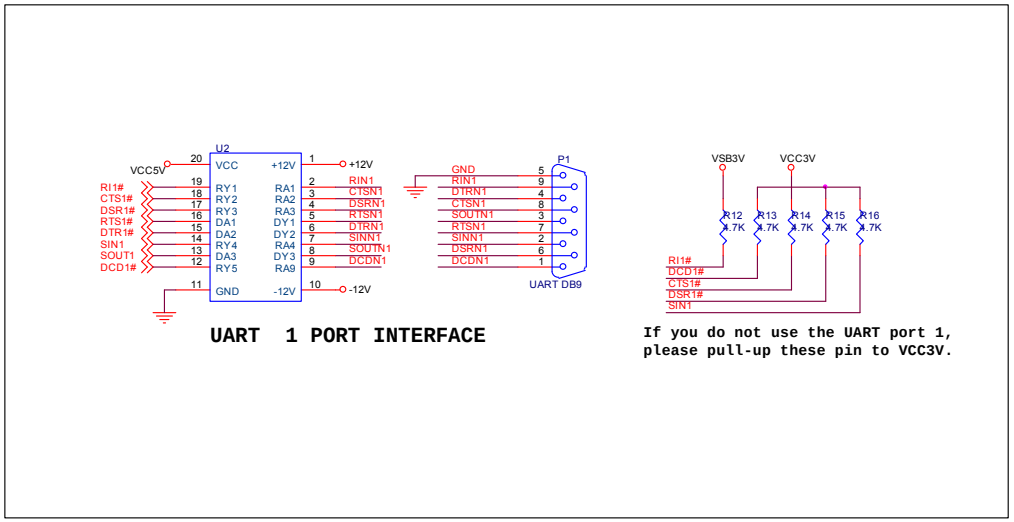


PIN NO.	Symbol	Value	Description
		1	Configuration Register I/O port is 4E/4F.(Default)
59(SOUT1)	Config4E_2E	0	Configuration Register I/O port is 2E/2F.
		1	FAN power on speed is the last programmed value.
56(DTR1#)	FAN40_100	0	FAN power on speed is 100%.



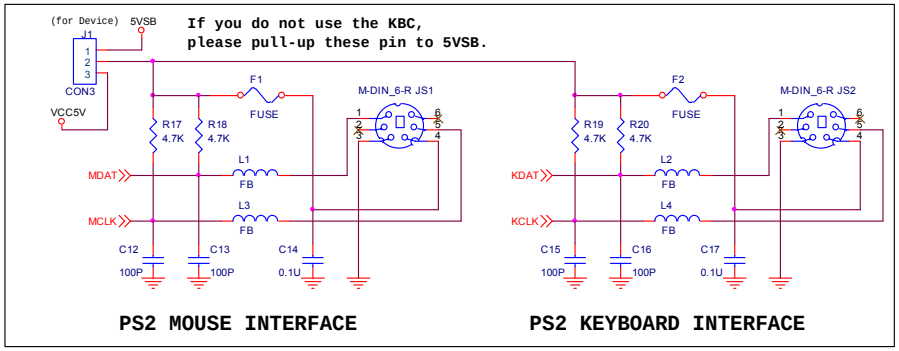


Title	<F71808E> Feature Integration Technology Inc.	
Size: Custom	Document Number: F71808E	Rev: 1.0
Date: Monday , August 16, 2010	Sheet 1 of 6	



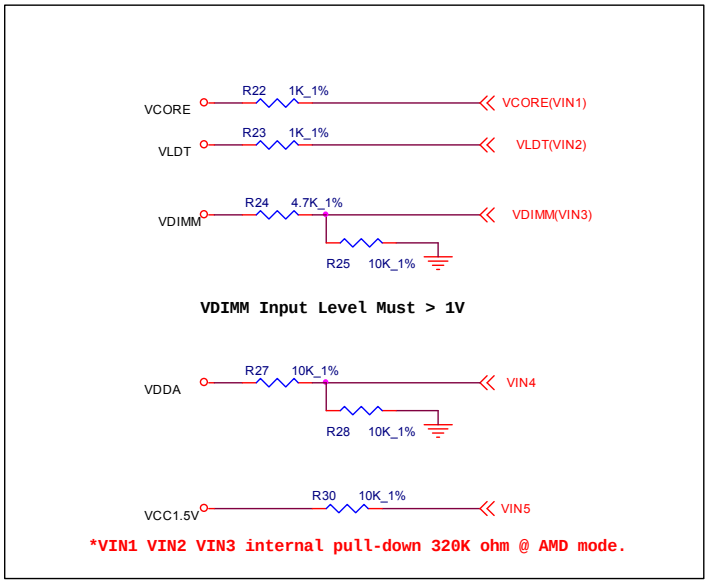
UART 1 PORT INTERFACE

If you do not use the UART port 1, please pull-up these pin to VCC3V.

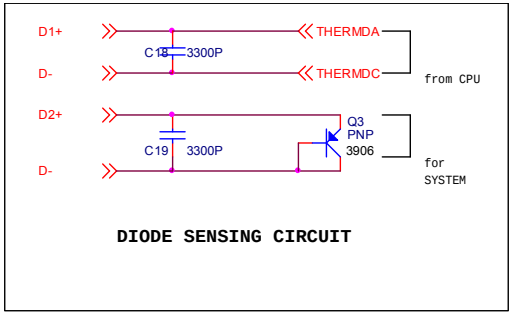


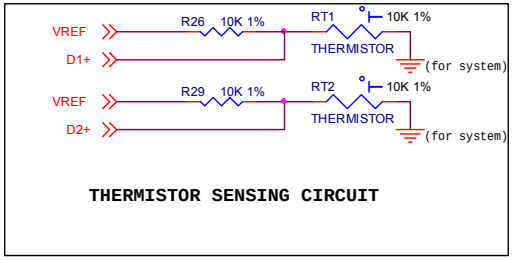
PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

Title	<F71808E> Feature Integration Technology Inc.		
Size: Custom	Document Number: UART_PS/2		Rev: 1.0
Date: Monday, August 16, 2010	Sheet 2 of 6		

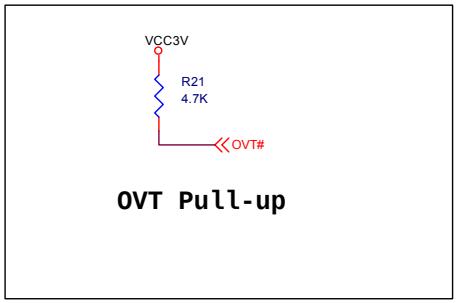


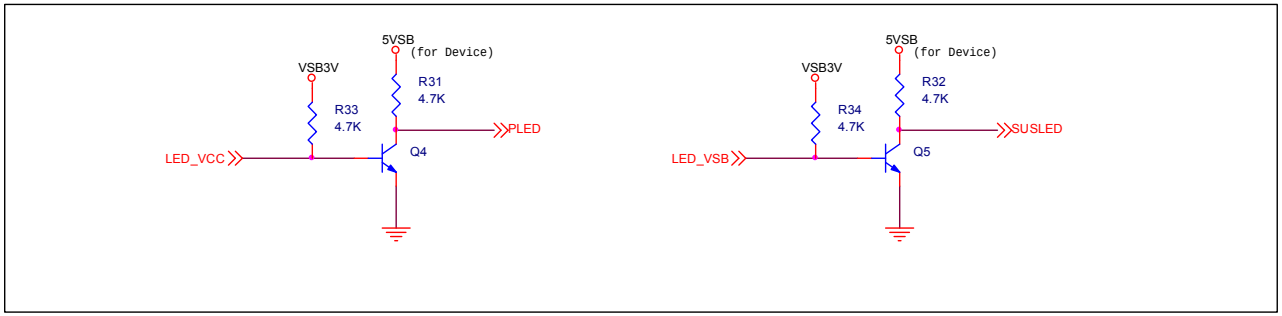
VOLTAGE SENSING.



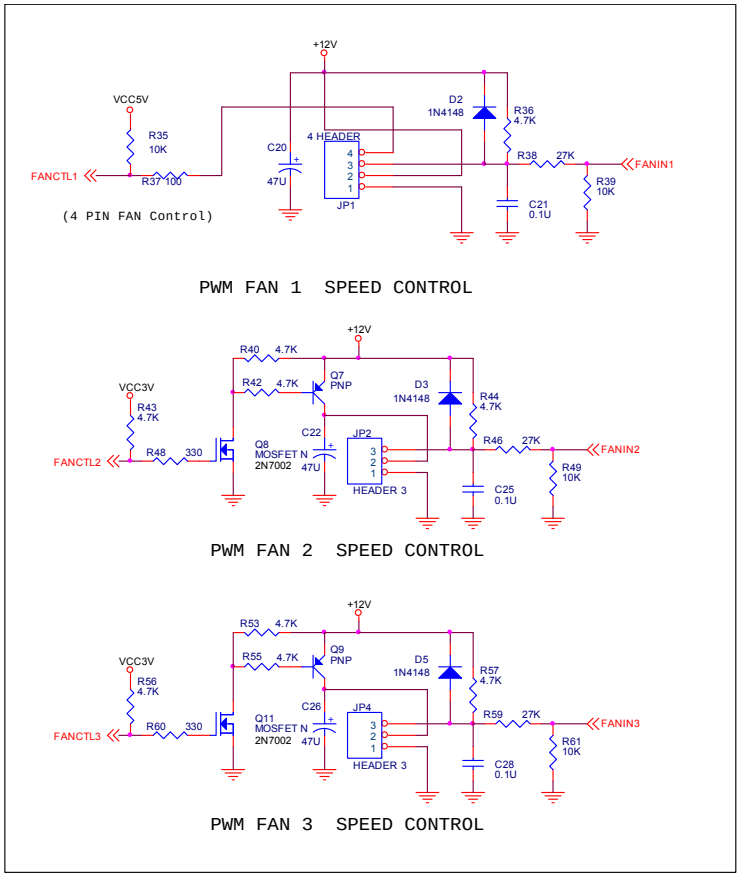


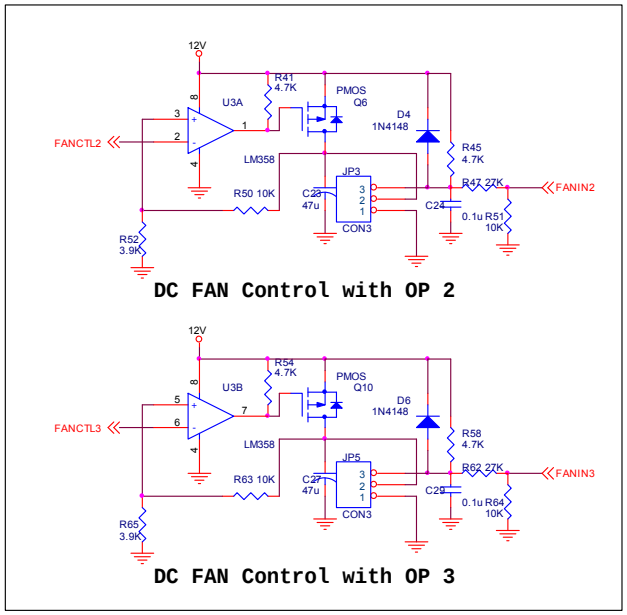
Temperature Sensing





Title	<F71808E> Feature Integration Technology Inc.		
Size: Custom	Document Number: HWM		Rev: 1.0
Date: Monday, August 16, 2010	Sheet 3 of 6		

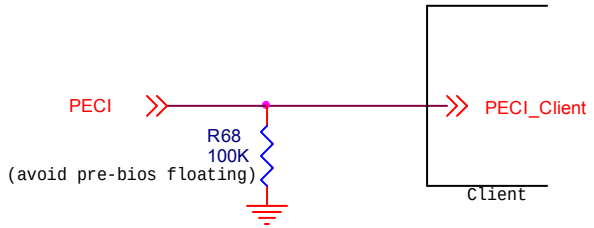




FAN CONTROL FOR PWM OR DC

Title	<F71808E> Feature Integration Technology Inc.	
Size: Custom	Document Number: FAN	Rev: 1.0
Date: Monday, August 16, 2010	Sheet 4 of 6	

Power Sequence Pull-up



INTEL PECI

Title: <F71808E> Feature Integration Technology Inc.			
Size: Custom	Document Number: AMDTSI/PECI & Power Sequence		Rev: 1.0
Date: Monday, August 16, 2010		Sheet 5 of 6	

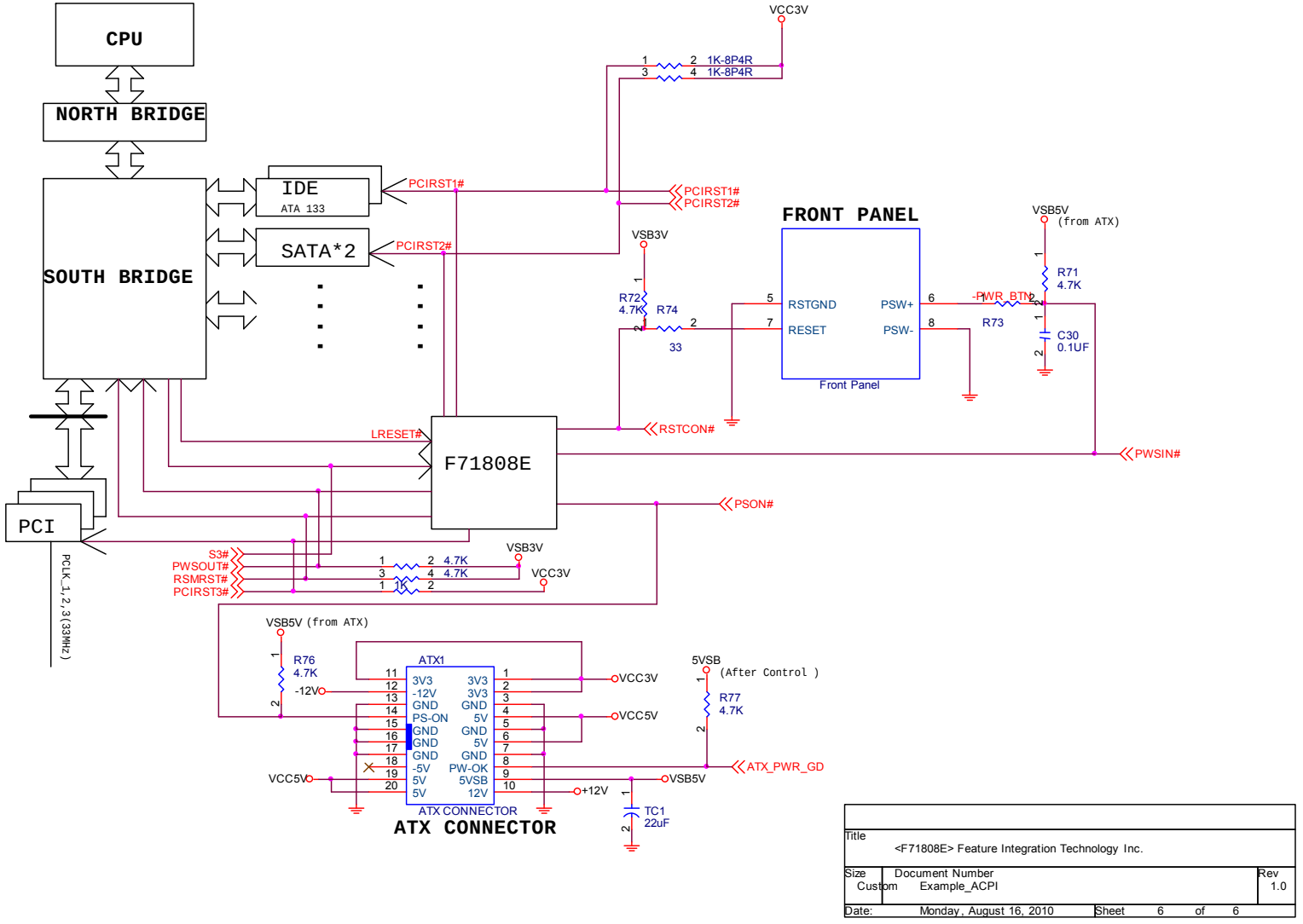


Figure 20 F71808EU Application Circuit