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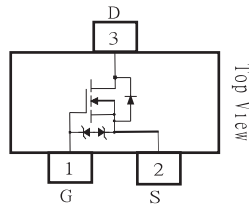
50V N-Channel Enhancement Mode MOSFET - ESD Protected

FEATURES

- $R_{DS(ON)}, V_{GS}@10V, I_{DS}@500mA=3\Omega$
- $R_{DS(ON)}, V_{GS}@4.5V, I_{DS}@200mA=4\Omega$
- $R_{DS(ON)}, V_{GS}@2.5V, I_{DS}@100mA=6\Omega$
- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Very Low Leakage Current In Off Condition
- Specially Designed for Battery Operated Systems, Solid-State Relays
Drivers : Relays, Displays, Lamps, Solenoids, Memories, etc.
- ESD Protected
- In compliance with EU RoHS 2002/95/EC directives

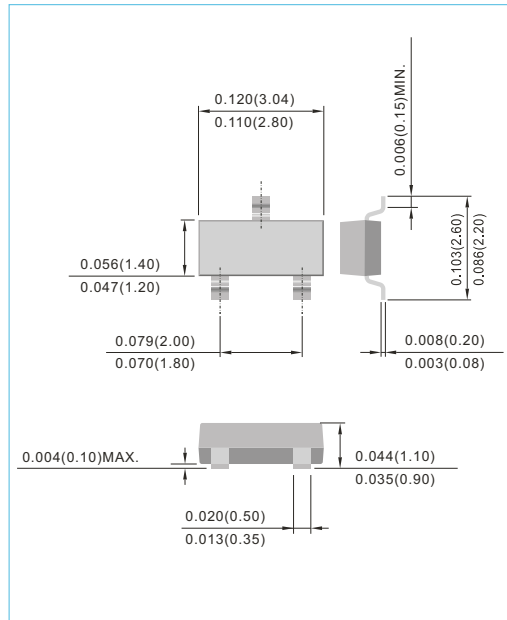
MECHANICAL DATA

- Case: SOT-23 Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Marking : 138
- Apporx. Weight: 0.0003 ounce, 0.0084 gram



SOT-23

Unit : inch(mm)



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	50	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	300	mA
Pulsed Drain Current ¹⁾	I_{DM}	2000	mA
Maximum Power Dissipation	P_D	$T_A=25^\circ\text{C}$ 350 $T_A=75^\circ\text{C}$ 210	mW
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	$^\circ\text{C}$
Junction-to Ambient Thermal Resistance(PCB mounted) ²	$R_{\theta JA}$	357	$^\circ\text{C}/\text{W}$

Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, $t < 5$ sec

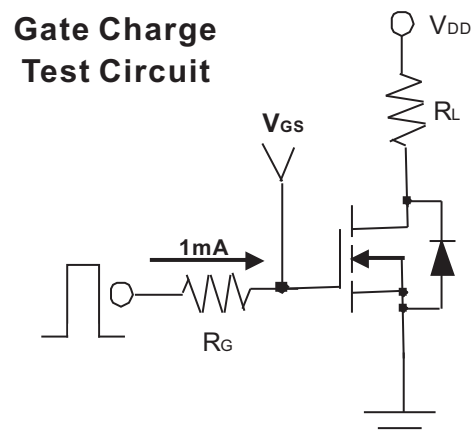
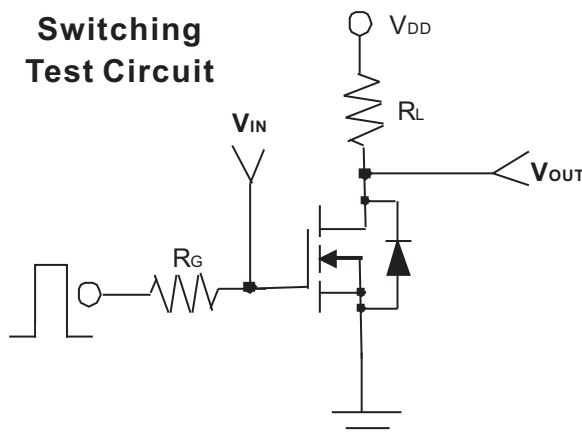
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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=10\mu A$	50	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.8	-	1.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=2.5V, I_D=100mA$	-	2.8	6.0	Ω
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=200mA$	-	1.8	4.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	1.6	3.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=50V, V_{GS}=0V$	-	-	1	μA
Gate Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±10	μA
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=250mA$	100	-	-	mS
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=25V, I_D=250mA$ $V_{GS}=4.5V$	-	-	1.0	nC
Turn-On Time	t_{on}	$V_{DD}=30V, R_L=100\Omega$ $I_D=300mA, V_{GEN}=10V$ $R_G=6\Omega$	-	-	40	ns
Turn-Off Time	t_{off}		-	-	150	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1.0MHz$	-	-	50	pF
Output Capacitance	C_{oss}		-	-	10	
Reverse Transfer Capacitance	C_{rss}		-	-	5	
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	$I_S=250mA, V_{GS}=0V$	-	0.82	1.2	V
Continuous Diode Forward Current	I_S	-	-	-	300	mA
Pulse Diode Forward Current	I_{SM}	-	-	-	2000	mA





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Typical Characteristics Curves ($T_A=25^\circ\text{C}$, unless otherwise noted)

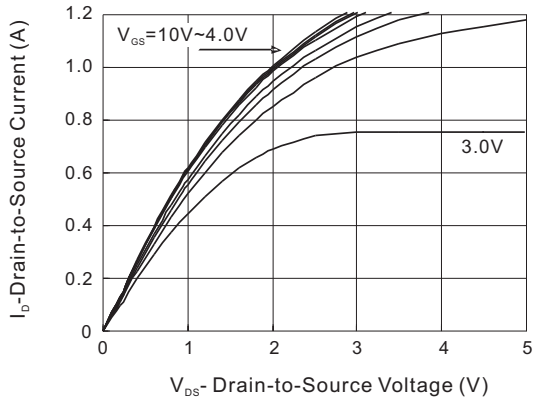


FIG.1- Output Characteristic

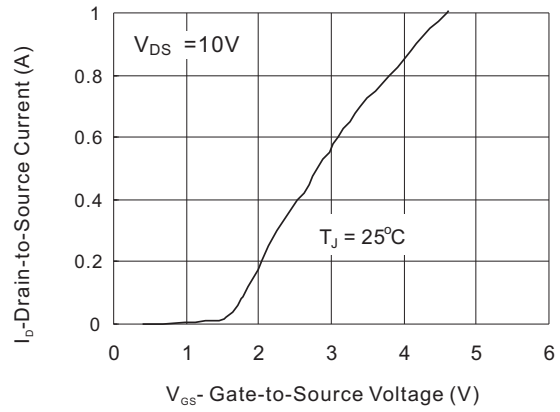


FIG.2- Transfer Characteristic

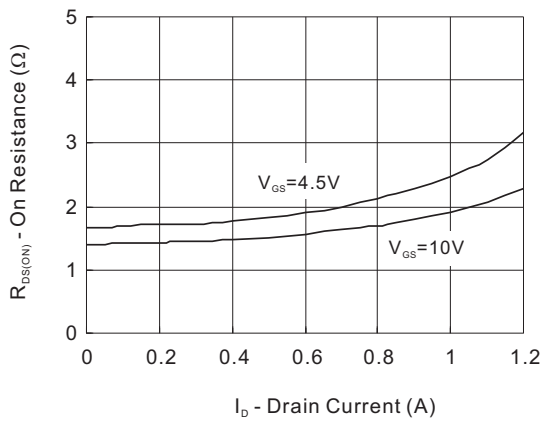


FIG.3- On Resistance vs Drain Current

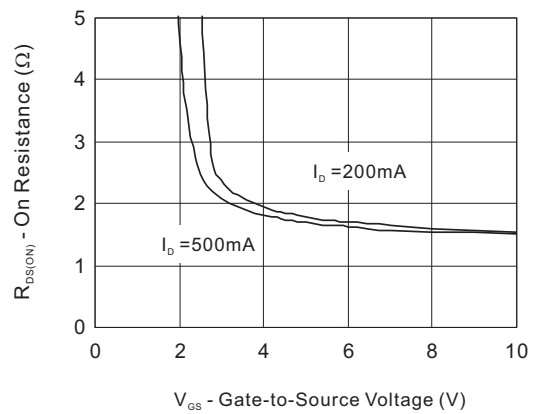


FIG.4- On Resistance vs Gate to Source Voltage

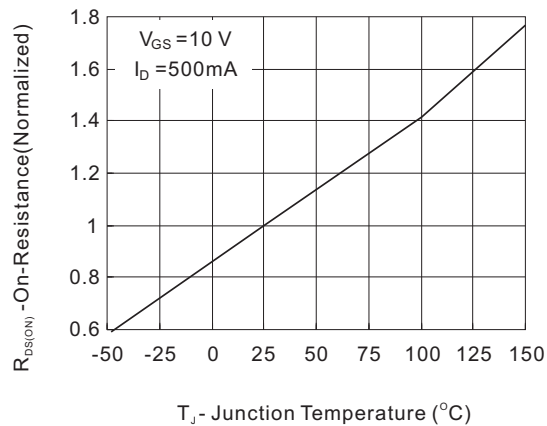


FIG.5- On Resistance vs Junction Temperature



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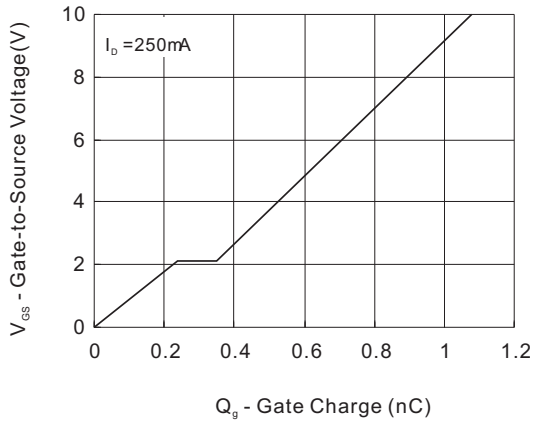


Fig.6 - Gate Charge Waveform

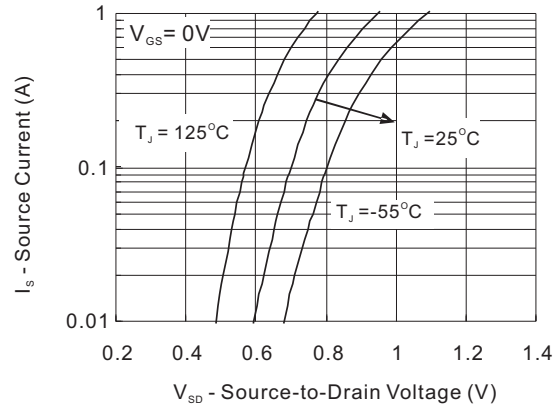


Fig.7 Source-Drain Diode Forward Voltage

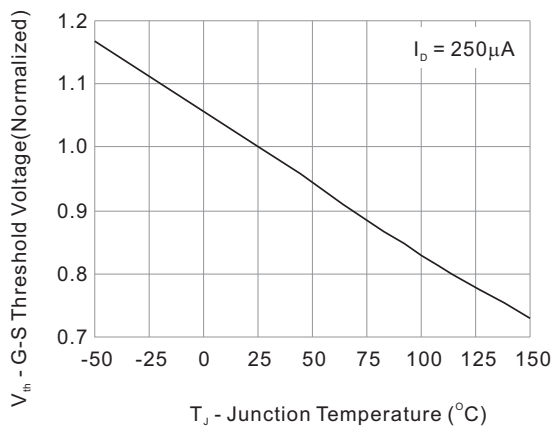


Fig.8 - Threshold Voltage vs Temperature

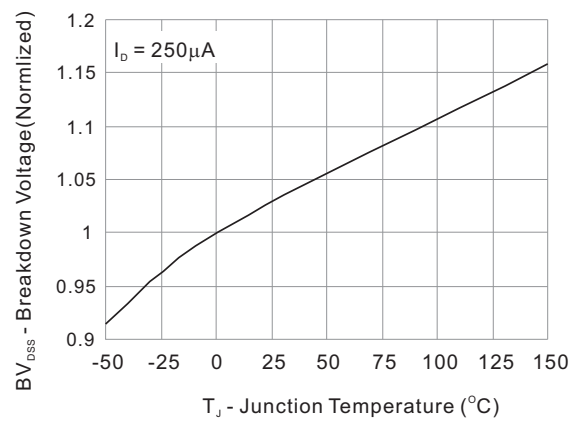
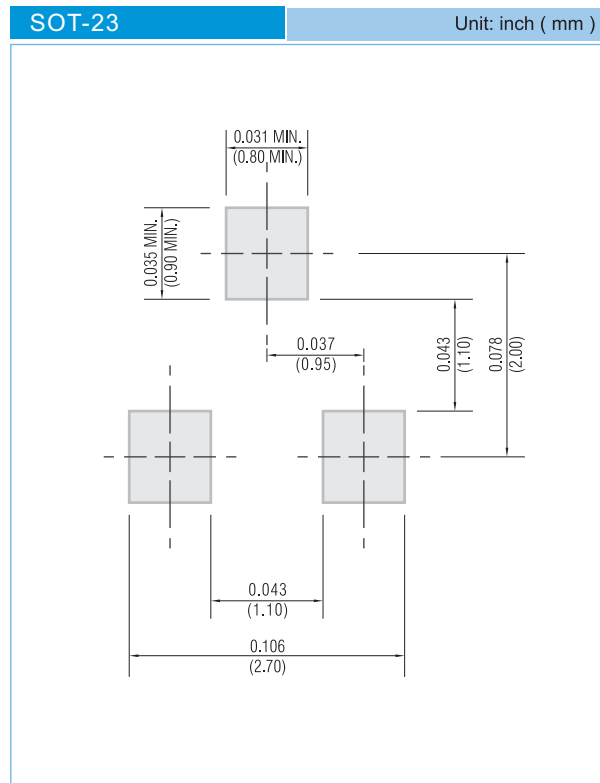


Fig.9 - Breakdown Voltage vs Junction Temperature



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MOUNTING PAD LAYOUT



ORDER INFORMATION

- Packing information
 - T/R - 12K per 13" plastic Reel
 - T/R - 3K per 7" plastic Reel

LEGAL STATEMENT

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