



## UR6515D

## LINEAR INTEGRATED CIRCUIT

### 3A DDR BUS TERMINATION REGULATOR

#### DESCRIPTION

The **UR6515D** is a linear regulator sourcing or sinking continuous 2A or up to 3A transient peak current while regulating an output voltage to within 40mV in the DDR SDRAM bus terminator applications. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

The **UR6515D** output termination voltage tracks the reference voltage applied at  $V_{REF}$  pin. A resistor divider connected to  $V_{IN}$ , GND and  $V_{REF}$  pins is used to force the reference voltage to  $V_{REF}$  pin. Additional features include current limiting protection and thermal shutdown protection.

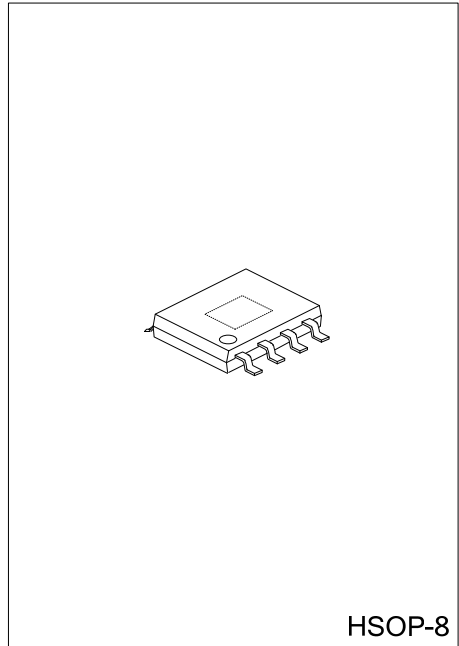
#### FEATURES

- \*DDR1/ DDR2/DDR3 termination voltage applications
- \*Sink and Source Current
  - 2A Continuous Current
  - Peak 3A for DDR1&DDR2
  - Peak 2.5A for DDR3
- \*Low output voltage offset within 20mV
- \*Source and sink 3A peak current
- \*Adjustable output voltage by external resistors
- \*Integrated power MOS devices
- \*Suspend to RAM(STR) functionality
- \*Current Limiting Protection
- \*Thermal Shutdown Protection
- \*Cost-effective and easy to use
- \*Halogen Free

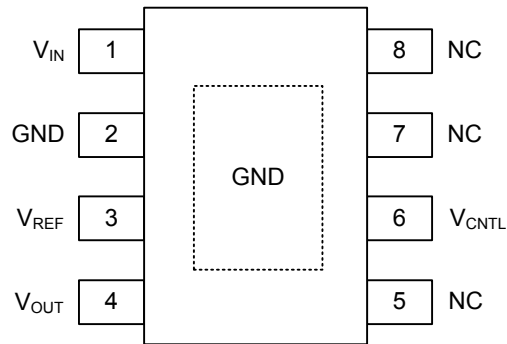
#### ORDERING INFORMATION

Order Number	Package	Packing
UR6515DG-SH2-R	HSOP-8	Tape Reel

<p>UR6515DG-SH2-R</p>	<p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Halogen Free</p>	<p>(1) R: Tape Reel</p> <p>(2) SH2: HSOP-8</p> <p>(3) G: Halogen Free</p>
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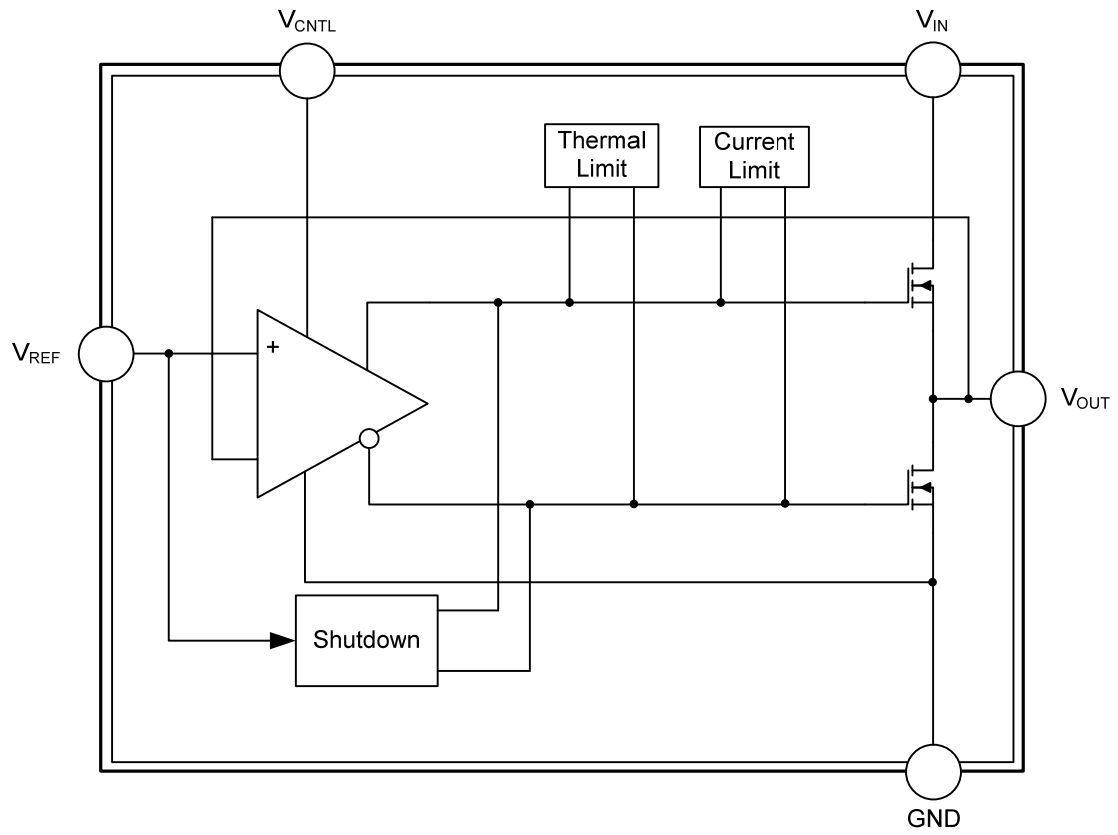
### ■ PIN CONFIGURATIONS



### ■ PIN DESCRIPTION

PIN NAME	PIN TYPE	PIN DESCRIPTION
$V_{CNTRL}$	I	Power supply pin for the internal control circuits
GND	O	Ground pin
$V_{IN}$	I	Power supply pin for the $V_{OUT}$ output
$V_{REF}$	I	Reference voltage input and active-low shutdown control pin
$V_{OUT}$	O	Output voltage pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
V <sub>CNTL</sub> Control Voltage	V <sub>CNTL</sub>	6	V
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>	6	V
Power Dissipation (Ta=25°C)	P <sub>D</sub>	1.33	W
Junction Temperature	T <sub>J</sub>	125	°C
Storage Temperature	T <sub>STG</sub>	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient (Note 1)	$\theta_{JA}$			75	°C/W
Junction to Case	$\theta_{JC}$			28	°C/W

Note: 1.  $\theta_{JA}$  is measured in the natural convection at Ta = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard

■ RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
V <sub>CNTL</sub> Control Voltage	V <sub>CNTL</sub>	5 or 3.3±5%	V
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>	2.5~1.5±3%	V
V <sub>REF</sub> Input Voltage	V <sub>REF</sub>	1.25~0.75±3%	V
Junction Temperature	T <sub>J</sub>	-40~+125	°C

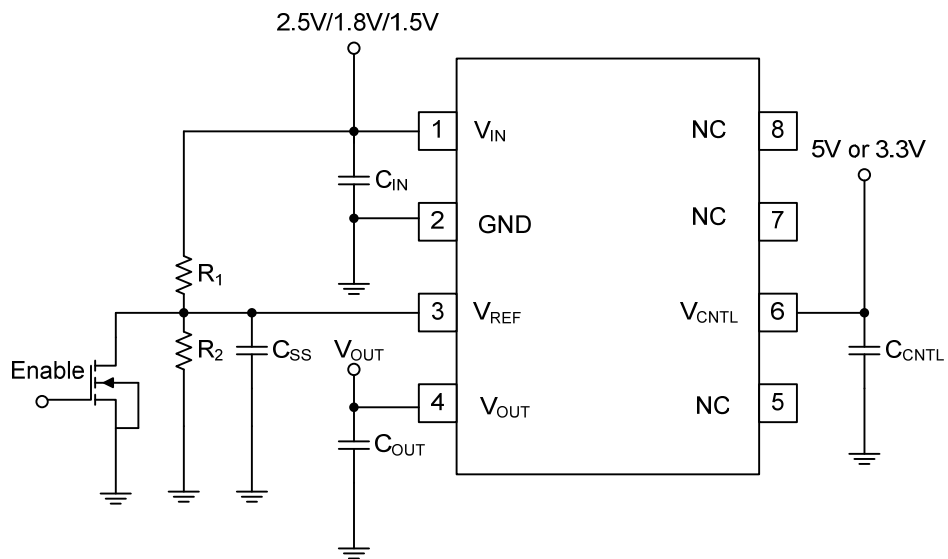
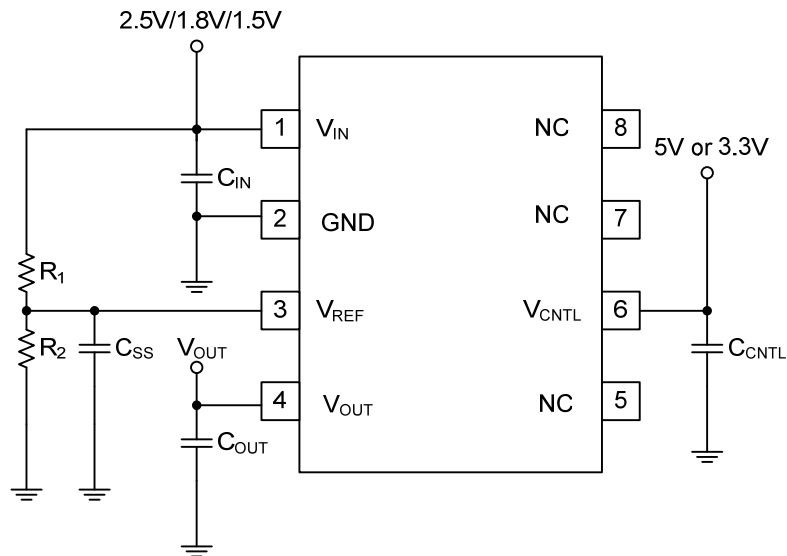
Notes: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise specified)

(V<sub>IN</sub>=2.5V/1.8V/1.5V, V<sub>CNTL</sub>=3.3V, V<sub>REF</sub>=1.25V/0.9V/0.75V, C<sub>OUT</sub> = 10μF (Ceramic))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CURRENT</b>						
Operation Current of V <sub>CNTL</sub>	I <sub>CNTL</sub>	I <sub>OUT</sub> =0A		1	2.5	mA
Standby Current	I <sub>STB</sub>	V <sub>REF</sub> <0.2V, R <sub>LOAD</sub> =180Ω		50	90	μA
<b>OUTPUT VOLTAGE (DDR/DDR II/DDR III)</b>						
Output Voltage Offset (V <sub>REF</sub> -V <sub>OUT</sub> )	V <sub>OS</sub>	I <sub>OUT</sub> =0A	-20		20	mV
Load Regulation	$\Delta V_{LOAD}$	I <sub>OUT</sub> =±2A	-20		20	mV
<b>PROTECTION</b>						
Current Limit	I <sub>LIMIT</sub>	V <sub>IN</sub> =2.5V/1.8V/1.5V	3			A
Thermal Shutdown Temperature	T <sub>SD</sub>	V <sub>CNTL</sub> =3.3V~5V	125	170		°C
Thermal Shutdown Hysteresis	$\Delta T_{SD}$	V <sub>CNTL</sub> =3.3V~5V		35		°C
<b>V<sub>REF</sub> Shutdown</b>						
Shutdown Threshold	V <sub>IH</sub>	Enable	0.6			V
	V <sub>IL</sub>	Shutdown			0.2	V

### ■ TYPICAL APPLICATIONS CIRCUITS

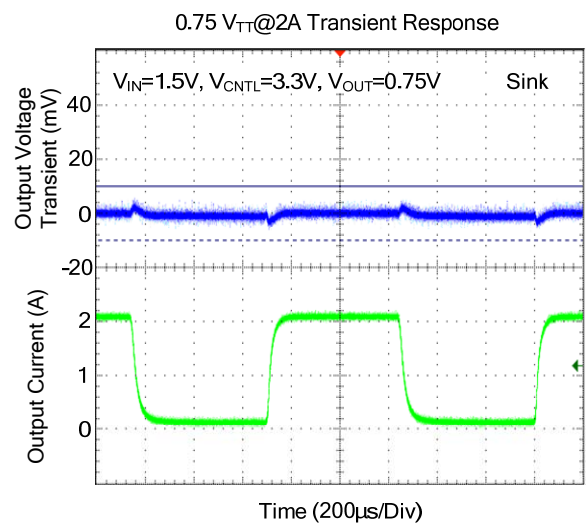
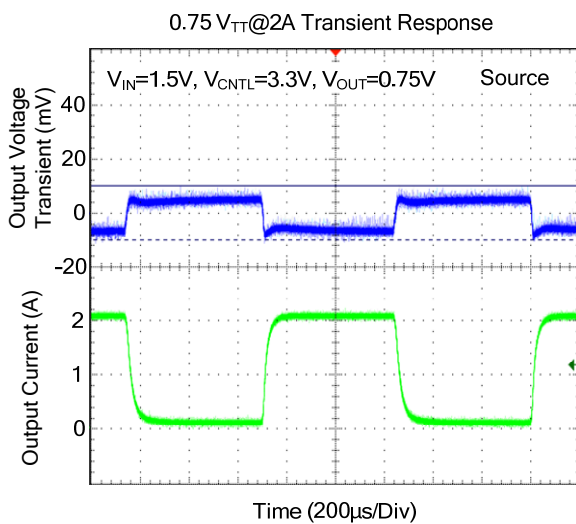
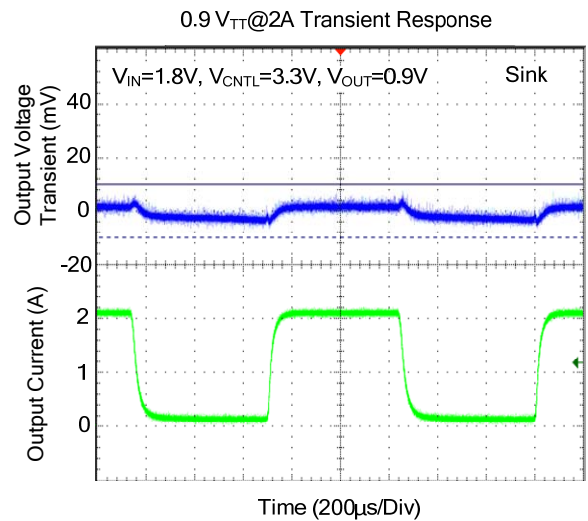
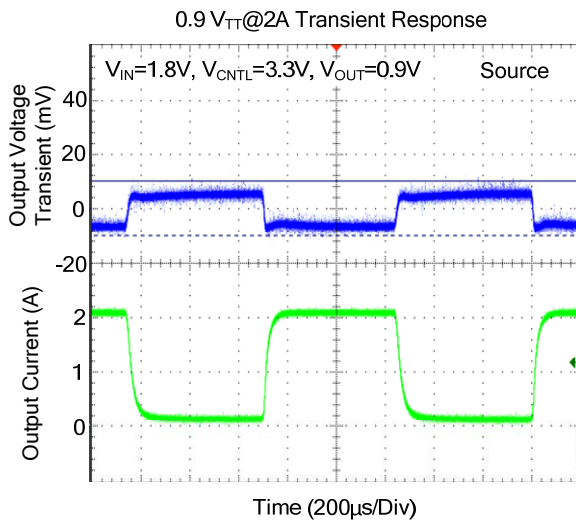
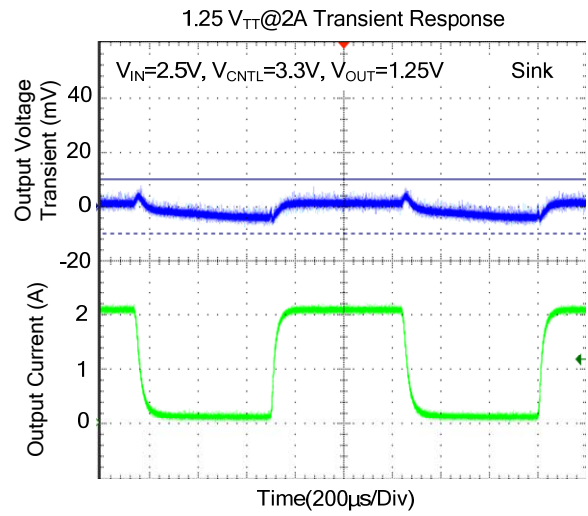
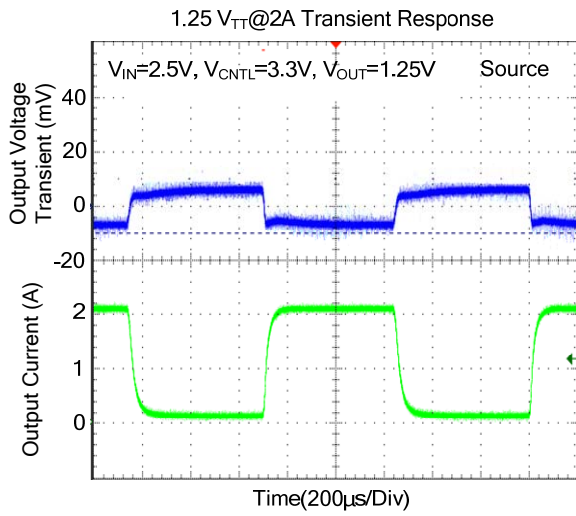


$R_1=R_2=100\text{K}\Omega$ ,  $C_{OUT}=10\mu\text{F}(\text{Ceramic})+1000\mu\text{F}$  under the worst case testing condition

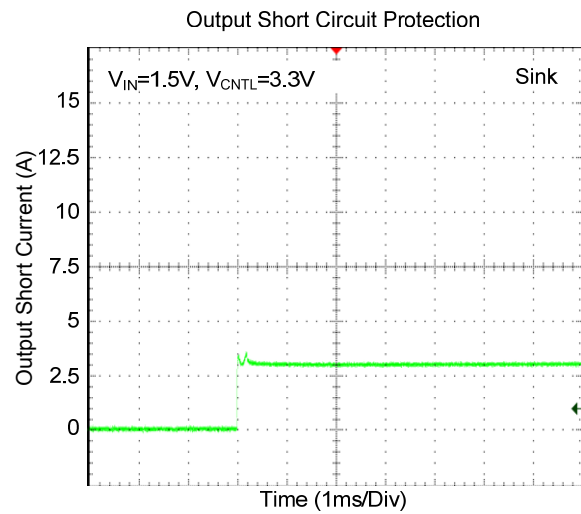
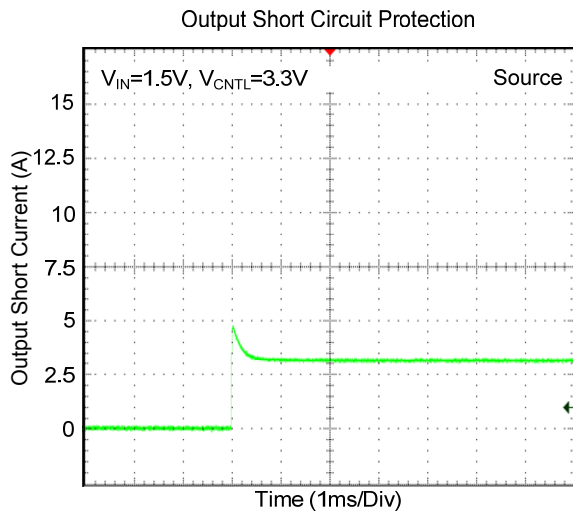
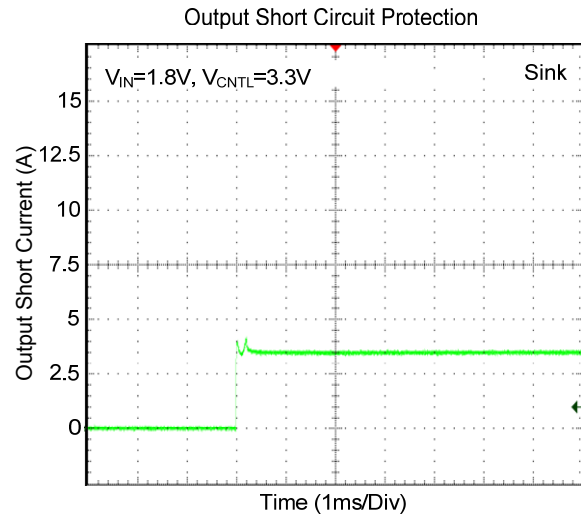
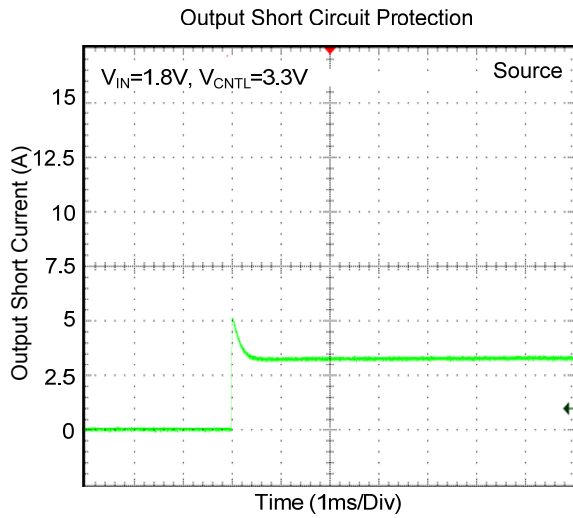
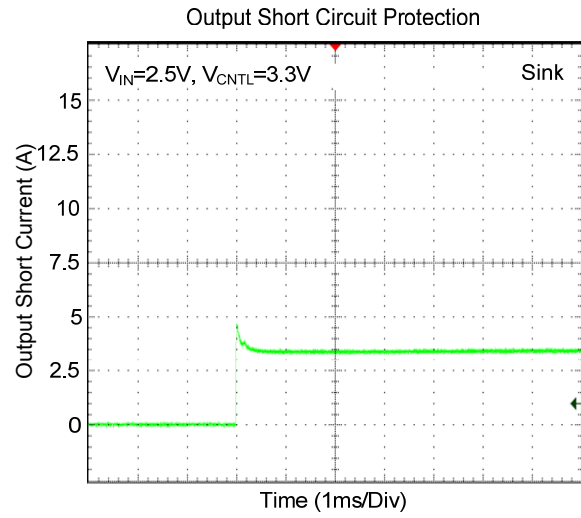
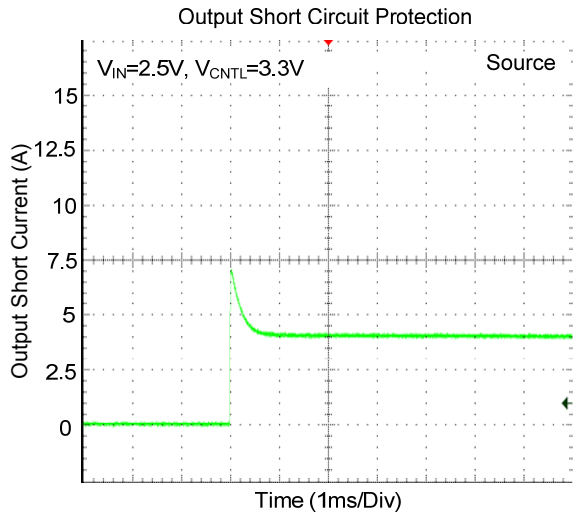
$C_{SS}=1\mu\text{F}$ ,  $C_{IN}=470\mu\text{F}(\text{Low ESR})$ ,  $C_{CNTL}=47\mu\text{F}$

$$V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V), V_{OUT} \text{ track } V_{REF}$$

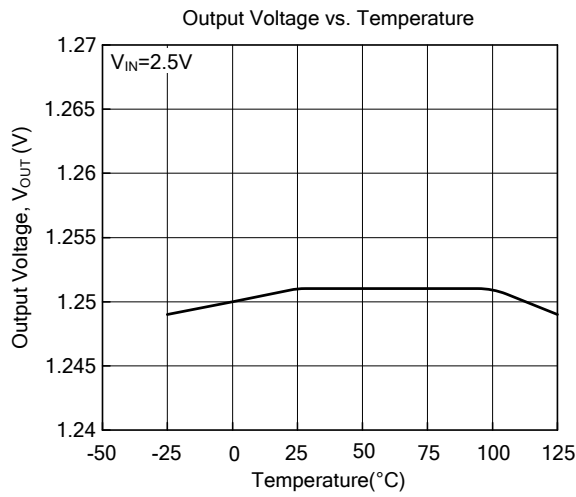
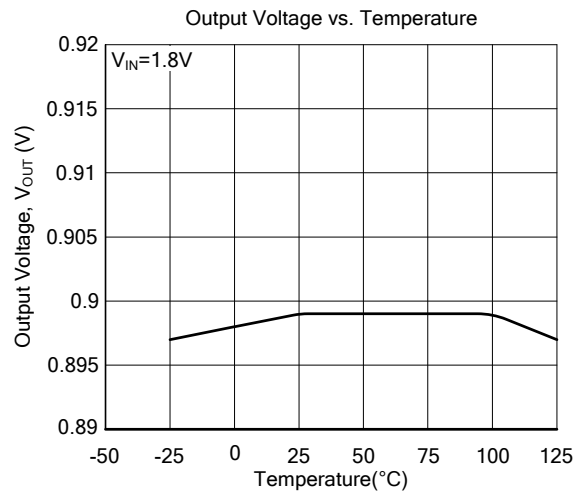
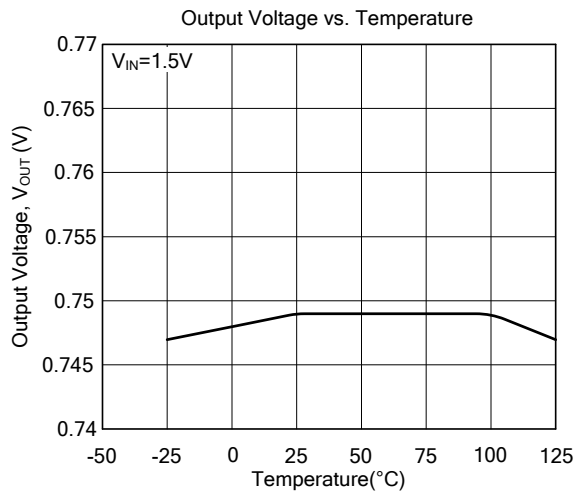
## TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS(Cont.)



## ■ TYPICAL CHARACTERISTICS(Cont.)





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