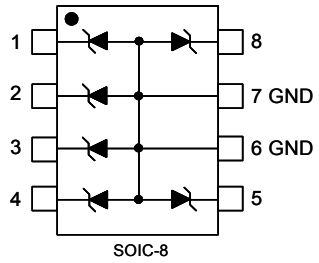
HEX TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This 6 TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5V, 12V, 15V and 24V. This TVS array offers an integrated solution to protect up to 6 data lines where the board space is a premium.

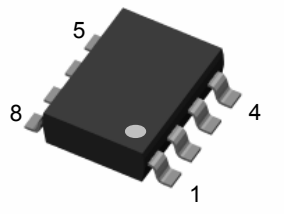
SPECIFICATION FEATURES

- **350W Power Dissipation (8x20µsec Waveform)**
- **Low Leakage Current, Maximum of 5µA at rated voltage**
- **Very Low Clamping Voltage**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **Packaged in the Industry Standard SOIC-8**



APPLICATIONS

- **RS-232C or RS-422 Communication ports**
- **GPIB/IEEE 485 Ports**
- **Portable Instrumentation**



MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8x20µsec Waveform)	P_{pp}	350	W
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-50 to +125	°C
Storage Temperature Range	T_{stg}	-50 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMDA05-6

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1mA	6			V
Reverse Leakage Current	I_R	V_R = 5V			5	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			9.8	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 24A			13	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 6, 7			225	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 6, 7			125	pF

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

PJSMDA12-6

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				12	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	13.3			V
Reverse Leakage Current	I_R	V_R = 12V			5	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			20	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 15A			25	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 6, 7			100	pF

PJSMDA15-6

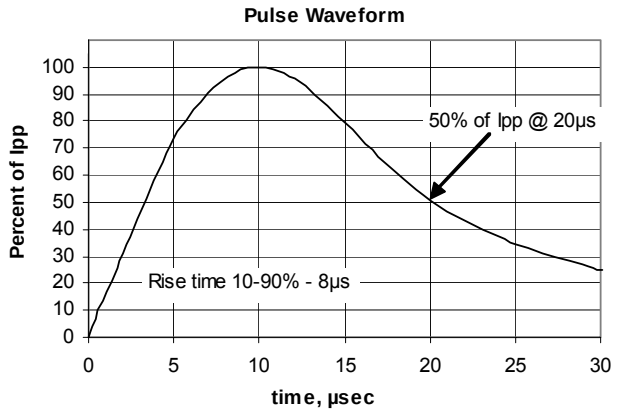
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				15	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	16.7			V
Reverse Leakage Current	I_R	V_R = 15V			5	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			24	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 12A			29	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 6, 7			80	pF

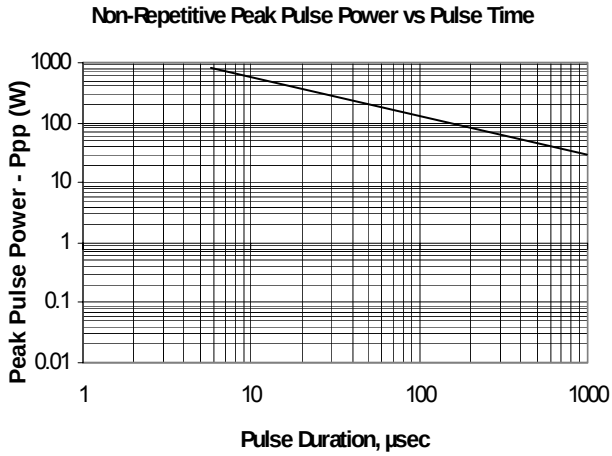
PJSMDA24-6

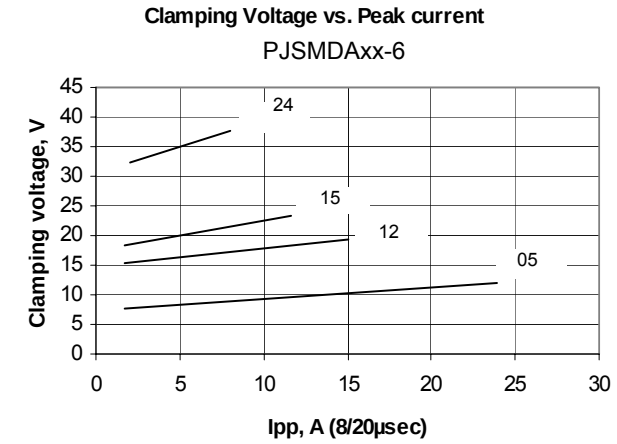
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				24	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1mA	26.7			V
Reverse Leakage Current	I_R	V_R = 24V			5	µA
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 5A			40	V
Clamping Voltage (8x20µsec)	V_{cl}	I_{pp} = 8A			44	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 6, 7			60	pF

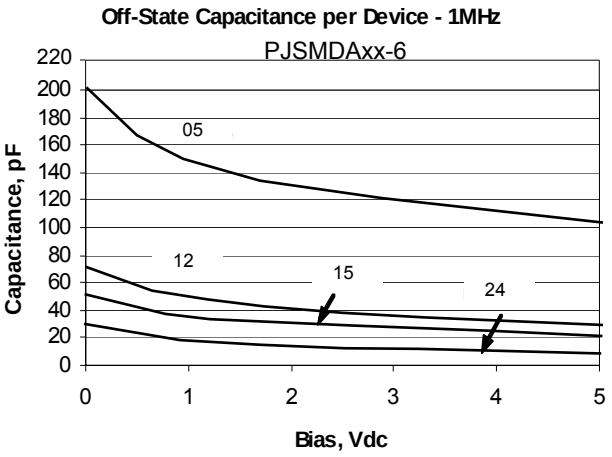
TYPICAL CHARACTERISTICS TJ = 25°C unless otherwise noted

Surge Pulse Waveform Definition





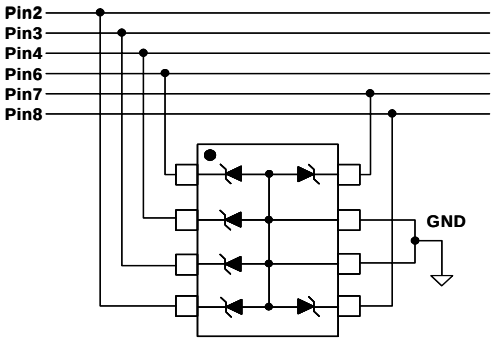




TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS

RS232 Pinout

Pin	Name	RS232	V.24	Dir	Description
1	CD	CF	109		Carrier Detect
2	RXD	BB	104		Receive Data
3	TXD	BA	103		Transmit Data
4	DTR	CD	108.2		Data Terminal Ready
5	GND	AB	102		System Ground
6	DSR	CC	107		Data Set Ready
7	RTS	CA	105		Request to Send
8	CTS	CB	106		Clear to Send
9	RI	CE	125		Ring Indicator



Dimensions in inches