Data Sheet June 13, 2008 FN6726.0

Monolithic Quad SPST CMOS Analog Switches

The DG411/883 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, and TTL and CMOS compatible digital inputs.

These switches feature lower analog ON-resistance (<35Ω) and faster switch time (t_{ON} <175ns) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411/883 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON-resistance variation with analog signals is quite low over a ±15V analog input range. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting “break-before-make” or “make-before-break” operation with a minimum of external logic.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG411AK/883	-55 to +125	16 Ld CerDIP	F16.3

Features

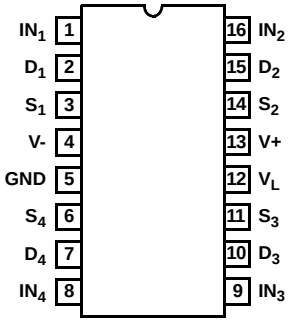
- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- ON-Resistance <35W Max
- Low Power Consumption (P_D <35mW)
- Fast Switching Action
  - t_{ON} <175ns
  - t_{OFF} <145ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Pinout

DG411/883,
(16 LD CERDIP)
TOP VIEW



(NC) NO CONNECTION

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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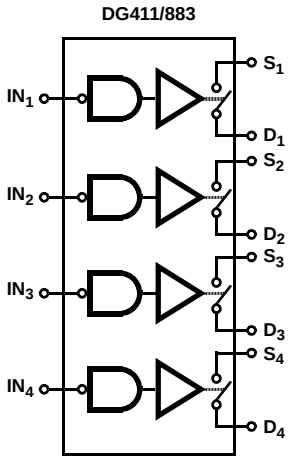
Functional Diagram Four SPST Switches per Package Switches Shown for Logic “1” Input



Pin Description

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	V_L	Logic Reference Voltage
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

TABLE 1. TRUTH TABLE

LOGIC	SWITCH
0	ON
1	OFF

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V.

Absolute Maximum Ratings

V+ to V- 44V
GND to V-. 25V
V_L (Note 3). . . . . .(GND -0.3V) to (V+) +0.3V
Digital Inputs, V_S, V_D (Note 4) . . . . . .(V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle). 100mA

Operating Conditions

Operating Voltage Range. . . . . .±20V Max
Operating Temperature Range . . . . . .-55°C to +125°C
Input Low Voltage . . . . . 0.8V Max
Input High Voltage . . . . . .2.4V Min
Input Rise and Fall Time . . . . . .≤20ns

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld CERDIP Package.	75	20

Junction Temperature . . . . . .+175°C
Operating Temperature (A Suffix) . . . . . .-55°C to +125°C
Storage Temperature Range (A Suffix) . . . . . .-65°C to +125°C
Lead Temperature (Soldering 10s) . . . . . .+300°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. V_{IN} = Input Voltage to Perform Proper Function.
4. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

DC Electrical Specifications

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE (°C)	LIMITS MIN	LIMITS MAX	UNITS
Drain-to-Source ON-Resistance	$r_{DS(ON)}$	V+ = +13.5V, V- = -13.5V, I_S = -10mA, V_D = ±8.5V V_{IN} = 0.8V	1, 3	+25, -55	0	35	Ω
			2	+125	0	45	Ω
		V+ = +10.8V, V- = -0V, I_S = -10mA, V_D = 3.0V and 8.0V V_{IN} = 0.8V	1, 3	+25, -55	0	80	Ω
			2	+125	0	100	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = -15.5V, V_S = 15.5V V_{IN} = 2.4V	1	+25	-0.25	+0.25	nA
			2, 3	+125, -55	-20	+20	nA
		V+ = 16.5V, V- = -16.5V, V_D = 15.5V, V_S = -15.5V V_{IN} = 2.4V	1	+25	-0.25	+0.25	nA
			2, 3	+125, -55	-20	+20	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = -15.5V, V_S = 15.5V V_{IN} = 2.4V	1	+25	-0.25	+0.25	nA
			2, 3	+125, -55	-20	+20	nA
		V+ = 16.5V, V- = -16.5V, V_D = 15.5V, V_S = -15.5V V_{IN} = 2.4V	1	+25	-0.25	+0.25	nA
			2, 3	+125, -55	-20	+20	nA

DC Electrical Specifications

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE (°C)	LIMITS		UNITS
					MIN	MAX	
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, $V_S = V_D = \pm 15.5V$	1	+25	-0.4	+0.4	nA
			2, 3	+125, -55	-40	+40	nA
Input Current with V_{IN} Low	I_{IL}	Input Under Test = 0.8V, All Others = 2.4V	1, 2, 3	+25, +125, -55	-0.5	+0.5	µA
Input Current with V_{IN} High	I_{IH}	Input Under Test = 2.4V, All Others = 0.8V	1, 2, 3	+25, +125, -55	-0.5	+0.5	µA
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V	1	+25	-	+1.0	µA
			2, 3	+125, -55	-	+5.0	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V	1	+25	-	+1.0	µA
			2, 3	+125, -55	-	+5.0	µA
Negative Supply Current	I-	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V	1	+25	-1.0	-	µA
			2, 3	+125, -55	-5.0	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V	1	+25	-1.0	-	µA
			2, 3	+125, -55	-5.0	-	µA
Logic Supply Current	I_L	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V	1	+25	-	+1.0	µA
			2, 3	+125, -55	-	+5.0	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V	1	+25	-	+1.0	µA
			2, 3	+125, -55	-	+5.0	µA
Ground Current	I_{GND}	V+ = 16.5V, V- = -16.5, V_{IN} = 0V or 5.0V	1	+25	-1.0	-	µA
			2, 3	+125, -55	-5.0	-	µA
		V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5.0V V_L = 5.25V	1	+25	-1.0	-	µA
			2, 3	+125, -55	-5.0	-	µA

AC Electrical Specifications

Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE (°C)	LIMITS		UNITS
					MIN	MAX	
Turn ON Time	t_{ON}	C_L = 35pF, V_S = ±10V, R_L = 300Ω	9, 11	+25, -55	0	175	ns
			10	+125	0	240	ns
		V+ = 12V, V- = 0V, C_L = 35pF, V_S = +8V, R_L = 300Ω	9, 11	+25, -55	0	250	ns
			10	+125	0	400	ns
Turn OFF Time	t_{OFF}	C_L = 35pF, V_S = ±10V, R_L = 300Ω	9, 11	+25, -55	0	145	ns
			10	+125	0	160	ns
		V+ = 12V, V- = 0V, C_L = 35pF, V_S = +8V, R_L = 300Ω	9, 11	+25, -55	0	125	ns
			10	+125	0	140	ns

Electrical Specifications Device Tested at: V+ = +15V, V- = -15V, V_L = 5V, GND = 0V, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE (°C)	LIMITS		UNITS
					MIN	MAX	
Charge Injection	Q	V_G = 0V, R_G = 0Ω, T_A = +25°C, C_L = 10nF (see Figure 2)	9	+25	-100	+100	pC
				+25			pC
		V_G = 6V, R_G = 0Ω, T_A = +25°C C_L = 10nF, V+ = 12V, V- = 0V (see Figure 2)	9	+25	-100	+100	pC
				+25			pC

TABLE 2. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (See "Electrical Spec Tables" on page 3 and page 4)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 5), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

5. PDA applies to Subgroup 1 only.

Typical Performance Curves

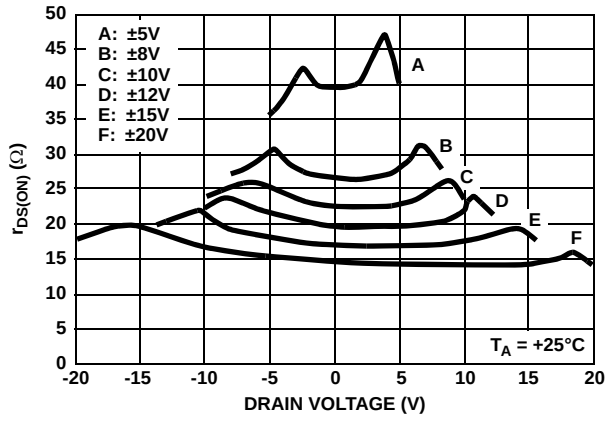


FIGURE 1. ON-RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE

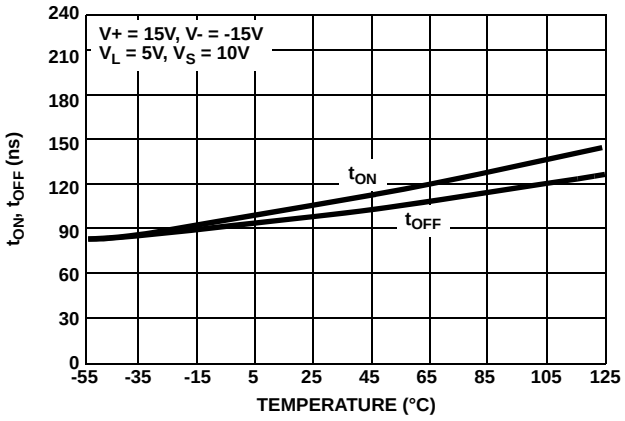


FIGURE 2. SWITCHING TIME vs TEMPERATURE

Typical Performance Curves (Continued)

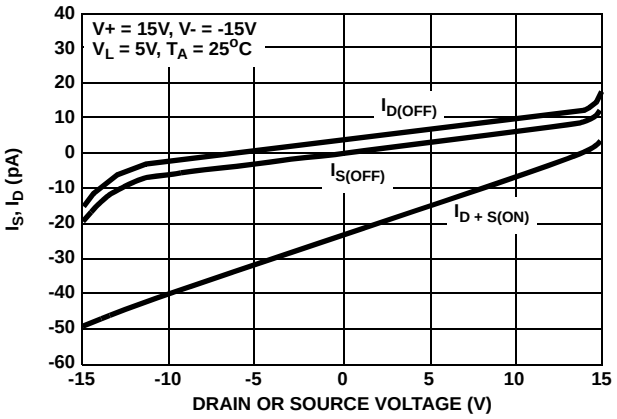


FIGURE 3. LEAKAGE CURRENT vs ANALOG VOLTAGE

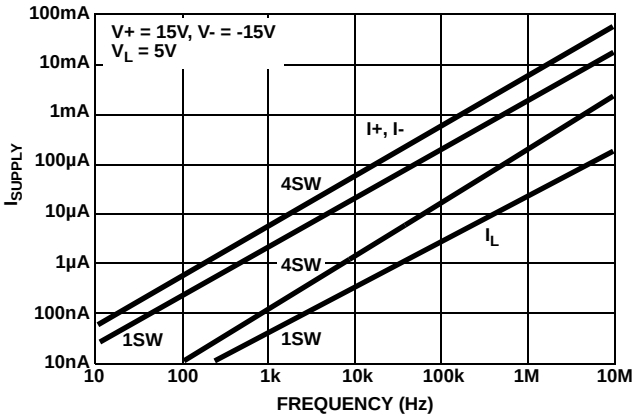


FIGURE 4. SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY

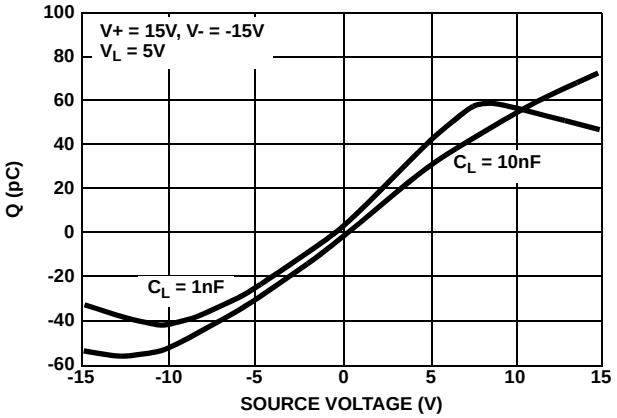


FIGURE 5. CHARGE INJECTION vs ANALOG VOLTAGE (V_D)

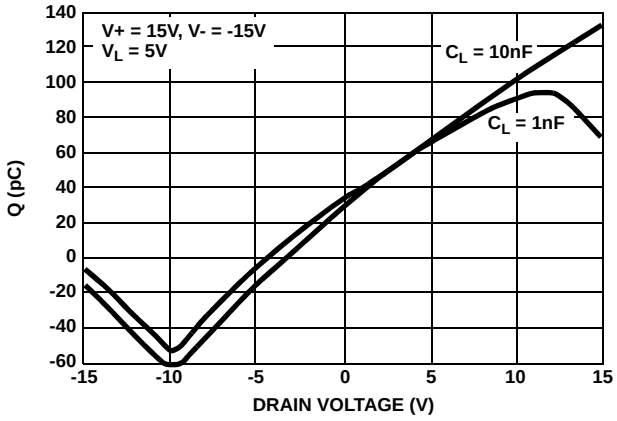
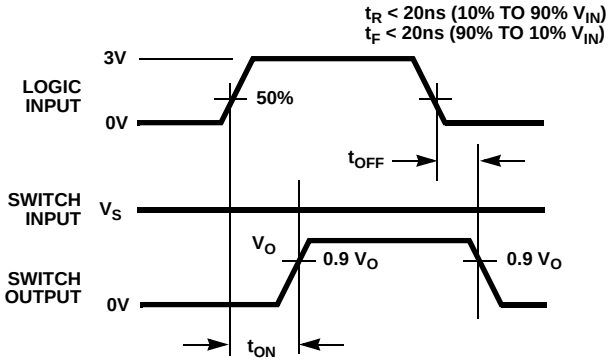


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

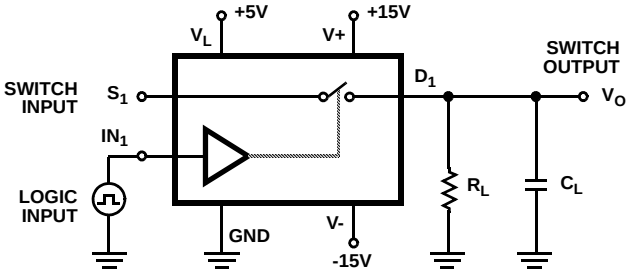
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 7A.



Repeat test for all IN and S.

For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 7B.

FIGURE 7. SWITCHING TIME

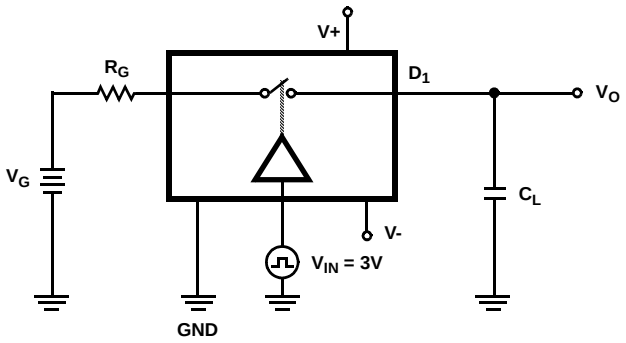
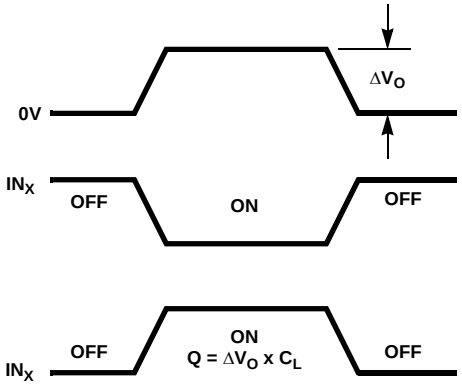


FIGURE 8A.

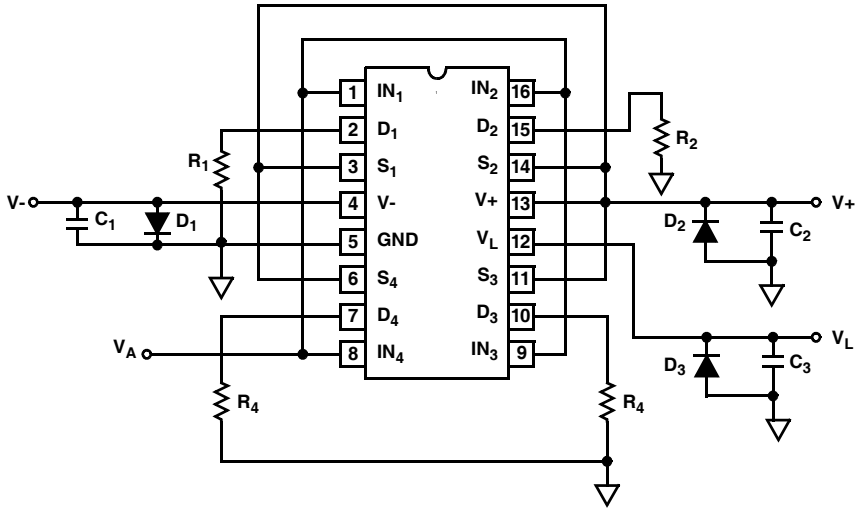


IN_X dependent on switch configuration input polarity determined by sense of switch.

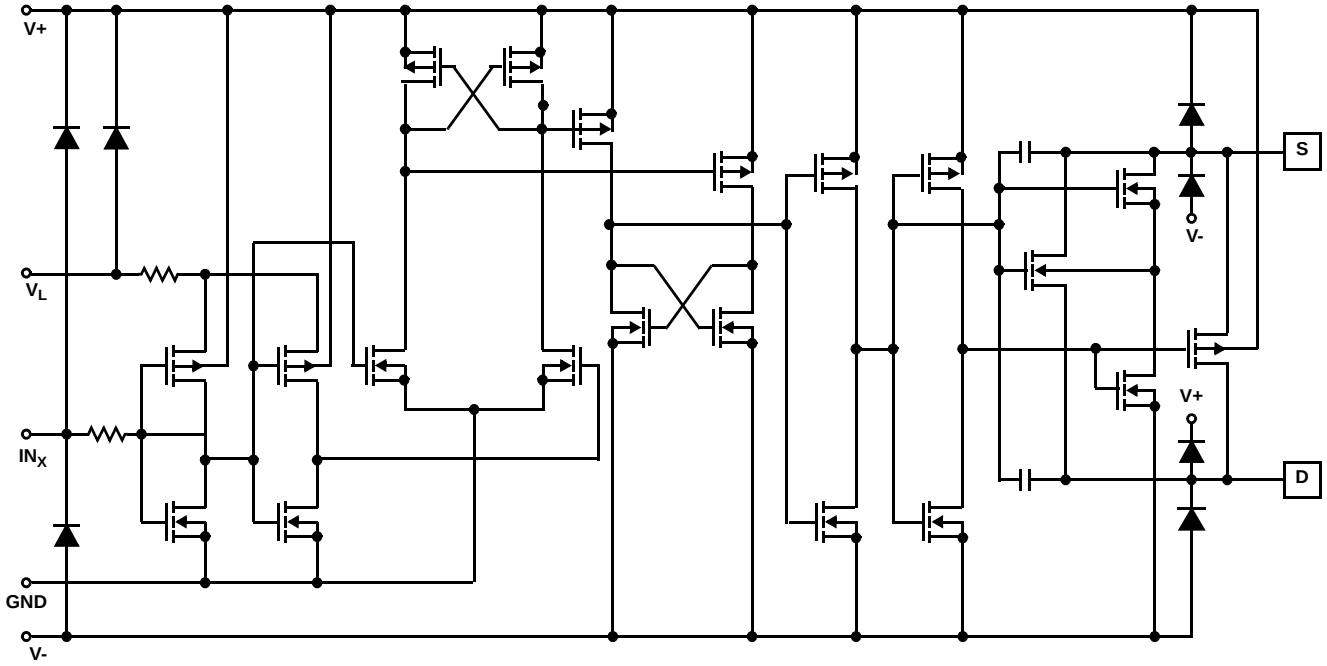
FIGURE 8B.

FIGURE 8. CHARGE INJECTION

Burn-In Circuit



Typical Schematic Diagram (Typical Channel)



Die Characteristics

DIE DIMENSIONS:

2760µm x 1780µm x 485 ± 25µm

METALLIZATION:

Type: SiAl

Thickness: 12kÅ ± 1kÅ

GLASSIVATION:

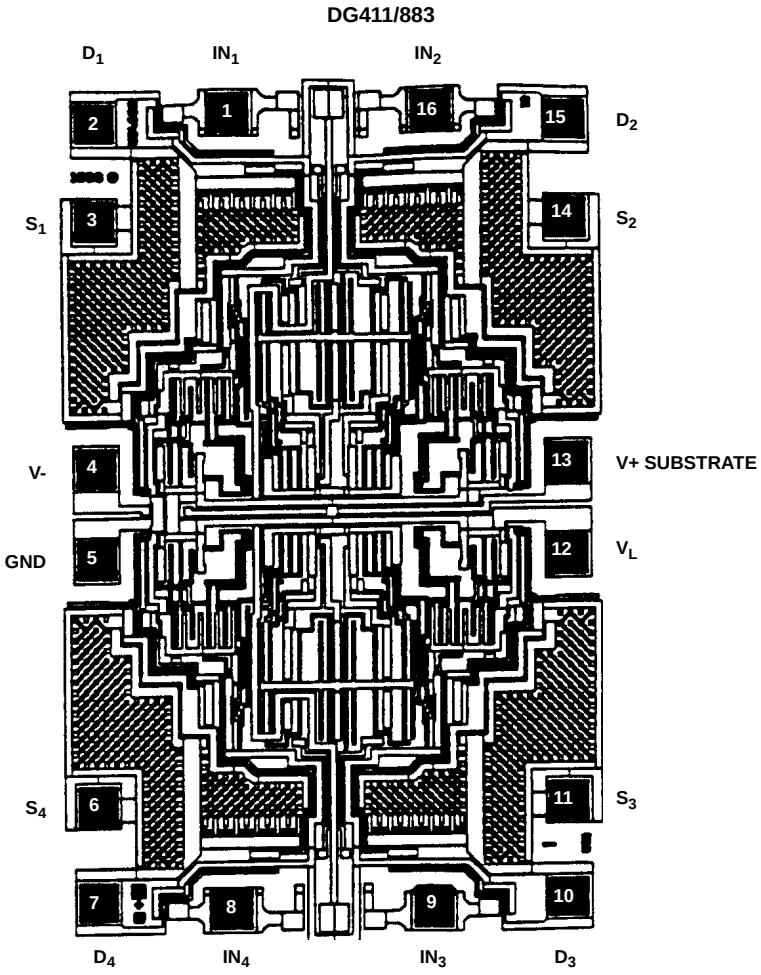
Type: Nitride

Thickness: 8kÅ ± 1kÅ

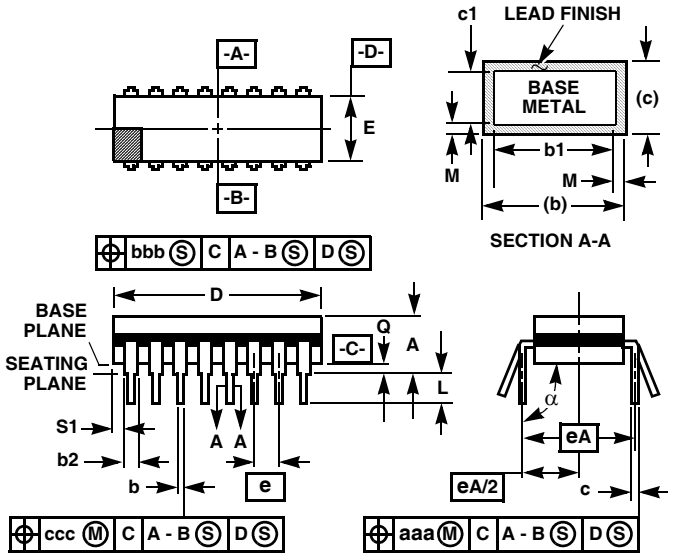
WORST CASE CURRENT DENSITY:

$1.5 \times 10^5 A/cm^2$

Metallization Mask Layout



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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