C8051

Legacy-Speed 8-Bit Processor Core

The C8051 core implements a single-chip, 8-bit microcontroller that executes all ASM51 instructions and has the same instruction set and timing of the 80C31. On-chip debugging is an option.

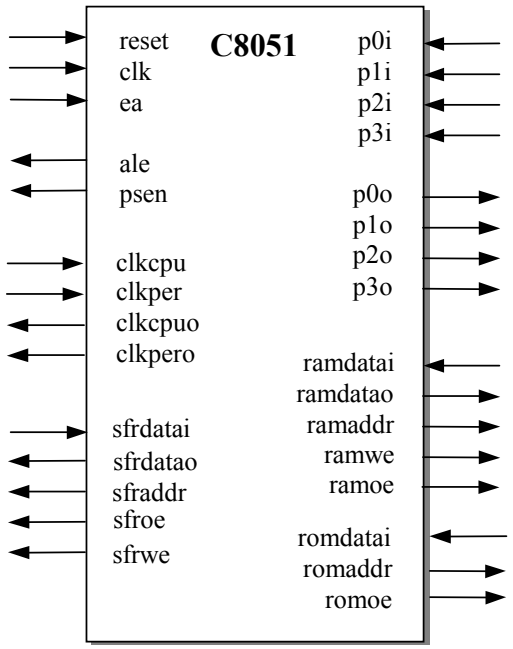
The microcode-free design was developed for reuse in ASICs and FPGAs. It is strictly synchronous, with positive-edge clocking (except for a flip-flop for internal reset and two flip-flops for gated clocks in the PMU), no internal tri-states and a synchronous reset. Scan insertion is therefore straightforward.

Applications

The C8051 can be utilized for a variety of applications including:

- Embedded microcontroller systems
- Data computation and transfer
- Communication systems
- Professional audio and video

Symbol



Features

- 8-bit Control Unit
- 8-bit Arithmetic-Logic Unit with 8-bit multiplication and division
- Instruction decoder
- Four 8-bit Input / Output ports
- Two 16-bit Timer/Counters
- Serial Peripheral Interface in full duplex mode
- Synchronous mode, fixed baud rate
- 8-bit & 9-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- Multiprocessor communication
- Two Level Priority Interrupt System
- 5 Interrupt Sources
- Internal Clock prescaler and Phase Generator
- 256 bytes of Read/Write Data Memory Space
- 64KB External Program Memory Space
- 64KB External Data Memory Space
- Services up to 107 External Special Function Registers
- Power Management Unit supports stop and idle modes
- On-Chip-Instrumentation Debugging (optional)

Optional Features

- Fast Multiplication-Division Unit
  - 16 x 16 bit multiplication
  - 32 / 16 bit division
  - 16 / 16 bit division
  - 32 bit normalization
  - 32 bit L/R shifting
- Compare/Capture Unit
  - Four 16-bit Compare registers used for Pulse With Modulation
  - Four external Capture inputs used for Pulse With Measuring
  - 16-bit Reload register used for Pulse Generation
- Programmable Watchdog Timer
- Third 16-bit Timer/Counter
- Second Serial Peripheral Interfaces
- Real Time Clock
- On-Chip-Instrumentation Debugging

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Functional Description

The C8051 is partitioned into modules described below:

Memory Control Unit

- Can address up to 64K bytes of External Program Memory Space
- Can address up to 64K bytes of External Data Memory Space

Core Engine

The C8051 engine is composed of four components:

- Control unit
- Arithmetic-logic unit
- Memory control unit
- RAM and SFR control unit

The C8051 engine allows fetching instructions from program memory and execution using RAM or SFR.

Control Unit

The Control Unit performs instruction fetch and execution from the Memory Control Unit and the RAM_SFR Control Unit.

RAM and SFR Unit

- Can Address up to 256 bytes of Read/Write Data Memory space
- Serves the interface for off-core Special Function Registers

Arithmetic-logic Unit

- 8-bit arithmetic & logic operations
- Boolean manipulations
- 8 x 8-bit multiplication
- 8 / 8-bit division

Timer 0 and 1

Timers 0 and 1 are nearly identical. Timers 0 and 1 both have four modes. They are:

- 13-bit Timer/counter
- 16-bit Timer/counter
- 8-bit timer/counter with auto reload
- two 8-bit timers

The later mode is available to Timer 0 only. Each timer can also serve as a counter of external pulses (1 to 0 transition) on the corresponding T0 or T1 pin. One other option is to gate the timer/counter using an external control signal. This allows the timer to measure the pulse width of external signals.

Serial

The C8051 core provides interface for serial communication. The serial port is capable of both synchronous and asynchronous modes. In synchronous mode, the microcontroller generates the clock and operates in a half-duplex mode. In asynchronous mode, full duplex operation is available. Receive data is buffered in a holding register. This allows the serial to receive an incoming word before software has read the previous value.

The port provides four operating modes. These offer different communication protocols and baud rates:

- Synchronous mode, fixed baud rate
- 8-bit UART mode, variable baud rate
- 9-bit UART mode, fixed baud rate
- 9-bit UART mode, variable baud rate

Interrupt Service Routine

The C8051 core improves two-priority interrupt system. There are 5 interrupt sources. Each source has an independent priority bit, flag, interrupt vector, and enable. In addition, interrupts can be globally enabled or disabled.

Ports

The C8051 provides four I/O ports. Port 0 – Port 3 is an 8-bit bi-directional I/O ports with separated inputs and outputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memories.

Port 1 also serves the special features like external interrupt inputs, Serial 1 interface, and Timer 2 inputs.

Port 2 emits the high-order address byte during fetches from external program memory that use 16-bit addresses (MOVX @DPTR).

Port 3 also serves the special features such as read and write strobes for external data memory, Serial 0 interface, Timer 0 and Timer 1 inputs.

Clock Control

The Clock Control unit generates the internal synchronous reset. It also contains registers for selecting the clock for timers.

Interface for On-Chip Instrumentation

The OCI unit serves as an interface for On-Chip Instrumentation. The OCI provides the following functions for communication with On-Chip Instrumentation:

- the run/stop control
- single-step mode
- software breakpoint
- debugger program
- hardware breakpoint
- program trace
- access to ACC register

Power Management Unit

Power Management Unit serves two power management modes IDLE and STOP.

Support

The core as delivered is warranted against defects for three years from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The C8051 core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model that contained the original Intel 80C31 chip, and the results compared with the core's simulation outputs.

Deliverables

The core includes everything required for successful implementation:

- HDL source code for the C8051
- Synthesis & simulation scripts
- Example CHIP_C8051 – 8051 compatible design
  This design uses the C8051 and illustrates how to build and connect memories and port modules
- Extensive HDL testbench that instantiates:
  - Example design CHIP_C8051
  - External RAM
  - External ROM
  - Clock generator
  - Process that compares your simulation results with the expected results
- A collection of 8051 assembler programs which are executed directly by the testbench
- A set of expected results
- Documentation
- Design support including consulting

CAST
info@cast-inc.com
www.cast-inc.com

CAST, Inc. 11 Stonewall Court
Woodcliff Lake, NJ 07677 USA
tel 201-391-8300 fax 201-391-8694

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This core developed by the processor experts at Evatronix SA.