

GENERAL DESCRIPTION

The **SP3495E - SP3497E** transceivers are suitable for high speed bidirectional communication on multipoint bus transmission lines. They are designed for balanced data transmission and comply with both RS-485 and RS-422 EIA standards. Each device contains one differential driver and one differential receiver

Driver differential outputs and receiver differential inputs are connected internally to form a half-duplex input/output to the RS-485 bus. Separate RE and DE pins enable and disable the driver and receiver independently or may be externally connected together as a direct control. The device enters a low power shutdown mode if both driver and receiver are disabled. The bus-pin outputs of disabled or powered down devices are in high impedance state. The high impedance driver output is maintained over the entire common-mode voltage range of -7V to +12V.

SP3495E - SP3497E operates from a single 3.3V power supply. SP3495E - SP3497E transceivers load the data bus only half as much as a standard RS-485 unit load. This allows up to 64 devices to be connected simultaneously on a bus without violating required RS-485 signal margin and without using repeaters. Excessive power dissipation caused by bus contention or by shorting outputs to ground or a voltage source is prevented by short circuit protection and thermal shutdown. This feature forces the driver output into high impedance state if the absolute value of the output current exceeds 250mA or if junction temperature exceeds 165°C. Receivers will fail-safe to a logic high output state if the inputs are unconnected (floating) or shorted. All RS-485 inputs

and outputs are ESD protected up to +/-15kV Human Body Model.

FEATURES

- 3.3V Single Supply Operation
- High Speed up to 32Mbps
- Robust +/-15kV ESD protection
- Hot Swap glitch protection
- Advanced Fail-safe Receiver Inputs
- Half Unit Load, 64 Transceivers on bus
- Driver short circuit current limit and thermal shutdown for overload protection
- Low Current 1uA shutdown mode

TYPICAL APPLICATIONS

- Factory Automation Controls
- Motor Control
- Industrial Process Control
- Building Automation
- Security Systems
- Remote Utility Meter Reading
- Long or un-terminated transmission lines

FIGURE 1. TYPICAL APPLICATION CIRCUIT

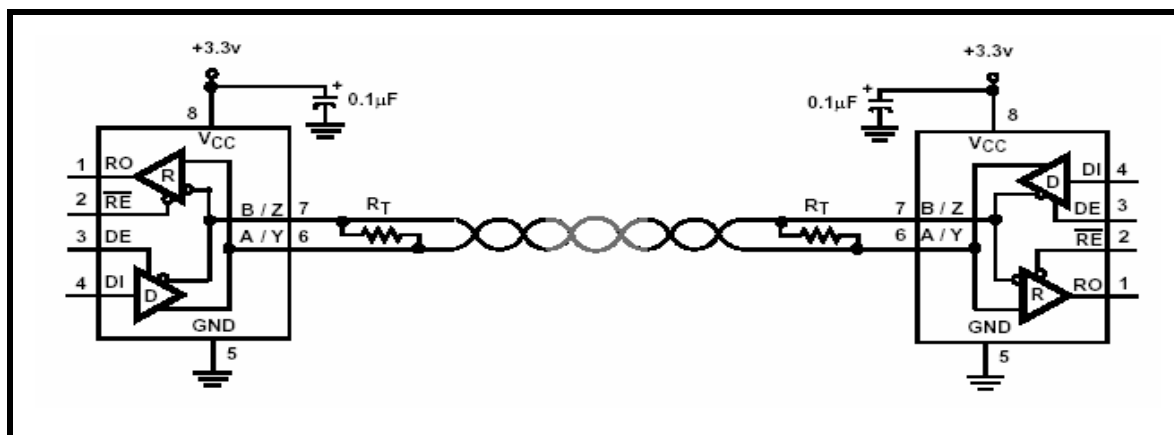
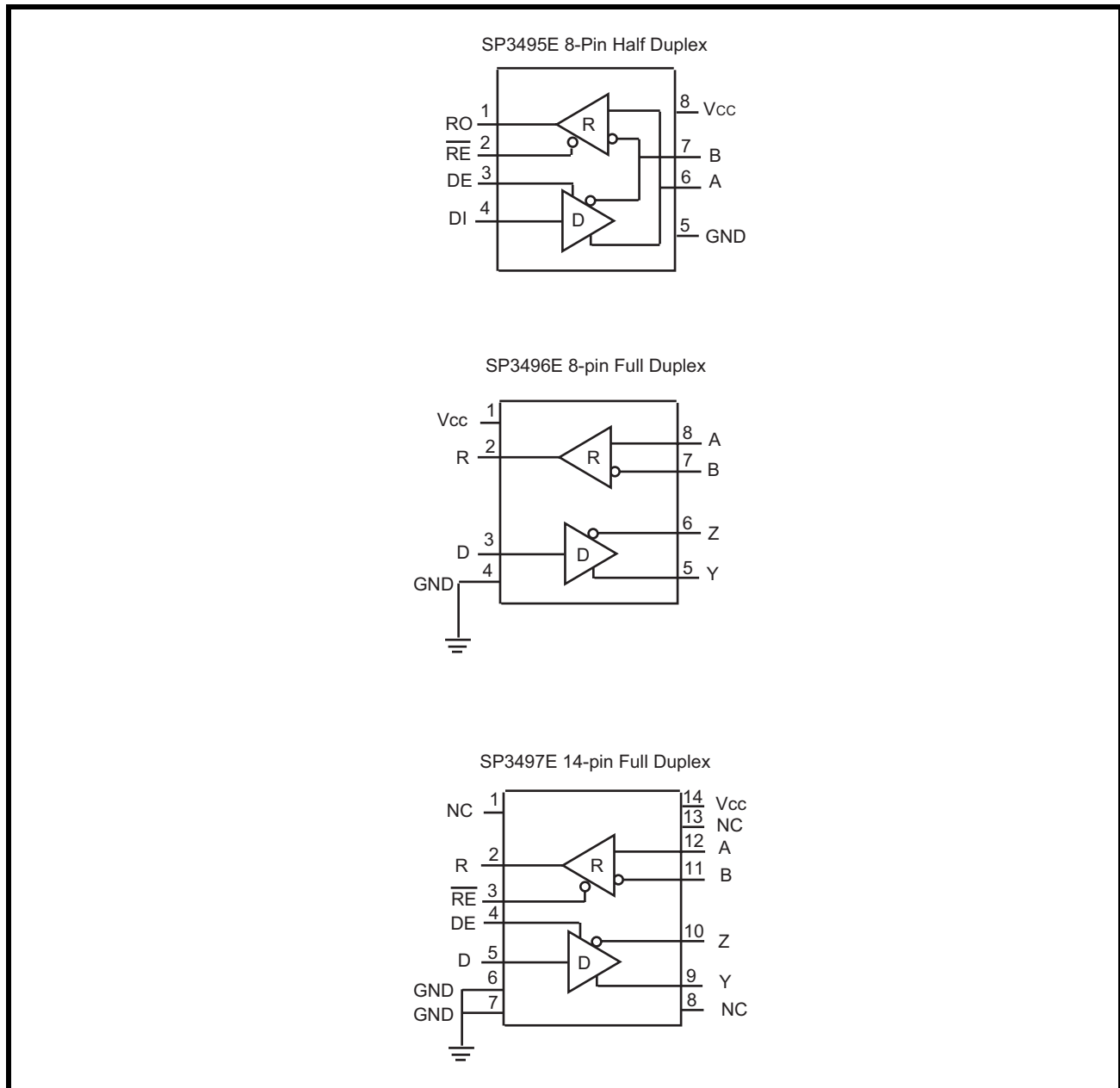


FIGURE 2. PIN OUT ASSIGNMENT



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
SP3495EEN-L	8-pin Narrow SOIC	-40°C to +85°C	Active
SP3495EEN-L/TR	8-pin Narrow SOIC	-40°C to +85°C	Active
SP3496EEN-L	8-pin Narrow SOIC	-40°C to +85°C	Active
SP3496EEN-L/TR	8-pin Narrow SOIC	-40°C to +85°C	Active
SP3497EEN-L	14-pin Narrow SOIC	-40°C to +85°C	Active
SP3497EEN-L/TR	14-pin Narrow SOIC	-40°C to +85°C	Active

Note: To order Tape and Reel option include "/TR" in ordering part number. All packages are Pb-free/ RoHS compliant.



PIN DESCRIPTIONS

Pin Assignments

PIN NUMBER			PIN NAME	TYPE	DESCRIPTION
HALF DUPLEX	FULL DUPLEX				
SP3495E	SP3496E	SP3497E			
1	2	2	RO	O	Receiver Output. When \overline{RE} is low and if $(A-B) \geq -40mV$, RO is High. If $(A-B) \leq -200mV$, RO is Low.
2	-	3	\overline{RE}	I	Receiver Output Enable, When \overline{RE} is Low, RO is enabled. When \overline{RE} is High, RO is high impedance. \overline{RE} should be High and \overline{DE} should be low to enter shutdown mode. \overline{RE} is a hot-swap input.
3	-	4	DE	I	Driver Output Enable. When DE is High, outputs are enabled. When DE is low, outputs are high impedance. DE should be low and \overline{RE} should be High to enter shutdown mode. DE is a hot-swap input
4	3	5	DI	I	Driver Input. With DE high, a low level on DI forces Non-Inverting output low and inverting output high. Similarly, a high level on DI forces Non-Inverting output High and Inverting output Low.
5	4	6, 7	GND	Pwr	Ground
6	-	-	A	O	Non-Inverting Receiver Input and Non-Inverting Driver Output
7	-	-	B	O	Inverting Receiver Input and Inverting Driver Output
8	1	14	Vcc	Pwr	+3.3V power supply input. Bypass with 0.1uF capacitor.
-	8	12	A	I	Non-Inverting Receiver Input
-	7	11	B	I	Inverting Receiver Input
-	5	9	Y	O	Non-Inverting Driver Output
-	6	10	Z	O	Inverting Driver Output
-	-	1, 8, 13	NC	-	No Connect, not internally connected

Pin type: I=Input, O=Output.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}	+6.0V
Input Voltage at control pins (\overline{RE} , DE and DI)	-0.5V to ($V_{CC} + 0.3V$)
Voltage Range on A and B pins	-9V to +14V
Storage Temperature Range	-65°C to + 150°C
Power Dissipation Maximum Junction Temperature 150°C 8-Pin SO $\theta_{JA} = 128.4^{\circ}C/W$ 14-Pin SO $\theta_{JA} = 86^{\circ}C/W$	

CAUTION:

ESD (Electrostatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

ELECTRICAL CHARACTERISTICS

UNLESS OTHERWISE NOTED: $V_{CC} = +3.0V$ TO $+3.6V$ WITH T_A FROM $-40^{\circ}C$ TO $+85^{\circ}C$. TYPICAL VALUES ARE AT $V_{CC} = +3.3V$ AND $25^{\circ}C$.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DC CHARACTERISTICS						
V_{OD}	Differential Driver Output			V_{CC}	V	No Load
		2.0				$R_L = 100\Omega$ (RS-422), Figure 3
		1.5				$R_L = 54\Omega$ (RS-485), Figure 3
		1.5				$V_{CM} = -7V$, Figure 4
		1.5				$V_{CM} = +12V$, Figure 4
ΔV_{OD}	Change in Magnitude of Differential Output	-0.20		0.20	V	$R_L = 100\Omega$ (RS-422), Figure 3, See note 1
		-0.20		0.20		$R_L = 54\Omega$ (RS-485), Figure 3, See note 1
		-0.20		0.20		$V_{CM} = -7V$, Figure 4, See note 1
		-0.20		0.20		$V_{CM} = +12V$, Figure 4, See note 1
V_{OC}	Driver Common Mode Output Voltage steady state	1.3		2.5	V	Figure 3
ΔV_{OC}	Change in Magnitude of Common Mode Output Voltage	-0.2		0.2	V	Figure 3, See note 1
I_{DSC}	Driver Short Circuit Current Limit	-250			mA	V_{OUT} Forced to -7V, Figure 5
				250	mA	V_{OUT} Forced to +12V, Figure 5



UNLESS OTHERWISE NOTED: $V_{CC} = +3.0V$ TO $+3.6V$ WITH T_A FROM $-40^{\circ}C$ TO $+85^{\circ}C$. TYPICAL VALUES ARE AT $V_{CC} = +3.3V$ AND $25^{\circ}C$.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Logic Input Thresholds (DI, DE, \overline{RE})	2.0			V	Logic Input High
V_{IL}				0.8	V	Logic Input Low
V_{HYS}	Driver Input Hysteresis		100		mV	$T_A = 25^{\circ}C$
I_{IN}	Logic Input Current (DI, DE and \overline{RE})			10	μA	$I_N = 0V$
		-10			μA	$I_N = V_{CC}$

Driver AC Characteristics

freq	Data Signaling Rate	32			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{PLH}	Driver Propagation Delay (low to High)	5	11	24	ns	$C_L = 50pF$, $R_L = 54\Omega$, freq = 8MHz, Figures 6 and 7
t_{PHL}	Driver Propagation Delay (High to Low)	5	11	24	ns	$C_L = 50pF$, $R_L = 54\Omega$, freq = 8MHz, Figures 6 and 7
t_R	Driver Rise Time	2.5	4.5	10	ns	$C_L = 50pF$, $R_L = 54\Omega$, freq = 8MHz, Figures 6 and 7
t_F	Driver Fall time	2.5	4.5	10	ns	$C_L = 50pF$, $R_L = 54\Omega$, freq = 8MHz, Figures 6 and 7
$ t_{PLH}-t_{PHL} $	Differential Pulse Skew			3	ns	Figures 6 and 7
t_{OZH}	Driver Enable to Output High			50	ns	$C_L = 50pF$, $R_L = 500\Omega$, Figures 8 and 9
t_{OZL}	Driver Enable to Output Low			50	ns	$C_L = 50pF$, $R_L = 500\Omega$, Figures 10 and 11
t_{OHZ}	Driver Disable from Output High			50	ns	$C_L = 50pF$, $R_L = 500\Omega$, Figures 8 and 9
t_{OLZ}	Driver Disable from Output Low			50	ns	$C_L = 50pF$, $R_L = 500\Omega$, Figures 10 and 11
t_{OZV}	Shutdown to Driver Output Valid			6	μs	$C_L = 50pF$, $R_L = 500\Omega$
t_{SHDN}	Time to Shutdown	50		600	ns	Note 2 and 3

RECEIVER DC CHARACTERISTICS

I_{IN}	Input Current (A, B pins)	-290		500	μA	$DE = 0$, $V_{CC} = 0$ or $3.3V$ V_A or $V_B = 12V$, other input $0V$ V_A or $V_B = -7V$, other input $0V$
V_{IH}	Receiver Differential Thresholds ($V_A - V_B$)		-85	-40	mV	$-7V \leq V_{CM} \leq 12V$, rising
V_{IL}			-200	-125	mV	$-7V \leq V_{CM} \leq 12V$, falling
	Receiver Input Hysteresis		25		mV	$V_{CM} = 0V$
V_{OH}	Receiver Output Voltage High	2.4			V	$I_{OUT} = -8mA$, $V_{ID} = 200mV$
V_{OL}	Receiver Output Voltage Low			0.4	V	$I_{OUT} = 8mA$, $V_{ID} = -200mV$

UNLESS OTHERWISE NOTED: $V_{CC} = +3.0V$ TO $+3.6V$ WITH T_A FROM $-40^{\circ}C$ TO $+85^{\circ}C$. TYPICAL VALUES ARE AT $V_{CC} = +3.3V$ AND $25^{\circ}C$.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{OZ}	High-Z Receiver Output Current	-1			μA	$RE = V_{CC}, V_{OUT} = 0V$
				1	μA	$RE = V_{CC}, V_{OUT} = V_{CC}$
I_{OSS}	Receiver Output Short Circuit Current	-95			mA	$V_{OUT} = 0V$
				95	mA	$V_{OUT} = V_{CC}$
R_{IN}	Receiver Input Resistance	24			$K\Omega$	$-7V \leq V_{CM} \leq 12V$
RECEIVER AC CHARACTERISTICS						
freq	Data Signaling Rate	32			Mbps	$1/t_{UI}$, Duty Cycle 40 to 60%
t_{PLH}	Receiver Propagation Delay (Low to High)		15	40	ns	$V_{ID} = +/-2V, C_L = 15pF$, Freq = 8MHz, Figure 12 and 13
t_{PHL}	Receiver Propagation Delay (High to Low)		15	40	ns	$V_{ID} = +/-2V, C_L = 15pF$, Freq = 8MHz, Figure 12 and 13
skew	Receiver Propagation Delay Skew			3	ns	$V_{ID} = +/-2V, C_L = 15pF$, Freq = 8MHz, Figure 12 and 13 $skew = t_{PLH} - t_{PHL} $
t_R	Receiver Output Rise Time	1	2	6	ns	$C_L = 15pF$, Freq = 8MHz
t_F	Receiver Output Fall Time	1	2	6	ns	$C_L = 15pF$, Freq = 8MHz
t_{ZH}	Receiver Enable to Output High			50	ns	$C_L = 15pF, R_L = 1k\Omega$, Figure 14
t_{ZL}	Receiver Enable to Output Low			50	ns	$C_L = 15pF, R_L = 1k\Omega$, Figure 14
t_{HZ}	Receiver Output High to Disable			50	ns	$C_L = 15pF, R_L = 1k\Omega$, Figure 14
t_{LZ}	Receiver Output Low to Disable			50	ns	$C_L = 15pF, R_L = 1k\Omega$, Figure 14
$t_{ZH(SHDN)}$	Shutdown to Receiver Output Valid High			6	μs	$C_L = 15pF, R_L = 1k\Omega$
$t_{ZL(SHDN)}$	Shutdown to Receiver Output Valid Low			6	μs	$C_L = 15pF, R_L = 1k\Omega$
t_{SHDN}	Time to Shutdown	50		600	ns	Note 2 and 3
POWER REQUIREMENTS AND RECOMMENDED OPERATING CONDITIONS						
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
I_{CC1}	Supply Current - Driver Enabled			5.0	mA	$DE = V_{CC}$, No Load, \overline{RE} and $DI = 0V$ or V_{CC}
I_{CC2}	Supply Current - Receiver Enabled			5.0	mA	$DE = 0V, \overline{RE} = 0V$, No Load
I_{CC3}	Supply Current - Shutdown Mode		1	6	μA	$DE = 0V, \overline{RE} = V_{CC}, DI = V_{CC}$ or $0V$
T_{SD}	Thermal Shutdown Temperature		165		$^{\circ}C$	



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SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Thermal Shutdown Hysteresis		20		$^{\circ}C$	
	ESD Protection at Pins A, B, Y and Z		+/-15		kV	Human Body Model

NOTE:

1. *Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.*
2. *The transceivers are put into shutdown by bringing \overline{RE} High and DE Low simultaneously for at least 600ns. If the control inputs are in this state for less than 50ns, the device is guaranteed not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. Note that the receiver and driver enable times increase during shutdown*
3. *Gauranteed by design and bench characterization.*

FIGURE 3. DRIVER DC TEST CIRCUIT

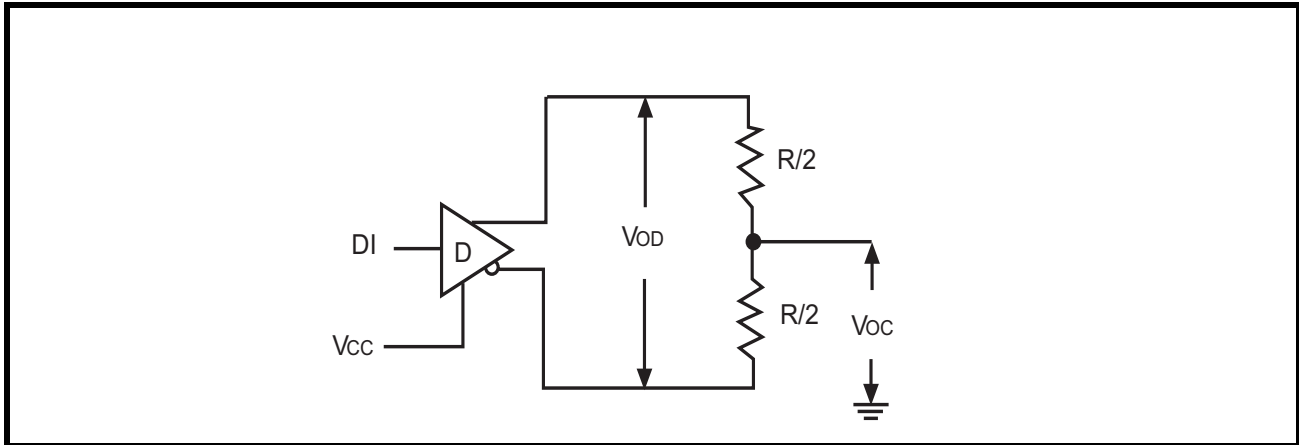


FIGURE 4. DRIVER COMMON MODE LOAD TEST

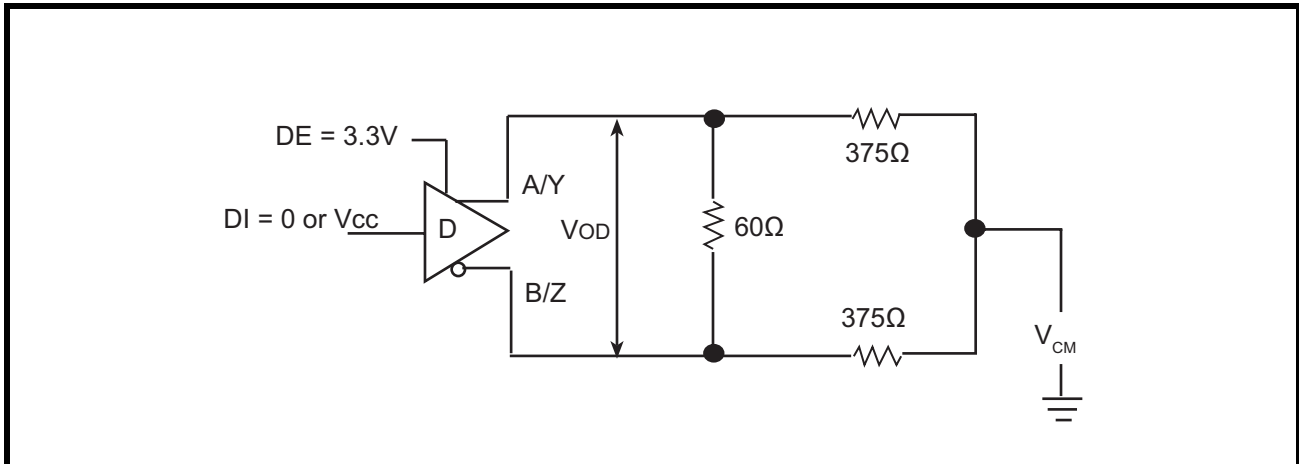


FIGURE 5. DRIVER SHORT CIRCUIT CURRENT LIMIT TEST

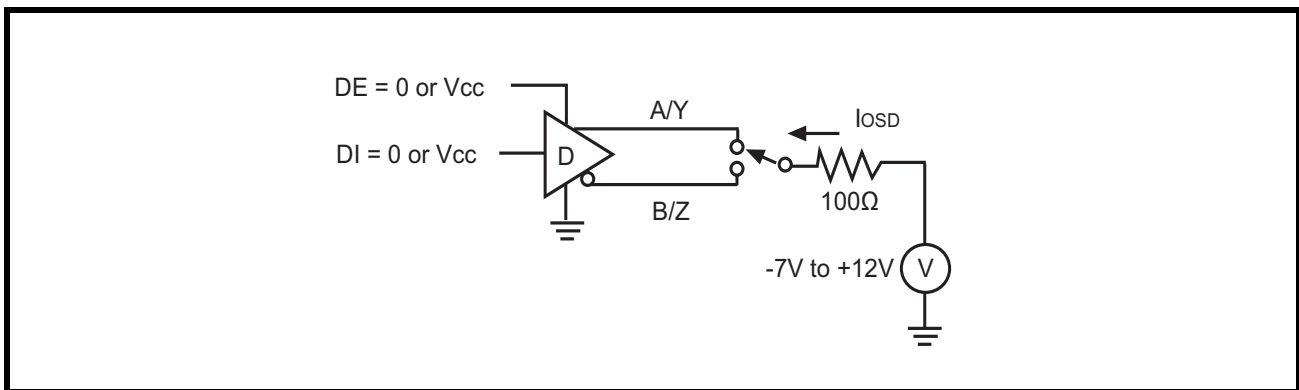


FIGURE 6. DRIVER PROPAGATION DELAY TEST CIRCUIT

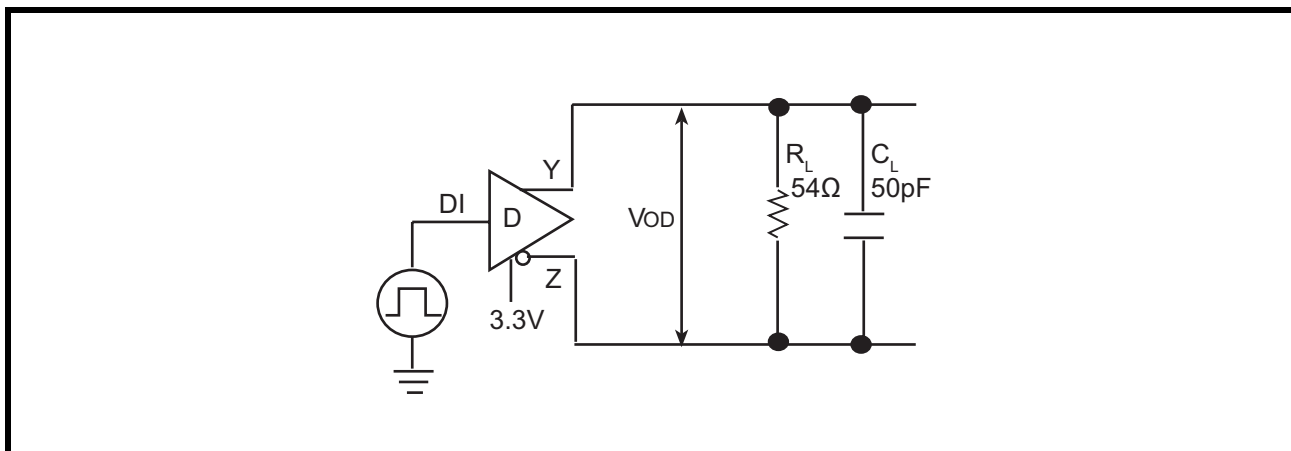


FIGURE 7. DRIVER PROPAGATION DELAY TIMING DIAGRAM

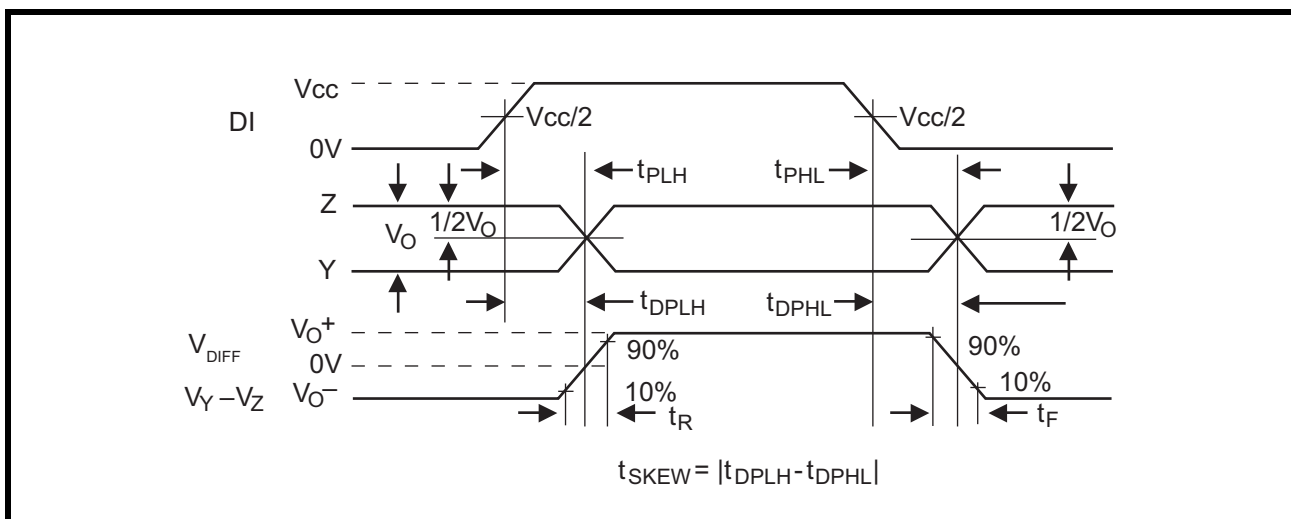


FIGURE 8. DRIVER ENABLE AND DISABLE TIME TEST CIRCUIT 1

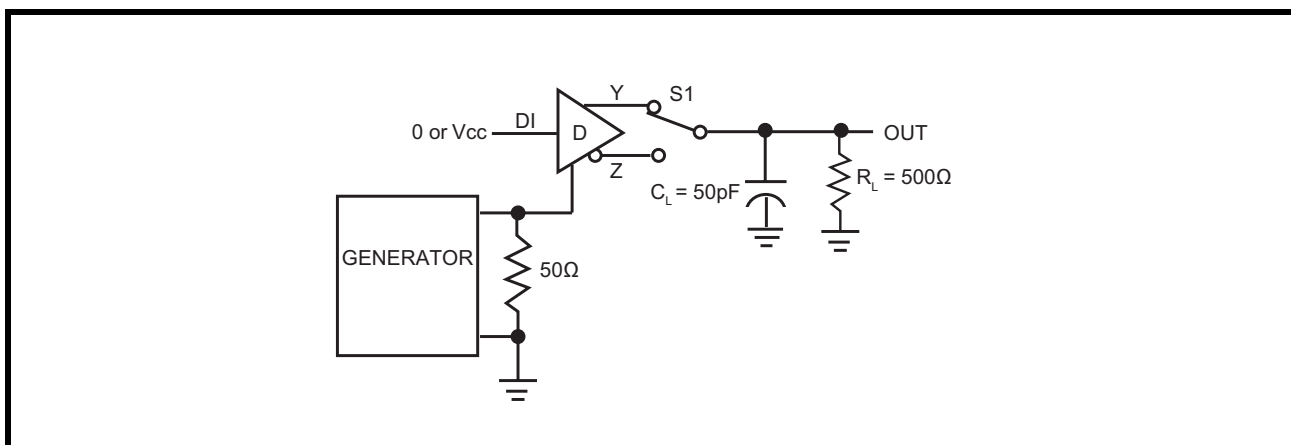


FIGURE 9. DRIVER ENABLE DISABLE TIMING DIAGRAM 1

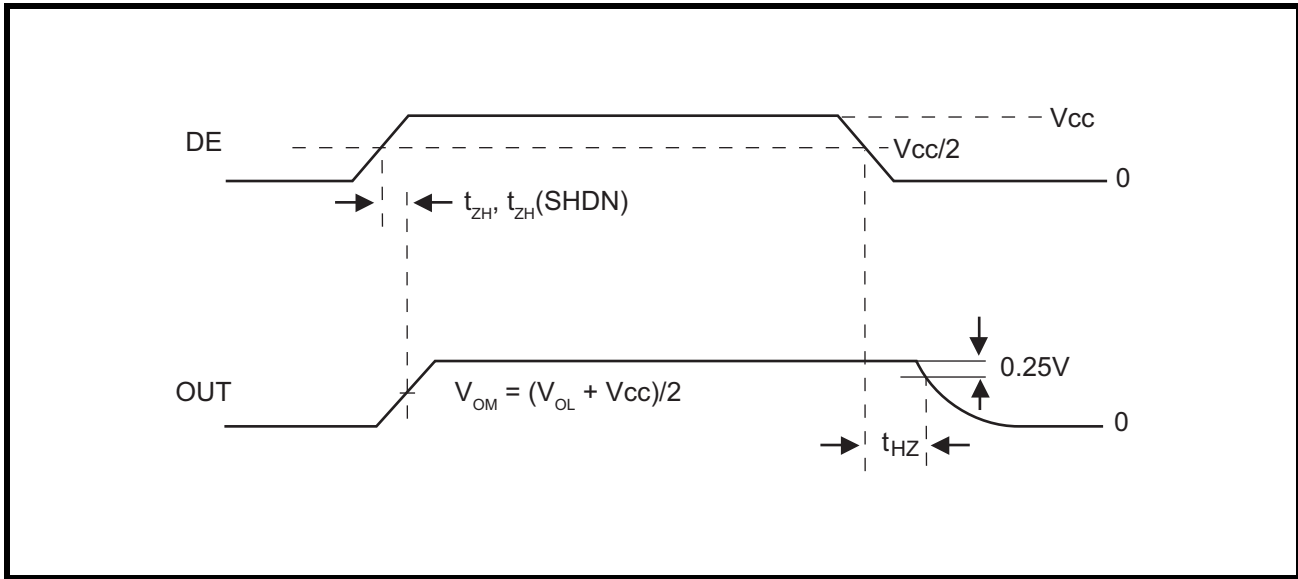


FIGURE 10. DRIVER ENABLE AND DISABLE TIME TEST CIRCUIT 2

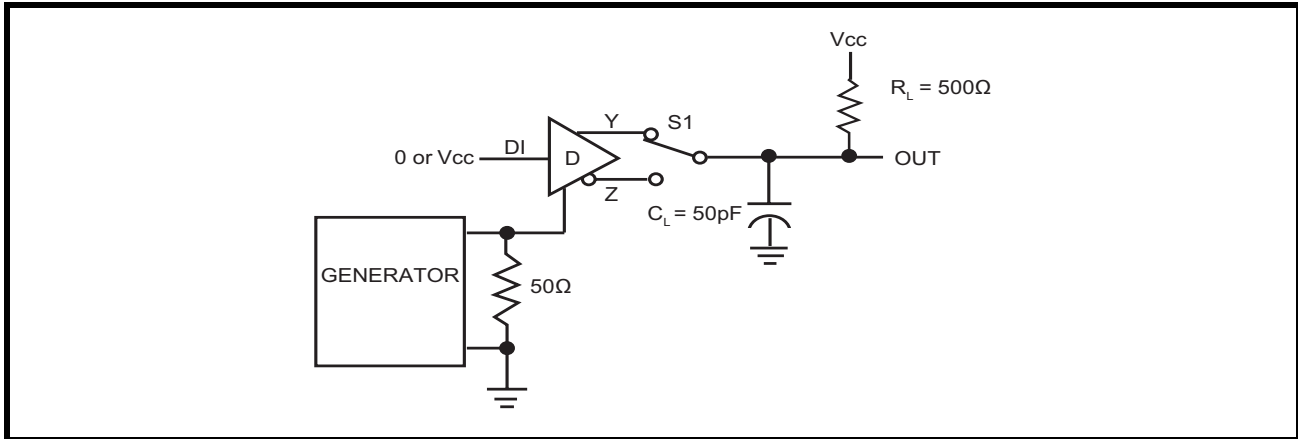


FIGURE 11. DRIVER ENABLE AND DISABLE TIMING DIAGRAM 2

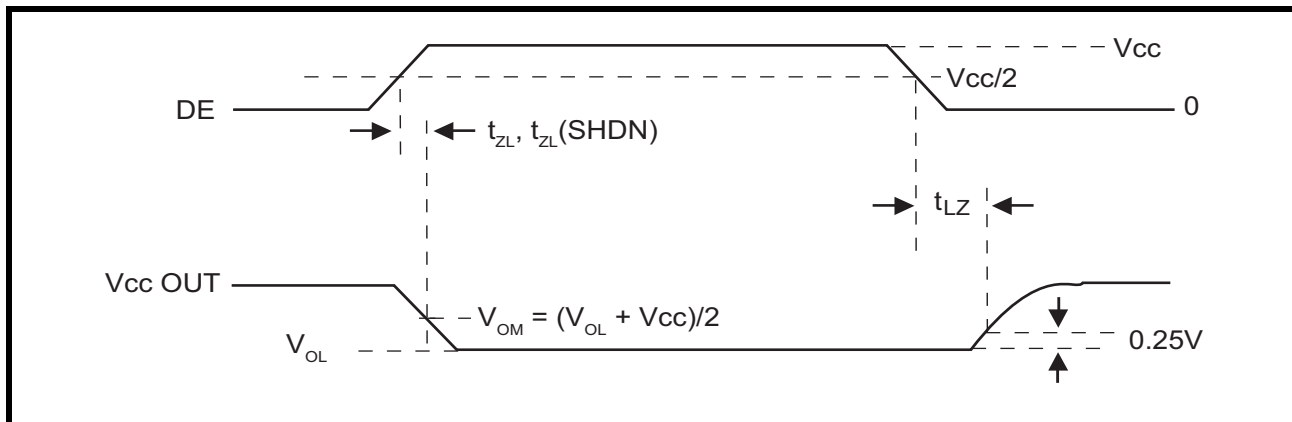


FIGURE 12. RECEIVER PROPAGATION DELAY TEST CIRCUIT

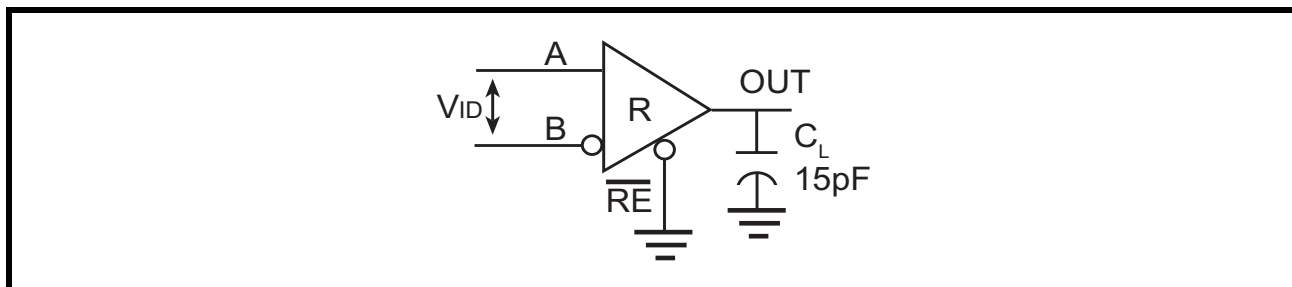


FIGURE 13. RECEIVER PROPAGATION DELAY TIMING DIAGRAM

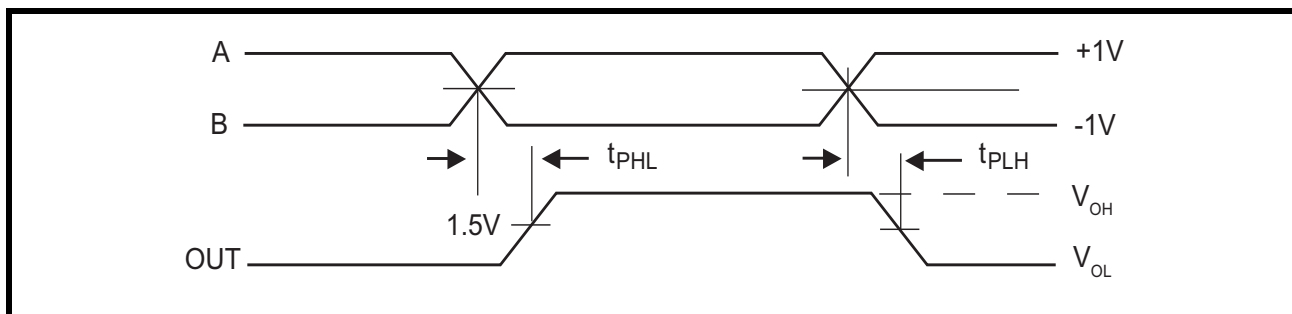


FIGURE 14. RECEIVER ENABLE AND DISABLE TIMES TEST CIRCUIT

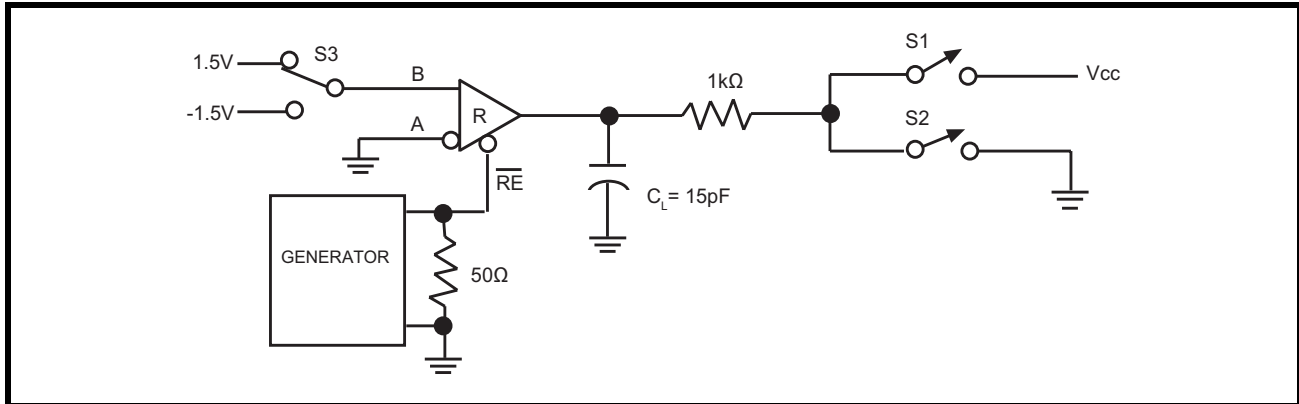


FIGURE 15. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 1

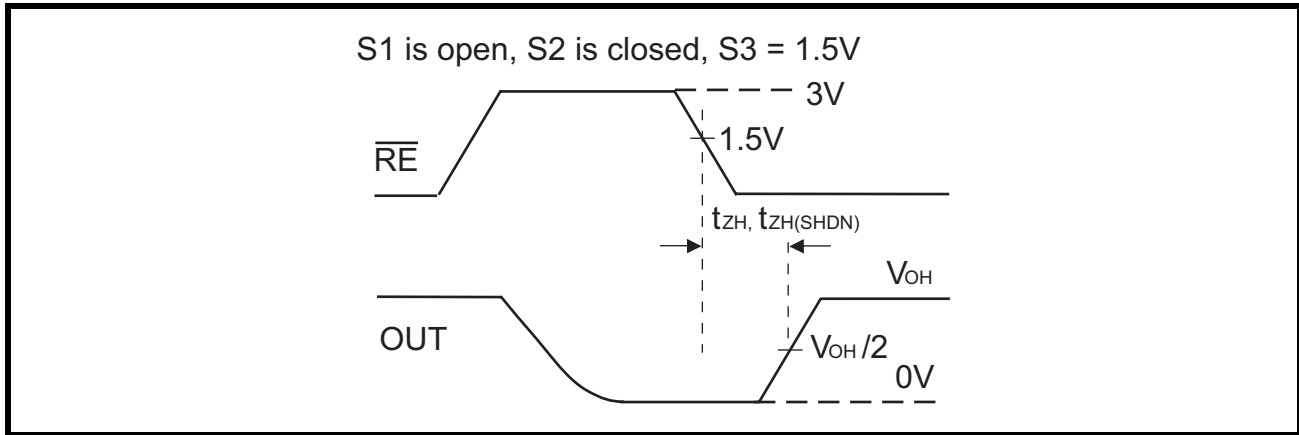


FIGURE 16. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 2

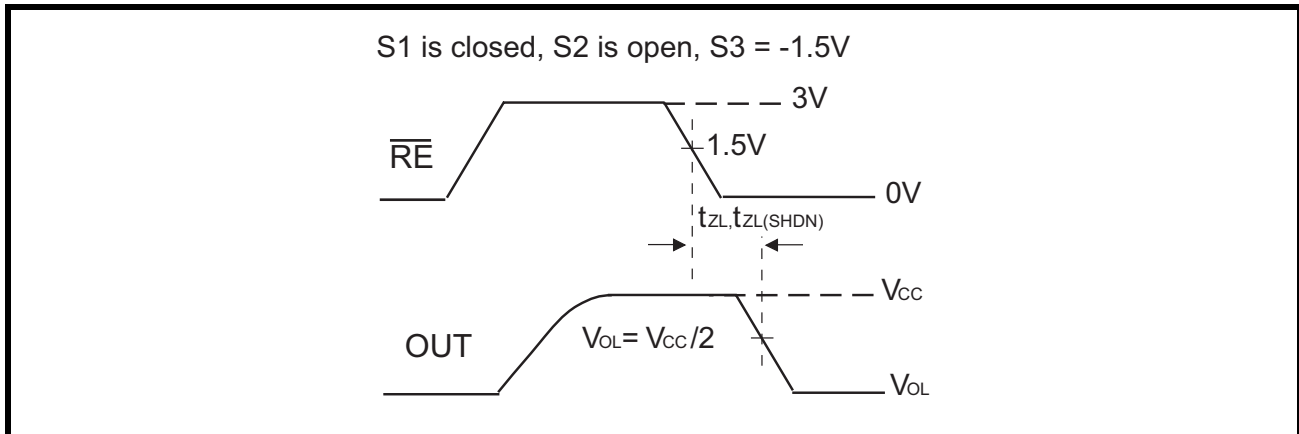


FIGURE 17. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 3

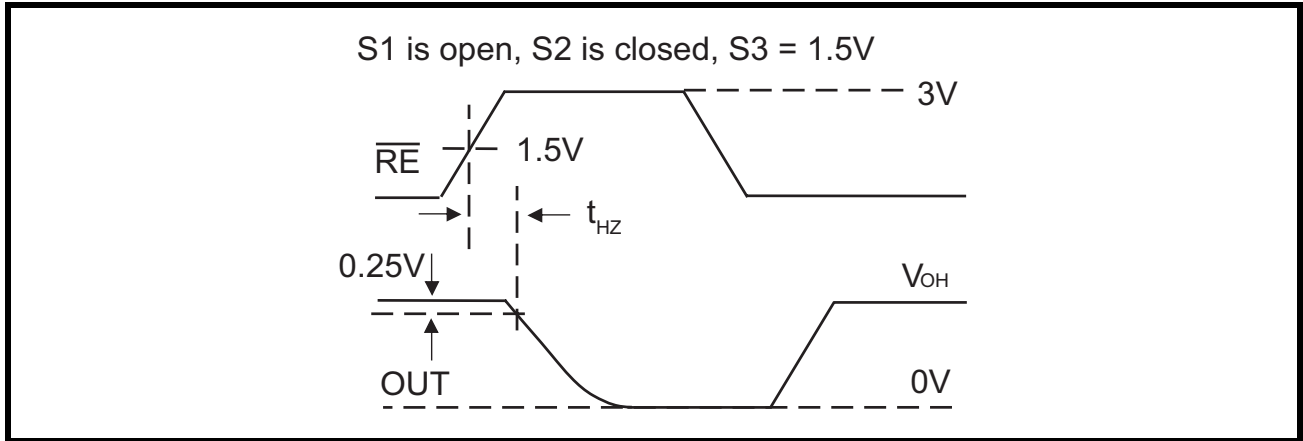
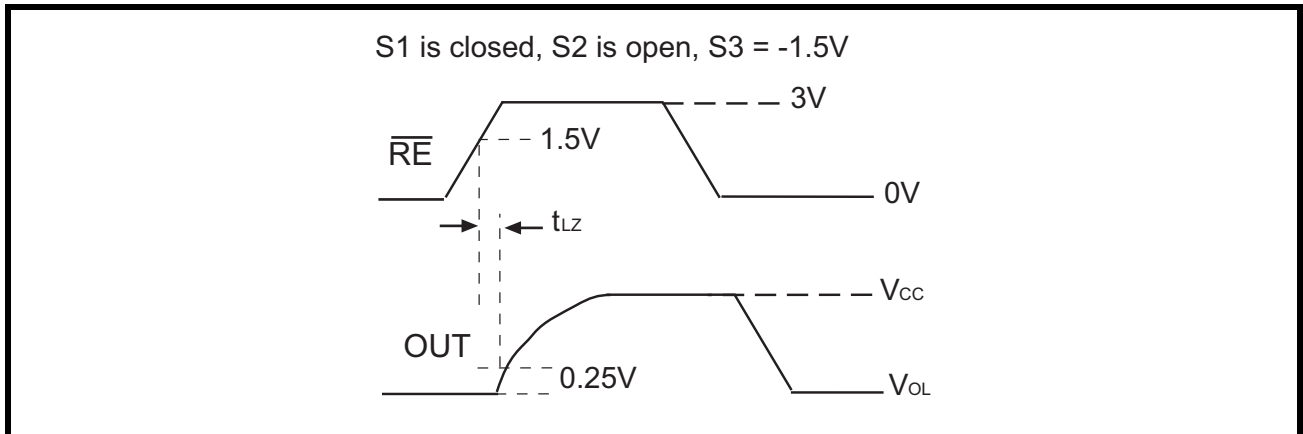


FIGURE 18. RECEIVER ENABLE AND DISABLE TIMING DIAGRAM 4



1.0 PRODUCT DESCRIPTION

The SP349xE high speed transceivers contain one driver and one receiver. The SP3495 is a half-duplex design while the SP3496E and SP3497E are full-duplex designs. The control pins \overline{RE} and DE feature a hotswap capability allowing live insertion without spurious data transfer. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry forces the driver output into a high-impedance state.

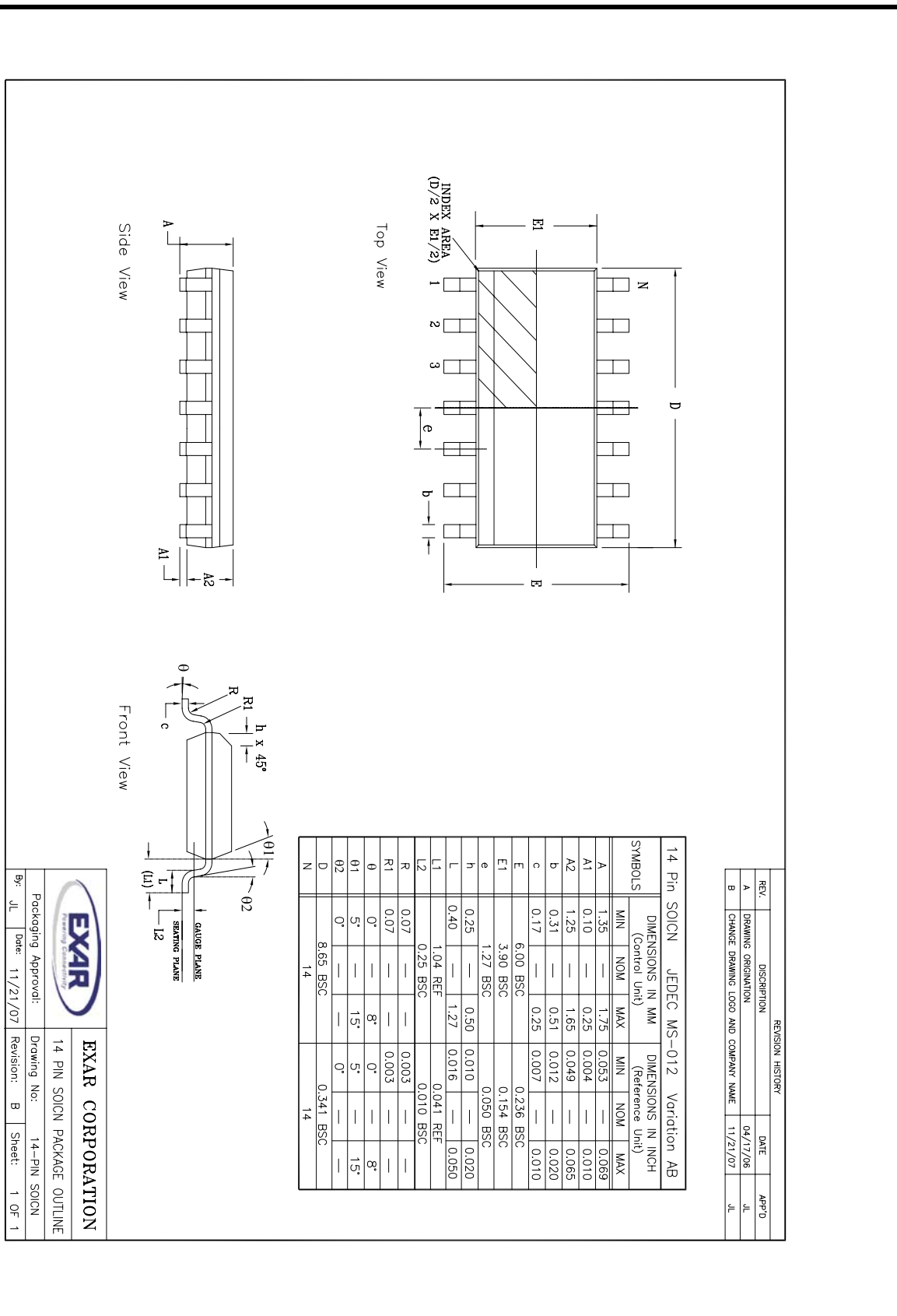
Advanced Failsafe

The Receivers incorporate fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled. In a terminated bus with all transmitters disabled the receivers differential input voltage is pulled to 0V by the termination. The SP349xE interprets 0V differential as a logic high with a minimum 40mV noise margin.

HOT-SWAP CAPABILITY

When Vcc is first applied the SP349xE holds the driver enable and receiver enable inactive for approximately 10 microseconds. During power ramp-up other system IC's may drive unpredictable values. Hot-swap capability prevents the SP349xE from driving any output signal until power has stabilized. After the initial power-up sequence, the hot-swap circuit becomes transparent and driver enable and receiver enable resume their normal functions and timings

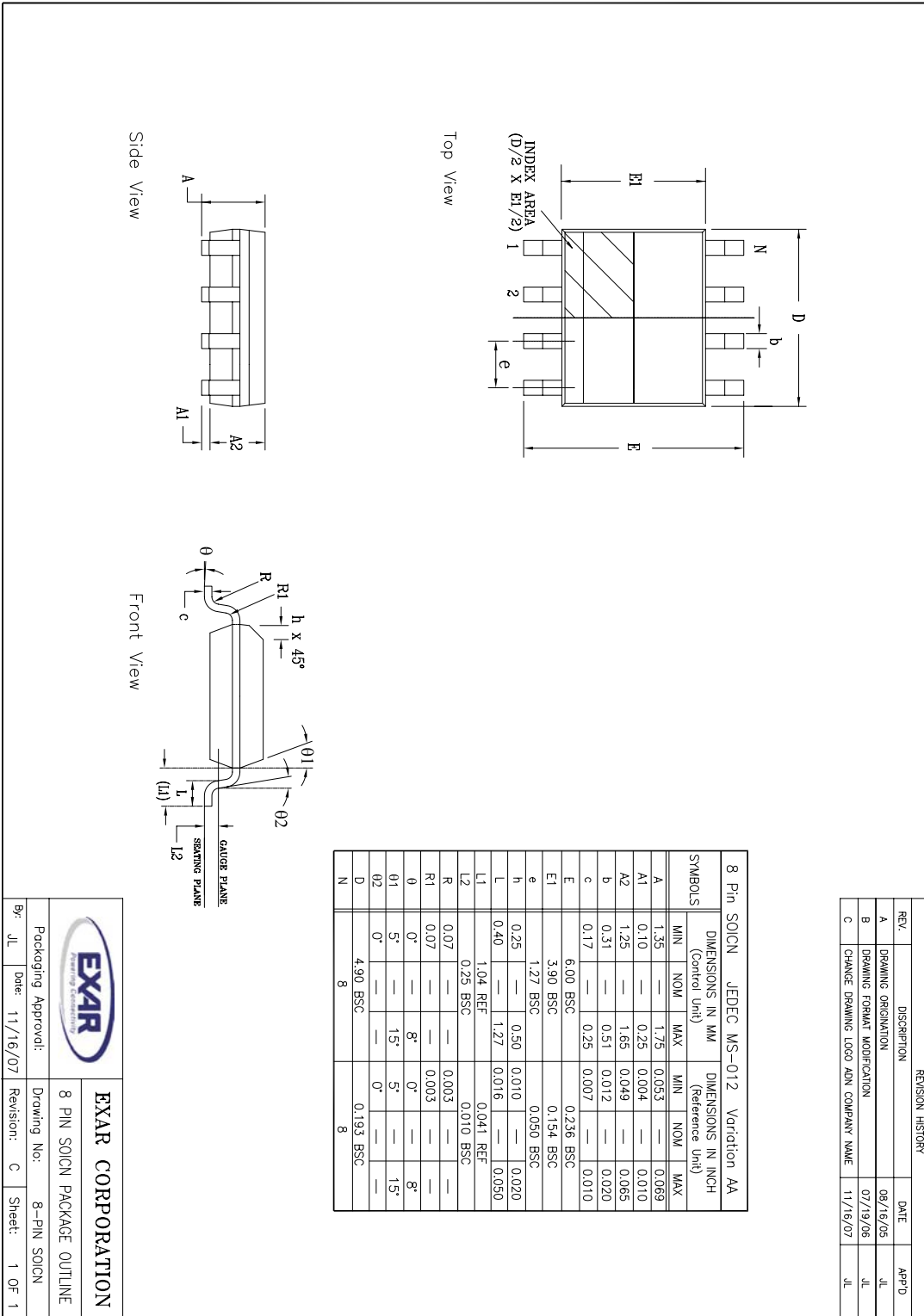
PACKAGE DIMENSIONS (14 PIN NSOIC)



REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	04/17/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

		EXAR CORPORATION	
Packaging Approval:		Drawing No: 14-PIN SOICN	
14 PIN SOICN PACKAGE OUTLINE		14-PIN SOICN	
By: JL	Date: 11/21/07	Revision: B	Sheet: 1 OF 1

PACKAGE DIMENSIONS (8 PIN NSOIC)



REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	08/19/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOCO ADN COMPANY NAME	11/19/07	JL

		EXAR CORPORATION	
		8 PIN SOICN PACKAGE OUTLINE	
Packaging Approval:		Drawing No:	
By: JL	Date: 11/16/07	8-PIN SOICN	
		Revision: C	Sheet: 1 OF 1



REVISION HISTORY

DATE	REVISION	DESCRIPTION
5/01/09	1.0.0	Production Release.

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