PRELIMINARY

MoBL® UniClock CY22M1

Single Output, Low Power Programmable Clock Generator for Portable Applications

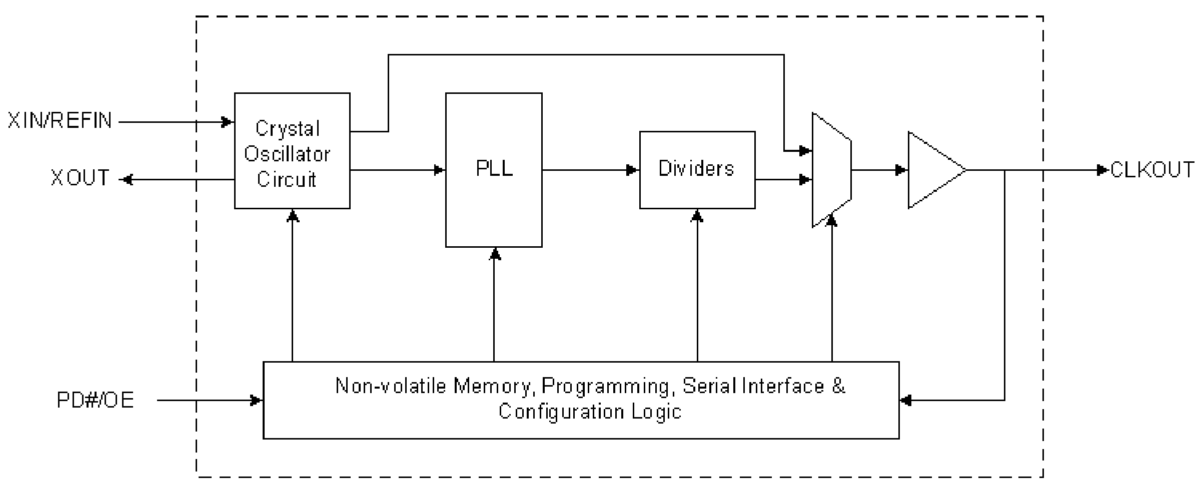
Features

- Small Footprint, 8-Pin QFN 1.7 x 1.7 x 0.6 mm^3 Package
- Low Power and Low Jitter Operation
- Multiple Operating Voltages:
  - CY22M1S: 2.5V, 3.0V, or 3.3V
  - CY22M1L: 1.8V
- Programmable Single Output Clock Generator Frequency Range:
  - 1 to 80 MHz
- Crystal or External Reference Clock Input Frequency Range:
  - Fundamental Tuned Crystal: 8 to 48 MHz
  - External Reference Clock: 1 to 80 MHz
- Programmable Capacitor Tuning Array
- Programmable PD# or OE Control Pin
- Programmable Asynchronous or Synchronous OE and PD# Modes
- Programmable Output Buffer Drive Strength

Benefits

- Services handsets, portable media players, personal navigation devices, digital cameras, digital camcorders, and other portable applications.
- Saves PCB space due to small form factor.
- Enables quick turnaround as well as flexibility and adaptability to design changes through programmability.
- Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM error.
- Enables fine tuning of output clock frequency by adjusting the crystal load C_{Load} using programmable internal capacitors.
- Lowers clock solution cost by pairing a high frequency PLL programmability with a low cost, low frequency crystal.
- Enables low power during the power down or output disable function.
- Provides flexibility for system applications through selectable asynchronous or synchronous output enable and disable.

Logic Block Diagram



Pin Description

Figure 1. Package Pinout Drawing: CY22M1 8-Pin 1.7 x 1.7 mm^2 QFN

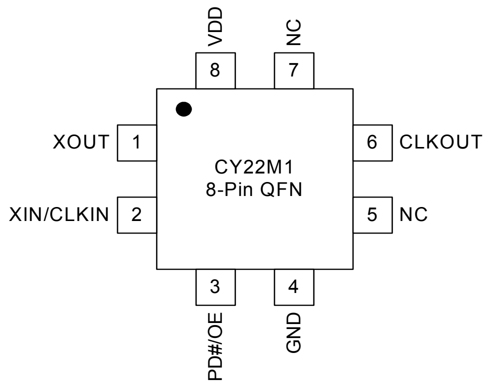


Table 1. Pin Definition: CY22M1 8-Pin 1.7 x 1.7 mm^2 QFN

Pin Number	Name	IO	Description
1	XOUT	Output	Crystal output. Float for external clock input.
2	XIN/CLKIN	Input	Crystal or external clock input.
3	PD#/OE	Input	Multifunction pin. Active low power down or active high output enable pin. Has weak internal pull up.
4	GND	Power	Power supply ground.
5	NC	–	No connect. Pin has no internal connection.
6	CLKOUT	Output	Programmable clock output. Output voltage depends on VDD. Has weak internal pull down.
7	NC	–	No connect. Pin has no internal connection.
8	VDD	Power	Programmable power supply: CY22M1S: 2.5V, 3.0V, 3.3V (standard voltage) CY22M1L: 1.8V (low voltage)

Functional Description

The MoBL® UniClock CY22M1 is a programmable, high accuracy, PLL-based clock generator device designed for low power, space constrained applications. The low jitter and accurate outputs makes this device suitable for handsets, portable media players, personal navigation devices, digital cameras, digital camcorders, and other portable applications.

The device has several programmable options listed in the section Programmable Features on page 4 of this data sheet. The entire configuration is one time programmable.

Configurable PLL

The device uses a programmable PLL to generate output frequencies from 1 to 80 MHz. The high resolution of the PLL and flexible output dividers provide this flexibility.

Input Reference Clock Option

There is an option of a crystal or clock signal for the input reference clock. The frequency range for crystal (XIN) is 8 MHz to 48 MHz, while the range for an external reference clock (CLKIN) is 1 MHz to 80 MHz. A PLL bypass mode enables this device to be used as a crystal oscillator.

Multiple VDD Power Supply Option

The device has programmable power supply options. The operating supply voltages are 2.5V, 3.0V, or 3.3V for CY22M1S and 1.8V for CY22M1L.

Programmable Output Drive Strength

The DC drive strength of the clock output can be programmed to one of two settings, enabling control of output rise and fall times. Table 2 shows the typical rise and fall times for both of the drive strength settings.

Table 2. Output Drive Strength

Output Drive Strength	Rise/Fall Time (ns) (Typical Value)
Low	2.0
High	1.0

Power Management Feature

The MoBL® UniClock CY22M1 offers PD# (active LOW) and OE (active HIGH) functions. When the power down mode is selected (PD# =0), the oscillator and PLL are placed in a low supply current standby mode and the output is tristated and weakly pulled LOW. The oscillator and PLL circuits must relock when the part exits the power down mode. If the output is disabled (OE=0), the output is tristated and weakly pulled LOW. In this mode, the oscillator and PLL circuits continue to operate, which enables a rapid return to normal operation when the output is enabled.

In addition, the PD# or OE mode can be programmed to occur asynchronously or synchronously with respect to the output signal. When the asynchronous setting is used, entering power down or disabling the output occurs immediately (enabling logic delays) regardless of the position in the clock cycle. Similarly, exiting power down or enabling the output occurs immediately with no guarantee of full output clock pulses. However, when the synchronous setting is used, the part waits for a falling edge at the output before entering power down or disabling the output. This prevents output glitches. The first output pulse is guaranteed to be a full clock pulse when enabling outputs with a synchronous OE pin. The first output pulse is not guaranteed to be a full clock when exiting power down in synchronous or asynchronous mode.

Output Frequency Tuning

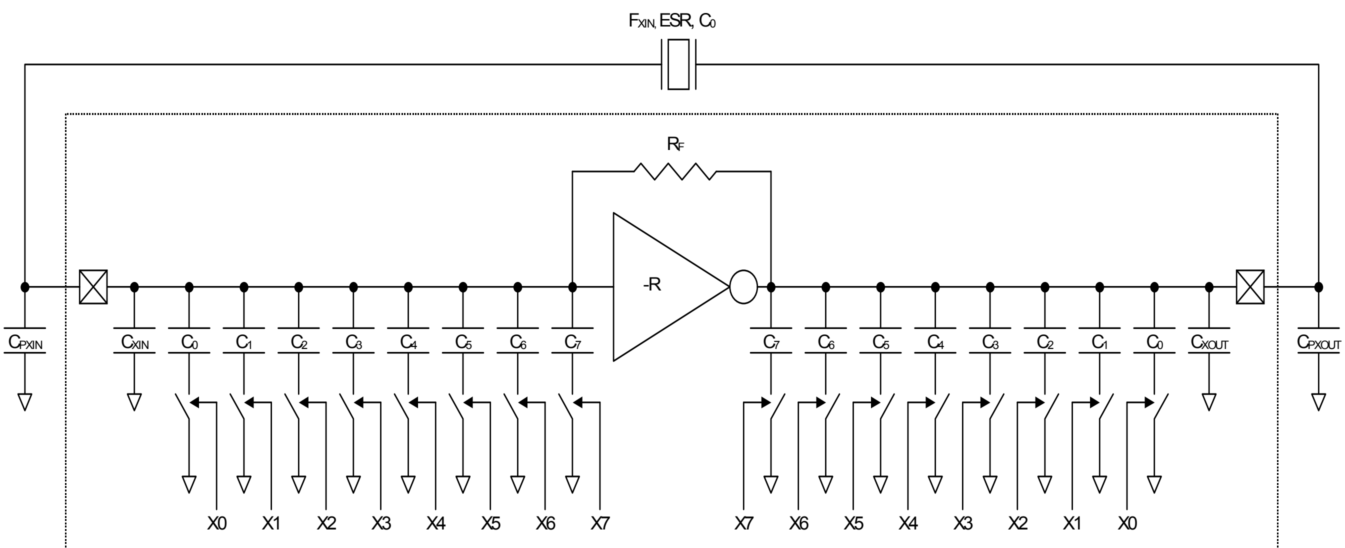
The MoBL® UniClock CY22M1 contains an on-chip oscillator with a built-in programmable capacitor array for fine tuning of the output frequency. The capacitive load seen by the crystal is adjusted by programming the memory bits. This feature can compensate for crystal variations or provide a more accurate synthesized frequency. Figure 2 on page 4 shows the crystal oscillator tuning circuit block diagram.

Crystal Oscillator Tuning Circuit

Table 3. Crystal Oscillator Tuning Capacitor Values

Cap	Value[1]	Unit
C_7	5.000	pF
C_6	2.500	pF
C_5	1.250	pF
C_4	0.625	pF
C_3	0.313	pF
C_2	0.156	pF
C_1	0.078	pF
C_0	0.039	pF

Figure 2. Crystal Oscillator Tuning Block Diagram



Programmable Features

The following list of features can be custom configured:

- PLL frequency and output divider value
- Oscillator tuning (crystal load) capacitance value
- Direct oscillator output (PLL bypass)
- High or low power supply voltage operation
- Power management mode (OE or PD#)
- Power management timing (synchronous or asynchronous)
- Programmable output drive strength

Programming Support

The device is available in factory and field programmable versions. The CyClockMaker Programming kit along with CyClockDesigner configuration software is used for field programming the device. For specific programming needs, contact your local Cypress field application engineer (FAE) or sales representative.

Note
1. The capacitor values are nominal.

Absolute Maximum Ratings

Parameter[2]	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage, 2.5V/3.0V/3.3V range		–0.5	4.4	V
	Supply voltage, 1.8V range		–0.5	2.8	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
T_S	Temperature, storage	Non functional	–55	+125	°C
T_J	Temperature, junction	Non functional	–40	+125	°C
ESD_{HBM}	ESD protection (human body model)	JEDEC EIA/JESD22-A114-E	2000	–	Volts
D_{RET}	Data retention at T_J = 125°C		10	–	Yr.
PR_{CYCLE}	Maximum programming cycle		1		
UL-94	Flammability rating		V-0 at 1/8 in.		
MSL	Moisture sensitivity level		3		

Recommended Operating Conditions

Parameter[2]	Description	Min	Typ	Max	Unit
V_{DD}	Supply voltage, 1.8V operating range for CY22M1L	1.6	–	2.0	V
	Supply voltage, 2.5V operating range for CY22M1S	2.2	–	2.8	V
	Supply voltage, 3.0V operating range for CY22M1S	2.7	–	3.3	V
	Supply voltage, 3.3V operating range for CY22M1S	3.0	–	3.6	V
T_{AC}	Commercial ambient temperature	0	–	70	°C
T_{AI}	Industrial ambient temperature	-40	–	85	°C
T_{PU}	Power up time for V_{DD} to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms
T_{PD}	Minimum pulse width of PD#/OE input	100	–	–	ns
C_{OUT}	Output load capacitance	–	–	15	pF

Note

2. Stresses beyond those listed underAbsolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to Absolute-Maximum-Rated Conditions for extended periods may affect device reliability or cause permanent device damage.

DC Electrical Specifications

Parameter[3]	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL1}	Input low voltage of PD#/OE		–	–	0.2^*V_{DD}	V
V_{IH1}	Input high voltage of PD#/OE		0.8^*V_{DD}	–	–	V
V_{IL2}	Input low voltage of REFIN	CY22M1S	-0.2	–	0.4	V
		CY22M1L	-0.2	–	0.4	V
V_{IH2}	Input high voltage of REFIN	CY22M1S	1.2	–	2.1	V
		CY22M1L	1.2	–	V_{DD}+0.3[4]	V
V_{OL1}	Output low voltage	I_{OL} = 8 mA, V_{DD} = 3.0/3.3V	–	–	0.4	V
V_{OH1}	Output high voltage	I_{OH} = 8 mA, V_{DD} = 3.0/3.3V	V_{DD}–0.4	–	–	V
V_{OL2}	Output low voltage	I_{OL} = 4 mA, V_{DD} = 1.8/2.5V	–	–	0.1^*V_{DD}	V
V_{OH2}	Output high voltage	I_{OH} = 4 mA, V_{DD} = 1.8/2.5V	0.9^*V_{DD}	–	–	V
I_{IL}	Input low current	Input = V_{SS}	–	<1	10	µA
I_{IH}	Input high current	Input = V_{DD}	–	<1	10	µA
I_{OZL}	Output leakage current	Output = V_{SS}, Tj = 85°C	–	<1	5	µA
I_{OZH}	Output leakage current	Output = V_{DD}	–	–	50	µA
I_{DD}	Power supply current for CY22M1L	F_{OUT} = 12 MHz, no load F_{OUT} = 12 MHz, 15 pF load F_{OUT} = 48 MHz, no load F_{OUT} = 48 MHz, 15 pF load	– – – –	1.0 1.2 1.6 2.8	– – – –	mA mA mA mA
	Power supply current for CY22M1S	F_{OUT} = 12 MHz, no load F_{OUT} = 12 MHz, 15 pF load F_{OUT} = 48 MHz, no load F_{OUT} = 48 MHz, 15 pF load	– – – –	1.5 3.3 2.5 6.5	– – – –	mA mA mA mA
I_{PD}	Power down current	Tj = 85°C	–	25	50	µA
R_{UP}	Input pull up resistors	PD#/OE = low PD#/OE = high	1 100	– –	6 250	MΩ kΩ
R_{DN}	Output pull down resistors		500	–	1500	kΩ
C_{IN}	Input capacitance of PD#/OE pin		–	–	7	pF

Notes

3. Parameters are guaranteed by design and characterization. Not 100% tested in production.
4. V_{IH2} absolute maximum value is 2.1V. For V_{DD} = 1.6V to 1.8V, the maximum V_{IH2} is V_{DD} + 0.3V.

AC Electrical Specifications

Parameter[6]	Description	Test Conditions	Min	Typ	Max	Unit
F_{IN} (Crystal)	Crystal frequency range (XIN)		8	–	48	MHz
F_{IN} (Clock)	Clock frequency range (REFIN)		1	–	80	MHz
F_{CLK}	Output frequency		1	–	80	MHz
T_R	Output rise time	Measured from 20% to 80% V_{DD}, C_{OUT} = 15 pF, drive strength set to high	–	–	1.5	ns
T_F	Output fall time	Measured from 80% to 20% V_{DD}, C_{OUT} = 15 pF, drive strength set to high	–	–	1.5	ns
DC	Output clock duty cycle	Using PLL as a source	45	50	55	%
T_{CCJ}	Cycle-to-cycle jitter of CLKOUT using PLL	80 MHz $\geq F_{OUT} \geq$ 50 MHz F_{OUT} < 50 MHz	– –	150 –	200 1	ps %T_{OUT}[5]
T_P	Period jitter of CLKOUT using PLL	80 MHz $\geq F_{OUT} \geq$ 50 MHz F_{OUT} < 50 MHz	– –	150 –	200 1	ps %T_{OUT}[5]
$T_{PO,CLK}$	Power on time for output clock		–	–	5	ms
$T_{PU,CLK}$	Power up time from power down for output clock		–	–	5	ms
$T_{PD,ASYNC}$	Time from falling edge of PD# to stopped outputs, asynchronous mode		–	–	100	ns
$T_{PD,SYNC}$	Time from falling edge of PD# to stopped outputs, synchronous mode		–	–	1.5T + 100	ns
$T_{OD,ASYNC}$	Time from falling edge of OE to stopped outputs, asynchronous mode		–	–	100	ns
$T_{OD,SYNC}$	Time from falling edge of OE to stopped outputs, synchronous mode		–	–	1.5T + 100	ns
$T_{OE,ASYNC}$	Time from rising edge of OE to running outputs, asynchronous mode		–	–	100	ns

Notes
5. %T_{OUT} is the percentage of the output clock period.
6. Parameters are guaranteed by design and characterization. Not 100% tested in production.

Recommended Crystal Specifications for SMD Package

Parameter	Description	Range 1	Range 2	Range 3	Unit
F_{MIN}	Minimum frequency	8	14	28	MHz
F_{MAX}	Maximum frequency	14	28	48	MHz
R_1	Maximum motional resistance (ESR)	135	50	30	Ω
C_0	Nominal shunt capacitance	4	4	2	pF
C_L	Nominal load capacitance	18	14	12	pF
D_L	Maximum crystal drive level	300	300	300	μW

Switching Waveforms

Figure 3. CLKOUT Rise and Fall Time

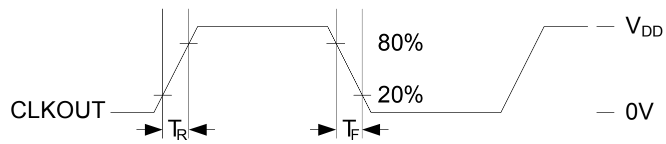


Figure 4. Duty Cycle Timing (DC)

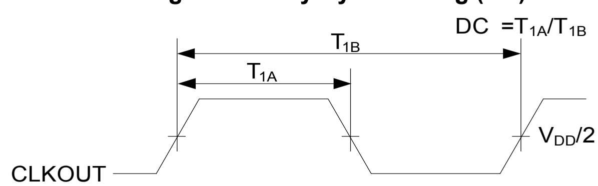


Figure 5. Period Jitter

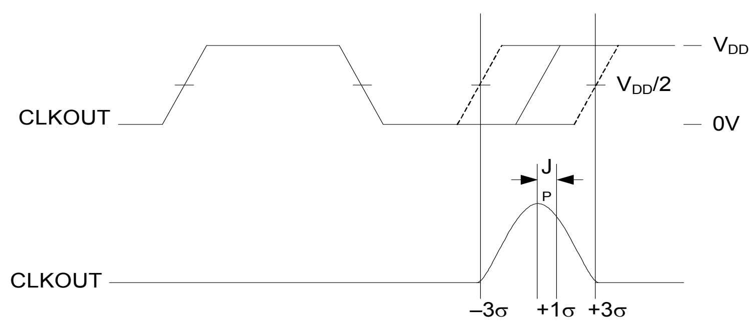


Figure 6. Cycle to Cycle Jitter

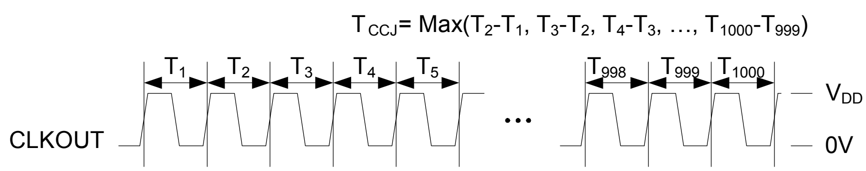


Figure 7. Power On Timing

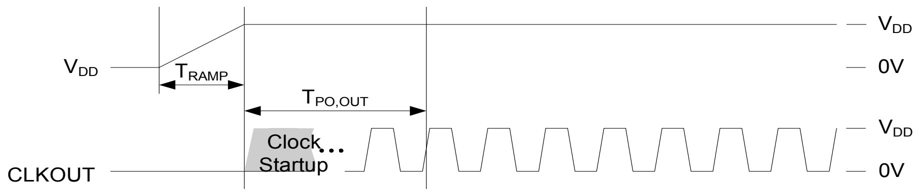


Figure 8. Power Down Timing (Synchronous and Asynchronous Modes) and Power Up Timing

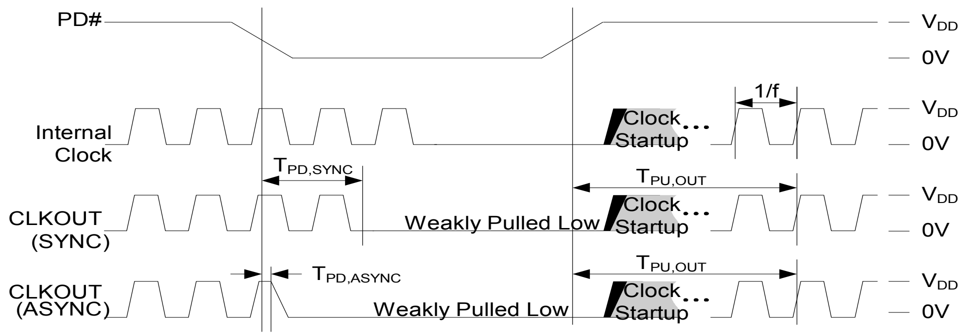
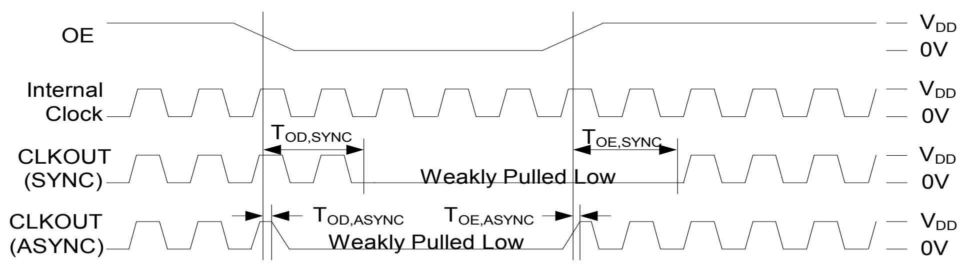


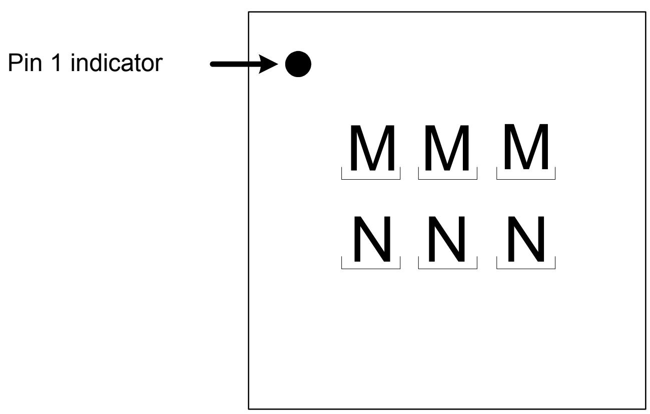
Figure 9. CLKOUT Enable (Synchronous and Asynchronous Modes) and CLKOUT DisableTiming



Ordering Information

Part Number[7],[8]	Type	VDD(V)	Production Flow
Pb-free			
CY22M1SCALGXC-00	8-pin QFN, Field Programmable	Supply voltage: 2.5V, 3.0V, or 3.3V	Commercial, 0°C to 70°C
CY22M1SCALGXC-00T	8-pin QFN, Field Programmable - tape and reel	Supply voltage: 2.5V, 3.0V, or 3.3V	Commercial, 0°C to 70°C
CY22M1LCALGXC-00	8-pin QFN, Field Programmable	Supply voltage: 1.8V	Commercial, 0°C to 70°C
CY22M1LCALGXC-00T	8-pin QFN, Field Programmable - tape and reel	Supply voltage: 1.8V	Commercial, 0°C to 70°C
CY22M1SCALGXI-00	8-pin QFN, Field Programmable	Supply voltage: 2.5V, 3.0V, or 3.3V	Industrial, -40°C to +85°C
CY22M1SCALGXI-00T	8-pin QFN, Field Programmable - tape and reel	Supply voltage: 2.5V, 3.0V, or 3.3V	Industrial, -40°C to +85°C
CY22M1LCALGXI-00	8-pin QFN, Field Programmable	Supply voltage: 1.8V	Industrial, -40°C to +85°C
CY22M1LCALGXI-00T	8-pin QFN, Field Programmable - tape and reel	Supply voltage: 1.8V	Industrial, -40°C to +85°C
CY22M1SCxLGXC-yy	8-pin QFN	Supply voltage: 2.5V, 3.0V, or 3.3V	Commercial, 0°C to 70°C
CY22M1SCxLGXC-yyT	8-pin QFN - tape and reel	Supply voltage: 2.5V, 3.0V, or 3.3V	Commercial, 0°C to 70°C
CY22M1LCxLGXC-yy	8-pin QFN	Supply voltage: 1.8V	Commercial, 0°C to 70°C
CY22M1LCxLGXC-yyT	8-pin QFN - tape and reel	Supply voltage: 1.8V	Commercial, 0°C to 70°C
CY22M1SCxLGXI-yy	8-pin QFN	Supply voltage: 2.5V, 3.0V, or 3.3V	Industrial, -40°C to +85°C
CY22M1SCxLGXI-yyT	8-pin QFN - tape and reel	Supply voltage: 2.5V, 3.0V, or 3.3V	Industrial, -40°C to +85°C
CY22M1LCxLGXI-yy	8-pin QFN	Supply voltage: 1.8V	Industrial, -40°C to +85°C
CY22M1LCxLGXI-yyT	8-pin QFN - tape and reel	Supply voltage: 1.8V	Industrial, -40°C to +85°C

Figure 10. Actual Marking



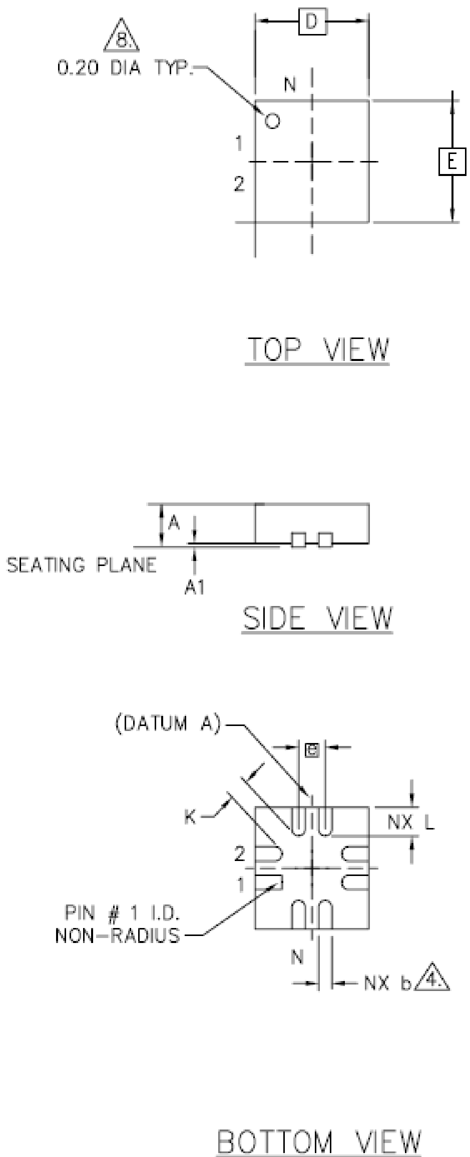
(MMM) = 7th, 8th and 9th characters of marketing part number

(NNN) = Last 3 digits of assembly lot number

Notes
7. x indicates a part marking placeholder to distinguish different configurations for the same customer, beginning alphabetically from “A”.
8. yy indicates “Factory Programmable” and are factory programmed configurations. For more details, contact your local Cypress FAE or Cypress Sales Representative.

Package Drawing and Dimensions

Figure 11. Package Outline Drawing: CY22M1 8-Pin 1.7 x 1.7 x 0.6 mm^3 QFN



NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. (△) DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. (△) PIN #1 ID ON TOP WILL BE LASER MARKED.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.50	0.55	0.60	
A1	0.00	0.02	0.05	
θ	0	——	12	2
K	0.20 MIN.			
D	1.7 BSC			
E	1.7 BSC			
e	0.40 BSC			
N	8			3
ND	2			5
NE	2			5
L	0.35	0.40	0.45	
b	0.15	0.20	0.25	4

001-49591 **

Document History Page

Document Title: MoBL® UniClock CY22M1 Single Output, Low Power Programmable Clock Generator for Portable Applications Document Number: 001-49075				
Rev	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2571065	DPF/CXQ/AESA	09/23/08	New Data Sheet
*A	2636981	CXQ/PYRS	01/15/09	Changed max output frequency to 80 MHz Changed min input reference frequency to 1 MHz Changed max input reference frequency to 80 MHz Changed Idd max conditions and specs Updated VIH/VIL specs for REFIN Added typical I_{PD} value of 25uA Added period jitter spec Removed maximum frequency from Output Drive Strength table Updated part numbers in Ordering Information Replaced CyberClocksOnline and CY3672 programmer kit reference with CyClockMaker and CyClockDesigner reference Added marking format information Updated package drawing to spec 001-49591
*B	2673516	CXQ/PYRS	03/13/09	Changed from Advanced to Preliminary datasheet Deleted “1.8V” when referring to external reference Updated V_{IH2} maximum for CY22M1L and added note 4 Added IDD values to DC Electrical Specifications table
*C	2756169	TSAI	08/20/2009	Post to external web

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