512K x 8 SRAM

Ultra Low Power SRAM

AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-95613[1,2]
- MIL STD-883[1]

FEATURES

- Ultra Low Power with 2V Data Retention (0.2mW MAX worst case Power-down standby)
- Fully Static, No Clocks
- Single +5V ±10% power supply
- Easy memory expansion with CE\ and OE\ options
- All inputs and outputs are TTL-compatible
- Three state outputs
- Operating temperature range:
  Ceramic -55°C to +125°C & -40°C to +85°C
  Plastic -40°C to +85°C[3]

1. Not applicable to plastic package
2. Applies to CW package only.
3. Contact factory for -55°C to +125°C

OPTIONS MARKING

- **Timing**

55ns access	-55[4]
70ns access	-70
85ns access	-85
100ns access	-100

- **Packages**

Ceramic Dip (600 mil)	CW	No. 112
Ceramic SOJ[5]	ECJ	No. 502
Plastic TSOP	DG	No. 1002

- **Options**
  2V data retention/very low power L

4. For DG package, contact factory
5. Contact Factory
NOTE: *Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.*

Pin Name	Function
WE\	Write Enable Input
CE\	Chip Select Input
OE\	Output Enable Input
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

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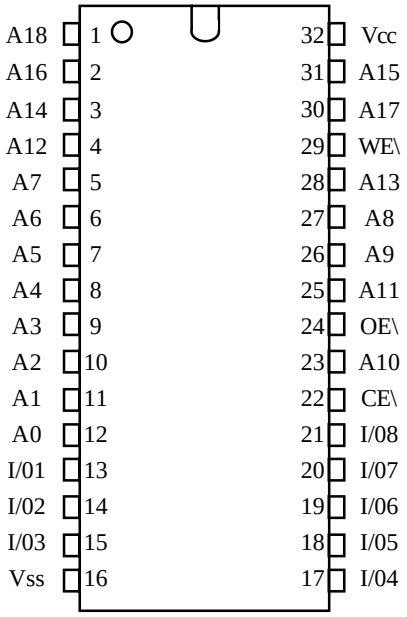
PIN ASSIGNMENT

(Top View)

32-Pin DIP, 32-Pin SOJ & 32-Pin TSOP



GENERAL DESCRIPTION

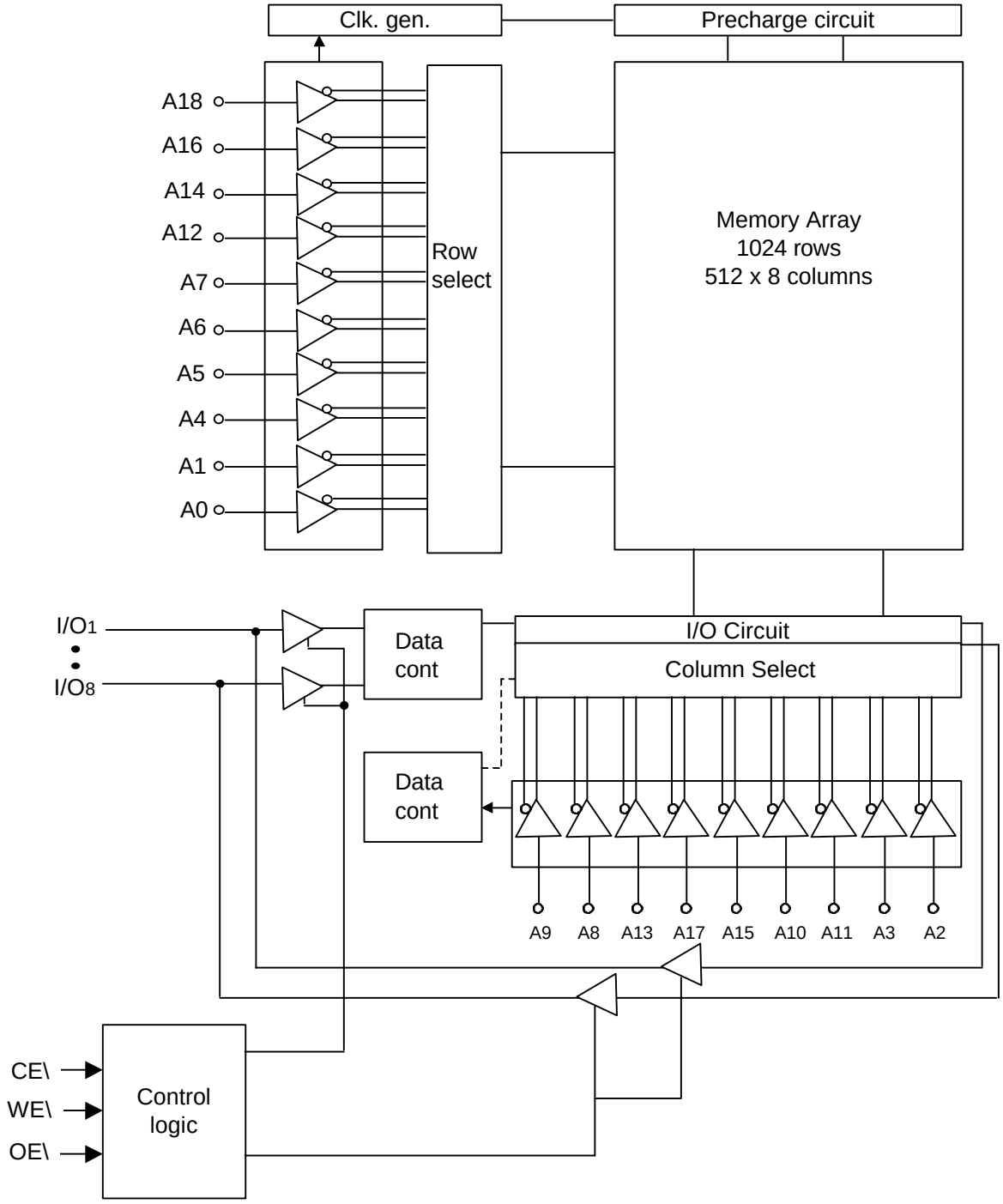
The AS5C4009 is organized as 524,288 x 8 SRAM utilizing a special ultra low power design process. ASI's pinout adheres to the JEDEC standard for pinout on 4 megabit SRAMs. The evolutionary 32 pin version allows for easy upgrades from the 1 meg SRAM design.

For flexibility in memory applications, ASI offers chip enable (CE\) and output enable (OE\) capabilities. These features can place the outputs in High-Z for additional flexibility in system design.

This devices operates from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ and OE\ go LOW. The device offers a reduced power standby mode when disabled, by lowering VCC to 2V and maintaining CE\ = 2V. This allows system designers to meet ultra low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss.....-.5V to +7.0V
Voltage on any pin Relative to Vss.....-.5V to +7.0V
Storage Temperature .....-65°C to +150°C
Operating Temperature Range.....-55°C to +125°C
Soldering Temperature Range.....260°C
Maximum Junction Temperature**.....+150°C
Power Dissipation.....1.0W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^{o}C \leq T_A \leq 125^{o}C$; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input Leakage Current (V_{IN} = V_{SS} to V_{CC})	I_{LI}	-5	5	µA	
Output Leakage Current ($CE\backslash=V_{IH}$ or $OE\backslash=V_{IH}$ or $WE\backslash=V_{IL}$, $V_{IO}=V_{SS}$ to V_{CC})	I_{LO}	-5	5	µA	
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}	--	0.4	V	15
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	--	V	15
Supply Voltage	V_{CC}	4.5	5.5	V	15
Input High (Logic 1) Voltage	V_{IH}	2.2	Vcc +0.5	V	1, 15
Input Low (Logic 0) Voltage	V_{IL}	-0.5	0.8	V	2, 15

				MAX					
PARAMETER		CONDITIONS	SYM	-55	-70	-85	-100	UNITS	NOTES
Power Supply Current: Operating		Cycle Time = Min., 100% Duty Cycle, I_{IO} = 0mA, $CE\backslash = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL}	I_{cc1}	100	90	80	70	mA	3
Power Supply Current: Standby	TTL	$CE\backslash = V_{IH}$, Other inputs = V_{IL} or V_{IH}	I_{SB}	6	6	6	6	mA	
	CMOS	$CE\backslash$ = Vcc -0.2V, Other inputs = 0 ~ Vcc	I_{SB1}	0.75	0.75	0.75	0.75	mA	

CAPACITANCE

PARAMETER	CONDITIONS		SYMBOL	MAXIMUM	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1MHz V_{CC} = 5V	V_{IN}=0V	C_{IN}	8	pF	4
Input/Output Capactiance		V_{IO}=0V	C_{IO}	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION		-55		-70		-85		-100			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle Time	t_{RC}	55		70		85		100		ns	
Address access time	t_{AA}		55		70		85		100	ns	
Chip Enable access time	t_{ACE}		55		70		85		100	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
Chip Enable to output in Low-Z	t_{LZCE}	10		10		10		10		ns	4,6
Chip disable to output in High-Z	t_{HZCE}		20		25		30		30	ns	4,6
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		55		70		85		100	ns	4
Output Enable access time	t_{AOE}		30		35		40		45	ns	
Output Enable to output in Low-Z	t_{LZOE}	5		5		5		5		ns	4,6
Output disable to output in High-Z	t_{HZOE}		20		25		30		30	ns	4,6
WRITE Cycle											
WRITE cycle time	t_{WC}	55		70		85		100		ns	
Chip Enable to end of write	t_{CW}	50		60		70		80		ns	
Address valid to end of write	t_{AW}	50		60		70		80		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP1}	50		60		70		80		ns	
Data setup time	t_{DS}	30		30		35		40		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	5		5		5		5		ns	4,6
Write Enable to output in High-Z	t_{HZWE}		25		25		30		30	ns	4,6

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1

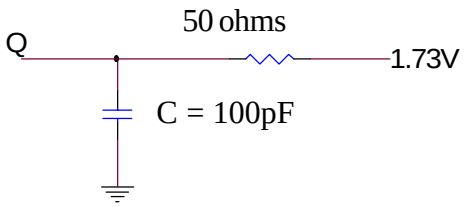


Fig. 1 Output Load Equivalent

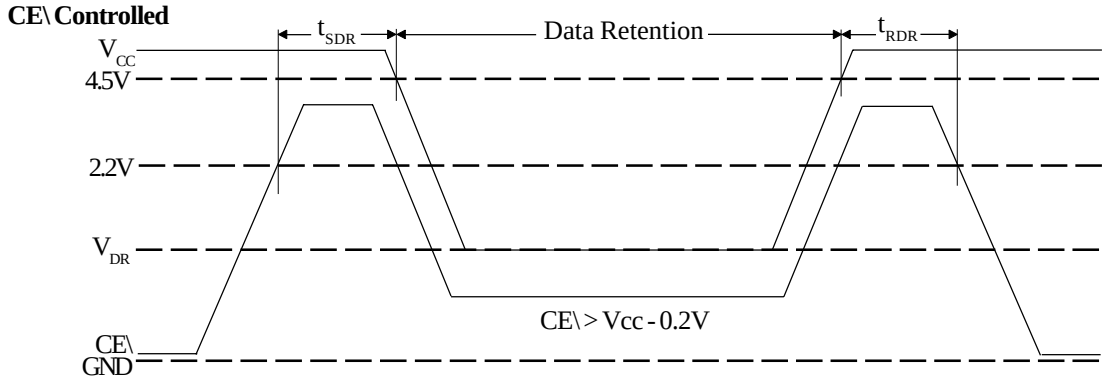
NOTES

1. Overshoot: Vcc +3.0V for pulse width < 20ms.
2. Undershoot: -3V for pulse width < 20ms.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
7. WE\ is HIGH for READ cycle.
8. Device is continuously selected. Chip enables and output enables are held in their active state.
9. Address valid prior to, or coincident with, latest occurring chip enable.
10. ^{t}RC = Read Cycle Time.
11. Chip enable and write enable can initiate and terminate a WRITE cycle.
12. Output enable (OE\) is inactive (HIGH).
13. Output enable (OE\) is active (LOW).
14. ASI does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.
15. All voltage referenced to Vss (GND).

DATA RETENTION ELECTRICAL CHARACTERISTICS

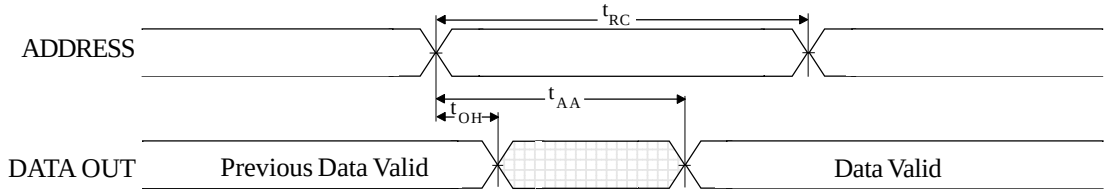
DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		V	
Data Retention Current	CE\ > (V_{CC} - 0.2V)	V_{CC} = 2V	I_{CCDR}		100	µA	
	V_{IN} > (V_{CC} - 0.2V)	V_{CC} = 3V	I_{CCDR}		200	µA	
Chip Deselect to Data Retention Time			t_{CDR}	0		ns	4
Operation Recovery Time			t_R	5		ms	4, 10

LOW V_{CC} DATA RETENTION WAVEFORM



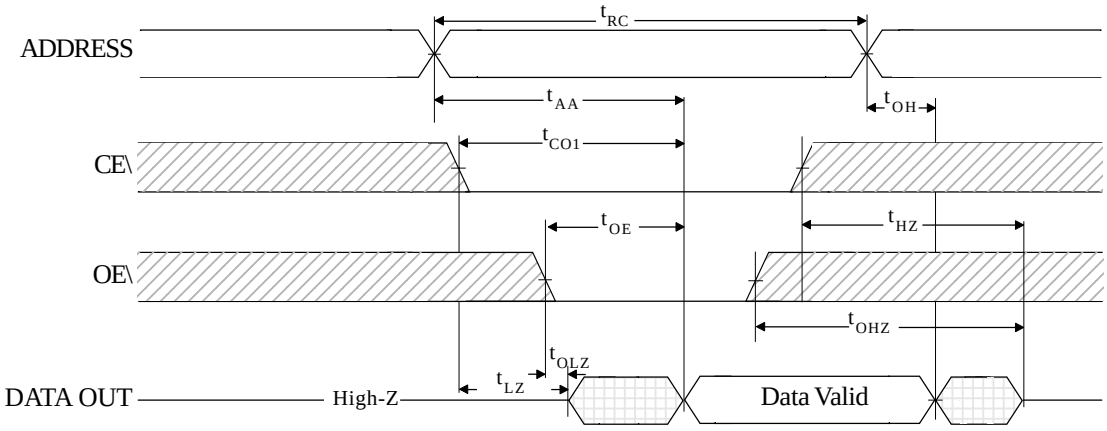
READ CYCLE NO. 1 [1]

(Address Controlled, CE\ = OE\ = V_{IL}, WE\ = V_{IH})



READ CYCLE NO. 2 [2]

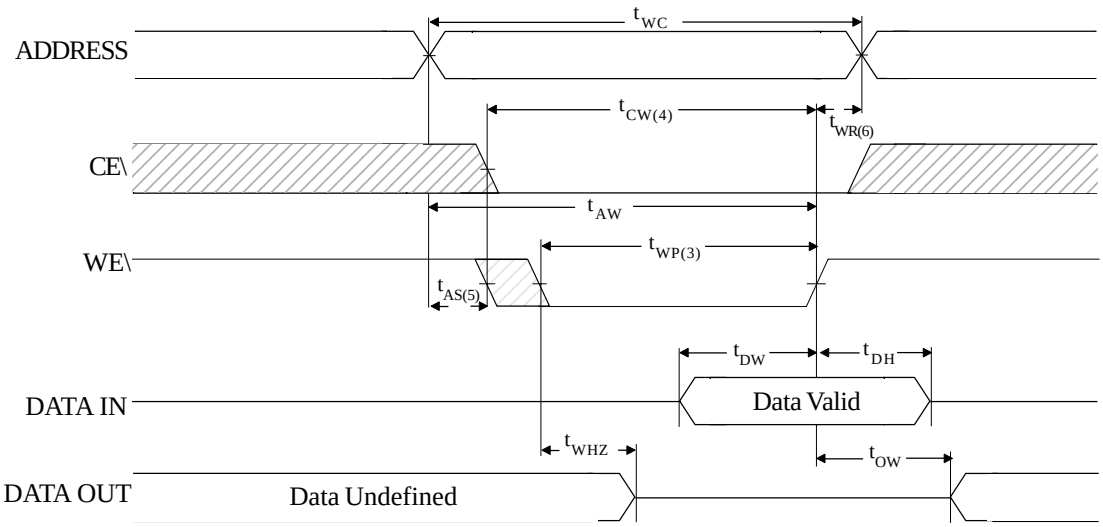
(WE\ = V_{IH})



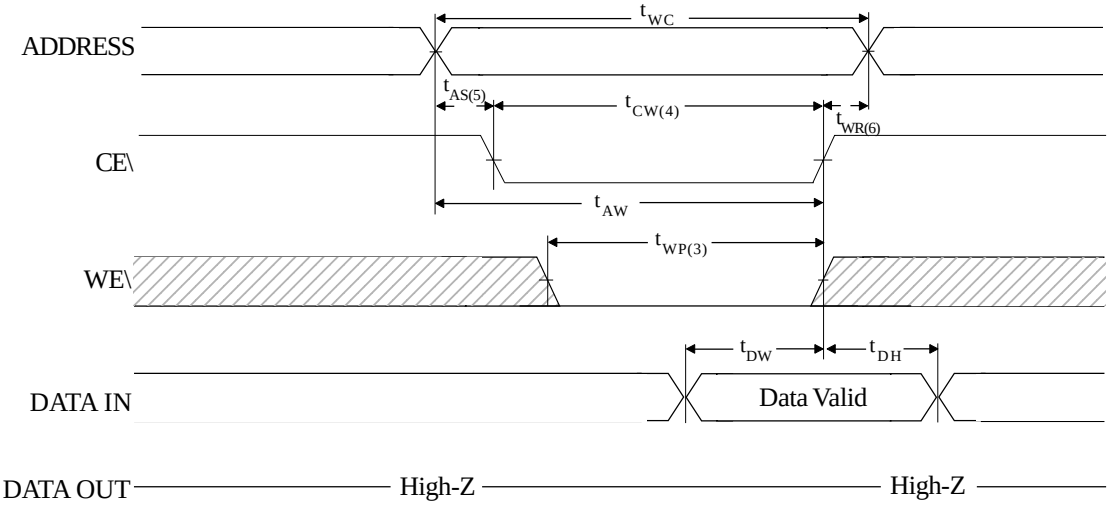
Don't Care

Undefined

WRITE CYCLE NO. 1
(WE Controlled)



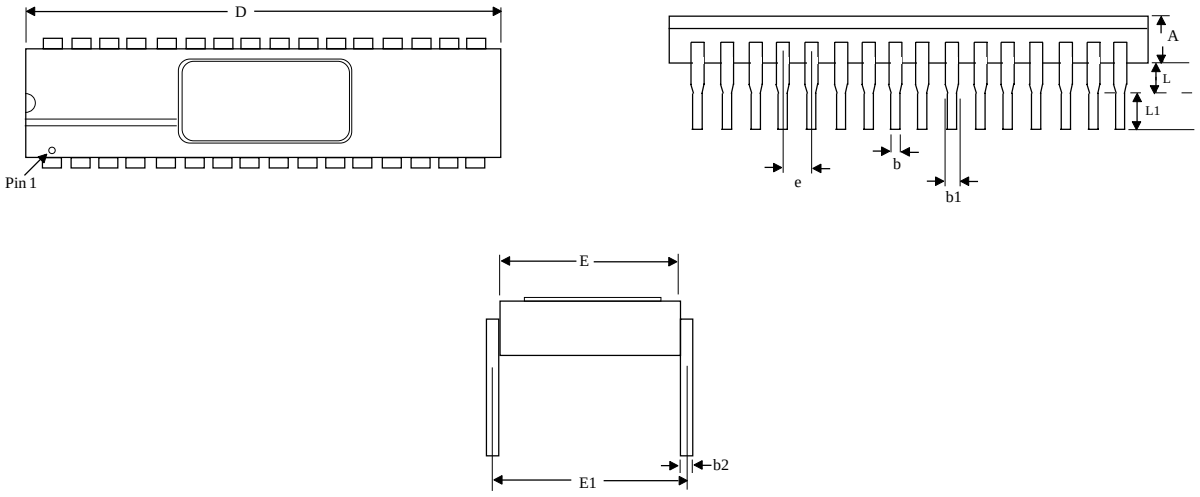
WRITE CYCLE NO. 2
(Write Enabled Controlled)



NOTES:
1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature adn voltage condition, tHZ (MAX) is less than tLZ (MIN) both for a given device and from device to device interconnection.
3. A write occurs during the overlap of a low CE\ adn a low WE\. A write begins at the latest transistion among CE\ going Low and WE\ going Low: A write end at the earliest transistion among CE\ going High and WE\ going High, tWP is measured from the beginning of write to the end of write.
4. tCW is measured from the CE\ going Low to end of write.
5. tAS is measured from the address valid to the beginning of write.
6. tWR is measure from the end of write to the address change. tWR applied in case a write ends are CE\ or WE\ going High.

MECHANICAL DEFINITION*

ASI Case #112 (Package Designator CW)

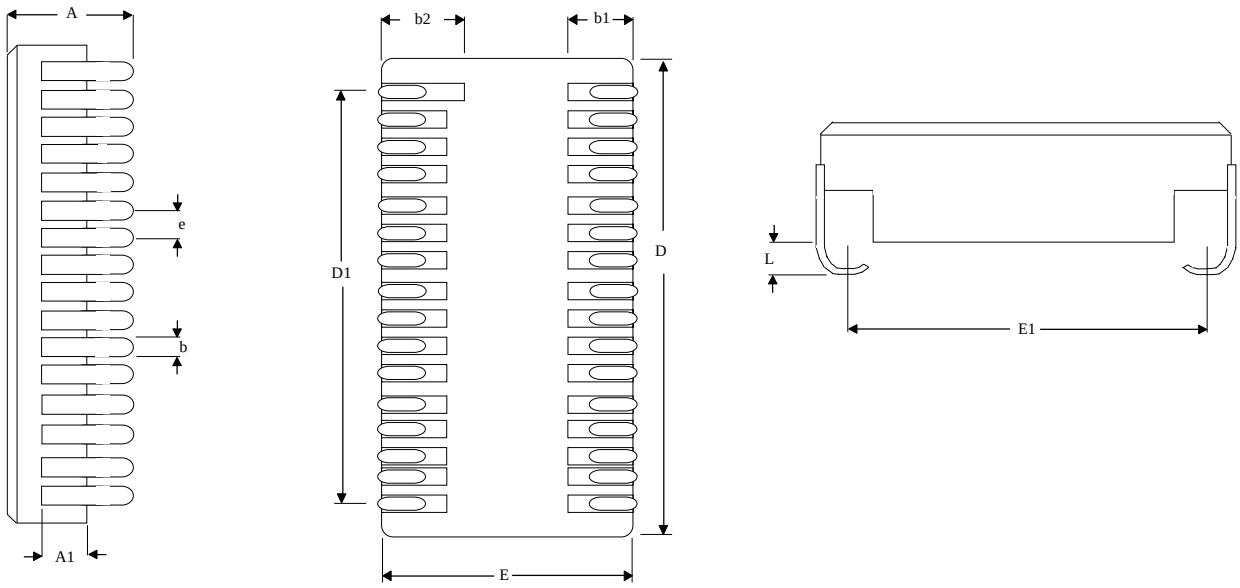


SYMBOL	ASI PACKAGE	
	MIN	MAX
A	0.089	0.111
b	0.016	0.020
b1	0.045	0.055
b2	0.008	0.012
D	1.585	1.615
E	0.585	0.605
E1	0.590	0.610
e	0.090	0.110
L	0.040	0.060
L1	0.125	0.175

All measurements are in inches.

MECHANICAL DEFINITION*

ASI Case #502 (Package Designator ECJ)

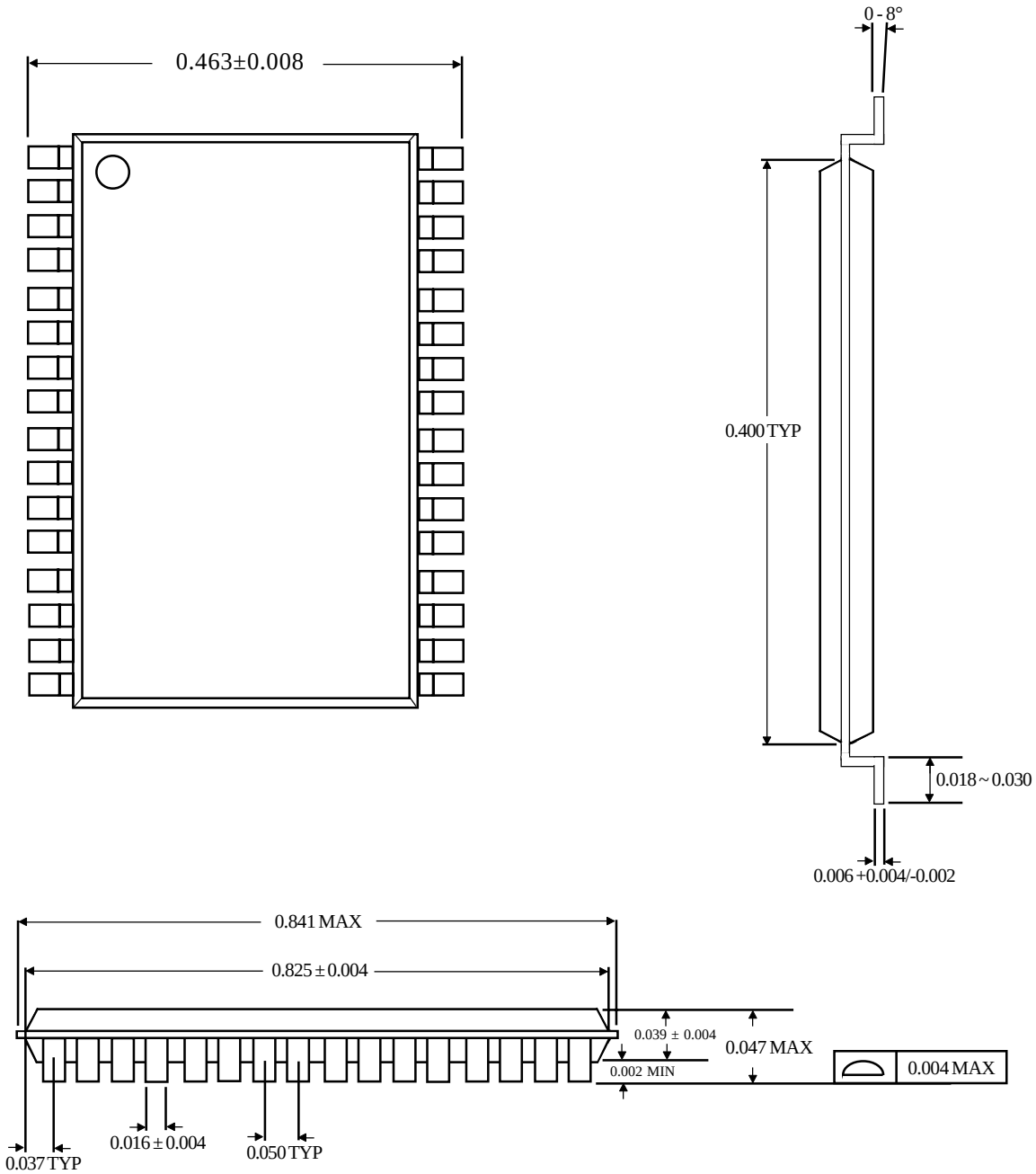


SYMBOL	ASI PACKAGE	
	MIN	MAX
A	0.140	0.160
A1	0.054	0.066
b	0.022	0.028
b1	0.100 TYP	
b2	0.115	0.135
D	0.815	0.835
D1	0.740	0.760
E	0.445	0.460
E1	0.395	0.410
e	0.045	0.055
L	0.057	0.063

All measurements are in inches.

MECHANICAL DEFINITION*

ASI Case #1002 (Package Designator DG)



All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS5C4009CW-55L/XT[1]

Device Number	Package Type	Speed ns	Options**	Process
AS5C4009	CW	-55	L	/*
AS5C4009	CW	-70	L	/*
AS5C4009	CW	-85	L	/*
AS5C4009	CW	-100	L	/*

EXAMPLE: AS5C4009ECJ-85L/883C[1]

Device Number	Package Type	Speed ns	Options**	Process
AS5C4009	ECJ	-55	L	/*
AS5C4009	ECJ	-70	L	/*
AS5C4009	ECJ	-85	L	/*
AS5C4009	ECJ	-100	L	/*

EXAMPLE: AS5C4009DG-70/IT[2]

Device Number	Package Type	Speed ns	Options**	Process
AS5C4009	DG	-55	L	/*
AS5C4009	DG	-70	L	/*
AS5C4009	DG	-85	L	/*
AS5C4009	DG	-100	L	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

** OPTIONS

L = 2V Data Retention/Ultra Low Power

NOTES:

1. All CSOJ devices, please consult factory. Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.
2. Plastic devices not available as 883. For XT or 55ns devices, contact factory.

ASI TO DSCC PART NUMBER CROSS REFERENCE FOR 5962-95613

Package Designator CW

ASI Part #	SMD Part
AS5C4009CW-120/H	5962-9561301HYA
AS5C4009CW-120L/H	5962-9561315HYA
AS5C4009CW-100/H	5962-9561302HYA
AS5C4009CW-100L/H	5962-9561316HYA
AS5C4009CW-85/H	5962-9561303HYA
AS5C4009CW-85L/H	5962-9561317HYA
AS5C4009CW-70/H	5962-9561304HYA
AS5C4009CW-70L/H	5962-9561318HYA
AS5C4009CW-120/H	5962-9561301HYC
AS5C4009CW-120L/H	5962-9561315HYC
AS5C4009CW-100/H	5962-9561302HYC
AS5C4009CW-100L/H	5962-9561316HYC
AS5C4009CW-85/H	5962-9561303HYC
AS5C4009CW-85L/H	5962-9561317HYC
AS5C4009CW-70/H	5962-9561304HYC
AS5C4009CW-70L/H	5962-9561318HYC

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*