TECHNICAL DATA SHEET

INT5130

Integrated Powerline MAC/PHY Transceiver

Intellon
No New Wires™

Features

- **Single-chip powerline networking controller with IEEE802.3u MII interface**
- **Implements Intellon's PowerPacket™ technology which is fully compliant with the *HomePlug Powerline Alliance Industry Specification v1.0***
- **General purpose 8-wire serial PHY data interface**
- **Selectable MDI/SPI PHY management interface**
- **Up to 14 Mbps data rate on the powerline**
- **Orthogonal Frequency Division Multiplexing (OFDM) with patented signal processing techniques for high data reliability in noisy media conditions**
- **Intelligent channel adaptation maximizes throughput under harsh channel conditions**
- **Integrated quality-of-service (QoS) features such as prioritized random access, contention-free access, and segment bursting**
- **56-bit DES Link Encryption with key management for secure powerline communications**
- **E^{2}PROM interface for fast access to configuration parameters allows system designs to leverage standard Ethernet drivers**
- **IEEE 1149.1 JTAG Test Access Port**
- **3.3 V signaling, 5 V tolerant interface**
- **Support for three status LEDs**
- **144-pin LQFP package**

Applications

- **Shared broadband Internet access using standard in-home powerlines**
- **Internet Appliances**
- **PC file and application sharing**
- **Peripheral and printer sharing**
- **Networked gaming**

General Description

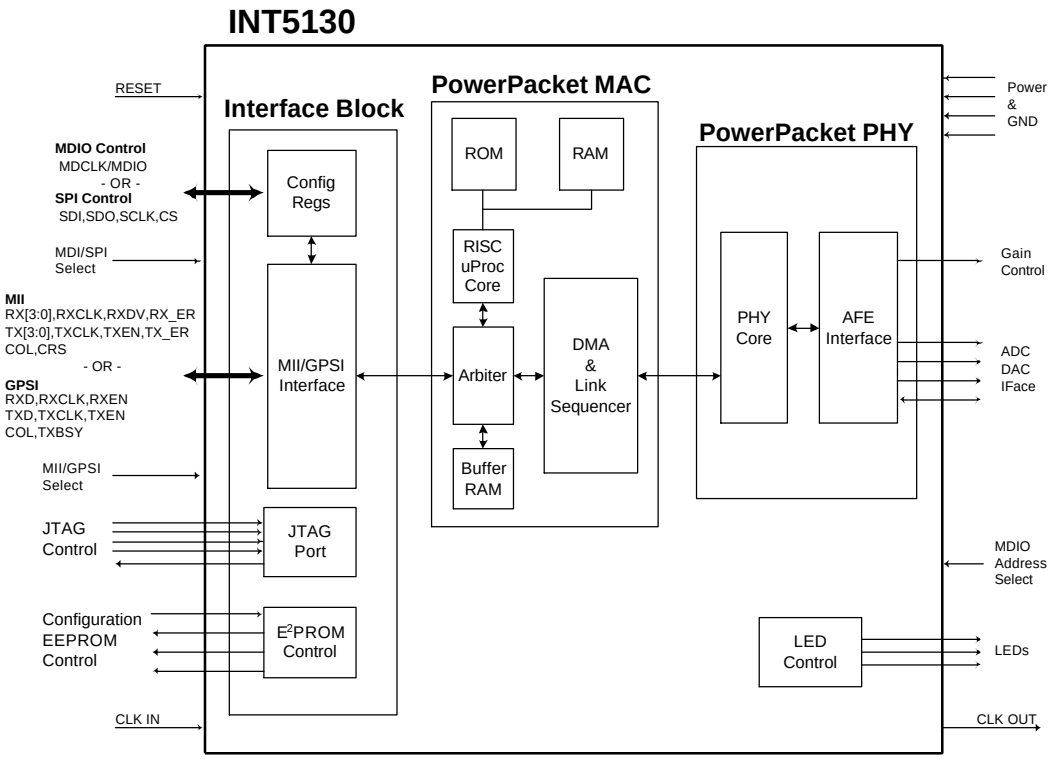
The INT5130 IC is an integrated powerline MAC/PHY transceiver providing *No New Wires™* communications to any room, over any wire, at speeds of up to 14 Mbps. The INT5130 provides the ability to select between a complete Media Independent Interface (MII) or a reduced General Purpose Serial Interface (GPSI) for interconnection to the external MAC controller. The INT5130 also provides the option of selecting between a Management Data Interface (MDI) or a simple Serial Peripheral Interface (SPI) for handling the management and control of the MII/GPSI interface.

The INT5130 implements Intellon's patented PowerPacket OFDM technology and is fully compliant with the *HomePlug Powerline Alliance Industry Specification v1.0*. Specifically tailored to reliably deliver up to 14 Mbps over the difficult powerline communication environment, the INT5130 combats deep attenuation notches, noises sources, and multi-path fading by allocating usable frequencies according to the signal to noise ratio (SNR). Synchronization is achieved in low SNR channels without the use of pilot carriers. The MAC implements a CSMA/CA scheme with prioritization and automatic repeat request (ARQ) for reliable delivery of Ethernet packets via packet encapsulation. Built-in quality-of-service (QoS) features provide the necessary bandwidth for multimedia payloads including voice, data, audio, and video. Prioritized random access along with segment bursting minimizes the demands on the receiver resources and maximizes the throughput of the network while still providing excellent latency response and jitter performance. The INT5130's contention-free access capability extends this concept of segment bursting to allow the transmission of multiple frames over the powerline without relinquishing the control of the medium. Utilizing contention-free access, a single station may act as a controller for the entire network.

System designers have the option of embedding PowerPacket-specific control information within the packet stream for optimal control and performance or may choose to provide this information via the separate E^2PROM interface. Providing this configuration and control information through a separate E^2PROM interface allows the system designer to leverage standard Ethernet drivers.

The INT5130 operates on both 2.5V and 3.3V supplies, offers 5V I/O tolerance, and is packaged in a 144-pin LQFP. Intellon offers a complete solution for powerline communication applications by providing the INT5130 in conjunction with the INT1000 Analog Conversion IC.

Functional Block Diagram



Contents

Pin I/O

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VDD_C	37	VDD_C	73	VDD_C	109	VDD_C
2	VDD_C	38	VDD_C	74	DAC_CLK	110	VDD_IO
3	VDD_IO	39	VDD_IO	75	VSS_C	111	TEST1
4	MII_TX3	40	MII_COL/ GPSI_COL	76	TX_EN	112	TEST2
5	VSS_C	41	VSS_C	77	RX_EN	113	VSS_C
6	MII_TX2	42	MII_CRS/ GPSI_RXEN	78	VDD_C	114	TCK
7	VDD_C	43	VDD_C	79	VDD_IO	115	VDD_C
8	MII_TX1	44	RESET_N	80	ADIO0	116	TDO
9	VSS_IO	45	VSS_IO	81	ADIO1	117	VSS_C
10	VSS_C	46	VSS_C	82	ADIO2	118	VSS_C
11	MII_TX0/ GPSI_TXD	47	VSS_C	83	VSS_IO	119	VSS_C
12	MII_TXEN/ GPSI_TXEN	48	CLKOUT	84	ADIO3	120	TDI
13	VDD_C	49	CLKIN	85	VSS_C	121	VDD_C
14	MII_TXCLK/ GPSI_TXCLK	50	VDD_C	86	ADIO4	122	VDD_C
15	VDD_Q	51	VDD_Q	87	ADIO5	123	VDD_C
16	MII_TX_ER	52	SPI_CS	88	VSS_C	124	TMS
17	VDD_C	53	VDD_C	89	VSS_Q	125	VDD_C
18	MII_RX_ER/ GPSI_RXD	54	SPI_CLK	90	ADIO6	126	MDI_SPIS_N
19	VSS_C	55	VSS_C	91	VDD_Q	127	VSS_C
20	VSS_C	56	VSS_C	92	ADIO7	128	VSS_C
21	VSS_Q	57	SPI_DI	93	ADIO8	129	TRST_N
22	MII_RXCLK/ GPSI_RXCLK	58	VSS_C	94	ADIO9	130	VSS_Q
23	VDD_C	59	SPI_DO	95	VDD_IO	131	NC
24	VDD_C	60	VDD_C	96	AGC0	132	VDD_C
25	MII_RXDV/GPSI_ TXBSY	61	LED0_N	97	AGC1	133	MII_MDCLK/ SPIS_SCLK
26	VSS_C	62	VSS_C	98	AGC2	134	VSS_C
27	MII_RX3	63	LED1_N	99	VDD_C	135	MII_MDIO/ SPIS_SDO
28	VDD_C	64	VDD_IO	100	AGC3	136	VDD_IO
29	MII_RX2	65	LED2_N	101	VSS_C	137	MDI_ADRSEL[1]/SPIS _SDI
30	VSS_C	66	VSS_C	102	AGC4	138	VSS_C
31	MII_RX1	67	ADC_CAL	103	AGC5	139	MDI_ADRSEL[0]/SPIS _CS_N
32	VDD_C	68	VDD_C	104	VDD_C	140	VDD_C
33	MII_RX0	69	AGCENC_N	105	AGC6	141	MII_GPSI_N
34	VSS_C	70	VSS_IO	106	AGC7	142	VSS_IO
35	VSS_IO	71	ADC_CLK	107	VSS_IO	143	VSS_C
36	VSS_C	72	VSS_C	108	VSS_C	144	VSS_C

Table 1: Pin I/O

Pin Descriptions by Group

Signal Name	I/O Pad Description	Signal Description
Media Independent Interface (MII) These pins are multiplexed with the GPSI pins and are selected when MII_GSPI_N signal is at VDD.		
MII_RX[3:0]	Output	*MII Receive Data.* Data is transferred from the INT5130 to the external MAC across these four lines one nibble at a time.
MII_RXCLK	Output	*MII Receive Clock* The receive clock outputs a continuous 25MHz clock to the external MAC.
MII_RXDV	Output	*MII Receive Data Valid* This signal indicates that the incoming data on the MII_RX[3:0] pins are valid.
MII_RX_ER	Output	*MII Receive Error* This signal indicates to the external MAC that an error has occurred during the frame reception.
MII_TX[3:0]	Input	*MII Transmit Data* Data is transferred to the INT5130 from the external MAC across these four lines one nibble at a time.
MII_TXCLK	Output	*MII Transmit Clock* The transmit clock outputs a continuous 25MHz clock to the external MAC.
MII_TXEN	Input	*MII Transmit Enable* This signal indicates to the INT5130 that valid data is present on the MII_TX[3:0] pins.
MII_TX_ER	Input	*MII Transmit Error* MII_TX_ER is activated by the external host controller when an error condition is detected during packet transmission. The INT5130 will ignore any MII transmission within which MII_TX_ER is asserted. MII_TX_ER is ignored if MII_TXEN is not asserted.
MII_CRS	Output	*MII Carrier Sense* This signal indicates to the external host that traffic is present on the powerline and the host should wait until the signal goes invalid before sending additional data. This signal is an asynchronous output signal.
MII_COL	Output	*MII Collision Detect* This signal indicates to the external host that a collision has occurred on the MII interface. This signal is an asynchronous output signal.
MII Management Data Interface (MDI) These pins are multiplexed with the SPIS_SDO and SPIS_SCLK signals and are selected when MDI_SPIS_N is at VDD.		
MII_MDIO	Input/Output	*MII Management Data Input/Output* This bi-directional signal carries the data for the Management Data Interface.
MII_MDCLK	Input	*MII Management Data Clock* Clock reference for the MII_MDIO signal.

General Purpose Serial Interface (GPSI) These pins are multiplexed with the MII pins and are selected when MII_GSPI_N signal is at VSS.		
GPSI_RXD	Output	*GPSI Receive Data* This signal carries data received from the powerline and delivers to the external host. Data is driven on the falling edge of the GPSI_RXCLK.
GPSI_RXCLK	Output	*GPSI Receive Clock* This signal is the timing reference for the serial data transfer from the INT5130 to the external host. This clock operates at 10 MHz.
GPSI_TXD	Input	*GPSI Transmit Data* This signal carries data transmitted from the external host to the INT5130 for transmission over the powerline. Data is latched on the falling edge of the GPSI_TXCLK.
GPSI_TXCLK	Output	*GPSI Transmit Clock* This signal is the timing reference for the serial data transfer from the external host to the INT5130. This clock operates at 10 MHz.
GPSI_RXEN	Output	*GPSI Receive Enable* Indicates valid data is on the GPSI_RXD line.
GPSI_TXEN	Input	*GPSI Transmit Enable* Indicates when the external host is providing valid data on GPSI_TXD.
GPSI_TXBSY	Output	*GPSI Transmit Busy* The GPSI Transmit Busy signal is asserted within 120 GPSI clocks after GPSI_TXEN indicates a TX frame is being sent by the local host. GPSI_TXBSY stays true until the entire TX frame is loaded into an internal buffer AND a new buffer is allocated to the GPSI TX interface. This signal should be monitored by the GPSI TX host. A new GPSI TX frame should not be sent until GPSI_TXBSY returns to false to prevent TX buffer overflows. GPSI_TXBSY is an asynchronous output signal.
GPSI_COL	Output	*GPSI Collision Detect* This signal is driven false in GPSI mode.
SPI Slave Port Selected when MDI_SPIS_N signal is at VSS.		
SPIS_SDO	Output	*SPI Slave Data Out* SPI data from the INT5130 to the external host.
SPIS_SDI	Input	*SPI Slave Data In* SPI data from the external host to the INT5130. This pin is shared with the MDI_ADRSEL[1].
SPIS_SCLK	Input	*SPI Slave Clock* Timing reference signal for SPI_SDI and SPI_SDO.
SPIS_CS_N	Input	*SPI Slave Chip Select* Enables SPI data transfers on the INT5130. This pin is shared with the MDI_ADRSEL[0].

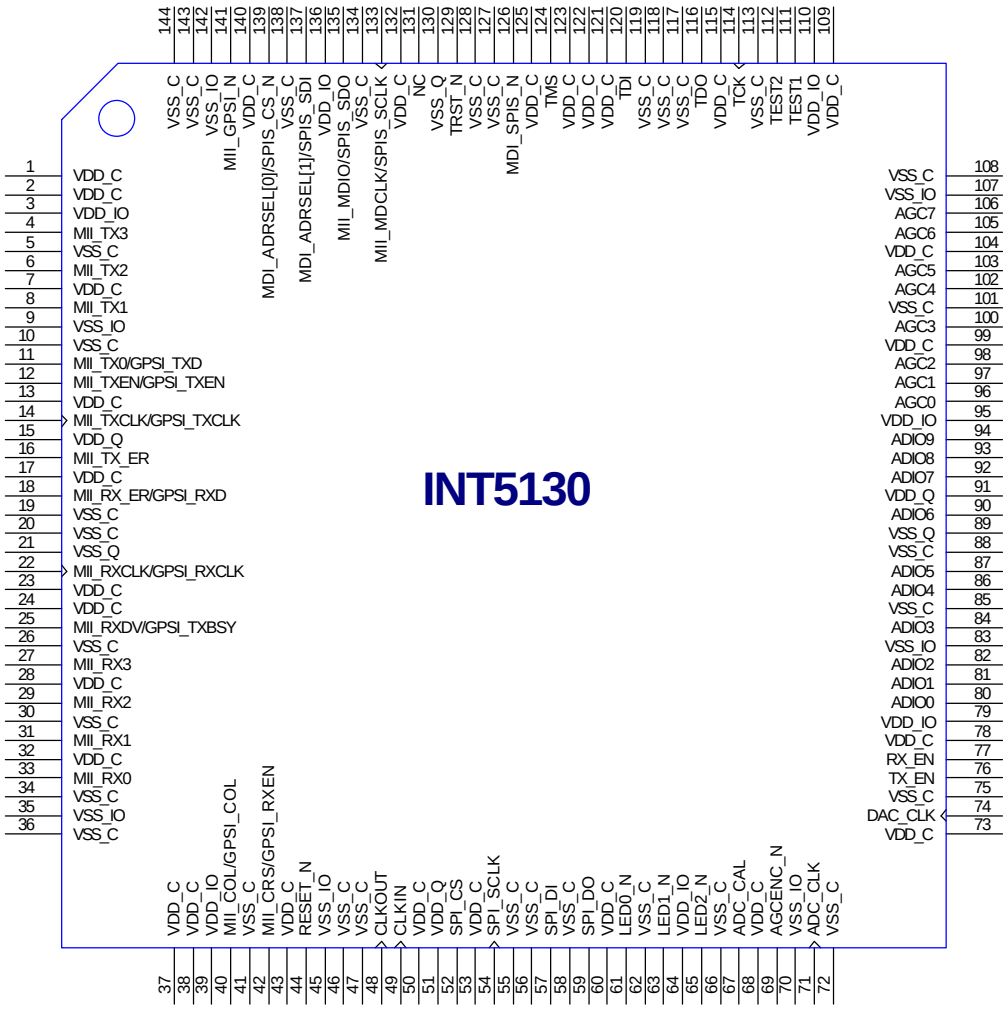
SPI Master Port (Configuration PROM Interface)		
SPI_DO	Output	*SPI Master Data Out* INT5130 configuration data from the INT5130 to the external E^2PROM.
SPI_DI	Input	*SPI Master Data In* INT5130 configuration data from the external E^2PROM to the INT5130.
SPI_CLK	Output	*SPI Master Clock* Timing reference signal for SPI_DI and SPI_DO.
SPI_CS	Output	*SPI Master Chip Select* Enables data transfers on the SPI Master Interface.
LED Control		
LED0_N	Output	*LED0_N: Collision Detection* Activate for a duration of 10 ms upon detection of a collision.
LED1_N	Output	*LED1_N: Activity Detection* Activate for a duration of 10 ms upon the receipt of a properly addressed unicast or broadcast frame or the transmission of a frame.
LED2_N	Output	*LED2_N: Link Detection* Turns on when initialization is complete successfully and “network” is established.
Analog Front End Interface		
ADC_CLK	Output	*ADC Clock* ADC clock output to the INT1000 Analog Conversion IC.
DAC_CLK	Output	*DAC Clock* DAC clock output to the INT1000 Analog Conversion IC.
TX_EN	Output	*Analog Front End Transmit Enable* Transmit Enable signal
RX_EN	Output	*Analog Front End Receive Enable* Receive Enable signal
ADIO[9:0]	Input/Output	*Analog/Digital I/O* ADC and DAC Data. Multiplexed parallel interface to INT1000 Analog Conversion IC.
AGC[7:0]	Output	*AGC Gain Select* Gain control driven by the INT5130 to set the AGC level.
ADC_CAL	Output	*ADC Calibrate* This pin must remain low during normal operation of the ADC. It is pulsed high to request a calibration cycle. The ADC_CAL minimum pulse width is 4 clock cycles. While this signal is high the ADC calibration registers are cleared and the calibration control circuitry is reset. The ADC_CAL pulse will go high 217 clock cycles (2.6 ms) after power on reset drops, and will remain high for the required 4 clock cycles.

AGCENC_N	Input	*AGC Encode* An inactive signal (logic 1) applied to this input selects unitary AGC format. An active signal (logic 0) applied to this input selects encoded AGC format
Test Access Port		
TCK	Input	*Test Clock* Test Clock for the IEEE 1149.1 JTAG Port
TDI	Input	*Test Data In* Data In for the IEEE 1149.1 JTAG Port
TMS	Input	*Test Mode Select* Test Mode Select for the IEEE 1149.1 JTAG Port
TDO	Output	*Test Data Out* Data Out for the IEEE 1149.1 JTAG Port
TRST_N	Input	*Test Reset* This pin will be used to reset the TAP controller. It should be connected to ground when the JTAG port is not in use.
System Control		
RESET_N	Input	*Reset* Resets logic circuitry, but not clock circuitry. Reset is active low and should be held low for a minimum of 100 ns.
CLKIN	Clock Pad	*Clock Input* 100 MHz clock input. Driven by an external oscillator or an external crystal (feedback path for crystal implementation provided by CLKOUT) **Note:** *CLKIN connects directly to the 2.5 V core of the IC and does not connect to the 3.3 V I/O ring. Therefore, this pin is not 3.3 or 5 V tolerant.*
CLKOUT	Clock Pad	*Clock Output* 100 MHz clock feedback path when a crystal is implemented. This pin should be left as NO CONNECT if an external oscillator is implemented on CLKIN. **Note:** *CLKOUT connects directly to the 2.5 V core of the IC and does not connect to the 3.3 V I/O ring. Therefore, this pin is not 3.3 or 5 V tolerant.*
MDI_ADRSEL[1:0]	Input	*MDI PHY Address Selection* Address select used to compare against the upper two bits of the MDI Address. These pins share function with SPIS_CS_N and SPIS_SDI and should be pulled-up or down with external resistors to set the appropriate value which is read by the INT5130 during power up.
MDI_SPIS_N	Input	*Management Data Interface/Serial Peripheral Interface Slave Select.* Selects which PHY management signals are active.
MII_GPSI_N	Input	*Media Independent Interface/General Purpose Serial Interface Select.* Selects which PHY data interface signals are active.

TEST1	Input	*Factory Test Pin 1* Tie to I/O Ground
TEST2	Input	*Factory Test Pin 2* Tie to I/O Ground
NC	---	*No Connect*
Power Supplies		
VDD_C	2.5v	*Digital Power*
VSS_C		*Digital Ground*
VDD_IO	3.3v	*I/O Power*
VSS_IO		*I/O Ground*
VDD_Q	3.3v	*Quiet Power* Connect to I/O Power
VSS_Q		*Quiet Ground* Connect to I/O Ground

Table 2: Pin Descriptions by Group

Pin Diagram



Functional Description

The interfaces that provide data, status, and control to and from the INT5130 include…

- External host interface provided via the Media Independent Interface (MII) format (described by IEEE802.3u, Clause 22) or a General Purpose Serial Interface (GPSI).
- Management control provided via the Management Data Interface (MDI) or the Serial Peripheral Interface (SPI).
- Analog Front End interface.
- LEDs indicating network status.
- Optional E^2PROM interface providing a path to initialize the INT5130 with PowerPacket-specific configuration information.
- The JTAG port implements the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

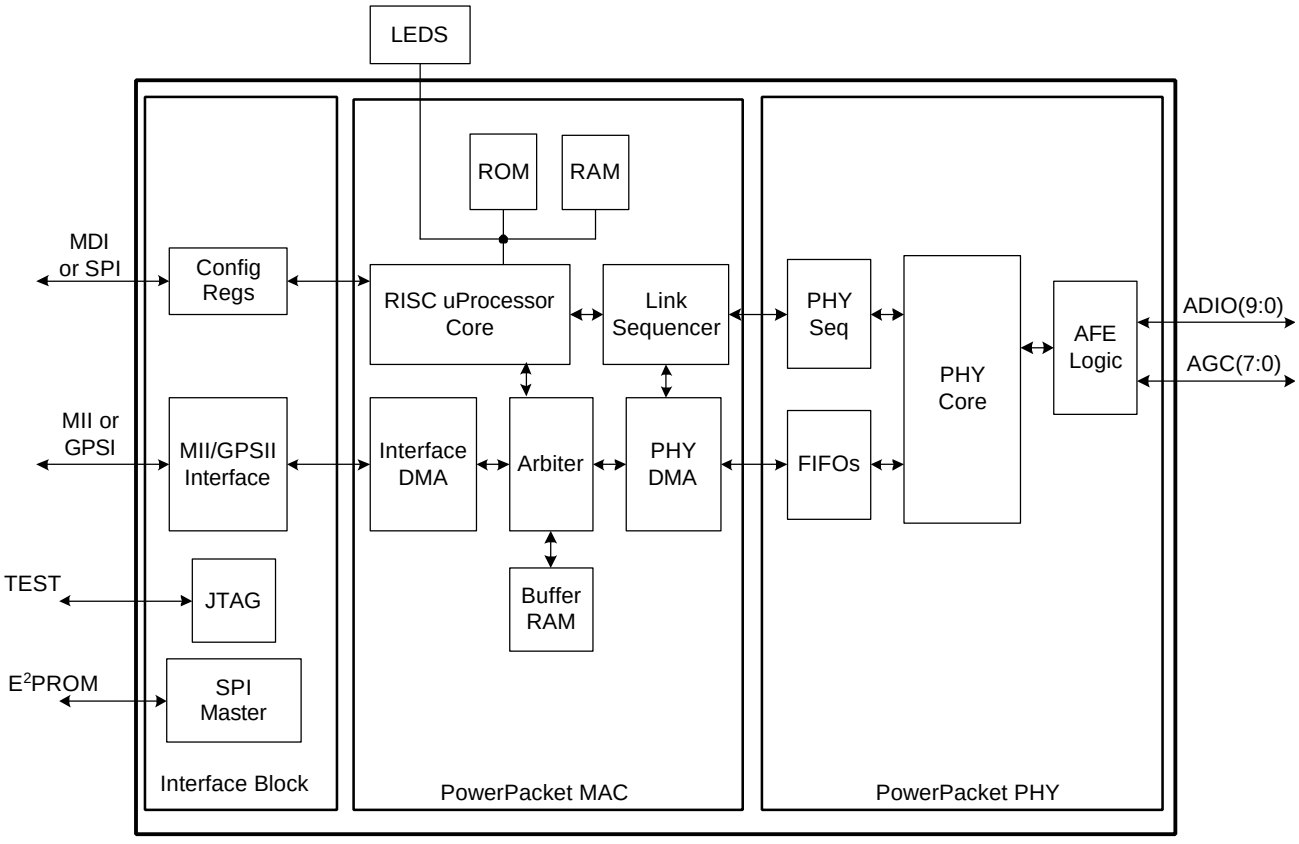


Figure 1: INT5130 Block Diagram

MII Data Interface with MDI Control

Data communication between the INT5130 and the external host controller is provided via the Media Independent Interface or a reduced General Purpose Serial Interface. The MII_GPSI_N select pin is included on the chip interface to configure the INT5130 in either MII mode or GPSI mode. Access to the INT5130's internal MII status and control registers is via the Management Data Interface or a SPI interface. The MDI_SPIS_N select pin is included on the chip interface to configure the INT5130 in either MDI mode or SPI mode. The information that follows describes the MII communication interface along with the MDI management interface as a typical example.

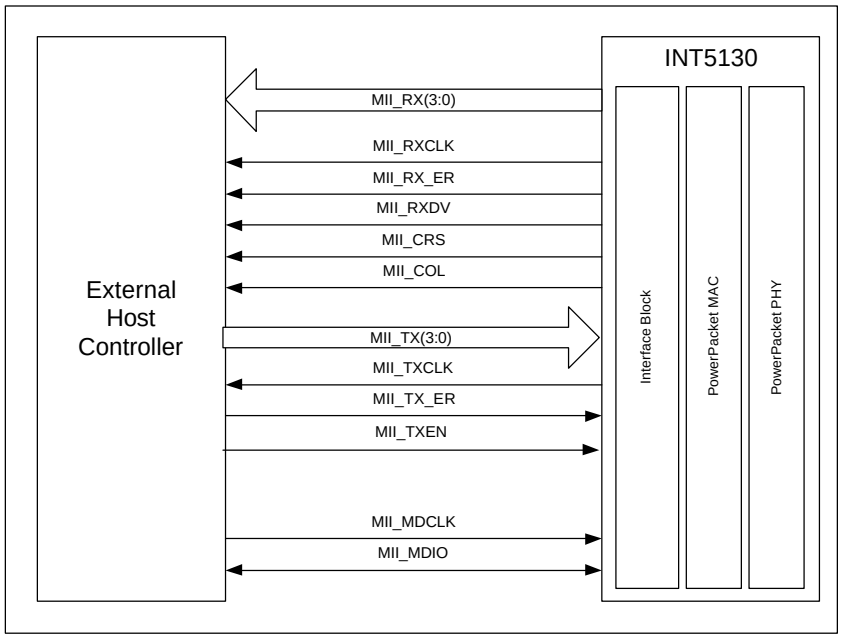


Figure 2: MII Data Interface with MDI Control

MII Interface

MII is an industry standard, multi-vendor, interoperable interface between separate MAC and PHY devices. It provides a simple interconnection between the INT5130 and IEEE802.3 Ethernet MAC controllers (commonly referred to as external host controllers in this document) available from a variety of IC suppliers. The MII consists of separate 4-bit data paths for transmit and receive data along with carrier sense and collision detection. Data is transferred between the MAC and PHY over each 4-bit data path synchronous with a clock signal supplied to the host by the INT5130. The MII interface also provides a two wire bi-directional serial management data interface (MDI). This interface provides access to the status and control registers in the INT5130.

MII Timing Diagrams

Figure 3 below shows the transmission behavior of the MII interface. Figure 4 shows the receive behavior of the MII interface. Figure 5 shows an unsuccessful attempt to transmit a packet, resulting in a collision.

NOTE: MII_CRS is asynchronous to MII_TXCLK.

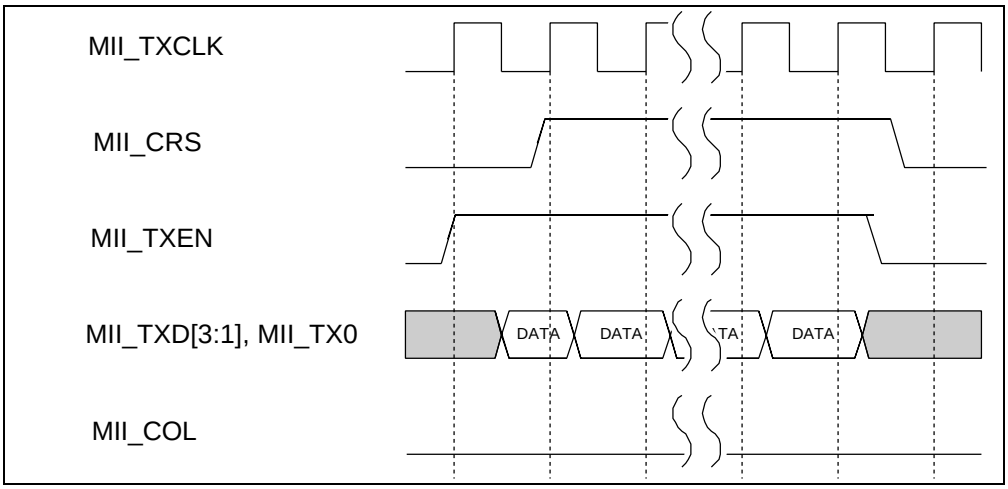


Figure 3: MII TX Waveform

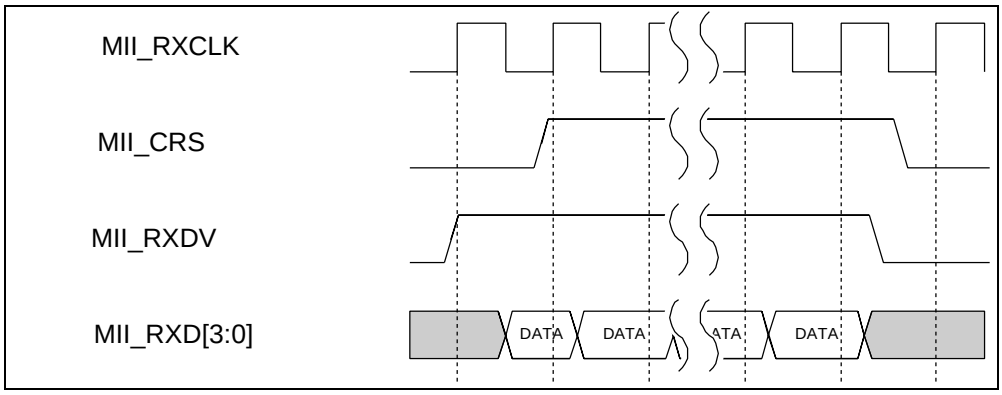


Figure 4: MII RX Waveform

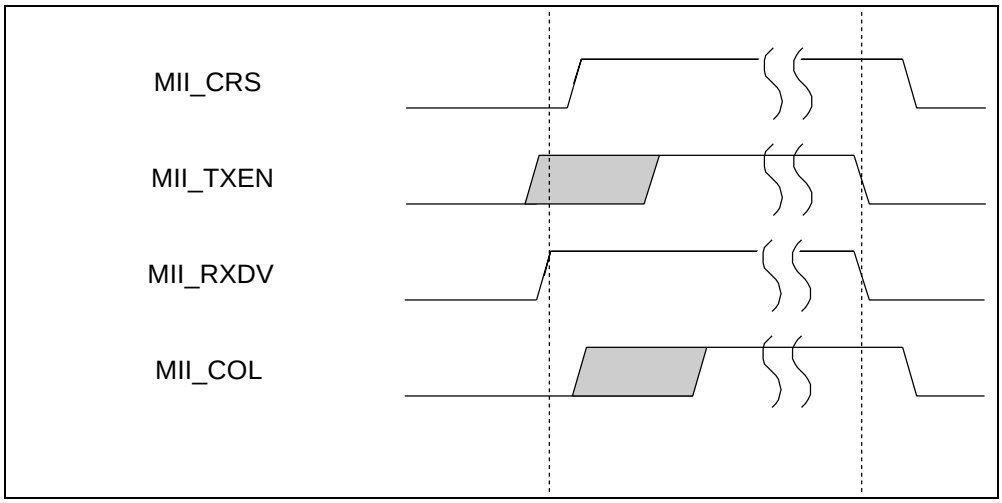


Figure 5: MII TX With Collision Based On RX Activity

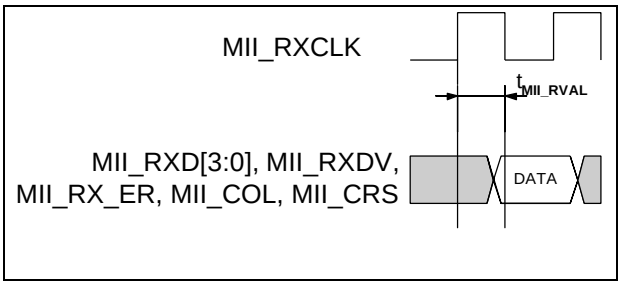


Figure 6: MII Receive Timing Diagram

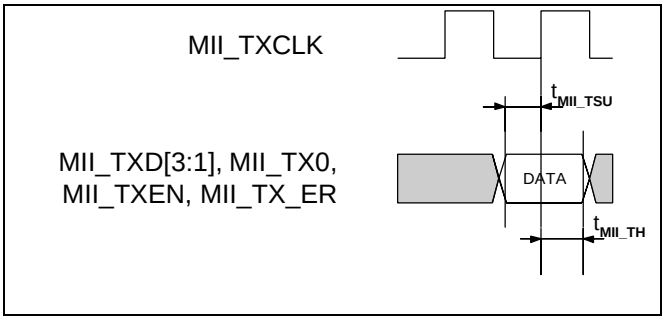


Figure 7: MII Transmit Timing Diagram

MII DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Receive Timing					
t_{MII_RVAL}	MII_RX[3:0], MII_RXDV valid from ↑ MII_RXCLK	measured from V_{ilmax} = 0.8V or measured from V_{ihmin} = 2.0V	0	25	ns
Transmit Timing					
t_{MII_TSU}	MII_TXEN, MII_TX0, MII_TX[3:1] setup to ↑ MII_TXCLK	measured from V_{ilmax} = 0.8V or measured from V_{ihmin} = 2.0V	8		ns
t_{MII_TH}	MII_TXEN, MII_TX0, MII_TX[3:1] hold to ↑ MII_TXCLK	measured from V_{ilmax} = 0.8V or measured from V_{ihmin} = 2.0V	0		ns

Table 3: MII DC Characteristics

MII Signal Descriptions

The following description references Clause 22, Media Independent Interface specification, used in the 100 Mbps half-duplex mode. The MII is used as a data channel that transfers data back and forth with flow controlled by the carrier sense signal (MII_CRS).

MII_TXCLK and MII_RXCLK

The INT5130 generates a stable, continuous 25 MHz square wave that is supplied on MII_TXCLK and MII_RXCLK. These clocks provide the timing reference for the transfer of the MII_TXEN and MII_TX signals, as well as MII_RX, MII_RX_ER, and MII_RXDV.

MII_RX_ER

MII_RX_ER is activated when the INT5130 detects an error in the receive stream as a result of decoding.

MII_TX_ER

MII_TX_ER is activated by the external host controller when an error condition is detected during packet transmission. The INT5130 will ignore any MII transmission within which MII_TX_ER is asserted. MII_TX_ER is ignored if MII_TXEN is not asserted.

MII_TXEN

MII_TXEN from the external host provides the framing for the Ethernet packet. An active MII_TXEN indicates to the INT5130 that data on MII_TX[3:0] should be sampled using MII_TXCLK.

MII_TX[3:0]

MII_TX[3:0] contains the data to be transmitted and transitions synchronously with respect to MII_TXCLK. MII_TX[0] is the least significant bit. It is generally assumed that the data will contain a properly formatted Ethernet frame. That is, the first bits on MII_TX[3:0] correspond to the preamble, followed by SFD and the rest of the Ethernet frame (DA, SA, length/type, data, CRC).

MII_RXDV

MII_RXDV is asserted by the INT5130 to indicate that the INT5130 has decoded receive data to present to the external host.

MII_RX[3:0]

MII_RX[3:0] contains the data recovered from the medium by the INT5130 and transitions synchronously with respect to MII_RXCLK. MII_RX[0] is the least-significant bit. The INT5130 formats the frame such that the external MAC will be presented with expected preamble plus SFD.

MII_CRS

MII_CRS is used to tell the external host when the INT5130 is available for sending a packet. MII_CRS is asynchronous to MII_TXCLK. When a packet is being transmitted, CRS is held high. CRS will go low whenever the INT5130 is ready to accept another packet.

On transmit, the INT5130 asserts MII_CRS some time after MII_TXEN becomes active, and drops MII_CRS after MII_TXEN goes inactive AND when the INT5130 is ready to receive another packet from the external host for transmission. When MII_CRS has been negated for at least 900ns, the external MAC may assert MII_TXEN again if there is another packet to send. This differs from nominal behavior of MII_CRS in that MII_CRS can extend past the end of the packet by an

arbitrary amount of time, while the INT5130 is gaining access to the channel and transmitting the packet.

MII_CRS does not affect the receive side of the channel. Once packets start arriving from the powerline medium and begin transmission to the external host controller over the MII interface, the external host MUST be ready to receive or the packet can be lost. Note that external MACs programmed to run in 100 Mbps mode do not use a jabber timeout, so there is no timing restriction on how long MII_CRS can be asserted.

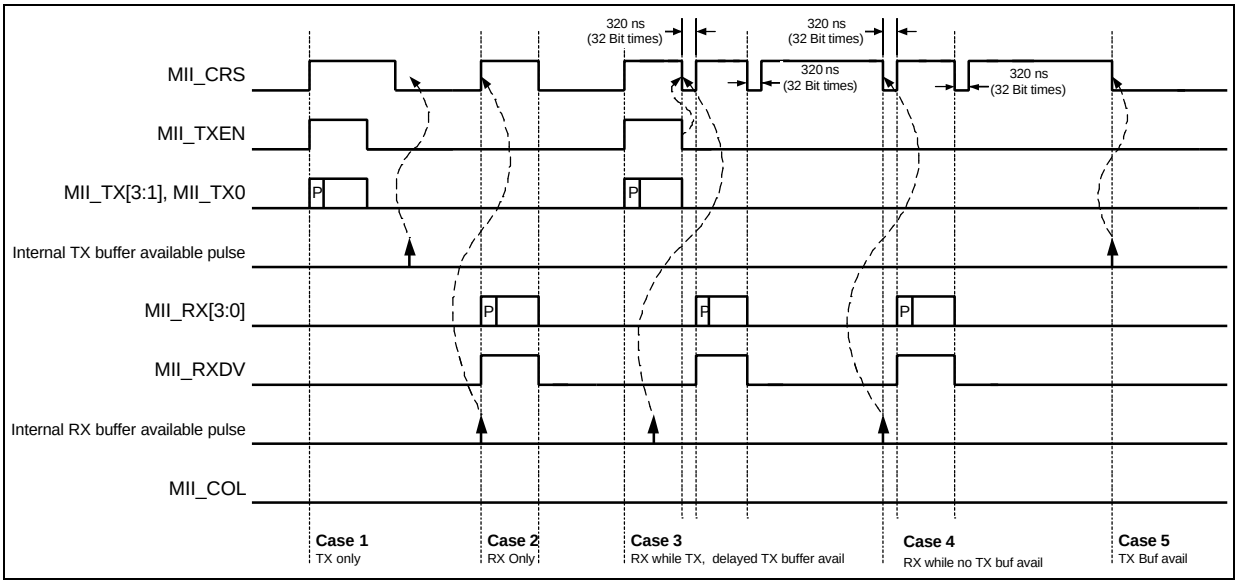


Figure 8: MII Flow Control Overview Part 1

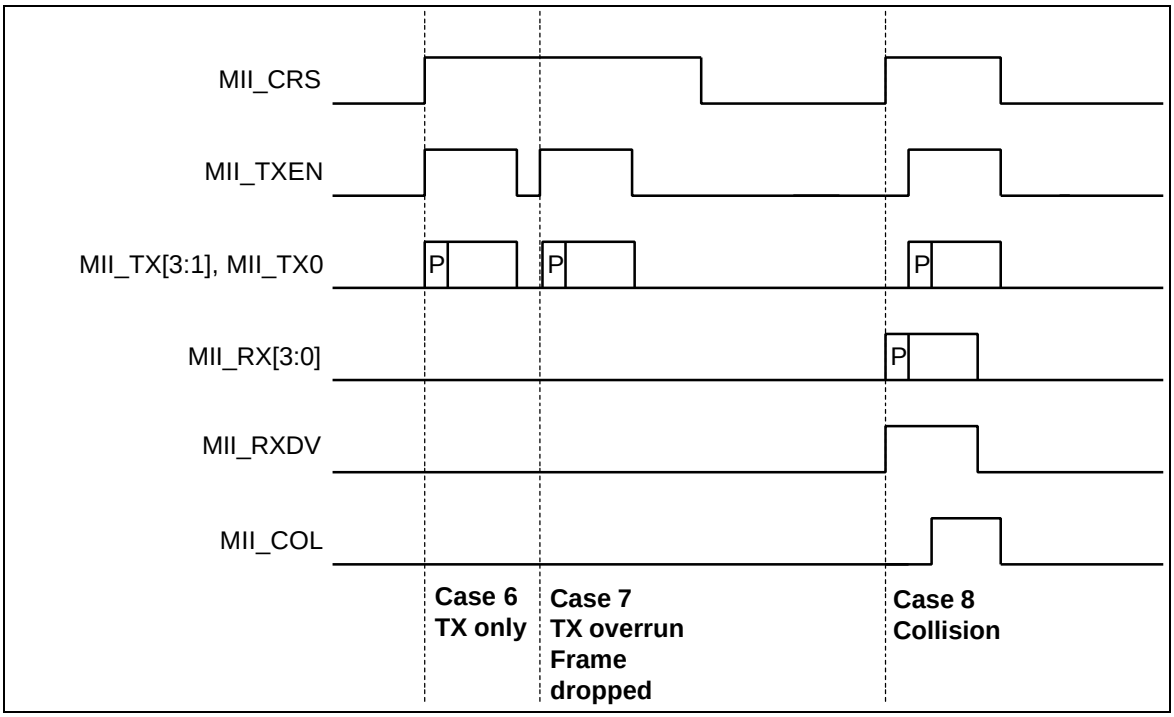


Figure 9: MII Flow Control Overview Part 2

MII Frame Structure

The frame structure transmitted on the MII or GPSI interface is the following sequence of fields:

Interframe Gap	Preamble	Start Frame Delimiter	Data

Interframe Gap

A period on the MII interface during which no data activity occurs on the MII.

Preamble

Begins a frame transmission that consists of 7 octets with the following bit values…

10101010 10101010 10101010 10101010 10101010 10101010 10101010

The preamble is stripped by the INT5130 when transmitting (the preamble is not transmitted on the PLC medium) and pre-pended by the INT5130 when receiving.

Start Frame Delimiter

Indicates the start of a frame and follows the preamble. The SFD bit sequence is 10101011.

The start frame delimiter is stripped by the INT5130 when transmitting (the SFD is not transmitted on the PLC medium) and pre-pended by the INT5130 when receiving.

Data

Data sent over the MII interface consists of N bytes of data transmitted as 2N nibbles.

The de-assertion of the MII_TXEN signals the End Of Frame (EOF) for data transmitted on the MII_TX[3:0] pins. Likewise, the de-assertion of the MII_RXDV signals the EOF for data transmitted on MII_RX[3:0].

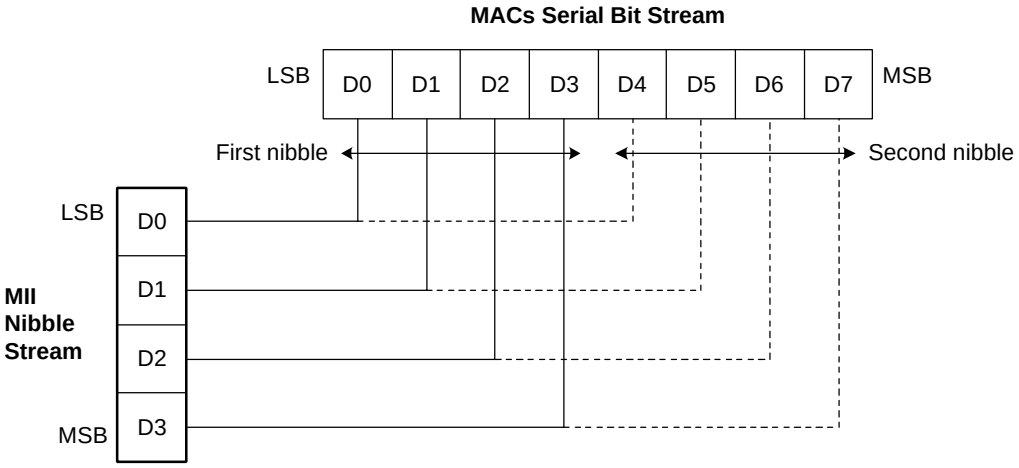


Figure 10: Partition of Serial Bit Stream to Nibble Stream

MDI Control Interface

The Management Data Interface connects the external host to the INT5130 for purposes of controlling the INT5130 and gathering status. A specific frame format and protocol definition exists for exchanging management frames over this interface. A register definition exists as well that specifies a basic register set with an extension mechanism. The INT5130 implements the basic register set only.

MDI Timing Diagrams

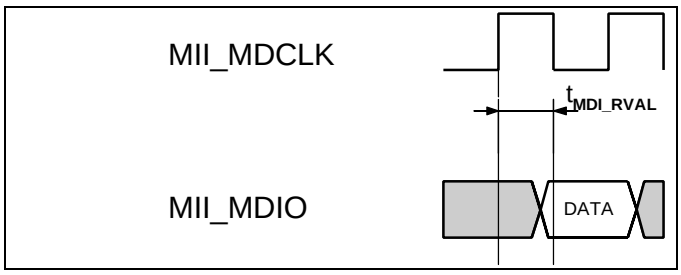


Figure 11: MDI Receive Timing Diagram

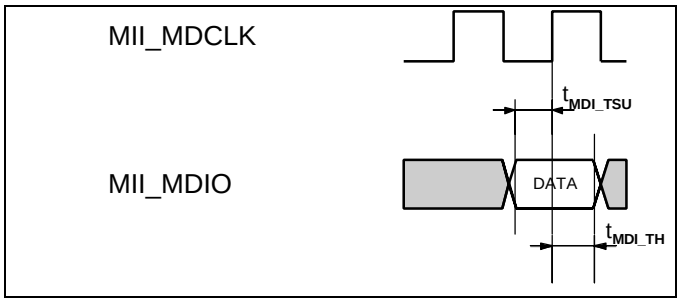


Figure 12: MDI Transmit Timing Diagram

MDI DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Receive Timing					
t_{MDI_RVAL}	MII_MDIO valid from ↑ MII_MDCLK	measured from V_{ilmax} = 0.8V or measured from V_{ihmin} = 2.0V	0	300	ns
Transmit Timing					
t_{MDI_TSU}	MII_MDIO setup to ↑ MII_MDCLK	measured from V_{ilmax} = 0.8V or measured from V_{ihmin} = 2.0V	10		ns
t_{MDI_TH}	MII_MDIO hold to ↑ MII_MDCLK	measured from V_{ilmax} = 0.8V or measured from V_{ihmin} = 2.0V	10		ns

Table 4: MDI DC Characteristics

MDI Signal Descriptions

Management Data Input/Output

MII_MDIO is a bi-directional signal that is used to transfer status and control information between the INT5130 and the external host. Control information is driven by the external host synchronously with respect to MII_MDCLK and is sampled synchronously by the INT5130. Status information is transferred from the INT5130 to the external host in the same manner.

Management Data Clock

MII_MDCLK is sourced by the external host as the timing reference for transfer of information on the MII_MDIO signal.

MII Management Register Set

The IEEE 802.3u mandated management data registers for control and status are accessible via the Management Data Interface (MDI). These registers are also accessible via the industry supported serial peripheral interface. The MDI Port will only respond to addresses 0xbXX000 when the XX field (MSBits of the MDI address) match the state of the MDI_ADRSEL[1:0] input signals. These registers can also be

accessed from the SPI Slave port when the MDI_SPIS_N select line has been tied low to select the SPI Slave port.

PLCSR	Register Name	MII Mandated
0	Control Register	X
1	Status Register	X

Table 5: Powerline Control and Status Register (PLCSR) Summary

	PRE	ST	OP	PHYAD	REGAD	TA	Data	Idle
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Figure 13: MDI Frame Structure

PRE (Preamble)

At the beginning of each MDI transaction, the external host shall send a sequence of 32 contiguous logic “1” bits on the MDIO signal so the INT5130 can establish synchronization. The INT5130 needs to observe this 32 bit sequence on the MII_MDIO signal before it responds to any transaction.

ST (Start of Frame)

Indicated by a “01” pattern.

OP (Operation Code)

“10” indicates a READ. “01” indicates a WRITE.

PHYAD (PHY Address)

The PHY Address is 5 bits, allowing up the 32 unique PHY addresses. The INT5130 will respond to PHY addresses indicated by 0bXX000. The “XX” bits of the PHY address are controlled by the INT5130 interface pins MDI_ADRSEL(0:1). This allows the designer to assign the INT5130 to one of 4 unique PHY addresses.

REGAD (Register Address)

The Register Address is 5 bits and is used to index the maximum of 32 individual registers in the MDI address space. The INT5130 only implements the two mandated MII registers. 0b00000 will index the MII Control Register and 0b00001 will index the MII Status Register.

TA (Turnaround)

The turnaround time is a 2 bit time spacing between the Register Address field and the Data field to avoid contention during a read transaction.

For reads, both the external host and the INT5130 will remain in tri-state for the first bit time. The INT5130 will drive a “0” during the second bit time.

For writes, the external host will drive a “1” for the first bit time and a “0” bit for the second bit time.

Data

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

GPSI Interface with SPI Control

The General Purpose Serial Interface (GPSI) is a flexible, bi-directional serial interface that can be utilized in place of the MII. It provides a straightforward interface to a communications controller through a synchronous serial data stream for transmit and receive data. When using the GPSI interface, the management interface can either be MDI or SPI, selected by the MDI_SPIS_N pin. The information that follows describes the GPSI communication interface along with the SPI management interface as a typical example.

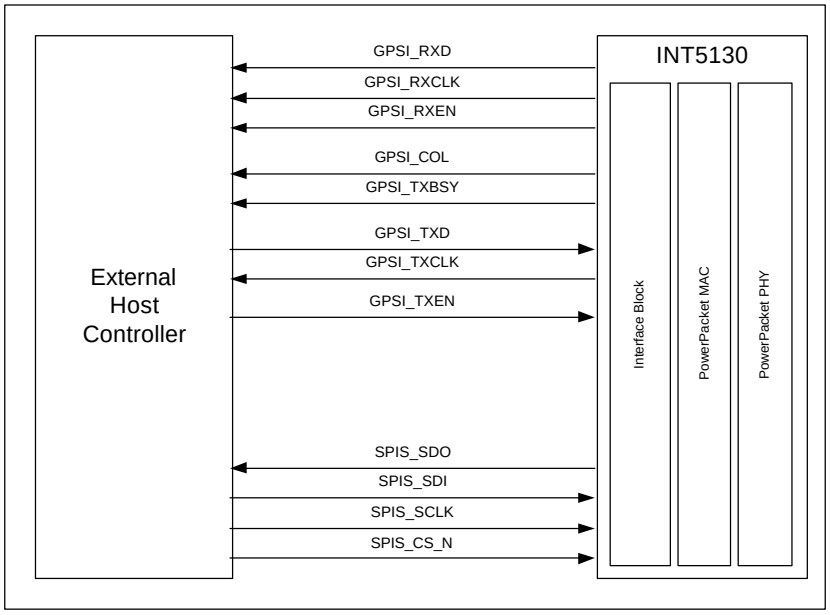


Figure 14: GPSI Data Interface with SPI Control

GPSI Interface

GPSI is an interoperable interface providing a simple interconnection between the INT5130 and embedded microcontrollers. Data is transferred between the host controller and the INT5130 over separate 1-bit transmit and receive data paths synchronous with clock signals supplied to the host by the INT5130.

GPSI Timing Diagrams

The figures below show the transmission and reception of packets and the corresponding behavior of the GPSI interface. A packet is transferred from the host when GPSI_TXEN goes high. An unsuccessful attempt is made to transmit a packet in Case 5. The received packet is passed to the host when GPSI_RXEN is high.

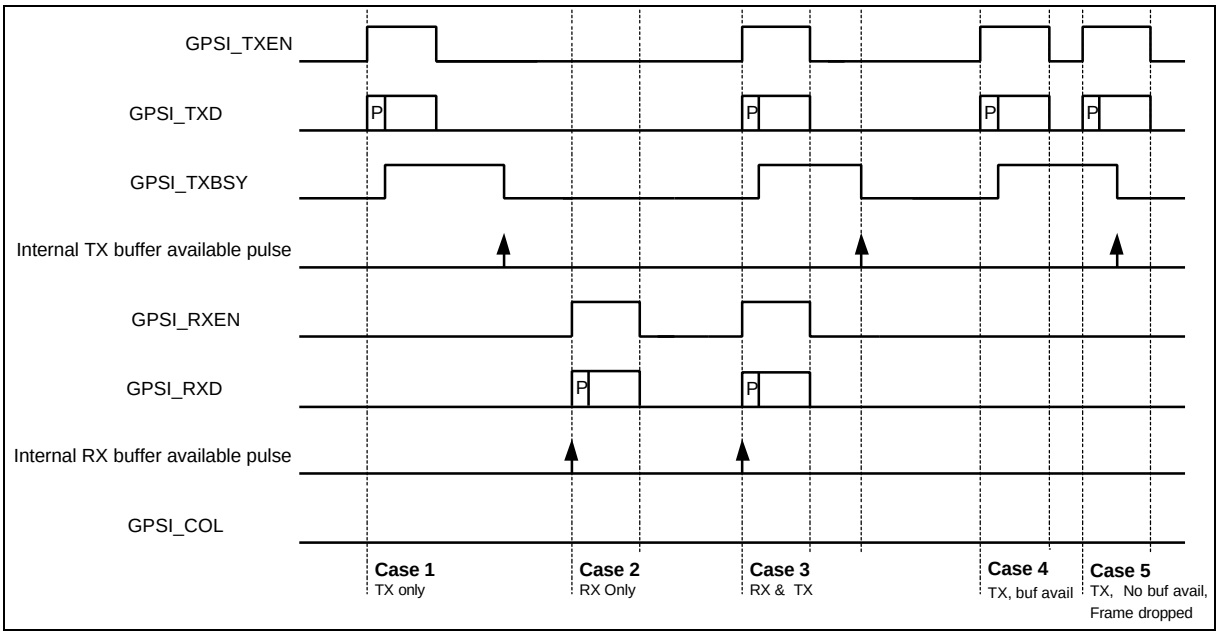


Figure 15: GPSI Flow Control Diagram

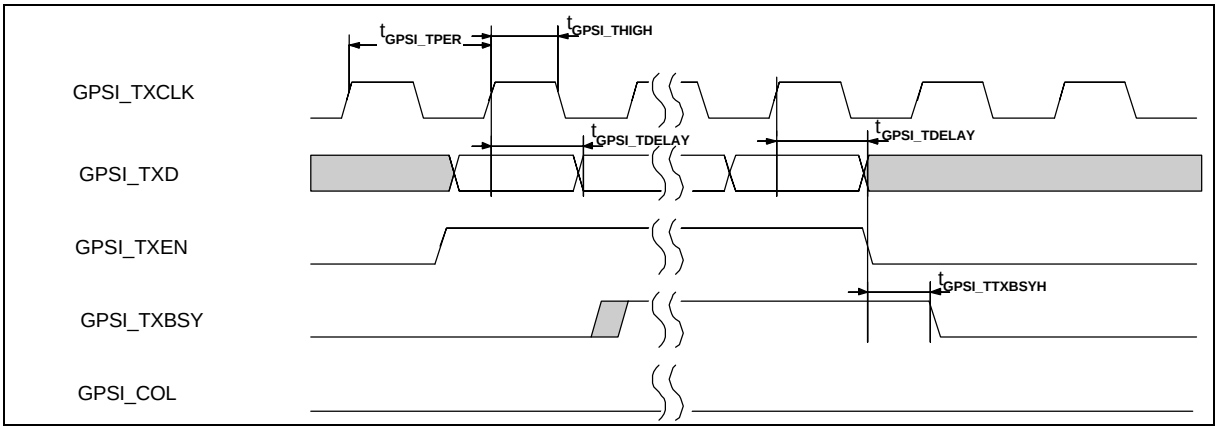


Figure 16: GPSI Transmit Timing Diagram

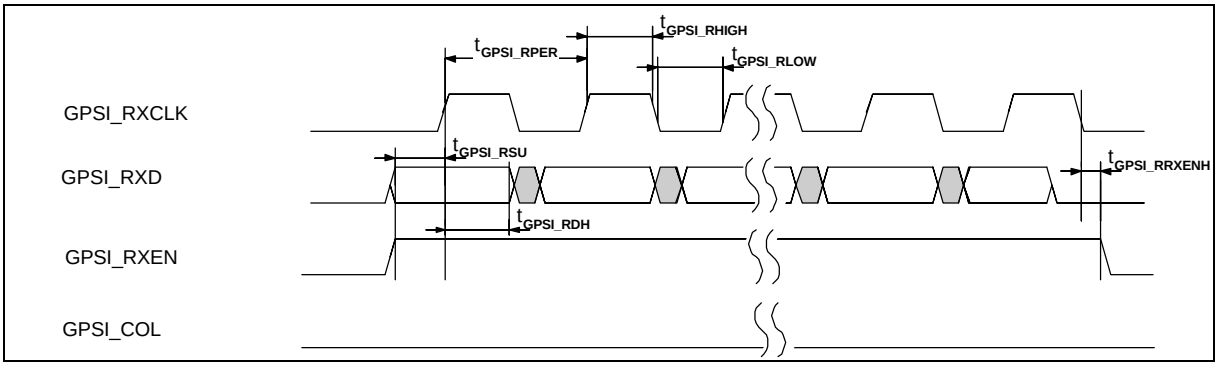


Figure 17: GPSI Receive Timing Diagram

GPSI DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
Receive Timing					
t_{GPSI_RPER}	GPSI_RXCLK Period	@ 1.5 V	99.99	100.01	ns
t_{GPSI_RHIGH}	GPSI_RXCLK High Time	@ 1.5 V	40	60	ns
t_{GPSI_RLOW}	GPSI_RXCLK Low Time	@ 1.5 V	40	60	ns
t_{GPSI_RSU}	GPSI_RXD and GPSI_RXEN Setup to ↑ GPSI_RXCLK	@ 1.5 V	15		ns
t_{GPSI_RDH}	GPSI_RXD Hold after ↑ GPSI_RXCLK	@ 1.5 V	15		ns
t_{GPSI_RRXENH}	GPSI_RXEN Hold after ↓ GPSI_RXCLK	@ 1.5 V	0		ns
Transmit Timing					
t_{GPSI_TPER}	GPSI_TXCLK Period	@ 1.5 V	99.99	100.01	ns
t_{GPSI_THIGH}	GPSI_TXCLK High Time	@ 1.5 V	40	60	ns
t_{GPSI_TDELAY}	GPSI_TXD and GPSI_TXEN Delay from ↑ GPSI_TXCLK	@ 1.5 V	0	70	ns
t_{GPSI_TRXENH}	GPSI_RXEN Hold after ↓ GPSI_TXEN	@ 1.5 V	0		ns

Table 6: GPSI DC Characteristics

GPSI Signal Descriptions

GPSI_TXCLK and GPSI_RXCLK: The INT5130 generates a stable, continuous 10 MHz square wave that is supplied on GPSI_TXCLK and GPSI_RXCLK. These clocks provide the timing reference for the transfer of the GPSI_TXEN and GPSI_TXD signal, as well as GPSI_RXEN and GPSI_RXD.

GPSI_RXD: GPSI_RXD contains the data recovered from the medium by the INT5130 and transitions synchronously with respect to GPSI_RXCLK. The INT5130 properly formats the frame such that the external host controller will be presented with the expected preamble plus SFD.

GPSI_RXEN: GPSI_RXEN is asserted by the INT5130 to indicate that the INT5130 has decoded receive data to present to the external host controller.

GPSI_TXBSY: GPSI_TXBSY is an optionally used signal to tell the external host controller when the INT5130 is available for sending packets. When a packet is being transmitted, GPSI_TXBSY is held high. GPSI_TXBSY will go low whenever the INT5130 is ready to send another packet. If this signal is not used, the transmitting logic must pace the packet transmissions to ensure that no packets are lost due to buffer overflow.

On transmit, the INT5130 asserts GPSI_TXBSY some time after GPSI_TXEN becomes active, and drops GPSI_TXBSY after GPSI_TXEN goes inactive AND when the INT5130 is ready to accept another packet for transmission. When GPSI_TXBSY falls, the external host controller may assert GPSI_TXEN again if there is another packet to send.

GPSI_TXBSY does not affect nor reflect the receive side of the channel. Once packets start arriving off of the powerline medium and begin transmission to the external host controller over the GPSI interface, the external host controller MUST be ready to receive or the packet can be lost.

GPSI_TXEN: GPSI_TXEN from the external host provides the framing for the Ethernet packet. An active GPSI_TXEN indicates to the INT5130 that data on GPSI_TXD should be sampled using GPSI_TXCLK.

GPSI_TXD: GPSI_TXD contains the data to be transmitted and transitions synchronously with respect to GPSI_TXCLK. It is generally assumed that the data will contain a properly formatted Ethernet frame (see MII Frame Structure above). That is, the first bits on GPSI_TXD correspond to the preamble, followed by Start Frame Delimiter (SFD) and the rest of the Ethernet frame (DA, SA, length/type, data, CRC).

SPI Slave Interface

The INT5130 implements a SPI Slave port that when connected to an external host controller containing a SPI Master, can be used to control access to the two configuration registers. The SPI Slave port uses a 16-bit control field (msb first) consisting of a 6-bit command field, a 5-bit reserved field, and a 5-bit address field to control access to the two configuration registers detailed above. Following the control field, the 16-bit register contents are written or read based on the command field.

Register function	**Control Field**															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Command Field						**Reserved Field**					**Address Field**				
	5	**4**	**3**	**2**	**1**	**0**	**4**	**3**	**2**	**1**	**0**	**4**	**3**	**2**	**1**	**0**
Write PLCSR0 (Control Register)	L	L	L	L	**H**	**L**	H	L	L	L	L	L	L	L	L	**L**
Read PLCSR0 (Control Register)	L	L	L	L	**H**	**H**	H	L	L	L	L	L	L	L	L	**L**
Write PLCSR1 (Status Register)	L	L	L	L	**H**	**L**	H	L	L	L	L	L	L	L	L	**H**
Read PLCSR1 (Status Register)	L	L	L	L	**H**	**H**	H	L	L	L	L	L	L	L	L	**H**

Table 7: SPI Slave Command Summary

SPI SlaveTiming Diagram

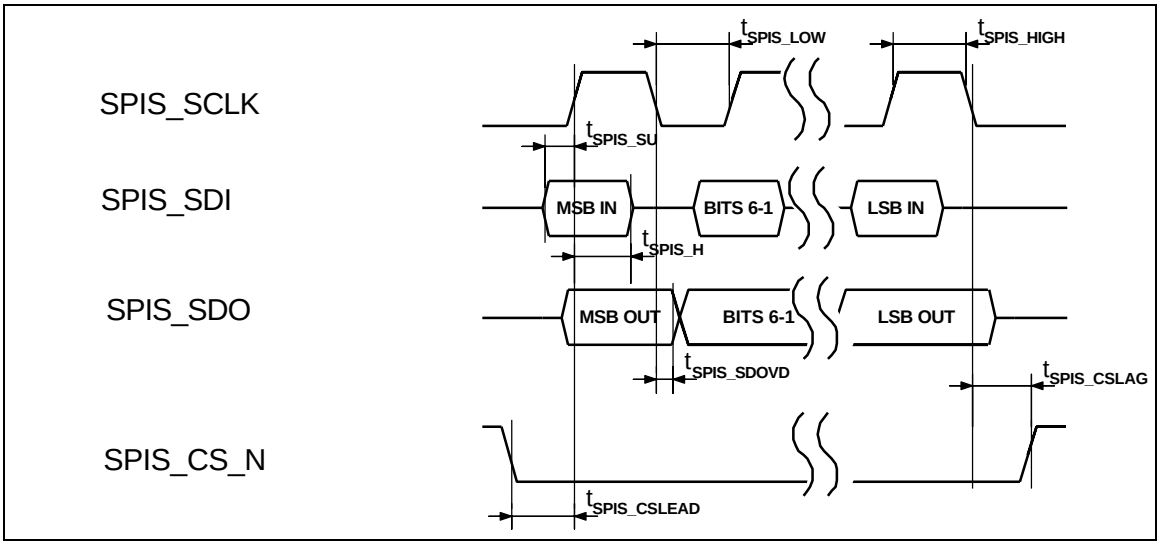


Figure 18: SPI Slave Signal Timing

SPI Slave DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
t_{SPIS_F}	SPIS_SCLK Frequency			2.1	MHz
t_{SPIS_HIGH}	SPIS_SCLK High Time	@ 1.5 V	400		ns
t_{SPIS_LOW}	SPIS_SCLK Low Time	@ 1.5 V	400		ns
t_{SPIS_SDOVD}	SPIS_SDO Valid Output Delay from SPIS_SCLK	@ 1.5 V	0	500	ns
t_{SPIS_CSLEAD}	SPIS_CS Lead to SPIS_SCLK	@ 1.5 V	500		ns
t_{SPIS_CSLAG}	SPIS_CS Lag from SPIS_SCLK	@ 1.5 V	1500		ns
t_{SPIS_SU}	SPIS_SDI Setup Time to SPIS_SCLK	@ 1.5 V	200		ns
t_{SPIS_H}	SPIS_SDI Hold Time to SPIS_SCLK	@ 1.5 V	200		ns

Table 8: SPI Slave DC Characteristics

Clocks

The INT5130 runs from a single 100MHz oscillator input and generates a 50MHz clock to feed the ADC, a 50MHz clock to feed the DAC, the 25MHz MII clock, and the 10MHz GPSI clock. The 100MHz clock input directly feeds the clock distribution network that clocks up to 60% of the digital logic. **Note:** *Both CLKIN and CLKOUT connect directly to the 2.5 V core of the IC and do not connect to the 3.3 V I/O ring. Therefore these pins are not 3.3V or 5V tolerant.*

The oscillator must have ±25 PPM RMS maximum tolerance including initial accuracy, temperature/voltage range and 5 years of aging. This oscillator must have a symmetry no worse than 40/60, jitter of 75 ps and 4 ns rise and fall time. The oscillator must be rated over the desired temperature range and ±10% voltage range. The INT5130 uses a crystal input cell to receive the clock input.

AFE Interface

The INT5130 provides a simple parallel interface to the analog front end (AFE). The analog data is clocked into or out of the INT5130 on a 10-bit bi-directional parallel data bus under control of transmit or receive enable signals and sample clock references provided to the AFE from the INT5130. The INT5130 also provides a parallel byte-wide automatic gain control interface.

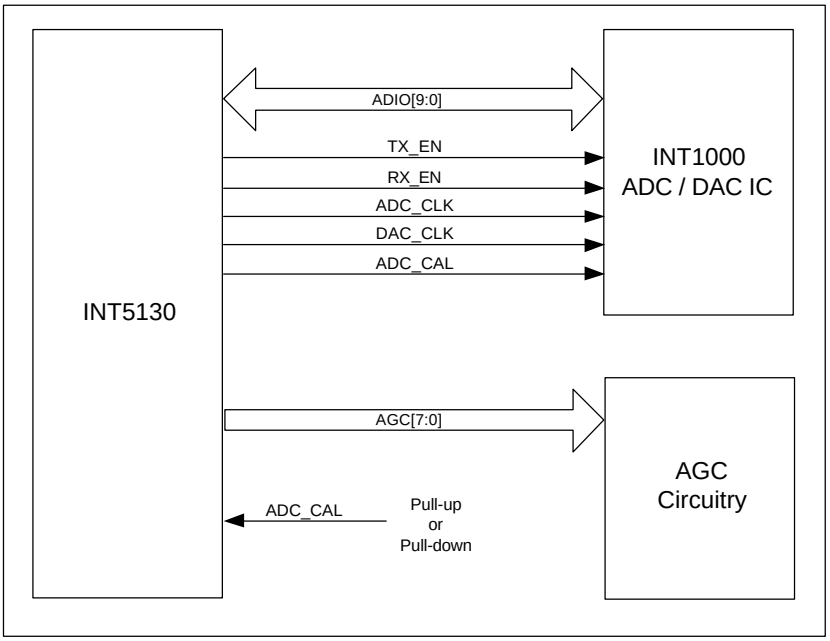


Figure 19: AFE Interface to INT5130

ADC/DAC Interface

The INT5130 outputs a sequential stream of digital time samples of the OFDM waveforms for transmission. The digital transmit signal is passed on to the INT1000 Integrated Converter. The INT1000 consists of a 10-bit ADC and 10-bit DAC on a multiplexed 10-bit bi-directional data bus. The ADC digitizes the analog OFDM receive signal for input to the INT5130. The DAC converts digital samples into analog waveforms.

ADC/DAC Timing Diagrams

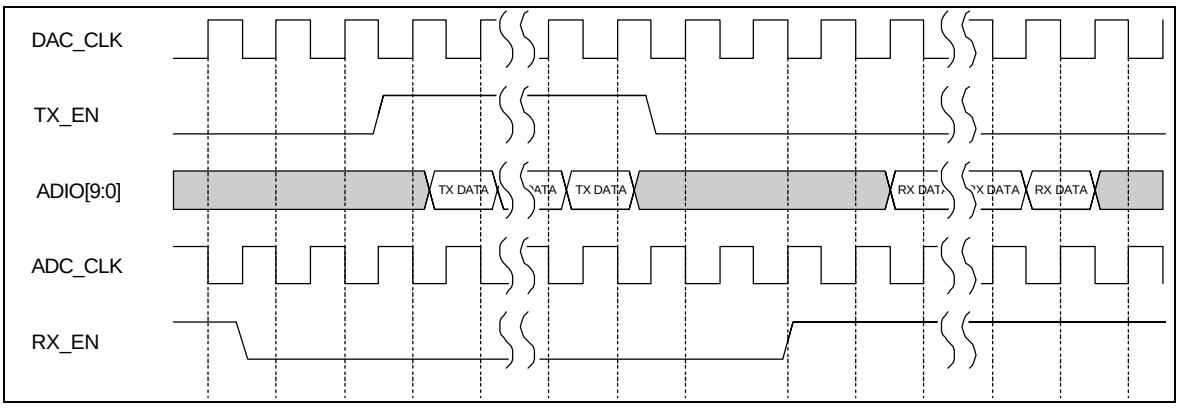


Figure 20: AFE TX and RX activity

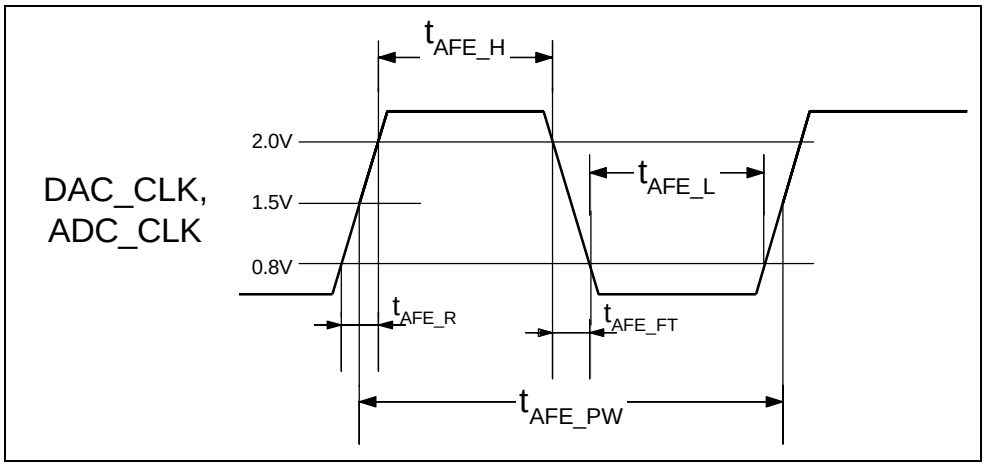


Figure 21: AFE Clock Waveforms

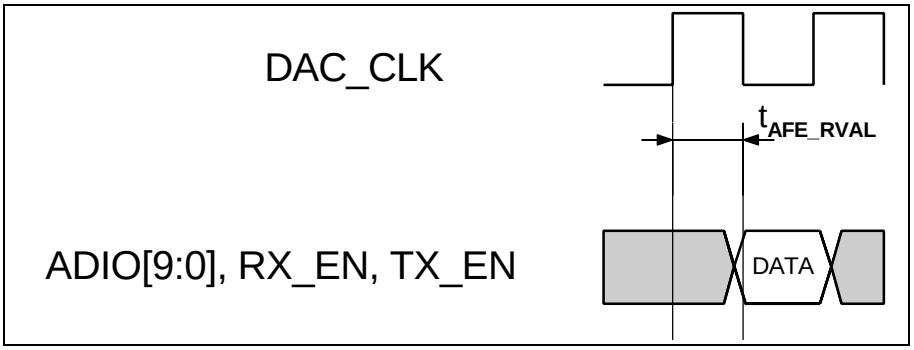


Figure 22: AFE Transmit Timing Diagram

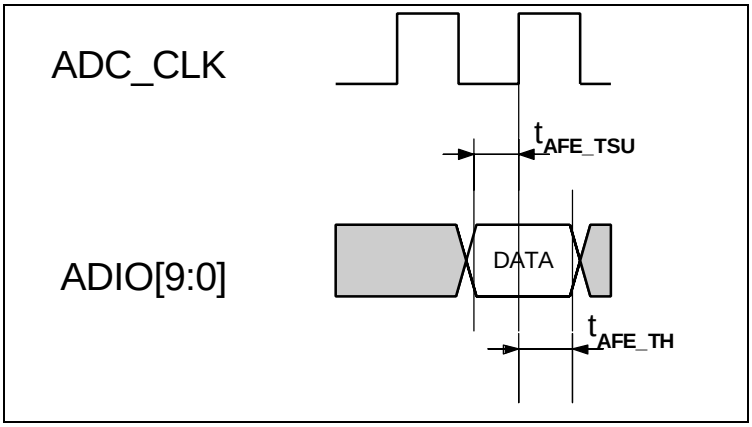


Figure 23: AFE Receive Timing Diagram

DAC DC Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
	Number of Bits			10		Bits
	Data Format			Straight Binary		
	Sample Rate		50			MSPS
DAC DATA OUTPUTS						
V_{OH}	HIGH level output voltage	1, 2	2.4			V
V_{OL}	LOW level output voltage	1, 3			0.4	V
T_{AFE_RVAL}	Propagation Delay Time	1	5.0	8.2	15.0	ns
DAC CLOCK OUTPUT						
t_{AFE_PW}	DAC Clock Pulse Width	1	10		15	ns
t_{AFE_R}	DAC Clock Rise Time	1			2	ns
t_{AFE_FT}	DAC Clock Fall Time	1			2	ns
t_J	DAC Clock Jitter	1			75	ps rms

Conditions: 1) V_{DD} = 3.3V, C_L = 15pF, R_L = 1KΩ
2) I_{OH} = -1mA
3) I_{OL} = 1mA

Table 9: DAC DC Characteristics

ADC DC Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
	Number of Bits			10		Bits
	Data Format			Straight Binary		
	Sample Rate		50			MSPS
ADC DATA INPUTS						
V_{IH}	HIGH level input voltage	1	2.0			V
V_{IL}	LOW level input voltage	1			0.8	V
T_A	Aperture Delay Time	1		2.7		ns
t_{AFE_TSU}	Data Setup Time	1	3			ns
t_{AFE_TH}	Data Hold Time	1	3			ns
ADC CLOCK OUTPUT						
V_{OH}	HIGH level output voltage	1	2.1			V
V_{OL}	LOW level output voltage	1			0.9	V
t_{AFE_H}	ADC/DAC Clock Pulse Width High	1	10		15	ns
t_{AFE_L}	ADC/DAC Clock Pulse Width Low	1	10		15	ns
t_{AFE_R}	ADC/DAC Clock Rise Time	1			2	ns
t_{AFE_FT}	ADC/DAC Clock Fall Time	1			2	ns
t_J	ADC/DAC Clock Jitter	1			75	ps rms

Conditions: 1) V_{DD} = 3.3V, C_L = 15pF, R_L = 1KΩ

Table 10: ADC DC Characteristics

AGC Circuitry

The INT5130 receives 10-bit digitized samples from the INT1000 and uses them to adjust the Switched Gain Amplifier (SGA) gain to maintain optimum signal level at the input of the ADC. The AGC[7:0] control bus is used to pass a Gain Control Value (GCV) to the SGA. If the AGCENC_N input pin is low, the GCV is encoded on pins [3:0] of the AGC[7:0] control bus. If the AGCENC_N input pin is high, the GCV is decoded on pins [7:0] of the AGC[7:0] control bus with pins [7:4] selecting the gain switch setting for the first stage amplifier and pins [3:0] selecting the gain switch setting for the second stage amplifier.

GCV (AGCENC_N = 0) AGC[3:0]	GCV (AGCENC_N = 1) AGC[7:4]	AGC[3:0]	Front End Gain (dB)	Note
0 0 0 0	0 0 0 0	0 0 0 0	OFF	Mute RX during TX mode
0 0 0 1	1 0 0 0	1 0 0 0	0	
0 0 1 0	0 1 0 0	1 0 0 0	8	
0 0 1 1	0 0 1 0	1 0 0 0	16	
0 1 0 0	0 0 0 1	1 0 0 0	24	
0 1 0 1	0 0 0 1	0 1 0 0	32	
0 1 1 0	0 0 0 1	0 0 1 0	40	
0 1 1 1	0 0 0 1	0 0 0 1	48	

Table 11: RX Gain Control Values

AGC DC Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
V_{OH}	HIGH level output voltage	1	2.1			V
V_{OL}	LOW level output voltage	1			0.9	V
t_R	Rise time	1		5		ns
t_F	Fall time	1		5		ns

Conditions: 1) V_{DD} = 3.3V, C_L = 15pF, R_L = 1KΩ

Table 12: AGC IDC Characteristics

SPI Master Interface

The SPI Master interface gives the system designer the option of providing the INT5130 with the necessary configuration information from a simple, SPI-controlled E^2PROM as opposed to supplying this information via PowerPacket MAC management frames (transmitted over the MII interface). The information stored in the E^2PROM is intended to initialize the INT5130 with specific information that will not be changed throughout its normal course of operation. For specific features that require real-time control, such as those features found within the Set Transmit Characteristics MAC management frame, this information must be provided via the MAC management frames and not from the E^2PROM.

The E^2PROM must be an Atmel AT93C46 programmed in 8-bit mode, or equivalent.

SPI Master Timing Diagram

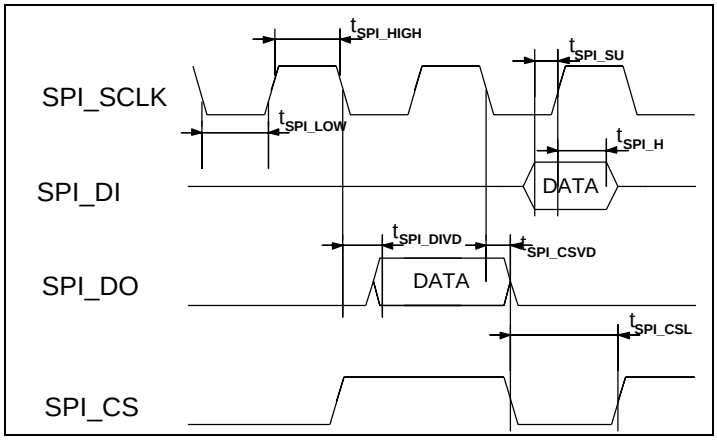


Figure 24: SPI Master Signal Timing Diagram

SPI Master DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
t_{SPI_F}	SPI_SCLK Frequency			6.125	MHz
t_{SPI_HIGH}	SPI_SCLK High Time	@ 1.5 V	70	90	ns
t_{SPI_LOW}	SPI_SCLK Low Time	@ 1.5 V	70	90	ns
t_{SPI_DIVD}	SPI_DI Valid Output Delay from SPI_SCLK	@ 1.5 V	0	15	ns
t_{SPI_CSVD}	SPI_CS Valid Output Delay from SPI_SCLK	@ 1.5 V	0	15	ns
t_{SPI_CSL}	SPI_CS Low Time	@ 1.5 V	1000		ns
t_{SPI_SU}	SPI_DO Setup Time to SPI_SCLK	@ 1.5 V	50		ns
t_{SPI_H}	SPI_DO Hold Time to SPI_SCLK	@ 1.5 V	0		ns

Table 13: SPI Master DC Characteristics

LEDs

Signal	Status	Description
LED0_N	Collision	*LED0_N: Collision Detection* Activate for a duration of 250 ms upon detection of a collision.
LED1_N	Activity	*LED1_N: Activity Detection* Activate for a duration of 250 ms upon the receipt of a properly addressed unicast or broadcast frame or the transmission of a frame.
LED2_N	Link	*LED2_N: Link Detection* Turns on when initialization is complete successfully and “network” is established.

Table 14: LED Descriptions

JTAG Port

The JTAG port is implements the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

JTAG Timing Diagrams

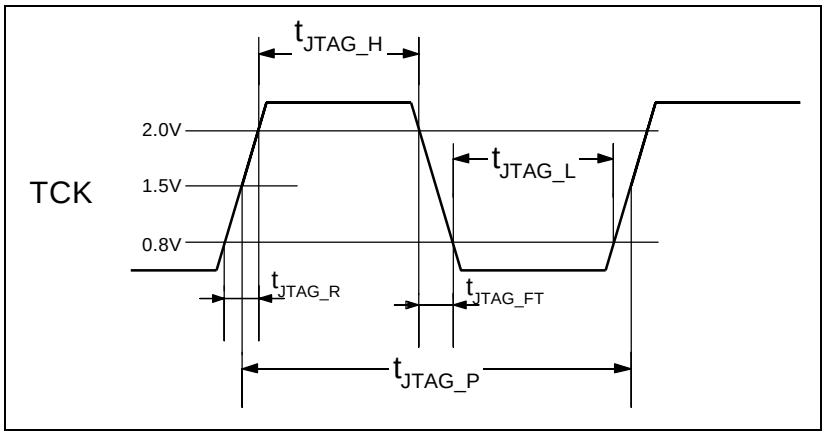


Figure 25: JTAG (IEEE 1149.1) TCK Waveform

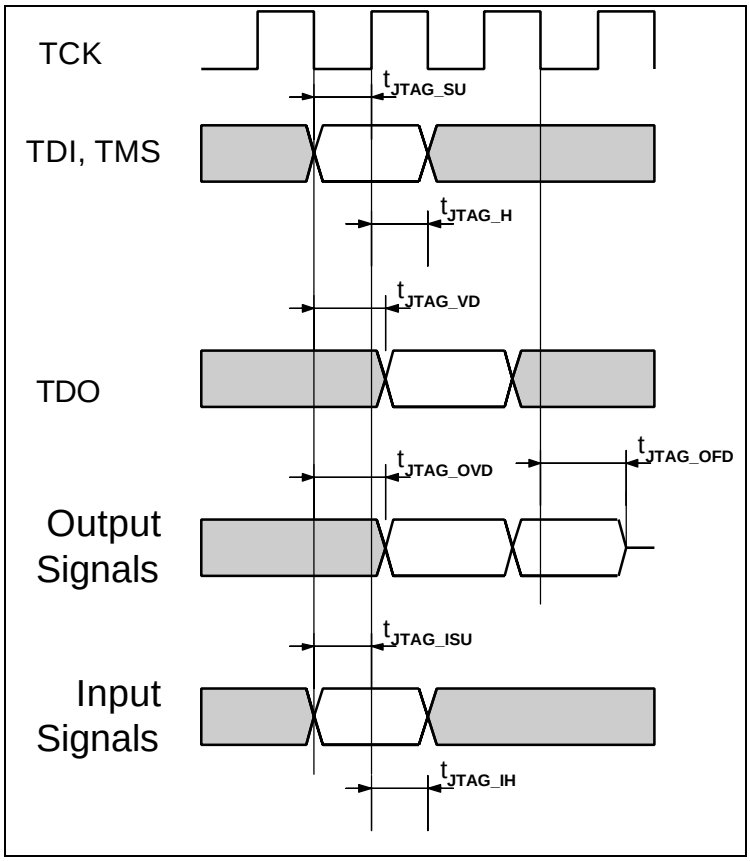


Figure 26: JTAG(IEEE 1149.1) Test Signal Timing

JTAG DC Characteristics

Parameter Symbol	Parameter Name	Test Condition	Min	Max	Unit
t_{JTAG_F}	TCK Frequency			10	MHz
t_{JTAG_P}	TCK Period		100		ns
t_{JTAG_H}	TCK High Time	@ 2.0V	45		ns
t_{JTAG_L}	TCK Low Time	@ 0.8V	45		ns
t_{JTAG_R}	TCK Rise Time			4	ns
t_{JTAG_FT}	TCK Fall Time			4	ns
t_{JTAG_SU}	TDI, TMS Setup Time		8		ns
t_{JTAG_H}	TDI, TMS Hold Time		10		ns
t_{JTAG_VD}	TDO Valid Delay		3	30	ns
t_{JTAG_FD}	TDO Float Delay			50	ns
t_{JTAG_OVD}	All Outputs (Non-Test) Valid Delay		3	25	ns
t_{JTAG_OFD}	All Outputs (Non-Test) Float Delay			36	ns
t_{JTAG_ISU}	All Inputs (Non-Test) Setup Time		8		ns
t_{JTAG_IH}	All Inputs (Non-Test) Hold Time		7		ns

Table 15: JTAG (IEEE 1149.1) DC Characteristics

Application Diagrams

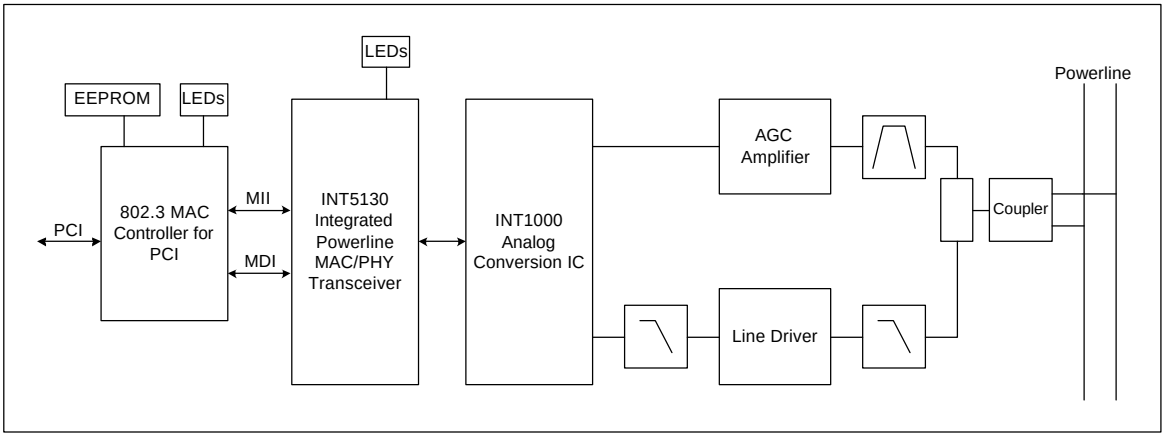


Figure 27: PCI to MII Application Diagram

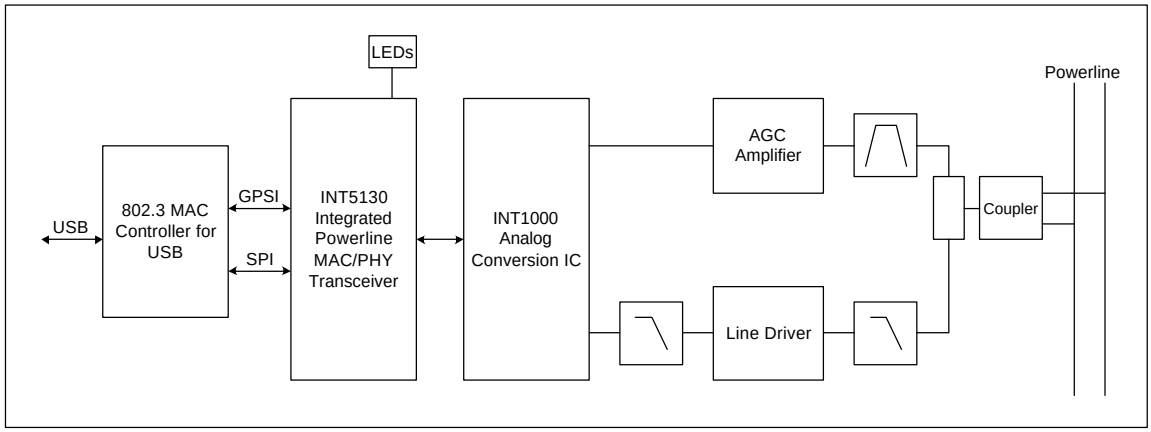


Figure 28: USB to MII Application Diagram

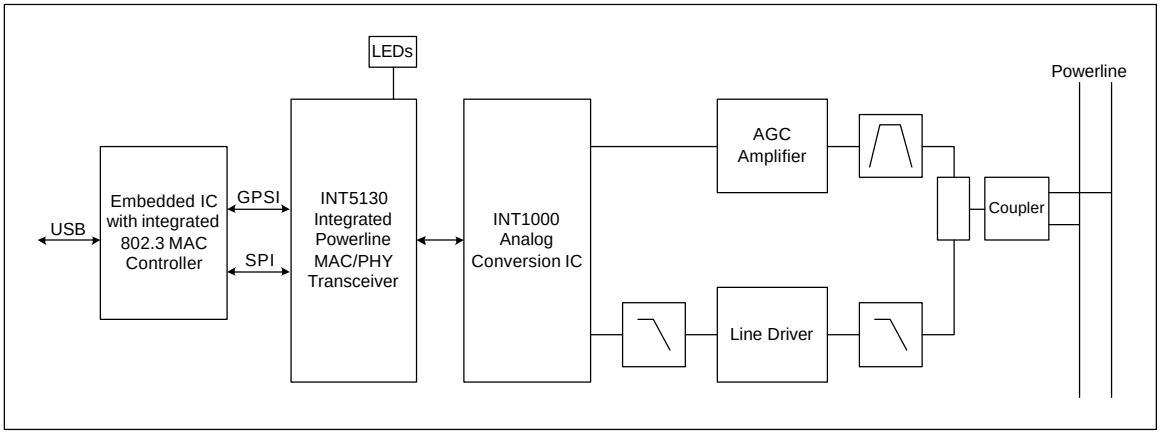


Figure 29: Embedded Application Diagram

Electrical Specifications

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Core Supply Voltage	V_{DD}	2.3	2.5	2.7	V
I/O Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Operational Temperature	T_A	0		+70	°C

Note: Recommended Operating Conditions are those values beyond which operation is not guaranteed.

DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input HIGH Voltage	V_{IH}		2.0			V
Input LOW Voltage	V_{IL}				0.8	V
Output HIGH Voltage	V_{OH}	I_{OH} = -1mA	2.4			V
Output LOW voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Input Current	I_I		-15		15	µA
Supply Current	I_{DD}			465		mA
Supply Current	I_{CC}			25		mA

Note: Any signal applied to the INT5130 clock pins, CLKIN and/or CLKOUT should not exceed 2.5 Volts.

Physical Dimensions

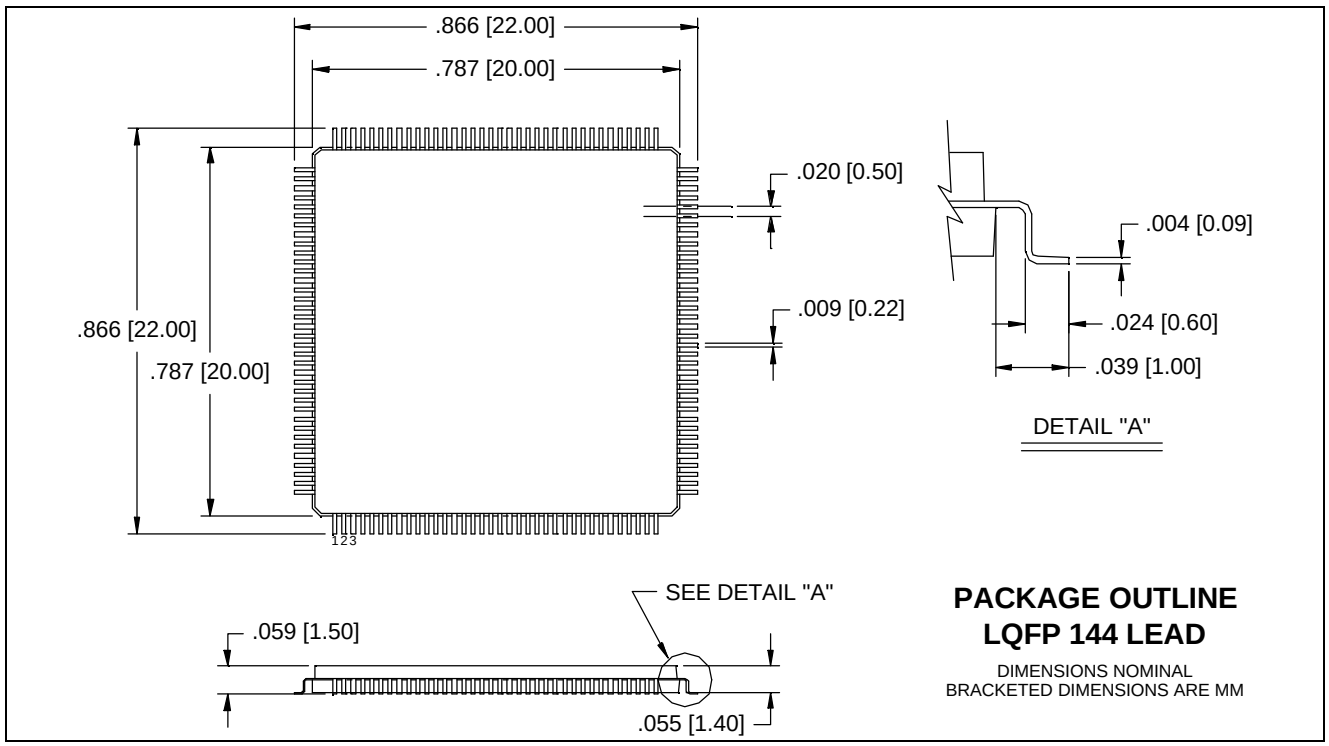
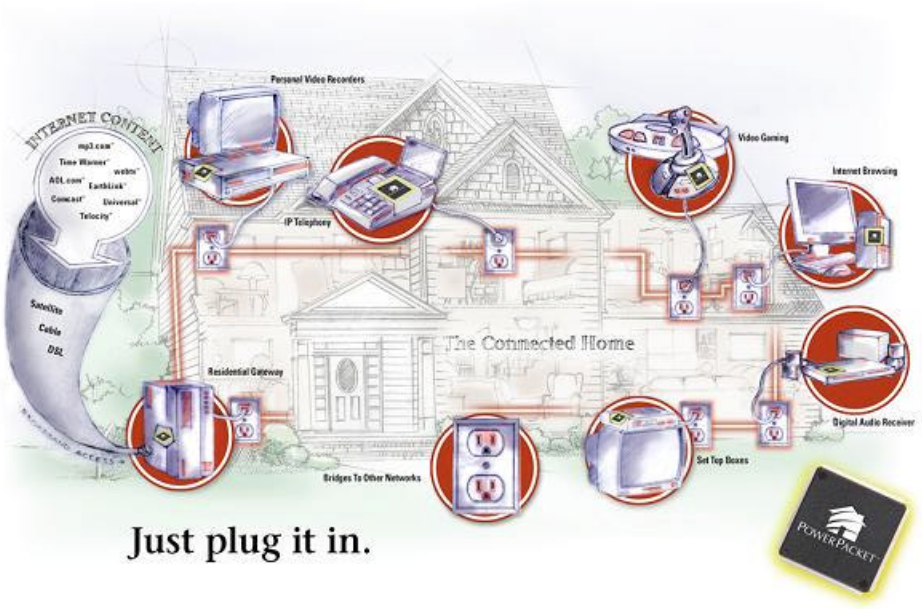


Figure 30: Physical Dimensions

Ordering Information

The INT5130 is available as part of the INT5130 Chipset, which includes both the INT5130 Integrated Powerline MAC/PHY Transceiver and the INT1000 Analog Conversion IC. Ordering information for the chipset is provided below.

Catalog Part Number	Package Type	Operating Range
INT5130 CS	INT5130: 144-pin LQFP INT1000: 64-pin LQFP	Commercial



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